# THE DATASHEET OF

# DM74ALS165N

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FAIRCHILD SEMICONDUCTOR™

January 1986
Revised February 2000

# DM74ALS165
# 8-Bit Parallel In/Serial Out Shift Register

## General Description

The DM74ALS165 is an 8-bit serial register that, when clocked, shifts the data toward serial output, $\overline{Q}_H$. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/$\overline{LD}$ input. The DM74ALS165 also features a clock inhibit function and a complemented serial output, $\overline{Q}_H$.

Clocking is accomplished by a LOW-to-HIGH transition of the CLK input while SH/$\overline{LD}$ is held HIGH and CLK INH is held LOW. The functions of the CLK and CLK INH (clock inhibit) inputs are interchangeable. Since a LOW CLK input and a LOW-to-HIGH transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is HIGH. Parallel loading is inhibited when SH/$\overline{LD}$ is held HIGH. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is LOW independently of the levels of CLK, CLK INH, or SER inputs.

## Features

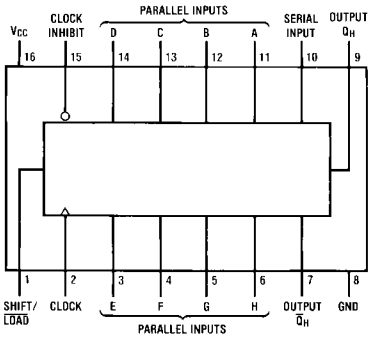
- Complementary outputs
- Direct overriding load (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| DM74ALS165M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74ALS165N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram




## Function Table

| Inputs | | | | | Internal Outputs | | Output |
|---|---|---|---|---|---|---|---|
| Shift/ Load | Clock Inhibit | Clock | Serial | Parallel A...H | $Q_A$ | $Q_B$ | $Q_H$ |
| L | X | X | X | a...h | a | b | h |
| H | L | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | L | ↑ | H | X | H | $Q_{An}$ | $Q_{Gn}$ |
| H | L | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | ↑ | L | H | X | H | $Q_{An}$ | $Q_{Gn}$ |
| H | ↑ | L | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | H | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |

H = HIGH Level (steady-state),
L = LOW Level (steady-state)
X = Don't Care (any input, including transitions)
↑ = Transition from LOW-to-HIGH level
a...h = The level of steady-state input at inputs A through H, respectively
$Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = The level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established
$Q_{An}$, $Q_{Gn}$ = The level of $Q_A$ or $Q_G$, respectively, before the most recent ↑ transition of the clock

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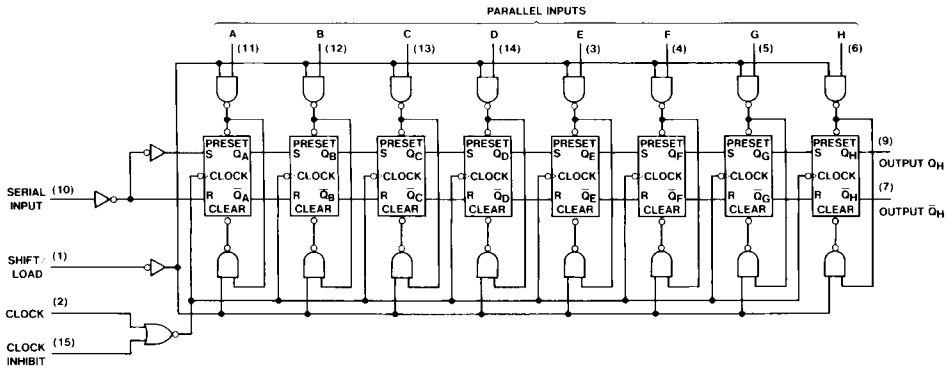
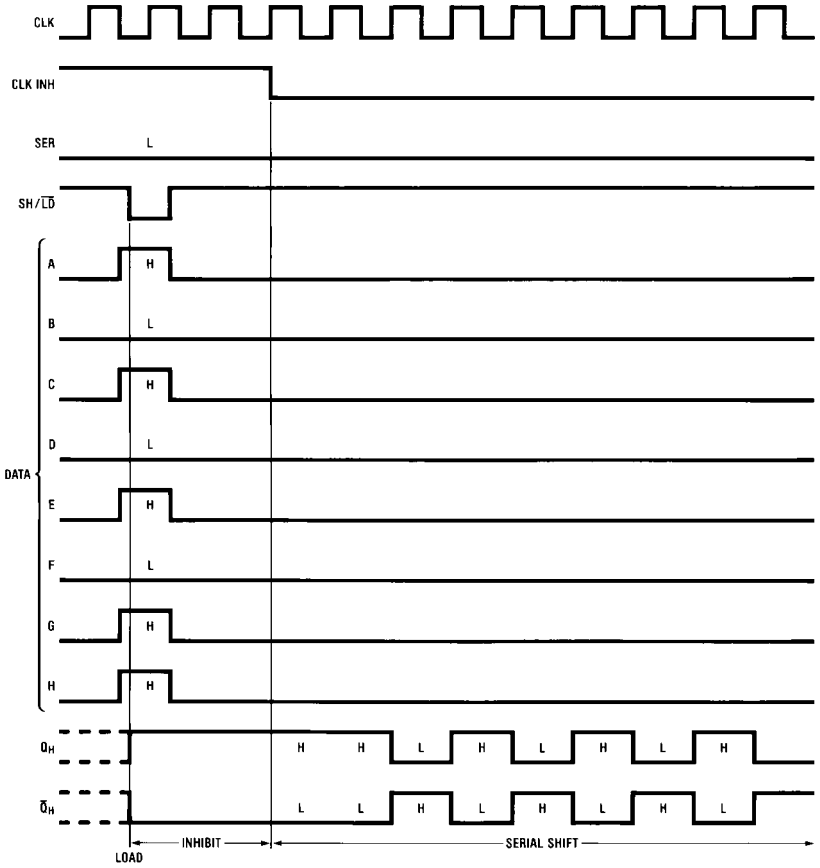
## Logic Diagram




## Timing Diagram

**Typical Shift, Load, and Inhibit Sequences**



## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Typical $\theta_{JA}$ | |
| N Package | 74.0°C/W |
| M Package | 104.0°C/W |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | HIGH Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | LOW Level Input Voltage | | | | 0.8 | V |
| $I_{OH}$ | HIGH Level Output Current | | | | −0.4 | mA |
| $I_{OL}$ | LOW Level Output Current | | | | 8 | mA |
| $f_{CLOCK}$ | Clock Frequency | | 45 | | | MHz |
| $t_W$ | Pulse Duration | CLK HIGH | 11 | | | ns |
| | | CLK LOW | 11 | | | |
| | | Load | 12 | | | |
| $t_{SU}$ | Setup Time | SH/$\overline{LD}$ | 10 | | | ns |
| | | Data | 10 | | | |
| $t_{SU}$ | Setup Time | CLK INH ↓ before CLK | 11 | | | ns |
| | | Serial before CLK | 10 | | | |
| $t_H$ | Hold Time | | 4 | | | ns |
| $T_A$ | Operating Free Air Temperature | | 0 | | 70 | °C |

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | | Min | Typ (Note 2) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input Clamp Voltage | $V_{CC}$ = 4.5V, $I_I$ = −18 mA | | | | −1.5 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $I_{OH}$ = −0.4 mA, $V_{CC}$ = 4.5V to 5.5V | | $V_{CC}$ − 2 | | | V |
| $V_{OL}$ | LOW Level Output Voltage | $V_{CC}$ = 4.5V | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | | 0.35 | 0.5 | |
| $I_I$ | Input Current at Max Input Voltage | $V_{CC}$ = 5.5V, $V_I$ = 7V | | | | 0.1 | mA |
| $I_{IH}$ | HIGH Level Input Current | $V_{CC}$ = 5.5V, $V_I$ = 2.7V | | | | 20 | μA |
| $I_{IL}$ | LOW Level Input Current | $V_{CC}$ = 5.5V, $V_I$ = 0.4V | | | | −0.1 | mA |
| $I_O$ (Note 3) | Output Drive Current | $V_{CC}$ = 5.5V, $V_O$ = 2.25V | | −30 | | −112 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 5.5V (Note 4) | | | 16 | 24 | mA |

**Note 2:** All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

**Note 3:** The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

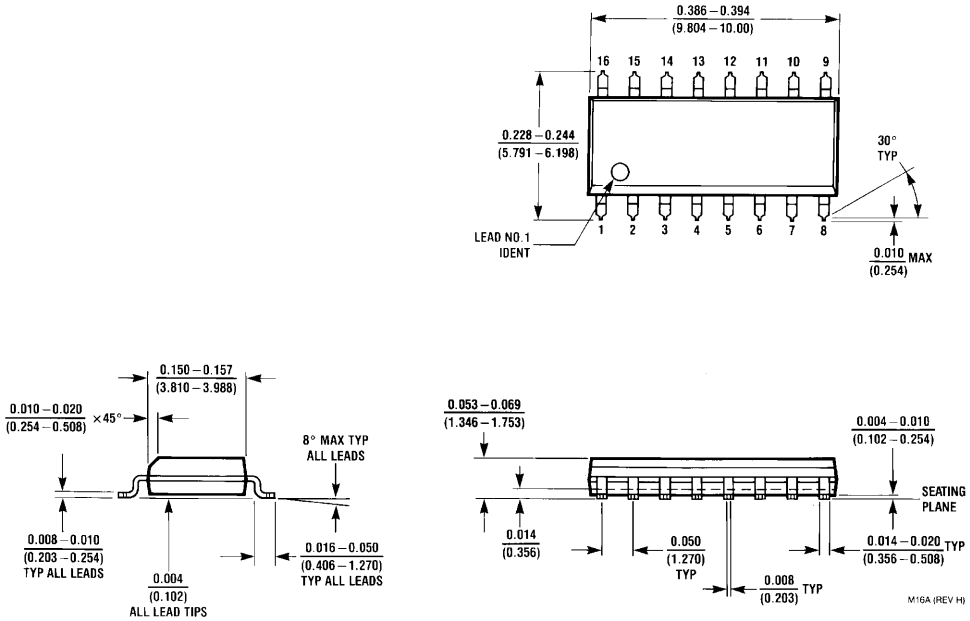
**Note 4:** With the outputs open, CLK INH and CLK at 4.5V, and a clock pulse applied to the SH/$\overline{LD}$ input, $I_{CC}$ is measured first with the parallel inputs at 4.5V, then with the parallel inputs grounded.

## Switching Characteristics

over recommended free air temperature range. All typical values are measured at $V_{CC}$ = 5V, $T_A$ = 25°C.

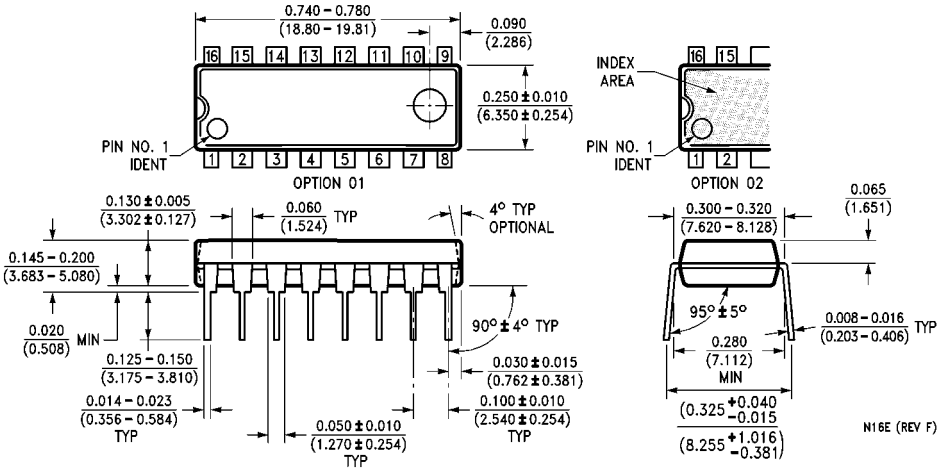
| Symbol | Parameter | Input | Output | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Frequency | | | $V_{CC}$ = 4.5V to 5.5V, | 45 | 60 | | MHz |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | Load | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF, $R_L$ = 500Ω $T_A$ = Min to Max | 4 | 13 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Load | $Q_H$ or $\overline{Q}_H$ | | 4 | 14 | 22 | |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | CLK | $Q_H$ or $\overline{Q}_H$ | | 3 | 7 | 13 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | CLK | $Q_H$ or $\overline{Q}_H$ | | 3 | 9 | 14 | |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | H | $Q_H$ | | 3 | 7 | 13 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | H | $Q_H$ | | 3 | 9 | 16 | |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | H | $\overline{Q}_H$ | | 2 | 8 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | H | $\overline{Q}_H$ | | 3 | 9 | 16 | |

## Physical Dimensions inches (millimeters) unless otherwise noted




**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow**
**Package Number M16A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N16E**

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