

## 16-Bit I<sup>2</sup>C™ I/O Expander

### Features

- 16-bit remote bidirectional I/O port
  - 16 I/O pins default to 16 inputs
- Fast I<sup>2</sup>C™ bus clock frequency (0 - 400 kbits/s)
- Three hardware address pins allow use of up to eight devices
- High-current drive capability per I/O: ±25 mA
- Open-drain interrupt output on input change
- Interrupt port capture register
- Internal Power-On Reset (POR)
- Polarity inversion register to configure the polarity of the input port data
- Compatible with most microcontrollers
- Available temperature range:
  - Industrial (I): -40°C to +85°C

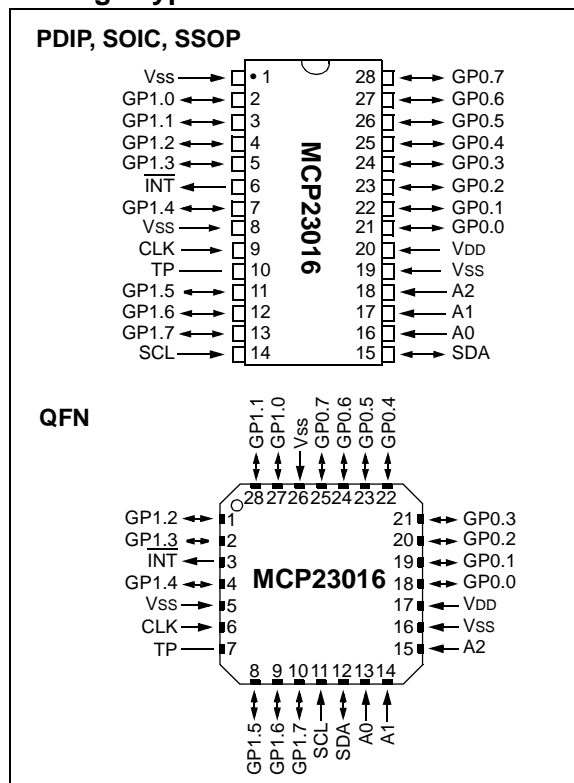
### CMOS Technology

- Operating Supply Voltage: 2.0V to 5.5V
- Low standby current

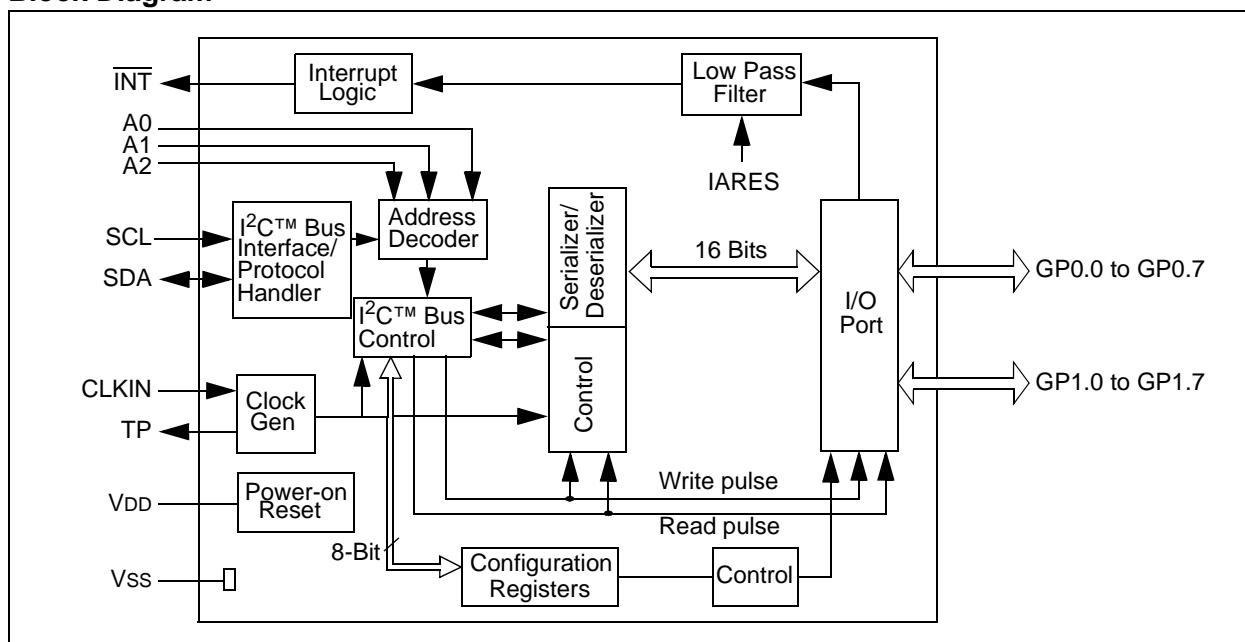
### Packages

- 28-pin PDIP, 300 mil; 28-pin SOIC, 300 mil
- 28-pin SSOP, 209 mil; 28-pin QFN, 6x6 mm

### Package Types



### Block Diagram



# MCP23016

---

NOTES:

## 1.0 DEVICE OVERVIEW

The MCP23016 device provides 16-bit, general purpose, parallel I/O expansion for I<sup>2</sup>C bus applications.

This device includes high-current drive capability, low supply current and individual I/O configuration. I/O expanders provide a simple solution when additional I/Os are needed for ACPI, power switches, sensors, push buttons, LEDs and so on.

The MCP23016 consists of multiple 8-bit configuration registers for input, output and polarity selection. The system master can enable the I/Os as either inputs or outputs by writing the I/O configuration bits. The data for each input or output is kept in the corresponding

input or output register. The polarity of the read register can be inverted with the polarity inversion register (see **Section 1.7.3, “Input Polarity Registers”**). All registers can be read by the system master.

The open-drain interrupt output is activated when any input state differs from its corresponding input port register state. This is used to indicate to the system master that an input state has changed. The interrupt capture register captures port value at this time. The Power-on Reset sets the registers to their default values and initializes the device state machine.

Three device inputs (A0 - A2) determine the I<sup>2</sup>C address and allow up to eight I/O expander devices to share the same I<sup>2</sup>C bus.

## 1.1 Pin Descriptions

**TABLE 1-1: PINOUT DESCRIPTION**

Pin Name	PDIP, SOIC, SSOP Pin No.	QFN Pin No.	I/O/P Type	Buffer Type	Description
CLK	9	6	I	ST	Clock source input
TP	10	7	O	—	Test Pin (This pin must be left floating)
GP1.0	2	27	I/O	TTL	D0 digital input/output for GP1
GP1.1	3	28	I/O	TTL	D1 digital input/output for GP1
GP1.2	4	1	I/O	TTL	D2 digital input/output for GP1
GP1.3	5	2	I/O	TTL	D3 digital input/output for GP1
GP1.4	7	4	I/O	TTL	D4 digital input/output for GP1
GP1.5	11	8	I/O	ST	D5 digital input/output for GP1
GP1.6	12	9	I/O	ST	D6 digital input/output for GP1
GP1.7	13	10	I/O	ST	D7 digital input/output for GP1
GP0.0	21	18	I/O	TTL	D0 digital input/output for GP0
GP0.1	22	19	I/O	TTL	D1 digital input/output for GP0
GP0.2	23	20	I/O	TTL	D2 digital input/output for GP0
GP0.3	24	21	I/O	TTL	D3 digital input/output for GP0
GP0.4	25	22	I/O	TTL	D4 digital input/output for GP0
GP0.5	26	23	I/O	TTL	D5 digital input/output for GP0
GP0.6	27	24	I/O	TTL	D6 digital input/output for GP0
GP0.7	28	25	I/O	TTL	D7 digital input/output for GP0
SCL	14	11	I	ST	Serial clock input
SDA	15	12	I/O	ST	Serial data I/O
$\overline{\text{INT}}$	6	3	O	OD	Interrupt output
A0	16	13	I	ST	Address input 1
A1	17	14	I	ST	Address input 2
A2	18	15	I	ST	Address input 3
Vss	1, 8, 19	5, 16, 26	P	—	Ground reference for logic and I/O pins
VDD	20	17	P	—	Positive supply for logic and I/O pins

# MCP23016

## 1.2 Power-on Reset (POR)

The on-chip POR circuit holds the chip in RESET until VDD has reached a high enough level to deactivate the POR circuit (i.e., release RESET). A maximum rise time for VDD is specified in the electrical specifications.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature) must be met to ensure proper operation.

## 1.3 Power-up Timer (PWRT)

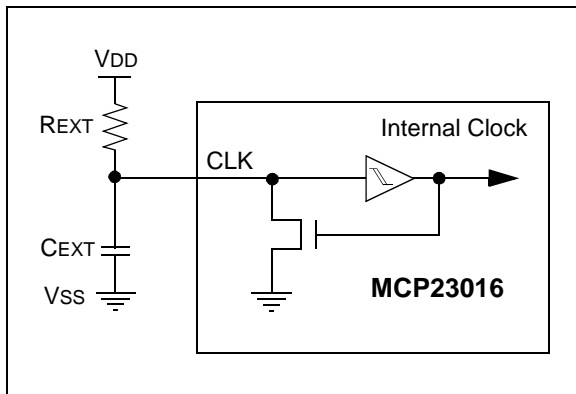
The Power-up Timer provides a 72 ms nominal time-out on power-up, keeping the device in RESET and allowing VDD to rise to an acceptable level.

The power-up time delay will vary from chip-to-chip due to VDD, temperature and process variation. See Table 2-4 for details (TPWRT, parameter 3).

## 1.4 Clock Generator

The MCP23016 uses an external RC circuit to determine the internal clock speed. The user must connect R and C to the MCP23016, as shown in Figure 1-1.

**FIGURE 1-1: CLOCK CONFIGURATION**



A 1 MHz (typ.) internal clock is needed for the device to function properly. The internal clock can be measured on the TP pin. Recommended REXT and CEXT values are shown in Table 1-2.

**Note:** Set IARES = 1 to measure the clock output on TP.

**TABLE 1-2: RECOMMENDED VALUES**

REXT	CEXT
3.9 kΩ	33 pF

## 1.5 I<sup>2</sup>C Bus Interface/ Protocol Handler

This block manages the functionality of the I<sup>2</sup>C bus interface and protocol handling. The MCP23016 supports the following commands:

**TABLE 1-3: COMMAND BYTE TO REGISTER RELATIONSHIP**

Command Byte	Result
0h	Access to GP0
1h	Access to GP1
2h	Access to OLAT0
3h	Access to OLAT1
4h	Access to IPOL0
5h	Access to IPOL1
6h	Access to IODIR0
7h	Access to IODIR1
8h	Access to INTCAP0 (Read-Only)
9h	Access to INTCAP1 (Read-Only)
Ah	Access to IOCON0
Bh	Access to IOCON1

## 1.6 Address Decoder

The last three LSb of the 7-bit address are user-defined (see Table 1-4). Three hardware pins (<A2:A0>) define these bits.

**TABLE 1-4: DEVICE ADDRESS**

0	1	0	0	A2	A1	A0
---	---	---	---	----	----	----

## 1.7 Register Block

The register block contains the Configuration and Port registers, as shown in Table 1-5.

**TABLE 1-5: REGISTER SUMMARY**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
<b>Port Registers</b>									
GP0	GP0.7	GP0.6	GP0.5	GP0.4	GP0.3	GP0.2	GP0.1	GP0.0	0000 0000
GP1	GP1.7	GP1.6	GP1.5	GP1.4	GP1.3	GP1.2	GP1.1	GP0.0	0000 0000
OLAT0	OL0.7	OL0.6	OL0.5	OL0.4	OL0.3	OL0.2	OL0.1	OL0.0	0000 0000
OLAT1	OL1.7	OL1.6	OL1.5	OL1.4	OL1.3	OL1.2	OL1.1	OL1.0	0000 0000
<b>Configuration Registers</b>									
IPOL0	IGP0.7	IGP0.6	IGP0.5	IGP0.4	IGP0.3	IGP0.2	IGP0.1	IGP0.0	0000 0000
IPOL1	IGP1.7	IGP1.6	IGP1.5	IGP1.4	IGP1.3	IGP1.2	IGP1.1	IGP1.0	0000 0000
IODIR0	IOD0.7	IOD0.6	IOD0.5	IOD0.4	IOD0.3	IOD0.2	IOD0.1	IOD0.0	1111 1111
IODIR1	IOD1.7	IOD1.6	IOD1.5	IOD1.4	IOD1.3	IOD1.2	IOD1.1	IOD1.0	1111 1111
INTCAP0	ICP0.7	ICP0.6	ICP0.5	ICP0.4	ICP0.3	ICP0.2	ICP0.1	ICP0.0	xxxx xxxx
INTCAP1	ICP1.7	ICP1.6	ICP1.5	ICP1.4	ICP1.3	ICP1.2	ICP1.1	ICP1.0	xxxx xxxx
IOCON0	—	—	—	—	—	—	—	IARES	---- ---0
IOCON1	—	—	—	—	—	—	—	IARES	---- ---0

**Legend:** '1' bit is set, '0' bit is cleared, x = unknown, — = unimplemented.

# MCP23016

---

## 1.7.1 DATA PORT REGISTERS

Two registers provide access to the two GPIO ports:

- GP0 (provides access to data port GP0)
- GP1 (provides access to data port GP1)

A read from this register provides status on pins of these ports. A write to these registers will modify the output latch registers (OLAT0, OLAT1) and data output.

### REGISTER 1-1: GP0 - GENERAL PURPOSE I/O PORT REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP0.7	GP0.6	GP0.5	GP0.4	GP0.3	GP0.2	GP0.1	GP0.0
bit 7				bit 0			

bit 7-0 **GP0.0:GP0.7:** Reflects the logic level on the pins.  
1 = Logic '1'  
0 = Logic '0'

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

### REGISTER 1-2: GP1 - GENERAL PURPOSE I/O PORT REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP1.7	GP1.6	GP1.5	GP1.4	GP1.3	GP1.2	GP1.1	GP1.0
bit 7				bit 0			

bit 7-0 **GP1.0:GP1.7:** Reflects the logic level on the pins.  
1 = Logic '1'  
0 = Logic '0'

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

## 1.7.2 OUTPUT LATCH REGISTERS

Two registers provide access to the two port output latches:

- OLAT0 (provides access to the output latch for port GP0)
- OLAT1 (provides access to the output latch for port GP1)

A read from these registers results in a read of the latch that controls the output and not the actual port. A write to these registers updates the output latch that controls the output.

### REGISTER 1-3: OLAT0 - OUTPUT LATCH REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OL0.7	OL0.6	OL0.5	OL0.4	OL0.3	OL0.2	OL0.1	OL0.0
bit 7				bit 0			

bit 7-0 **OL0.0:OL0.7**: Reflects the logic level on the output latch.  
 1 = Logic '1'  
 0 = Logic '0'

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

### REGISTER 1-4: OLAT1 - OUTPUT LATCH REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OL1.7	OL1.6	OL1.5	OL1.4	OL1.3	OL1.2	OL1.1	OL1.0
bit 7				bit 0			

bit 7-0 **OL1.0:OL1.7**: Reflects the logic level on the output latch.  
 1 = Logic '1'  
 0 = Logic '0'

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

# MCP23016

---

## 1.7.3 INPUT POLARITY REGISTERS

These registers allow the user to configure the polarity of the input port data (GP0 and GP1). If a bit in this register is set, the corresponding input port (GPn) data bit polarity will be inverted.

- IPOL0 (controls the polarity of GP0)
- IPOL1 (controls the polarity of GP1)

### REGISTER 1-5: IPOL0 - INPUT POLARITY PORT REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IGP0.7	IGP0.6	IGP0.5	IGP0.4	IGP0.3	IGP0.2	IGP0.1	IGP0.0
bit 7				bit 0			

bit 7-0 **IGP0.0:IGP0.7:** Controls the polarity inversion for the input pins  
1 = Corresponding GP0 bit is inverted  
0 = Corresponding GP0 bit is not inverted

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
- n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

### REGISTER 1-6: IPOL1 - INPUT POLARITY PORT REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IGP1.7	IGP1.6	IGP1.6	IGP1.4	IGP1.3	IGP1.2	IGP1.1	IGP1.0
bit 7				bit 0			

bit 7-0 **IGP1.0:IGP1.7:** Controls the polarity inversion for the input pins  
1 = Corresponding GP1 bit is inverted  
0 = Corresponding GP1 bit is not inverted

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
- n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

## 1.7.4 I/O DIRECTION REGISTERS

Two registers control the direction of data I/O:

- IODIR0 (controls GP0)
- IODIR1 (controls GP1)

When a bit in these registers is set, the corresponding pin becomes an input. Otherwise, it becomes an output. At Power-on Reset, the device ports are configured as inputs.

### REGISTER 1-7: IODIR0 - I/O DIRECTION REGISTER 0

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
IOD0.7	IOD0.6	IOD0.5	IOD0.4	IOD0.3	IOD0.2	IOD0.1	IOD0.0
bit 7				bit 0			

bit 7-0 **IOD0.0:IOD0.7:** Controls the direction of data I/O  
 1 = Input  
 0 = Output

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

### REGISTER 1-8: IODIR1 - I/O DIRECTION REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
IOD1.7	IOD1.6	IOD1.5	IOD1.4	IOD1.3	IOD1.2	IOD1.1	IOD1.0
bit 7				bit 0			

bit 7-0 **IOD1.0:IOD1.7:** Controls the direction of data I/O  
 1 = Input  
 0 = Output

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

# MCP23016

## 1.7.5 INTERRUPT CAPTURE REGISTERS

Two registers contain the value of the port that generated the interrupt:

- INTCAP0 contains the value of GP0 at time of GP0 change interrupt
- INTCAP1 contains the value of GP1 at time of GP1 change interrupt

These registers are 'read-only' registers (A write to these registers is ignored).

### REGISTER 1-9: INTCAP0 - INTERRUPT CAPTURED VALUE FOR PORT REGISTER 0

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ICP0.7	ICP0.6	ICP0.5	ICP0.4	ICP0.3	ICP0.2	ICP0.1	ICP0.0
bit 7							bit 0

bit 7-0 **ICP0.0:ICP0.7:** Reflects the logic level on the GP0 pins at the time of interrupt due to pin change  
1 = Logic '1'  
0 = Logic '0'

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
- n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

### REGISTER 1-10: INTCAP1 - INTERRUPT CAPTURED VALUE FOR PORT REGISTER 1

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ICP1.7	ICP1.6	ICP1.5	ICP1.4	ICP1.3	ICP1.2	ICP1.1	ICP1.0
bit 7							bit 0

bit 7-0 **ICP1.0:ICP1.7:** Reflects the logic level on the GP1 pins at the time of interrupt due to pin change  
1 = Logic '1'  
0 = Logic '0'

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
- n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

## 1.7.6 I/O EXPANDER CONTROL REGISTER

- IOCON0 controls the functionality of the MCP23016.

The IARES (Interrupt Activity Resolution) bit controls the sampling frequency of the GP port pins. The higher the sampling frequency, the higher the device current requirements. If this bit is '0' (default), the maximum time to detect the activity on the port is 32 ms (max.), which results in lower standby current. If this bit is '1', the maximum time to detect activity on the port is 200 μsec. (max.) and results in higher standby current.

### REGISTER 1-11: IOCON0 - I/O EXPANDER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	IARES
bit 7							bit 0

bit 1-7     **Unimplemented bit:** Read as '0'

bit 0     **IARES:** Interrupt Activity Resolution  
 1 = Fast sample rate  
 0 = Normal sample rate

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

**IOCON1** is a shadow register for IOCON0. Access to IOCON1 results in access to IOCON0.

# MCP23016

## 1.8 Serializer/Deserializer

The Serializer/Deserializer block converts and transfers data between the I<sup>2</sup>C bus and GPIO.

## 1.9 Interrupt Logic

The MCP23016 asserts the open-drain interrupt output ( $\overline{\text{INT}}$ ) low when one of the port pins changes state. Only those pins that are configured as an input can cause an interrupt. Pins defined as an output have no effect on  $\overline{\text{INT}}$ . The interrupt will remain active until a read from either the port (GPn) on which the interrupt occurred or the INTCAPn register is performed. If the input returns to its previous state before a read operation, it will reset the interrupt and the  $\overline{\text{INT}}$  pin output will tri-state. Each 8-bit port is read separately, so reading GP0 or INTCAP0 will not clear the interrupt generated by GP1 or INTCAP1, and vice versa.

Input change activity on each port will generate an interrupt and the value of the particular port will be captured and copied into INTCAP0/INTCAP1. The INTCAPn registers are only updated when an interrupt occurs on  $\overline{\text{INT}}$ . These values will stay unchanged until the user clears the interrupt by reading the port or the INTCAPn register.

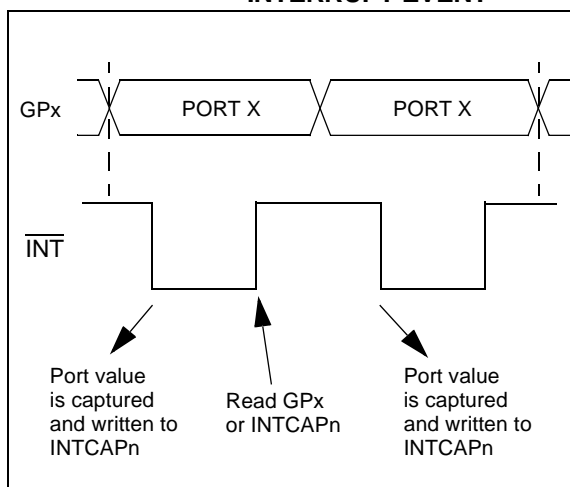
If the input port value changes back to normal before a user-read, the  $\overline{\text{INT}}$  output will be reset. However, the INTCAP0/INTCAP1 will still contain the value of the port at the interrupt change. If the port value changes again, it will re-activate the interrupt and the new value will be captured.

The first interrupt on change event following an interrupt RESET will result in a capture event. Any further change event that occurs before the interrupt is reset will not result in a capture event.

### 1.9.1 INTERRUPT EVENT DETECTION

The IARES bit controls the resolution for detecting an interrupt-on-change event. If this bit is '0' (default), the maximum time for detecting a change of event is high, which results in lower standby current. If this bit is '1', it takes less time for scanning the activity on the port and results in higher standby current.

**FIGURE 1-2: READING PORTX AFTER INTERRUPT EVENT**



## 1.9.2 WRITING THE REGISTERS

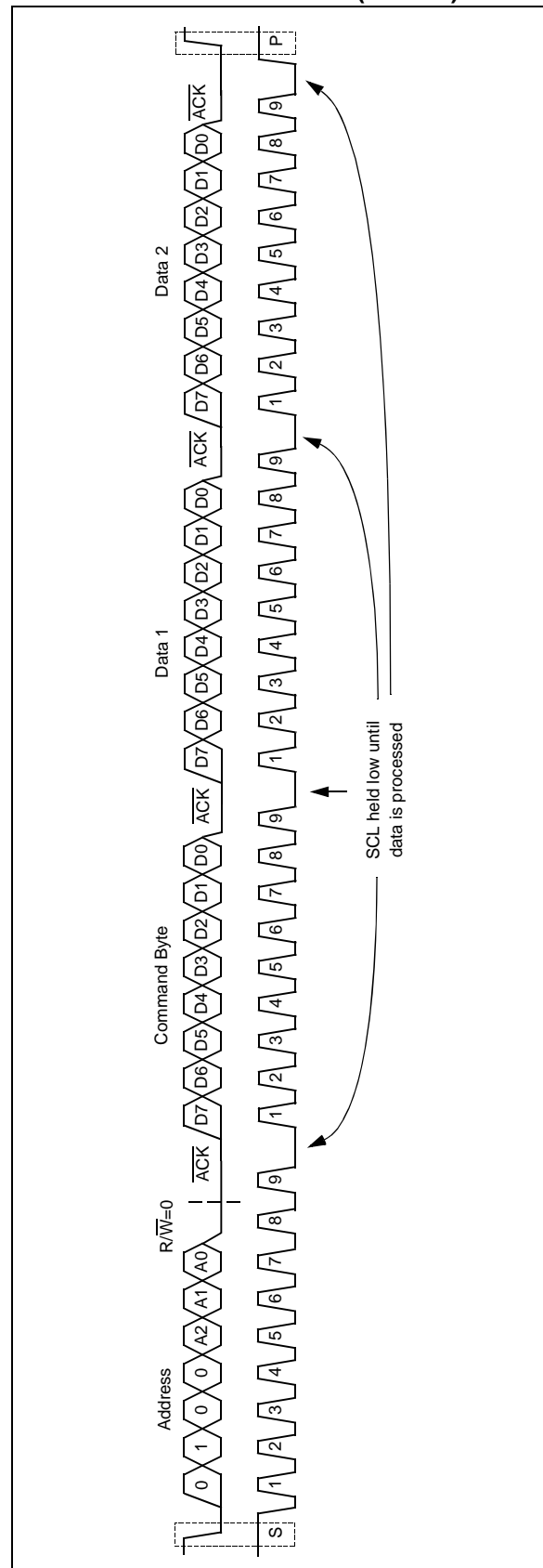
To write to a MCP23016 register, the Master I<sup>2</sup>C device needs to follow the requirements, as illustrated in Figure 1-3. First, the device is selected by sending the slave address and setting the R/W bit to logic '0'. The command byte is sent after the address and determines which register will be written. Table 1-3 shows the relationship of the command byte and register.

The MCP23016 has twelve 8-bit registers. They are configured to operate as six 16-bit register pairs, supporting the device's 16-bit port. These pairs are formed based on their functions (e.g., GP0 and GP1 are grouped together). The I<sup>2</sup>C commands apply to one register pair to provide faster access. The first data byte following a command byte is written into the register pointed to by the command byte, while the second data is written into another register in the same pair. For example, if the first byte is sent to OLAT1 (command byte 03h), the next data byte will be written into the second register of that pair, OLAT0. If the first byte is written to OLAT0 (command byte 02h), the second byte will be written to OLAT1.

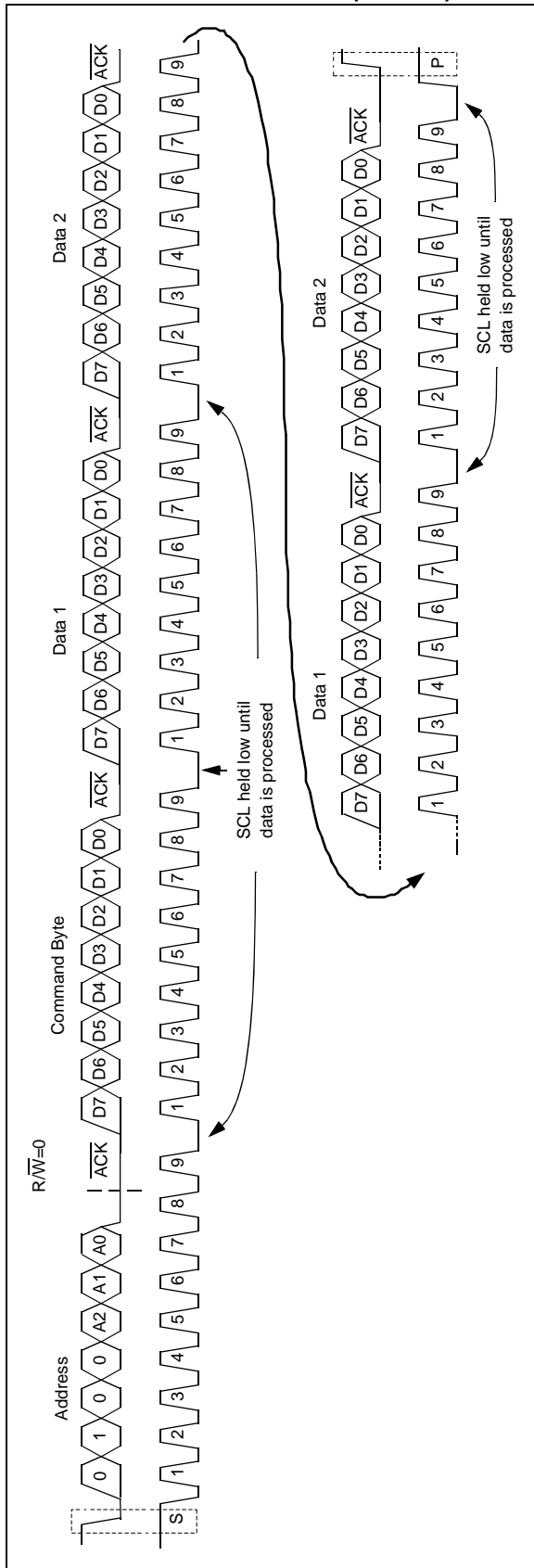
There is no limitation on the number of data bytes in one write transmission. Figure 1-4 shows the case of multiple byte writes in one write operation. In this case, the multiple writes are made to the same data pair.

**Note:** The bus must remain free until after the ninth clock pulse for a minimum of 12 μs (see Table 2-5 and Figure 2-4).

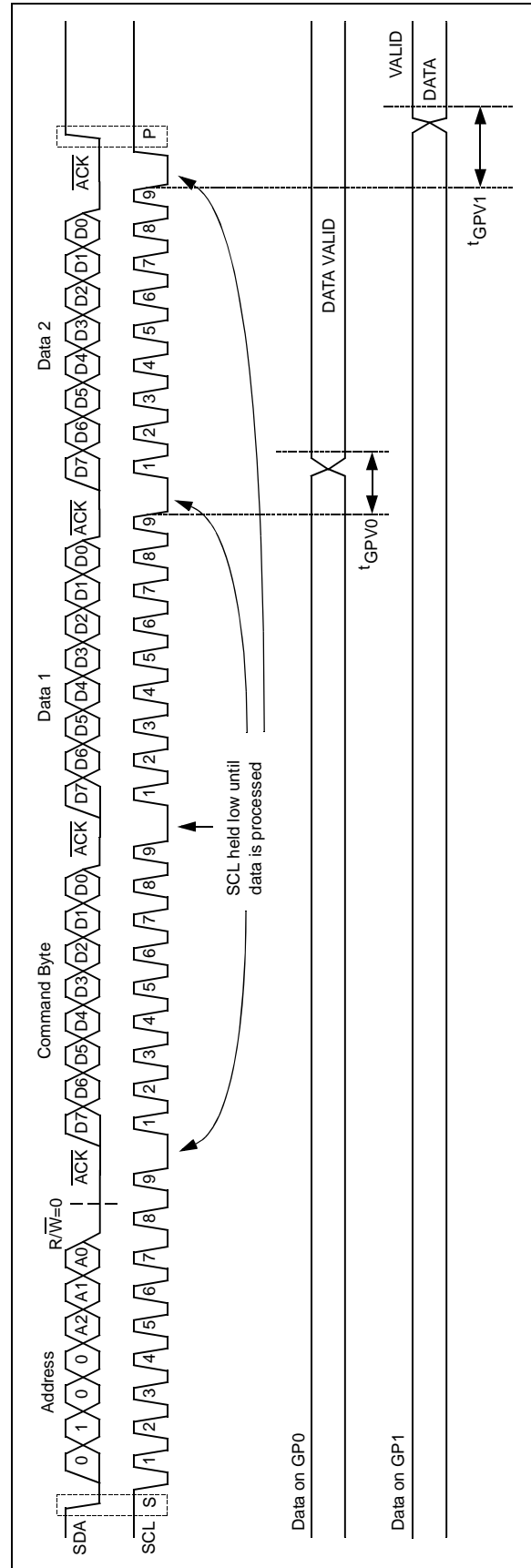
**FIGURE 1-3: WRITE TO CONFIGURATION REGISTERS (CASE 1)**



**FIGURE 1-4: WRITE TO CONFIGURATION REGISTERS (CASE 2)**



**FIGURE 1-5: WRITE TO OUTPUT PORTS**



## 1.9.3 READING THE REGISTERS

To read a MCP23016 register, the Master needs to follow the requirements shown in Figure 1-6. First, the device is selected by sending the slave address and setting the R/W bit to logic '0'. The command byte is sent after the address and determines which register will be read. A restart condition is generated and the device address is sent again with the R/W bit set to logic '1'. The data register defined by the command byte will be sent first, followed by the other register in the register pair. The logic for register selection is the same as explained in Write mode (**Section 1.9.2, "Writing the Registers"**).

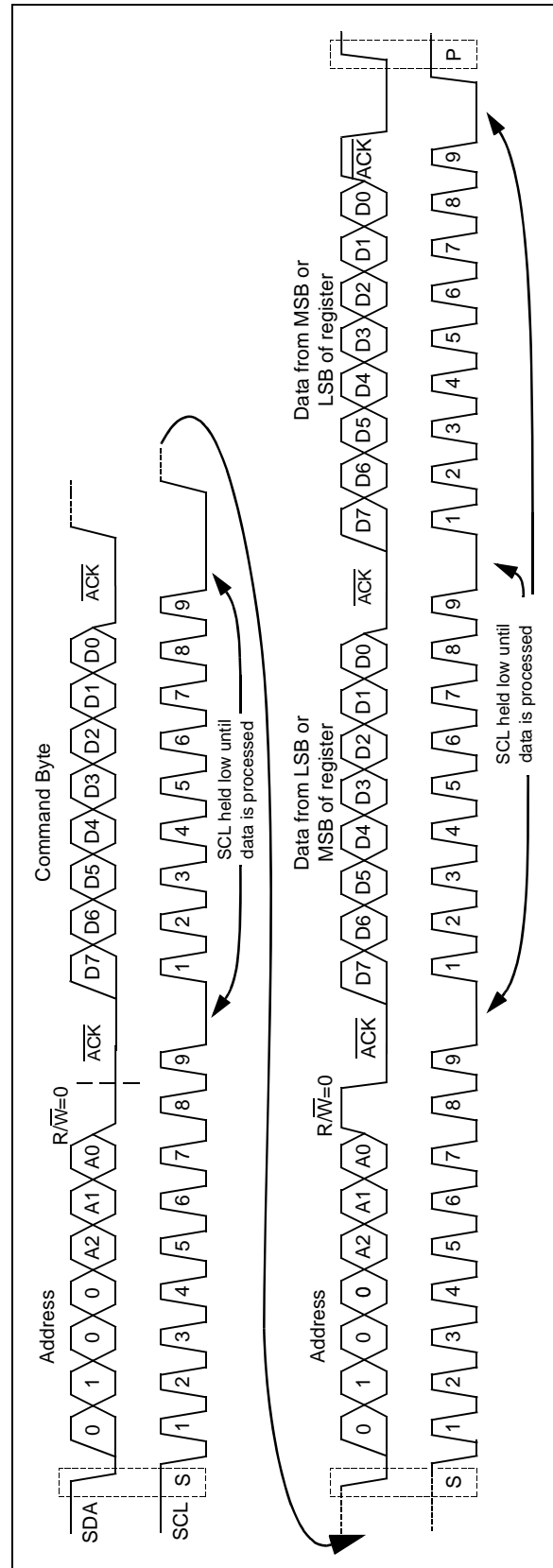
The falling edge of the ninth clock initiates the register read action. The SCL clock will be held low while the data is read from the register and is transferred to the I<sup>2</sup>C bus control block by the Serializer/Deserializer block.

The MCP23016 holds the clock low after the falling edge of the ninth clock pulse. The configuration registers (or port control registers) are read and the value is stored. Finally, the clock is released to enable the next transmission.

There is no limitation on the number of data bytes in one read transmission. Figure 1-8 shows the case of multiple byte read in one read operation. In this case, the multiple writes are made to the same data pair.

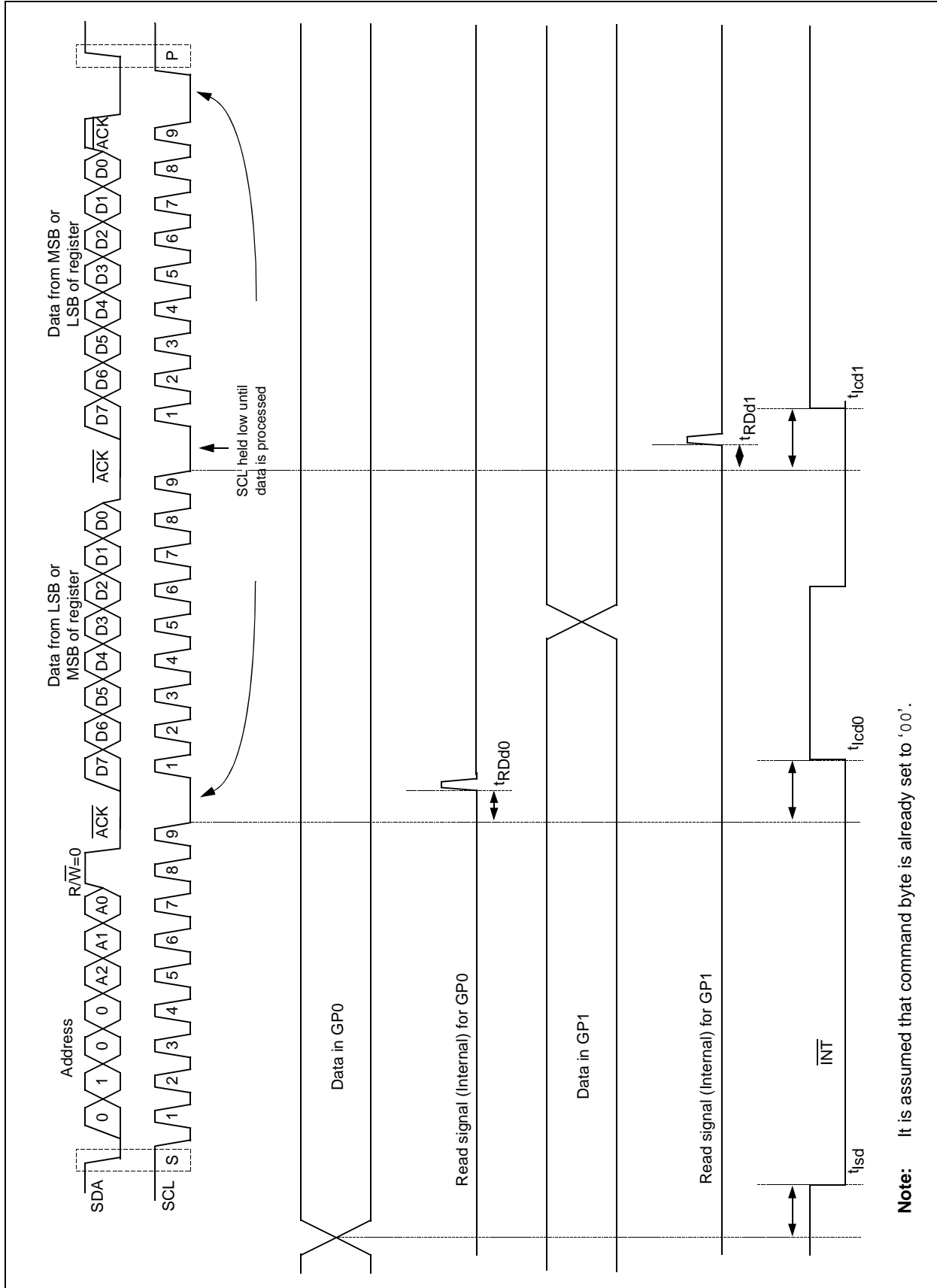
**Note:** The bus must remain free until after the ninth clock pulse for a minimum of 12  $\mu$ s (see Table 2-5 and Figure 2-4).

**FIGURE 1-6: READ FROM CONFIGURATION REGISTER**

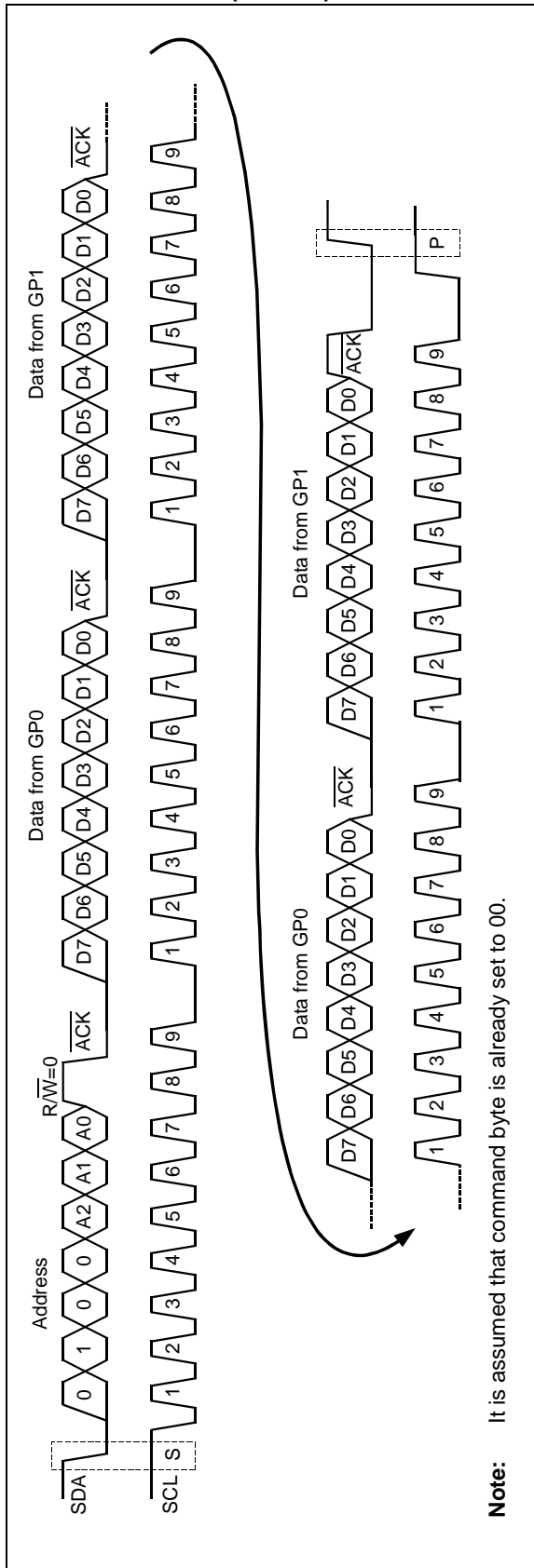


# MCP23016

FIGURE 1-7: READ FROM INPUT PORTS (CASE 1)



**FIGURE 1-8: READ FROM INPUT PORTS (CASE 2)**



# MCP23016

---

NOTES:

## 2.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Ambient temperature under bias .....	-55 to +125°C
Storage temperature .....	-65°C to +150°C
Voltage on any pin with respect to VSS .....	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS .....	-0.3V to +6.5V
Total power dissipation ( <b>Note 1</b> ) .....	1.0 W
Maximum current out of VSS pin .....	300 mA
Maximum current into VDD pin .....	250 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0, or V <sub>I</sub> > VDD) .....	± 20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0, or V <sub>O</sub> > VDD) .....	± 20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin .....	25 mA
Maximum current sunk by combined PORTS .....	200 mA
Maximum current sourced by combined PORTS .....	200 mA

**Note 1:** Power dissipation is calculated as follows:

$$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OI} \times I_{OL})$$

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# MCP23016

## 2.1 DC Characteristics

TABLE 2-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature: $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001	Supply Voltage	VDD	2.0	—	5.5	V	
D002	Standby Current	IDD	—	0.4		mA	IARES = 1
D003	Standby Current	IPD	—	25		$\mu\text{A}$	IARES = 0
<b>Input Low Voltage</b>							
D004	I/O ports TTL buffer	VIL	VSS	—	0.15 VDD	V	For entire VDD range $4.5\text{V} \leq V_{\text{DD}} \leq 5.5\text{V}$
D004A			VSS	—	0.8V		
D005	Schmitt Trigger buffer		VSS	—	0.2 VDD	V	
<b>Input High Voltage</b>							
D006	I/O ports TTL buffer	VIH	2.0	—	VDD	V	$4.5\text{V} \leq V_{\text{DD}} \leq 5.5\text{V}$
D006A			$0.25 V_{\text{DD}} + 0.8\text{V}$	—	VDD	V	For entire VDD range
D007	Schmitt Trigger buffer		$0.8 V_{\text{DD}}$	—	VDD	V	For entire VDD range
<b>Input Leakage Current</b>							
D008	I/O ports	IIL	—	—	$\pm 1.0$	$\mu\text{A}$	$V_{\text{SS}} \leq V_{\text{PIN}} \leq V_{\text{DD}}$ , Pin at hi-impedance
D009	CLK		—	—	$\pm 5.0$	$\mu\text{A}$	$V_{\text{SS}} \leq V_{\text{PIN}} \leq V_{\text{DD}}$
<b>Output Low Voltage</b>							
D010	I/O Ports	VOL	—	—	0.6	V	$I_{\text{OL}} = 8.5 \text{ mA}$ , $V_{\text{DD}} = 4.5\text{V}$
<b>Output High Voltage</b>							
D010	I/O Ports	VOH	$V_{\text{DD}} - 0.7$	—	—	V	$I_{\text{OH}} = 3.0 \text{ mA}$ , $V_{\text{DD}} = 4.5\text{V}$
D011	VDD start voltage to ensure internal POR signal	VPOR	—	VSS	—	V	
D012	VDD rise rate to ensure internal POR signal	SVDD	0.05	-	—	V/ms	<b>Note 1</b>
	DC Trip Point	VTPOR	1.5	1.7	1.9	V	DC Slow Ramp
D012	VDD rise rate to ensure internal POR signal with PWRT enabled	SVDD	0.05	—	—	V/ms	<b>Note 1</b>
	DC Current Draw	IPOR	—	5.0	—	$\mu\text{A}$	At 5.0V (1 $\mu\text{A}$ /Volt typical)

**Note 1:** These parameters are characterized but not tested.

**2:** Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

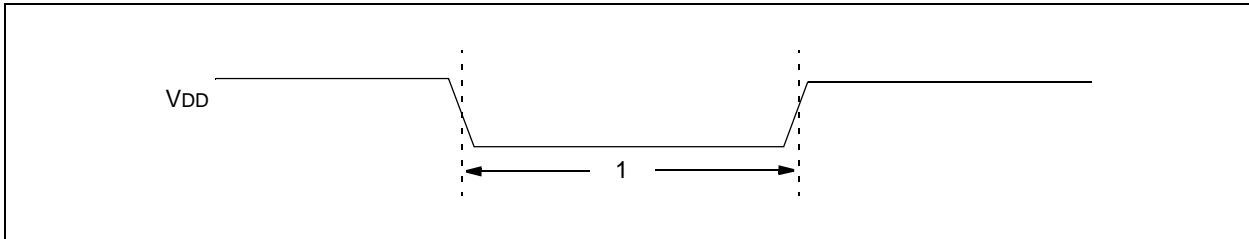
**3:** Standby current is measured with all I/O in hi-impedance state and tied to VDD and VSS.

**4:** For RC CLK, current through REXT is not included. The current through the resistor can be estimated by the formula

$$I_r = V_{\text{DD}} / 2 R_{\text{EXT}} \text{ (mA) with } R_{\text{EXT}} \text{ in kohm.}$$

**5:** Negative current is defined as coming out of the pin.

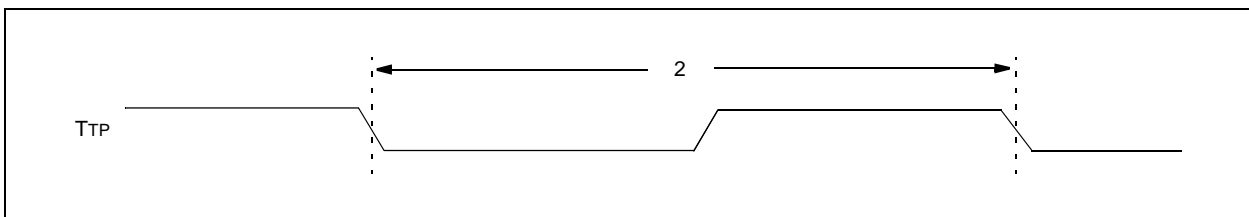
**FIGURE 2-1: RESPONSE TIME**



**TABLE 2-2: RESPONSE TIME**

Parameter No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
1		Response Time	100	—	—	ns	Minimum time where a VDD transition from 5.0V to 0.0V to 5.0V will cause a RESET. All times less than 100 ns will be filtered.

**FIGURE 2-2: TEST POINT CLOCK TIMING**



**TABLE 2-3: TEST POINT CLOCK TIMING**

Parameter No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	FTP	TP pin Frequency	—	1.0	—	MHz	Measured at TP pin, IARES = '1'.
2	TTP	TP pin CLK Period	—	1.0	—	μs	Measured at TP pin, IARES = '1'.

† Data in "Typ" column is at 5V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

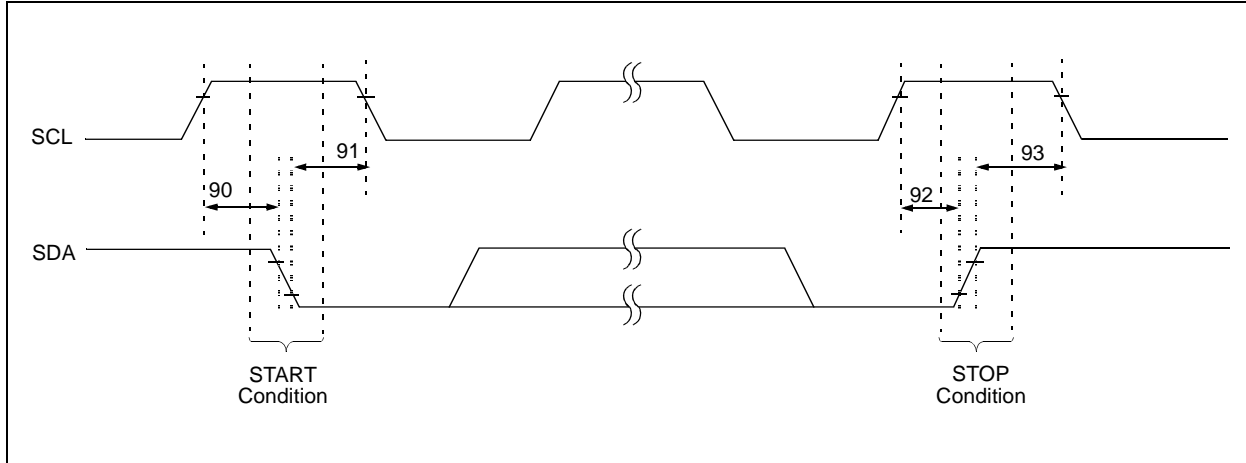
**TABLE 2-4: POWER-UP TIMER REQUIREMENTS**

Parameter No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
3	TPWRT	Power-up Timer Period	—	72	—	ms	

† Data in "Typ" column is at 5V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

# MCP23016

**FIGURE 2-3: I<sup>2</sup>C BUS START/STOP BITS TIMING**

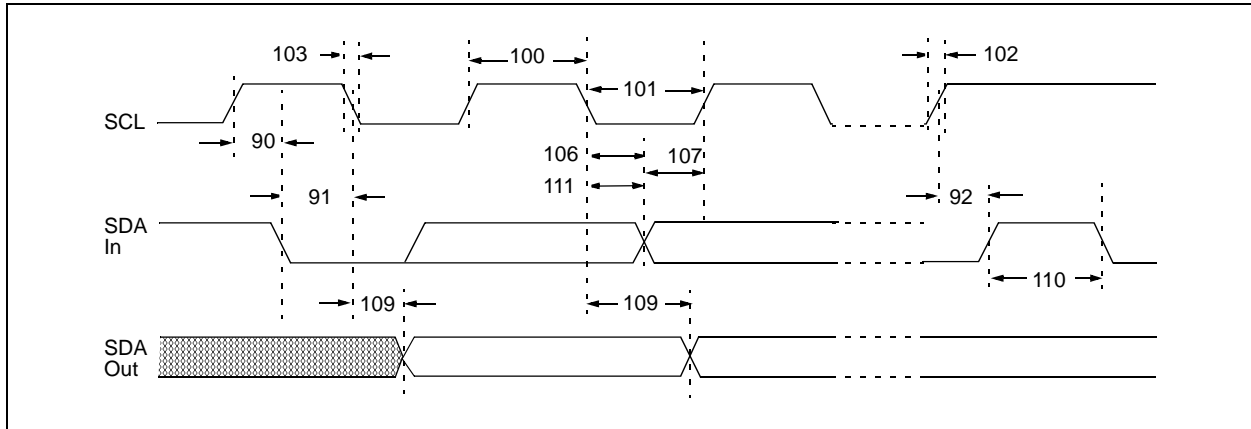


**TABLE 2-5: I<sup>2</sup>C BUS START/STOP BITS REQUIREMENTS**

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions	
90	T <sub>SU:STA</sub>	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for Repeated START condition ( <b>Note 1</b> )
			400 kHz mode	600	—	—		
91	T <sub>HD:STA</sub>	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period, the first clock pulse is generated ( <b>Note 1</b> )
			400 kHz mode	600	—	—		
92	T <sub>SU:STO</sub>	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93	T <sub>HD:STO</sub>	STOP condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

**Note 1:** These parameters are characterized but not tested.

**FIGURE 2-4: I<sup>2</sup>C BUS DATA TIMING**



# MCP23016

**TABLE 2-5: I<sup>2</sup>C BUS DATA REQUIREMENTS**

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions	
100	THIGH	Clock High Time	100 kHz mode	4.0	—	μs	<b>(Note 1)</b>
			400 kHz mode	0.6	—	μs	
101	TLOW	Clock Low Time	100 kHz mode	4.7	—	μs	<b>(Note 1)</b>
			400 kHz mode	1.3	—	μs	
102	TR	SDA and SCL Rise Time	100 kHz mode	—	1000	ns	<b>(Note 1)</b> CB is specified to be from 10 - 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
103	TF	SDA and SCL Fall Time	100 kHz mode	—	300	ns	<b>(Note 1)</b> CB is specified to be from 10 - 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
90	TSU:STA	START Condition Setup Time	100 kHz mode	4.7	—	μs	Only relevant for repeated START condition <b>(Note 1)</b>
			400 kHz mode	0.6	—	μs	
91	THD:STA	START Condition Hold Time	100 kHz mode	4.0	—	μs	After this period, the first clock pulse is generated <b>(Note 1)</b>
			400 kHz mode	0.6	—	μs	
106	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	<b>(Note 1)</b>
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	<b>(Note 1) (Note 3)</b>
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP Condition Setup Time	100 kHz mode	4.7	—	μs	<b>(Note 1)</b>
			400 kHz mode	0.6	—	μs	
109	TAA	Output Valid from Clock	100 kHz mode	—	3500	ns	<b>(Note 1) (Note 2)</b>
			400 kHz mode	—	—	ns	
110	TBUF	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start <b>(Note 1)</b>
			400 kHz mode	1.3	—	μs	
	CB	Bus Capacitive Loading	—	400	pF		
111	TWAIT	Clock wait time after ninth pulse	100 kHz mode	12 μs	—	μs	Time the bus must remain free after the ninth clock pulse before a new transmission can start.
			400 kHz mode	12 μs	—	μs	

**Note 1:** These parameters are characterized but not tested.

- 2:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
- 3:** A Fast mode (400 kHz) I<sup>2</sup>C bus device can be used in a Standard mode (100 kHz) I<sup>2</sup>C bus system, but the requirement TSU:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I<sup>2</sup>C bus specification), before the SCL line is released.

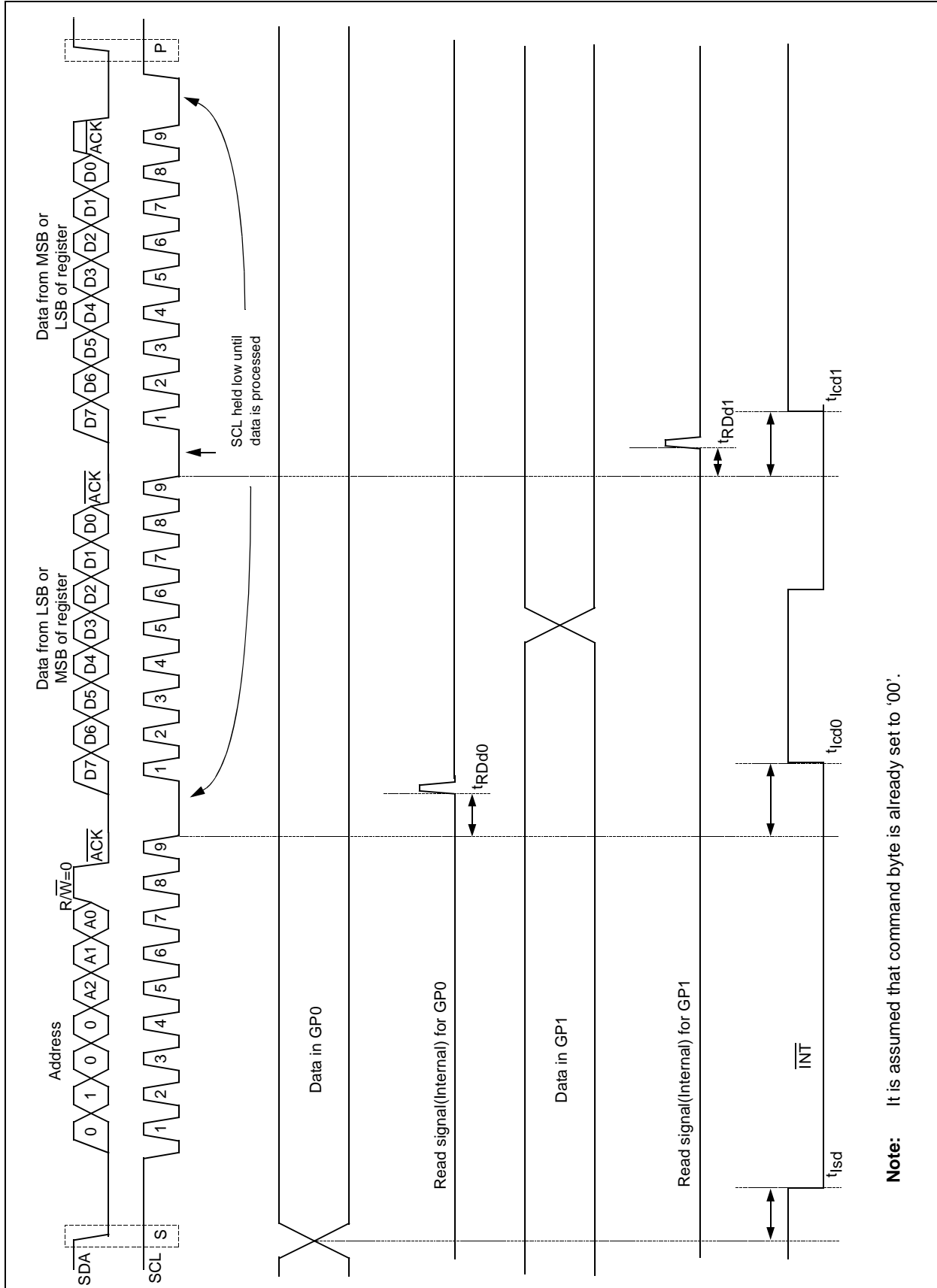
**TABLE 2-7: GP0 AND GP1 TIMING REQUIREMENTS**

Param No.	Symbol	Characteristic	Min	Typ.	Max	Units	Conditions
	t <sub>GPV0</sub>	GP0 output data valid time	—	40	—	μs	TP = 1 MHz
	t <sub>GPV1</sub>	GP1 output data valid time	—	50	—	μs	
	t <sub>RDd0</sub>	GP0 data read delay time	—	40	—	μs	
	t <sub>RDd1</sub>	GP1 data read delay time	—	50	—	μs	
	t <sub>ISD0</sub>	GP0 Interrupt set delay time	—	—	200	μs	IARES = 1, TP = 1 MHz
			—	—	32	ms	IARES = 0, TP = 1 MHz
	t <sub>ISD1</sub>	GP1 Interrupt set delay time	—	—	200	μs	IARES = 1, TP = 1 MHz
			—	—	32	ms	IARES = 0, TP = 1 MHz
	t <sub>LCD0</sub>	GP0 Interrupt clear delay time (for read)	—	100	—	μs	TP = 1 MHz
	t <sub>LCD1</sub>	GP1 Interrupt clear delay time (for read)	—	100	—	μs	

**Note 1:** These parameters are characterized but not tested.

# MCP23016

FIGURE 2-5: GP0 AND GP1 PORT TIMINGS



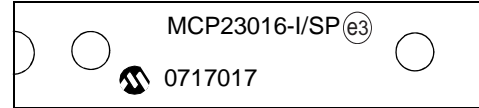
## 3.0 PACKAGE INFORMATION

### 3.1 Package Marking Information

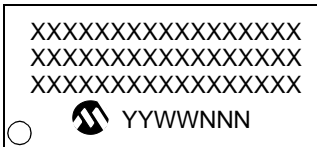
#### 28-Lead PDIP (Skinny DIP)



#### Example:



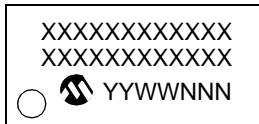
#### 28-Lead SOIC



#### Example:



#### 28-Lead SSOP



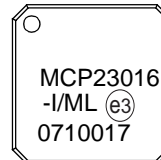
#### Example:



#### 28-Lead QFN



#### Example:

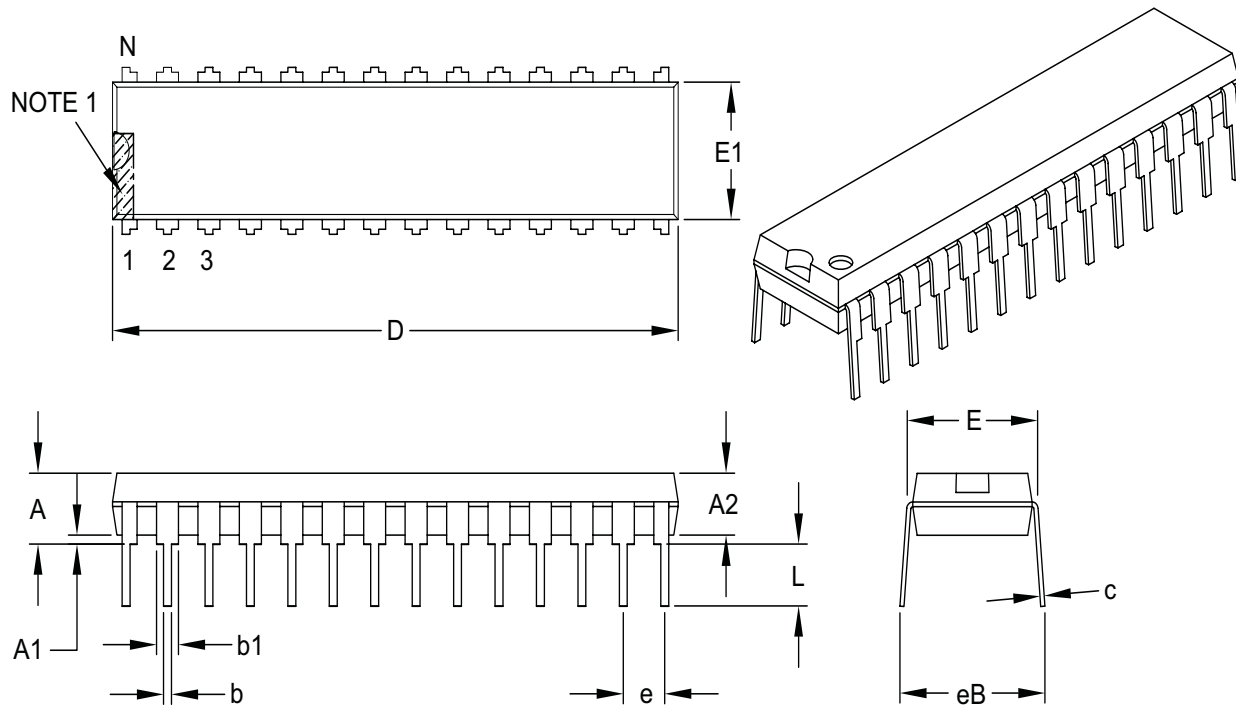


<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	* e3	This package is Pb-free. The Pb-free JEDEC designator ( ) can be found on the outer packaging for this package.
		e3
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

# MCP23016

## 28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



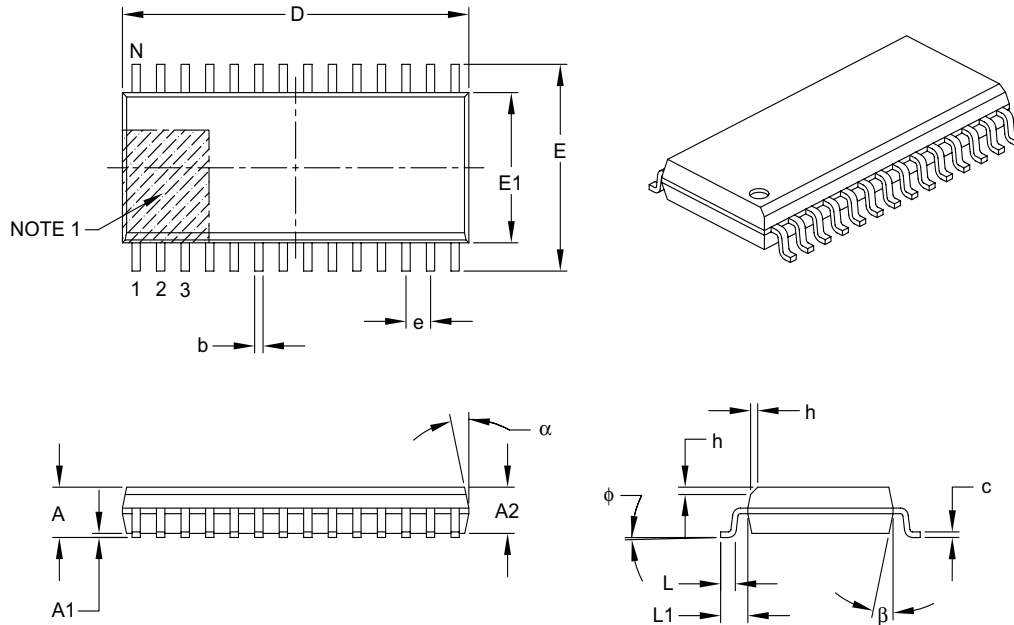
		Units	INCHES		
		Dimension Limits	MIN	NOM	MAX
Number of Pins	N		28		
Pitch	e		.100 BSC		
Top to Seating Plane	A	–	–	.200	
Molded Package Thickness	A2	.120	.135	.150	
Base to Seating Plane	A1	.015	–	–	
Shoulder to Shoulder Width	E	.290	.310	.335	
Molded Package Width	E1	.240	.285	.295	
Overall Length	D	1.345	1.365	1.400	
Tip to Seating Plane	L	.110	.130	.150	
Lead Thickness	c	.008	.010	.015	
Upper Lead Width	b1	.040	.050	.070	
Lower Lead Width	b	.014	.018	.022	
Overall Row Spacing §	eB	–	–	.430	

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

## 28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1	1.40 REF		
Foot Angle Top	$\phi$	0°	–	8°
Lead Thickness	c	0.18	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	$\alpha$	5°	–	15°
Mold Draft Angle Bottom	$\beta$	5°	–	15°

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

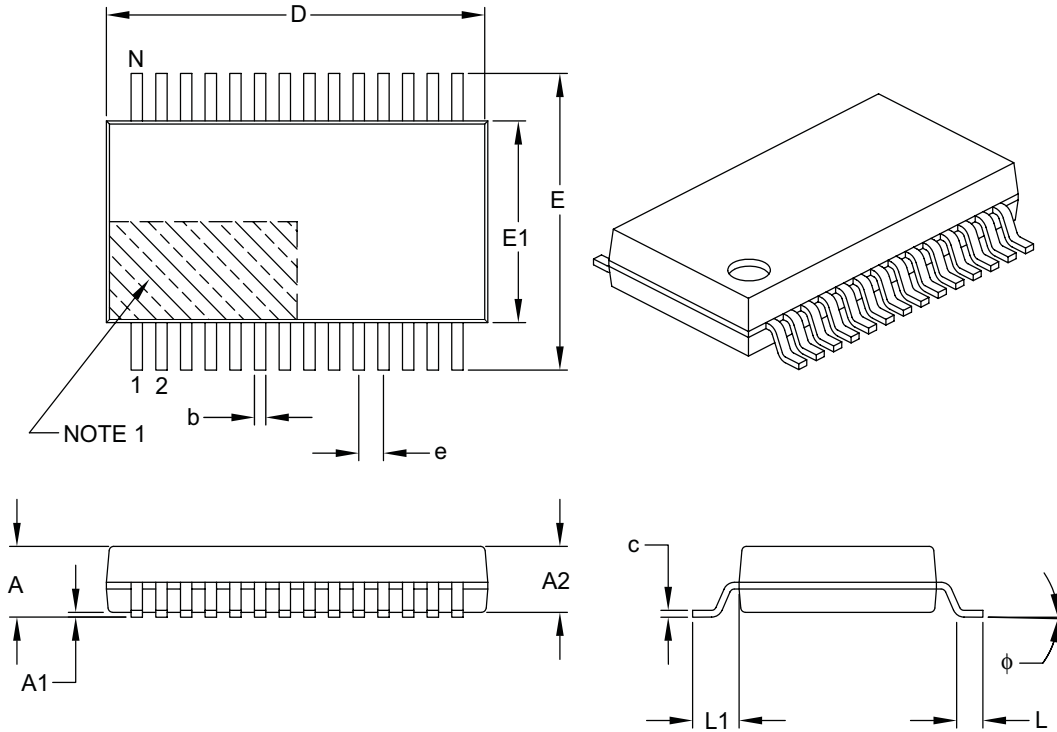
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

# MCP23016

## 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

**Notes:**

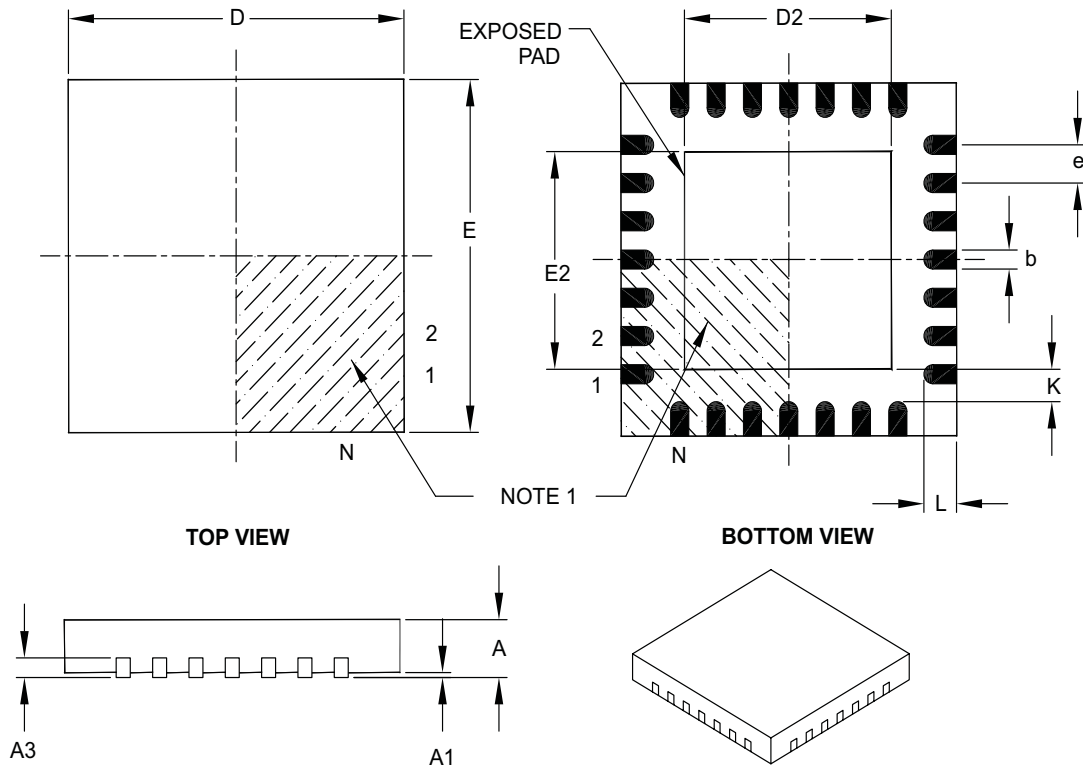
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

## 28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	–	–

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

# MCP23016

---

NOTES:

## APPENDIX A: REVISION HISTORY

### Revision A (December 2002)

Original data sheet for MCP23016 device.

### Revision B (September 2003)

1. Addition of Output Low Voltage section to Table 2-1 in Electrical Characteristics.
2. Addition of Output High Voltage section to Table 2-1 in Electrical Characteristics.

### Revision C (January 2007)

This revision includes updates to the packaging diagrams.

# MCP23016

---

NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information (e.g., on pricing or delivery) refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>
Device	Temperature Range	Package
Device:	DSTEMP: 16-Bit I <sup>2</sup> C I/O Expander	
Temperature Range:	I = -40°C to +85°C	
Package:	SP = Plastic DIP (300 mil Body), 28-lead SO = Plastic SOIC, Wide (300 mil Body), 28-lead SS = Plastic SOIC, (209 mil, 5.30mm), 28-lead ML = Plastic Quad, Flat No Leads (QFN), 28-lead	

**Examples:**

- a) DSTEMP-I/P: Industrial Temperature, PDIP package.
- a) DSTEMP-I/SO: Industrial Temperature, SOIC package.
- a) DSTEMP-I/SS: Industrial Temperature, SOIC package.
- a) DSTEMP-I/ML: Industrial Temperature, QFN package.

# MCP23016

---

NOTES:

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

**Trademarks**

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart, rPIC, and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


AmpLab, FilterLab, Migratable Memory, MXDEV, MXLAB, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Linear Active Thermistor, Mindi, MiWi, MPASM, MPLIB, MPLINK, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rLAB, rPICDEM, Select Mode, Smart Serial, SmartTel, Total Endurance, UNI/O, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2007, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949:2002 ==**

*Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona, Gresham, Oregon and Mountain View, California. The Company's quality system processes and procedures are for its PIC<sup>®</sup> MCUs and dsPIC DSCs, KEELOQ<sup>®</sup> code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*



---

---

## WORLDWIDE SALES AND SERVICE

---

---

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://support.microchip.com>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

#### Atlanta

Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

#### Boston

Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

#### Chicago

Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

#### Dallas

Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

#### Detroit

Farmington Hills, MI  
Tel: 248-538-2250  
Fax: 248-538-2260

#### Kokomo

Kokomo, IN  
Tel: 765-864-8360  
Fax: 765-864-8387

#### Los Angeles

Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

#### Santa Clara

Santa Clara, CA  
Tel: 408-961-6444  
Fax: 408-961-6445

#### Toronto

Mississauga, Ontario,  
Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

#### Asia Pacific Office

Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

#### Australia - Sydney

Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

#### China - Beijing

Tel: 86-10-8528-2100  
Fax: 86-10-8528-2104

#### China - Chengdu

Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

#### China - Fuzhou

Tel: 86-591-8750-3506  
Fax: 86-591-8750-3521

#### China - Hong Kong SAR

Tel: 852-2401-1200  
Fax: 852-2401-3431

#### China - Qingdao

Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

#### China - Shanghai

Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

#### China - Shenyang

Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

#### China - Shenzhen

Tel: 86-755-8203-2660  
Fax: 86-755-8203-1760

#### China - Shunde

Tel: 86-757-2839-5507  
Fax: 86-757-2839-5571

#### China - Wuhan

Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

#### China - Xian

Tel: 86-29-8833-7250  
Fax: 86-29-8833-7256

### ASIA/PACIFIC

#### India - Bangalore

Tel: 91-80-4182-8400  
Fax: 91-80-4182-8422

#### India - New Delhi

Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

#### India - Pune

Tel: 91-20-2566-1512  
Fax: 91-20-2566-1513

#### Japan - Yokohama

Tel: 81-45-471-6166  
Fax: 81-45-471-6122

#### Korea - Gumi

Tel: 82-54-473-4301  
Fax: 82-54-473-4302

#### Korea - Seoul

Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

#### Malaysia - Penang

Tel: 60-4-646-8870  
Fax: 60-4-646-5086

#### Philippines - Manila

Tel: 63-2-634-9065  
Fax: 63-2-634-9069

#### Singapore

Tel: 65-6334-8870  
Fax: 65-6334-8850

#### Taiwan - Hsin Chu

Tel: 886-3-572-9526  
Fax: 886-3-572-6459

#### Taiwan - Kaohsiung

Tel: 886-7-536-4818  
Fax: 886-7-536-4803

#### Taiwan - Taipei

Tel: 886-2-2500-6610  
Fax: 886-2-2508-0102

#### Thailand - Bangkok

Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

#### Austria - Wels

Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

#### Denmark - Copenhagen

Tel: 45-4450-2828  
Fax: 45-4485-2829

#### France - Paris

Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

#### Germany - Munich

Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

#### Italy - Milan

Tel: 39-0331-742611  
Fax: 39-0331-466781

#### Netherlands - Drunen

Tel: 31-416-690399  
Fax: 31-416-690340

#### Spain - Madrid

Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91



#### UK - Wokingham

Tel: 44-118-921-5869  
Fax: 44-118-921-5820

12/08/06

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View MCP23016-I/SS on WIN SOURCE](#)
-  [Microchip Technology](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management