



**THE DATASHEET OF
74LVTH273MTC**



74LVTH273

Low Voltage Octal D-Type Flip-Flop with Clear

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold on the data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Outputs source/sink $-32\text{mA}/+64\text{mA}$
- Functionally compatible with the 74 series 273
- Latch-up performance exceeds 500mA
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 1000V

General Description

The LVTH273 is a high-speed, low-power positive-edge-triggered octal D-type flip-flop featuring separate D-type inputs for each flip-flop. A buffered Clock (CP) and Clear (CLR) are common to all flip-flops.

The state of each D-type input, one setup time before the positive clock transition, is transferred to the corresponding flip-flop's output.


The LVTH273 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These octal flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH273 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

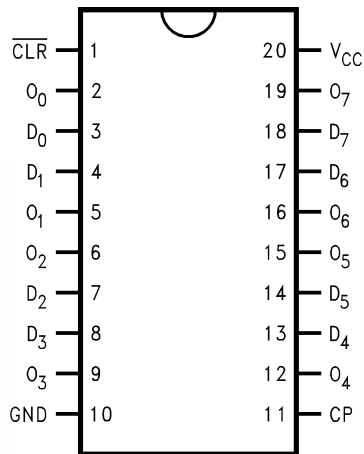
Ordering Information

Order Number	Package Number	Package Description
74LVTH273WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVTH273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVTH273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



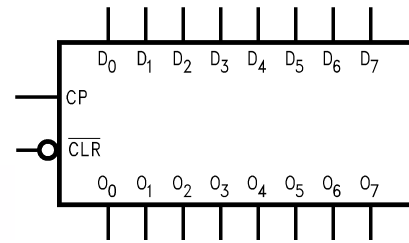
Pin Description

Pin Names	Description
D ₀ –D ₇	Data Inputs
CP	Clock Pulse Input
$\overline{\text{CLR}}$	Clear
O ₀ –O ₇	Outputs

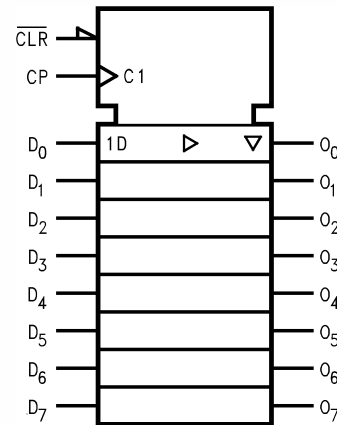
Functional Description

The LVTH273 consists of eight positive-edge-triggered flip-flops with individual D-type inputs. The buffered Clock and Clear are common to all flip-flops. The eight flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. When the Clock is either HIGH or LOW, the D-input signal has no effect at the output. When the Clear ($\overline{\text{CLR}}$) is LOW, all Outputs will be forced LOW.

Logic Symbols



IEEE/IEC



Truth Table

Inputs			Outputs
D _n	CP	$\overline{\text{CLR}}$	O _n
H	↗	H	H
L	↗	H	L
X	H or L	H	O ₀
X	X	L	L

H = HIGH Voltage Level

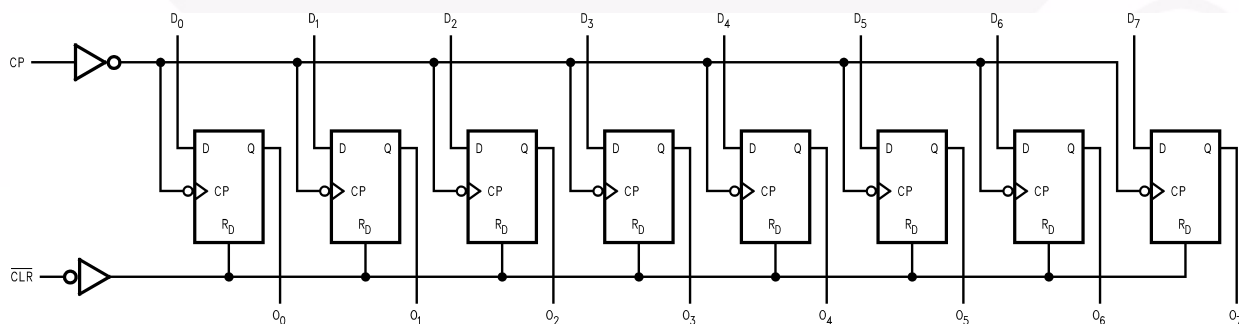
L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Transition

O₀ = Previous O₀ before HIGH-to-LOW of CP

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5V to +4.6V
V_I	DC Input Voltage	-0.5V to +7.0V
V_O	DC Output Voltage: Output in HIGH or LOW State ⁽¹⁾	-0.5V to +7.0V
I_{IK}	DC Input Diode Current, $V_I < GND$	-50mA
I_{OK}	DC Output Diode Current, $V_O < GND$	-50mA
I_O	DC Output Current, $V_O > V_{CC}$ Output at HIGH State	64mA
	Output at LOW State	128mA
I_{CC}	DC Supply Current per Supply Pin	±64mA
I_{GND}	DC Ground Current per Ground Pin	±128mA
T_{STG}	Storage Temperature	-65°C to +150°C

Note:

- I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		-32	mA
I_{OL}	LOW-Level Output Current		64	mA
T_A	Free-Air Operating Temperature	-40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$, $V_{CC} = 3.0V$	0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = -40°C to +85°C			Units	
				Min.	Typ. ⁽²⁾	Max.		
V _{IK}	Input Clamp Diode Voltage	2.7	I _I = -18mA			-1.2	V	
V _{IH}	Input HIGH Voltage	2.7–3.6	V _O ≤ 0.1V or	2.0			V	
V _{IL}	Input LOW Voltage	2.7–3.6	V _O ≥ V _{CC} - 0.1V			0.8	V	
V _{OH}	Output HIGH Voltage	2.7–3.6	I _{OH} = -100μA	V _{CC} - 0.2			V	
		2.7	I _{OH} = -8mA	2.4				
		3.0	I _{OH} = -32mA	2.0				
V _{OL}	Output LOW Voltage	2.7	I _{OL} = 100μA			0.2	V	
			I _{OL} = 24mA			0.5		
		3.0	I _{OL} = 16mA			0.4		
			I _{OL} = 32mA			0.5		
			I _{OL} = 64mA			0.55		
I _{I(HOLD)}	Bushold Input Minimum Drive	3.0	V _I = 0.8V	75			μA	
			V _I = 2.0V	-75				
I _{I(OD)}	Bushold Input Over-Drive Current to Change State	3.0	⁽³⁾	500			μA	
			⁽⁴⁾	-500				
I _I	Input Current	3.6	V _I = 5.5V			10	μA	
		Control Pins	3.6	V _I = 0V or V _{CC}				±1
			Data Pins	3.6	V _I = 0V			
		V _I = V _{CC}						1
I _{OFF}	Power Off Leakage Current	0	0V ≤ V _I or V _O ≤ 5.5V			±100	μA	
I _{CCH}	Power Supply Current	3.6	Outputs HIGH			0.19	mA	
I _{CCL}	Power Supply Current	3.6	Outputs LOW			5	mA	
ΔI _{CC}	Increase in Power Supply Current ⁽⁵⁾	3.6	One Input at V _{CC} - 0.6V, Other Inputs at V _{CC} or GND			0.2	mA	

Notes:

- All typical values are at V_{CC} = 3.3V, T_A = 25°C.
- An external driver must source at least the specified current to switch from LOW-to-HIGH.
- An external driver must sink at least the specified current to switch from HIGH-to-LOW.
- This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics⁽⁶⁾

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C			Units
			C _L = 50pF, R _L = 500Ω	Min.	Typ.	Max.	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	(7)		0.8		V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	(7)		-0.8		V

Notes:

6. Characterized in SOIC package. Guaranteed parameter, but not tested.
 7. Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter		T _A = -40°C to +85°C, C _L = 50pF, R _L = 500Ω					Units
			V _{CC} = 3.3V ± 0.3V			V _{CC} = 2.7V		
			Min.	Typ. ⁽⁸⁾	Max.	Min.	Max.	
f _{MAX}	Maximum Clock Frequency		150			150		MHz
t _{PLH}	Propagation Delay. CP to O _n		1.7		4.9	1.7	5.5	ns
t _{PHL}			1.9		4.8	1.9	5.1	
t _{PHL}	Propagation Delay $\overline{\text{CLR}}$ to O _n		1.6		4.8	1.6	5.4	ns
t _W	Pulse Duration		3.3			3.3		ns
t _S	Setup Time	Data HIGH or LOW before CP	2.3			2.7		ns
		$\overline{\text{CLR}}$ HIGH before CP	2.3			2.7		
t _H	Hold Time	Data HIGH or LOW after CP	0			0		ns

Note:

8. All typical values are at V_{CC} = 3.3V, T_A = 25°C.

Capacitance⁽⁹⁾

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 0V, V _I = 0V or V _{CC}	3	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}	6	pF

Note:

9. Capacitance is measured at frequency f = 1MHz, per MIL-STD-883B, Method 3012.

Physical Dimensions



Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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Physical Dimensions (Continued)



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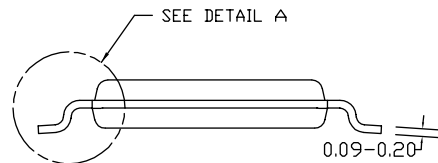
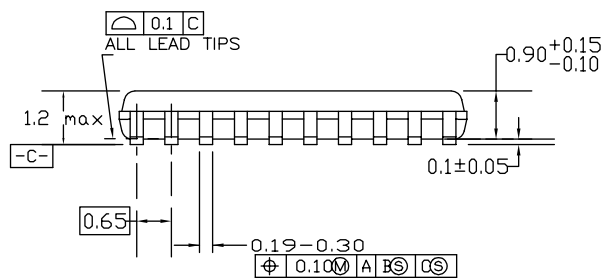
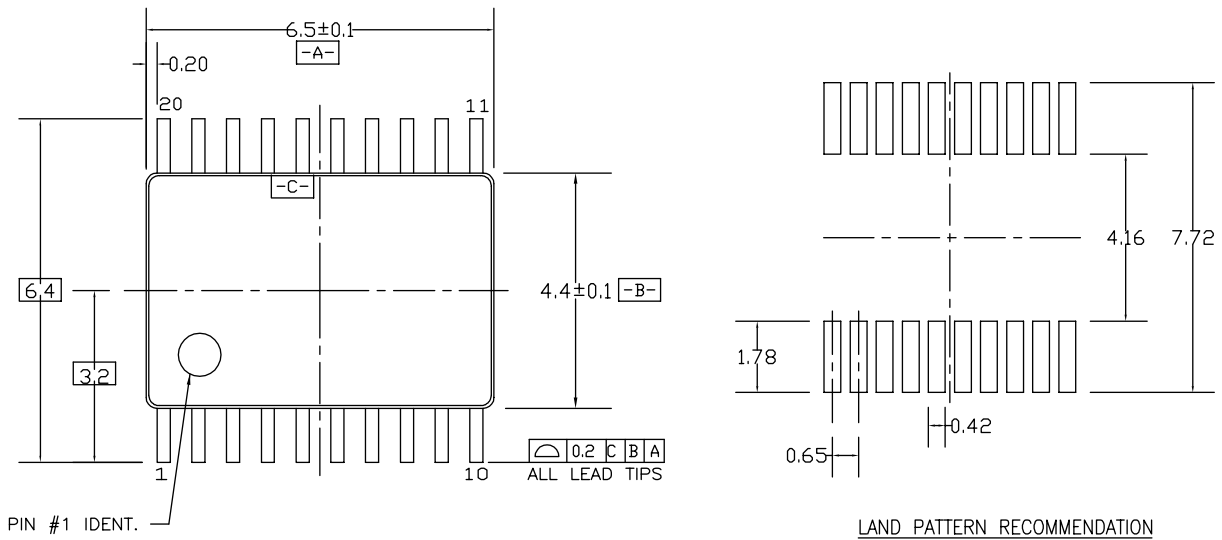
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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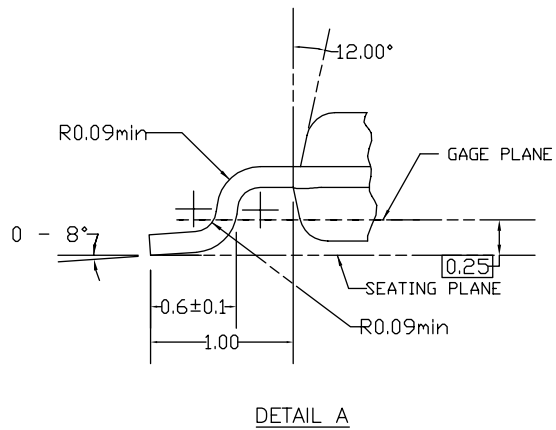
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Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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