



# THE DATASHEET OF MC74ACT74MELG



# MC74AC74, MC74ACT74

## Dual D-Type Positive Edge-Triggered Flip-Flop

The MC74AC74/74ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

### Asynchronous Inputs:

- LOW input to  $\bar{S}_D$  (Set) sets Q to HIGH level
- LOW input to  $\bar{C}_D$  (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

### Features

- Outputs Source/Sink 24 mA
- 'ACT74 Has TTL Compatible Inputs
- These are Pb-Free Devices

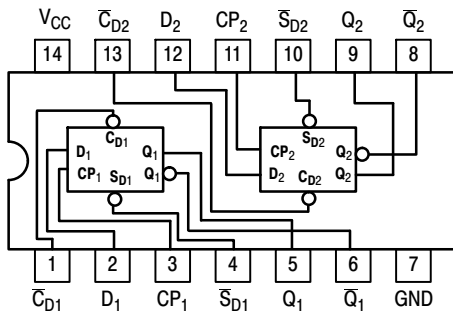


Figure 1. Pinout: 14-Lead Packages Conductors (Top View)

### PIN ASSIGNMENT

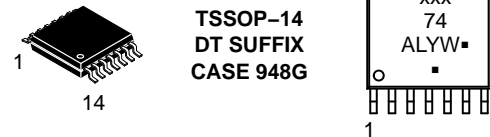
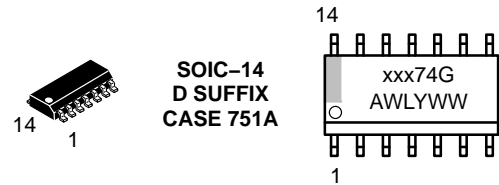
PIN	FUNCTION
D <sub>1</sub> , D <sub>2</sub>	Data Inputs
CP <sub>1</sub> , CP <sub>2</sub>	Clock Pulse Inputs
$\bar{C}_D1$ , $\bar{C}_D2$	Direct Clear Inputs
$\bar{S}_D1$ , $\bar{S}_D2$	Direct Set Inputs
Q <sub>1</sub> , $\bar{Q}_1$ , Q <sub>2</sub> , $\bar{Q}_2$	Outputs



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

### MARKING DIAGRAMS





xxx = AC or ACT  
 A = Assembly Location  
 WL or L = Wafer Lot  
 Y = Year  
 WW or W = Work Week  
 G or ■ = Pb-Free Package  
 (Note: Microdot may be in either location)


### ORDERING INFORMATION

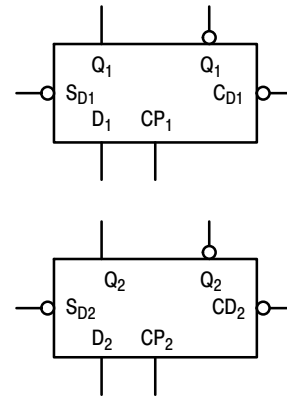
See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

# MC74AC74, MC74ACT74

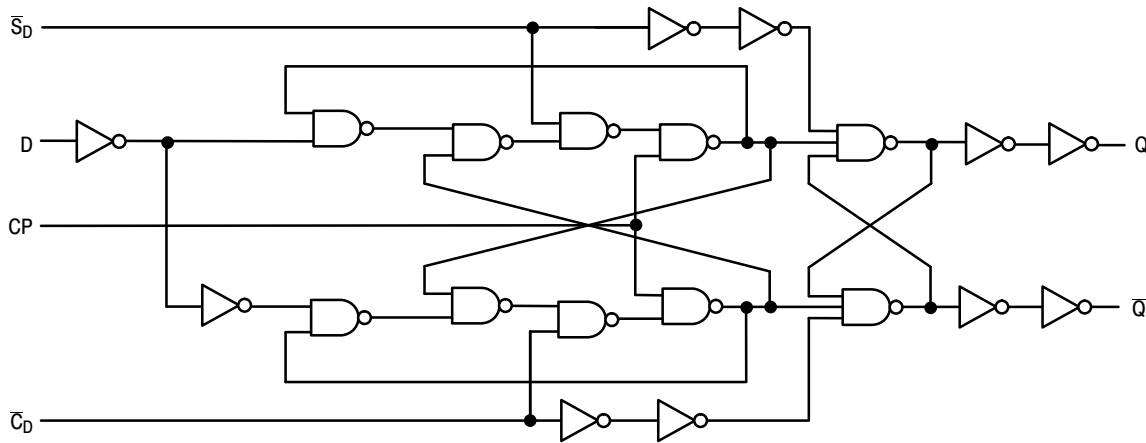
**TRUTH TABLE (Each Half)**

Inputs				Outputs	
$\bar{S}_D$	$\bar{C}_D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H		H	H	L
H	H		L	L	H
H	H	L	X	$Q_0$	$\bar{Q}_0$

NOTE: H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial;  
 = LOW-to-HIGH Clock Transition  
 $Q_0(\bar{Q}_0)$  = Previous Q( $\bar{Q}$ ) before LOW-to-HIGH Transition of Clock



**Figure 2. Logic Symbol**



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Figure 3. Logic Diagram**

# MC74AC74, MC74ACT74

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>I</sub>	DC Input Voltage	-0.5 ≤ V <sub>I</sub> ≤ V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	DC Output Voltage (Note 1)	-0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	±20	mA
I <sub>OK</sub>	DC Output Diode Current	±50	mA
I <sub>O</sub>	DC Output Sink/Source Current	±50	mA
I <sub>CC</sub>	DC Supply Current per Output Pin	±50	mA
I <sub>GND</sub>	DC Ground Current per Output Pin	±50	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
T <sub>J</sub>	Junction temperature under Bias	+150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 2)	SOIC TSSOP 125 170	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 85°C	SOIC TSSOP 125 170	mW
MSL	Moisture Sensitivity	Level 1	
F <sub>R</sub>	Flammability Rating	Oxygen Index: 30% – 35% UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5) > 2000 > 200 > 1000	V
I <sub>Latch-Up</sub>	Latch-Up Performance	Above V <sub>CC</sub> and Below GND at 85°C (Note 6)	±100 mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I<sub>O</sub> absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51-7.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V <sub>CC</sub>	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Ref. to GND)	0	-	V <sub>CC</sub>	V	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Note ) 'AC Devices except Schmitt Inputs	V <sub>CC</sub> @ 3.0 V	-	150	-	ns/V
		V <sub>CC</sub> @ 4.5 V	-	40	-	
		V <sub>CC</sub> @ 5.5 V	-	25	-	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Note ) 'ACT Devices except Schmitt Inputs	V <sub>CC</sub> @ 4.5 V	-	10	-	ns/V
		V <sub>CC</sub> @ 5.5 V	-	8.0	-	
T <sub>J</sub>	Junction Temperature (PDIP)	-	-	140	°C	
T <sub>A</sub>	Operating Ambient Temperature Range	-40	25	85	°C	
I <sub>OH</sub>	Output Current – High	-	-	-24	mA	
I <sub>OL</sub>	Output Current – Low	-	-	24	mA	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. V<sub>in</sub> from 30% to 70% V<sub>CC</sub>; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V<sub>in</sub> from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

# MC74AC74, MC74ACT74

## DC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	74AC		74AC		Unit	Conditions		
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C					
			Typ	Guaranteed Limits						
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V			
		4.5	2.25	3.15	3.15					
		5.5	2.75	3.85	3.85					
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V			
		4.5	2.25	1.35	1.35					
		5.5	2.75	1.65	1.65					
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = -50 μA			
		4.5	4.49	4.4	4.4					
		5.5	5.49	5.4	5.4					
	3.0	-	2.56	2.46	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> -12 mA I <sub>OH</sub> -24 mA -24 mA				
							4.5	-	3.86	3.76
							5.5	-	4.86	4.76
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA			
		4.5	0.001	0.1	0.1					
		5.5	0.001	0.1	0.1					
	3.0	-	0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 12 mA I <sub>OL</sub> 24 mA 24 mA				
							4.5	-	0.36	0.44
							5.5	-	0.36	0.44
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	-	±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND			
I <sub>OLD</sub>	†Minimum Dynamic Output Current	5.5	-	-	75	mA	V <sub>OLD</sub> = 1.65 V Max			
I <sub>OHD</sub>		5.5	-	-	-75	mA	V <sub>OHD</sub> = 3.85 V Min			
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	-	4.0	40	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND			

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V<sub>CC</sub>.

## AC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC			74AC		Unit	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	3.3	100	125	-	95	-	MHz	3-3
		5.0	140	160	-	125	-		
t <sub>PLH</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q <sub>n</sub>	3.3	5.0	8.0	12.5	4.0	13.0	ns	3-6
		5.0	3.5	6.0	9.0	3.0	10.0		
t <sub>PHL</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q <sub>n</sub>	3.3	4.0	10.5	12.0	3.5	13.5	ns	3-6
		5.0	3.0	8.0	9.5	2.5	10.5		
t <sub>PLH</sub>	Propagation Delay C <sub>Pn</sub> to Q <sub>n</sub> or Q <sub>n</sub>	3.3	4.5	8.0	13.5	4.0	16.0	ns	3-6
		5.0	3.5	6.0	10.0	3.0	10.5		
t <sub>PHL</sub>	Propagation Delay C <sub>Pn</sub> to Q <sub>n</sub> or Q <sub>n</sub>	3.3	3.5	8.0	14.0	3.5	14.5	ns	3-6
		5.0	2.5	6.0	10.0	2.5	10.5		

\*Voltage Range 3.3 V is 3.3 V ±0.3 V.

Voltage Range 5.0 V is 5.0 V ±0.5 V.

# MC74AC74, MC74ACT74

## AC OPERATING REQUIREMENTS

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC		74AC		Unit	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Typ	Guaranteed Minimum				
t <sub>s</sub>	Set-up Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	3.3	1.5	4.0	4.5	ns	3-9	
		5.0	1.0	3.0	3.0			
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	3.3	-2.0	0.5	0.5	ns	3-9	
		5.0	-1.5	0.5	0.5			
t <sub>w</sub>	C <sub>Pn</sub> or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.3	3.0	5.5	7.0	ns	3-6	
		5.0	2.5	4.5	5.0			
t <sub>rec</sub>	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3	-2.5	0	0	ns	3-9	
		5.0	-2.0	0	0			

\*Voltage Range 3.3 V is 3.3 V ±0.3 V.  
Voltage Range 5.0 V is 5.0 V ±0.5 V.

# MC74AC74, MC74ACT74

## DC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	74ACT		74ACT		Unit	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V	
		5.5	1.5	2.0	2.0			
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V	
		5.5	1.5	0.8	0.8			
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I <sub>OUT</sub> = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5	-	3.86	3.76	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> -24 mA	
		5.5	-	4.86	4.76			
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5	-	0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 24 mA	
		5.5	-	0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	-	±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
ΔI <sub>CCT</sub>	Additional Max. I <sub>CC</sub> /Input	5.5	0.6	-	1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V	
I <sub>OLD</sub>	†Minimum Dynamic Output Current	5.5	-	-	75	mA	V <sub>OLD</sub> = 1.65 V Max	
I <sub>OHD</sub>		5.5	-	-	-75	mA	V <sub>OHD</sub> = 3.85 V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	-	4.0	40	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

## AC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT			74ACT		Unit	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	5.0	145	210	-	125	-	MHz	3-3
t <sub>PLH</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q <sub>n</sub>	5.0	3.0	5.5	9.5	2.5	10.5	ns	3-6
t <sub>PHL</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q <sub>n</sub>	5.0	3.0	6.0	10.0	3.0	11.5	ns	3-6
t <sub>PLH</sub>	Propagation Delay C <sub>Pn</sub> to Q <sub>n</sub> or Q <sub>n</sub>	5.0	4.0	7.5	11.0	4.0	13.0	ns	3-6
t <sub>PHL</sub>	Propagation Delay C <sub>Pn</sub> to Q <sub>n</sub> or Q <sub>n</sub>	5.0	3.5	6.0	10.0	3.0	11.5	ns	3-6

\*Voltage Range 5.0 V is 5.0 V ±0.5 V.

# MC74AC74, MC74ACT74

## AC OPERATING REQUIREMENTS

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT		74ACT		Unit	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Typ	Guaranteed Minimum				
t <sub>s</sub>	Set-up Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	5.0	1.0	3.0	3.5	ns	3-9	
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	5.0	-0.5	1.0	1.0	ns	3-9	
t <sub>w</sub>	C <sub>Pn</sub> or C <sub>Dn</sub> or S <sub>Dn</sub> Pulse Width	5.0	3.0	5.0	6.0	ns	3-6	
t <sub>rec</sub>	Recovery Time C <sub>Dn</sub> or S <sub>Dn</sub> to CP	5.0	-2.5	0	0	ns	3-9	

\*Voltage Range 5.0 V is 5.0 V ±0.5 V.

## CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0 V
C <sub>PD</sub>	Power Dissipation Capacitance	35	pF	V <sub>CC</sub> = 5.0 V

## ORDERING INFORMATION

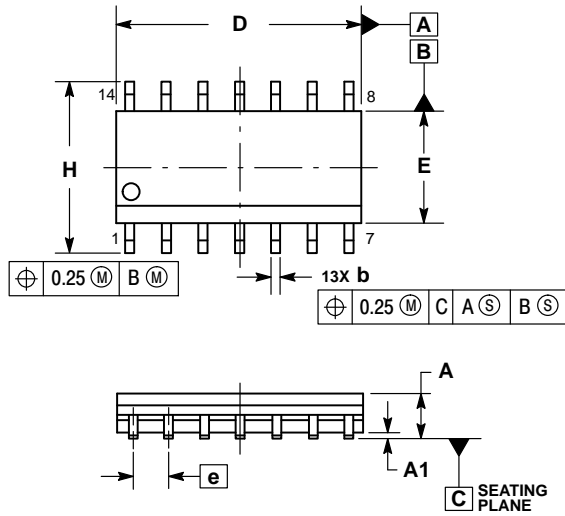
Device	Package	Shipping†
MC74AC74DG	SOIC-14 (Pb-Free)	55 Units/Rail
MC74AC74DR2G	SOIC-14 (Pb-Free)	2500/Tape & Reel
MC74AC74DTR2G	TSSOP-14 (Pb-Free)	2500/Tape & Reel
MC74ACT74DG	SOIC-14 (Pb-Free)	55 Units/Rail
MC74ACT74DR2G	SOIC-14 (Pb-Free)	2500/Tape & Reel
MC74ACT74DTR2G	TSSOP-14 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MC74AC74, MC74ACT74

## PACKAGE DIMENSIONS

SOIC-14 NB  
CASE 751A-03  
ISSUE K

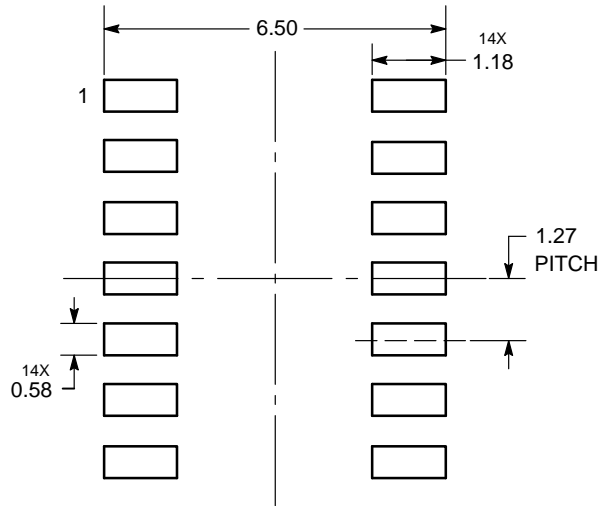


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

### SOLDERING FOOTPRINT\*



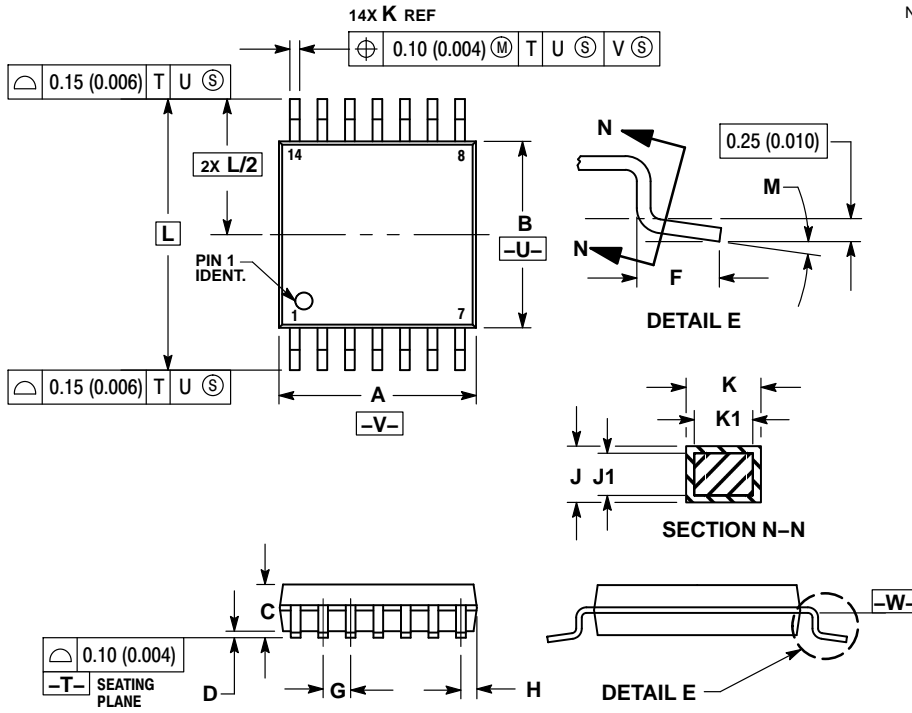
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74AC74, MC74ACT74

## PACKAGE DIMENSIONS

TSSOP-14  
CASE 948G  
ISSUE B

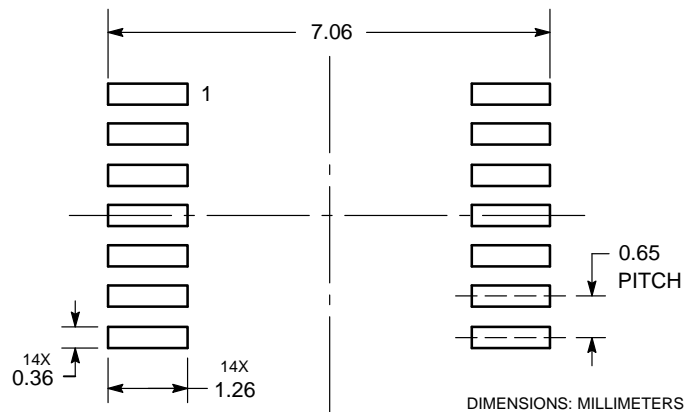


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0° 8°		0° 8°	

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74AC74, MC74ACT74

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View MC74ACT74MELG on WIN SOURCE](#)

 [ON Semiconductor](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management