THE DATASHEET OF

AD7225KRZ-REEL

LC²MOS Quad 8-Bit DAC with Separate Reference Inputs

AD7225

FEATURES

Four 8-bit DACs with output amplifiers
Separate reference input for each DAC
Microprocessor compatible with double-buffered inputs
Simultaneous update of all 4 outputs
Operates with single or dual supplies
Extended temperature range operation
No user trims required
Skinny 24-lead PDIP, CERDIP, SOIC, and SSOP packages
28-lead PLCC package

FUNCTIONAL BLOCK DIAGRAM

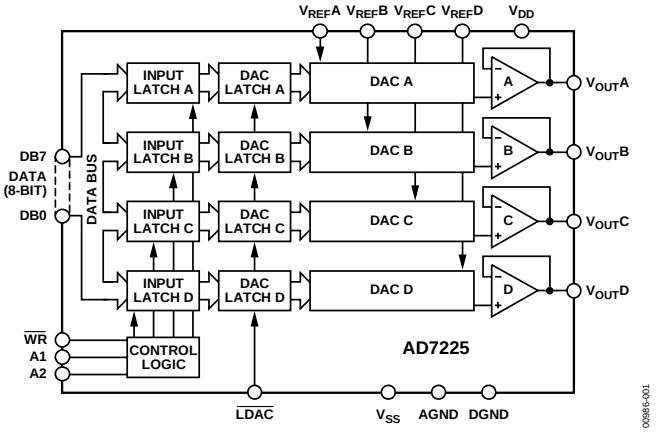

Figure 1.

GENERAL DESCRIPTION

The AD7225 contains four 8-bit voltage output digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. Each DAC has a separate reference input terminal. No external trims are required to achieve full specified performance for the part.

The double-buffered interface logic consists of two 8-bit registers per channel—an input register and a DAC register. Control Input A0 and Control Input A1 determine which input register is loaded when $\overline{WR}$ goes low. Only the data held in the DAC registers determines the analog outputs of the converters. The double-buffering allows simultaneous update of all four outputs under control of $\overline{LDAC}$. All logic inputs are TTL and CMOS (5 V) level compatible, and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from 2 V to 12.5 V when using dual supplies. The part is also specified for single-supply operation using a reference of 10 V. Each output buffer amplifier is capable of developing 10 V across a 2 kΩ load.

The AD7225 is fabricated on an all ion-implanted, high speed, linear-compatible CMOS (LC²MOS) process, which is specifically developed to integrate high speed digital logic circuits and precision analog circuitry on the same chip.

PRODUCT HIGHLIGHTS

1. DACs and Amplifiers on CMOS Chip.
   The single-chip design of four 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one end of the package and all digital inputs at the other.
2. Single- or Dual-Supply Operation.
   The voltage-mode configuration of the AD7225 allows single-supply operation. The part can also be operated with dual supplies, giving enhanced performance for some parameters.
3. Versatile Interface Logic.
   The AD7225 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. The double-buffered interface allows simultaneous update of the four outputs.
4. Separate Reference Input for Each DAC.
   The AD7225 offers great flexibility in dealing with input signals, with a separate reference input provided for each DAC and each reference having variable input voltage capability.

Rev. C

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SPECIFICATIONS

V_{DD} = 11.4 V to 16.5 V, V_{SS} = −5 V ± 10%; AGND = DGND = 0 V; $V_{REF}x$ = +2 V to (V_{DD} − 4 V)[1], unless otherwise noted. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	K, B Versions[2]	L, C Versions[2]	Unit	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±1	LSB max	V_{DD} = 15 V ± 5%, V_{REF} = 10 V
Relative Accuracy	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed monotonic
Full-Scale Error	±1	±1/2	LSB max	
Full-Scale Temperature Coefficient	±5	±5	ppm/°C typ	V_{DD} = 14 V to 16.5 V, V_{REF} = 10 V
Zero Code Error	±30	±20	mV max	
Zero Code Error Temperature Coefficient	±30	±30	µV/°C typ	
REFERENCE INPUT				
Voltage Range	2 to (V_{DD} − 4)	2 to (V_{DD} − 4)	V min to V max	
Input Resistance	11	11	kΩ min	
Input Capacitance[3]	50	50	pF max	Occurs when each DAC is loaded with all 1s
Channel-to-Channel Isolation[3]	60	60	dB min	V_{REF} = 10 V p-p sine wave at 10 kHz
AC Feedthrough[3]	−70	−70	dB max	V_{REF} = 10 V p-p sine wave at 10 kHz
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[3]	2.5	2.5	V/µs min	
Voltage Output Settling Time[3]	4	4	µs max	V_{REF} = 10 V; settling time to ±½ LSB
Digital Feedthrough[3]	50	50	nV sec typ	Code transition all 0s to all 1s
Digital Crosstalk[3]	50	50	nV sec typ	Code transition all 0s to all 1s
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = 10 V
POWER SUPPLIES				
V_{DD} Range	11.4/16.5	11.4/16.5	V min to V max	For specified performance
I_{DD}	10	10	mA max	Outputs unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}	9	9	mA max	Outputs unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3,4]				
t_1	50	50	ns min	Write pulse width
t_2	0	0	ns min	Address to write setup time
t_3	0	0	ns min	Address to write hold time
t_4	50	50	ns min	Data valid to write setup time
t_5	0	0	ns min	Data valid to write hold time
t_6	50	50	ns min	Load DAC pulse width

[1] Maximum possible reference voltage.
[2] Temperature range is as follows for all versions: −40°C to +85°C.
[3] Sample tested at 25°C to ensure compliance.
[4] Switching characteristics apply for single-supply and dual-supply operation.

SINGLE SUPPLY

V_{DD} = 15 V ± 5%; V_{SS} = AGND = DGND = 0 V; $V_{REF}x$ = 10 V, unless otherwise noted. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	K, B Versions[1]	L, C Versions[1]	Unit	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error[2]	±2	±1	LSB max	
Differential Nonlinearity[2]	±1	±1	LSB max	Guaranteed monotonic
REFERENCE INPUT				
Voltage Range	2 to (V_{DD} − 4)	2 to (V_{DD} − 4)	V min to V max	
Input Resistance	11	11	kΩ min	
Input Capacitance[3]	50	50	pF max	Occurs when each DAC is loaded with all 1s
Channel-to-Channel Isolation[2, 3]	60	60	dB min	V_{REF} = 10 V p-p sine wave at 10 kHz
AC Feedthrough[2, 3]	−70	−70	dB max	V_{REF} = 10 V p-p sine wave at 10 kHz
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[3]	2	2	V/µs min	
Voltage Output Settling Time[3]	4	4	µs max	
Digital Feedthrough[2, 3]	10	10	nV sec typ	Code transition all 0s to all 1s
Digital Crosstalk[2, 3]	10	10	nV sec typ	Code transition all 0s to all 1s
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = 10 V
POWER SUPPLIES				
V_{DD} Range	14.25/15.75	14.25/15.75	V min to V max	For specified performance
I_{DD}	10	10	mA max	Outputs unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3]				
t_1	50	50	ns min	Write pulse width
t_2	0	0	ns min	Address to write setup time
t_3	0	0	ns min	Address to write hold time
t_4	50	50	ns min	Data valid to write setup time
t_5	0	0	ns min	Data valid to write hold time
t_6	50	50	ns min	Load DAC pulse width

[1] Temperature range is as follows for all versions: −40°C to +85°C.
[2] Sample tested at 25°C to ensure compliance.
[3] Switching characteristics apply for single-supply and dual-supply operation.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V, +17 V
V_{DD} to DGND	−0.3 V, +17 V
V_{DD} to V_{SS}	−0.3 V, +24 V
AGND to DGND	−0.3 V, V_{DD}
Digital Input Voltage to DGND	−0.3 V, V_{DD} + 0.3 V
V_{REF}x to AGND	−0.3 V, V_{DD} + 0.3 V
V_{OUT}x to AGND[1]	V_{SS}, V_{DD}
Power Dissipation (Any Package) to 75°C	500 mW
Derates Above 75°C by	2.0 mW/°C
Operating Temperature	
Commercial (K, L Versions)	−40°C to +85°C
Industrial (B, C Versions)	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Outputs can be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short-circuit current for a short to AGND or V_{SS} is 50 mA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

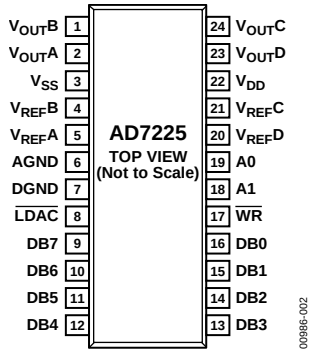


Figure 2. PDIP, SOIC, CERDIP, and SSOP

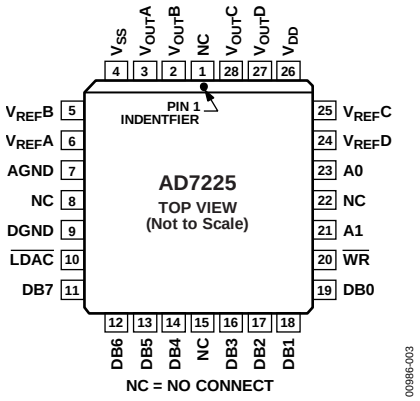


Figure 3. PLCC

Table 4. Pin Function Descriptions

Pin No.			
PDIP, SOIC, CERDIP, SSOP	**PLCC**	**Mnemonic**	**Description**
1	2	$V_{OUT}B$	DAC Channel B Voltage Output.
2	3	$V_{OUT}A$	DAC Channel A Voltage Output.
3	4	V_{SS}	Negative Power Supply Connection.
4	5	$V_{REF}B$	Reference Voltage Connection for DAC Channel B.
5	6	$V_{REF}A$	Reference Voltage Connection for DAC Channel A.
6	7	AGND	Analog Ground Reference Connection.
7	9	DGND	Digital Ground Reference Connection.
8	10	$\overline{LDAC}$	Active Low Load DAC Signal. DAC register data is latched on the rising edge of $\overline{LDAC}$.
9	11	DB7	Data Bit 7 (Most Significant Data Bit).
10	12	DB6	Data Bit 6.
11	13	DB5	Data Bit 5.
12	14	DB4	Data Bit 4.
13	16	DB3	Data Bit 3.
14	17	DB2	Data Bit 2.
15	18	DB1	Data Bit 1.
16	19	DB0	Data Bit 0 (Least Significant Data Bit).
17	20	$\overline{WR}$	Active Low Data Write Signal. Input register data is latched on the rising edge of $\overline{WR}$.
18	21	A1	DAC Address Select Pin.
19	23	A0	DAC Address Select Pin.
20	24	$V_{REF}D$	Reference Voltage Connection for DAC Channel D.
21	25	$V_{REF}C$	Reference Voltage Connection for DAC Channel C.
22	26	V_{DD}	Positive Power Supply Connection.
23	27	$V_{OUT}D$	DAC Channel D Voltage Output.
24	28	$V_{OUT}C$	DAC Channel C Voltage Output.
N/A	1, 8, 15, 22	NC	No Internal Connection.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 15 V, V_{SS} = −5 V, unless otherwise noted.

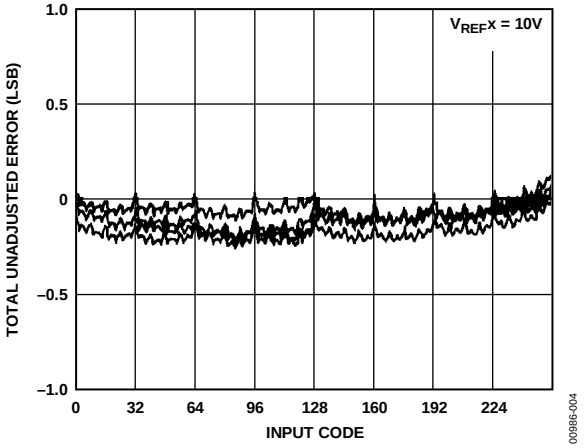


Figure 4. Channel-to-Channel Matching

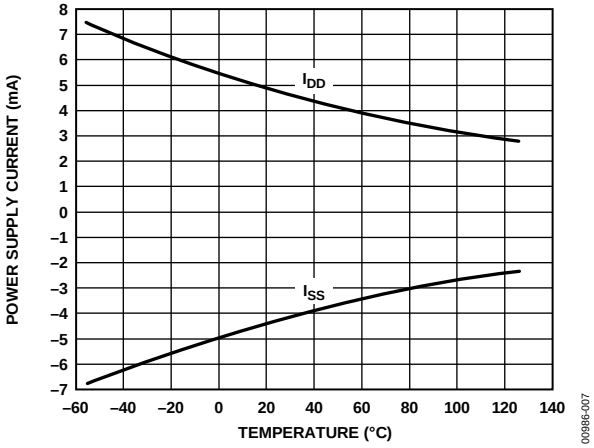


Figure 7. Power Supply Current vs. Temperature

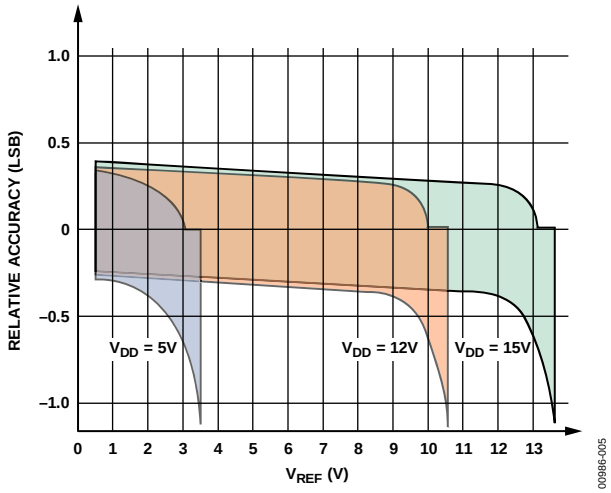


Figure 5. Relative Accuracy vs. V_{REF}

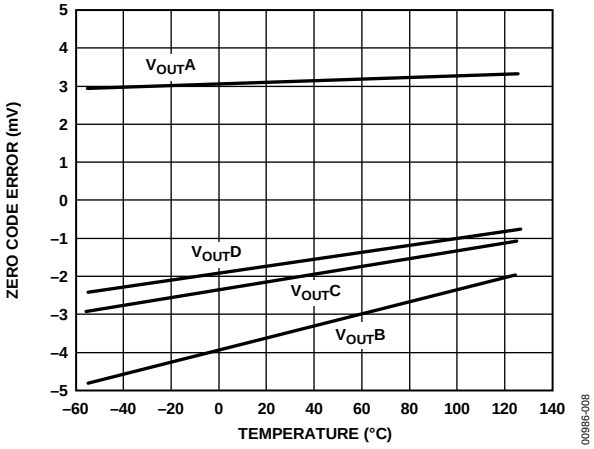


Figure 8. Zero Code Error vs. Temperature

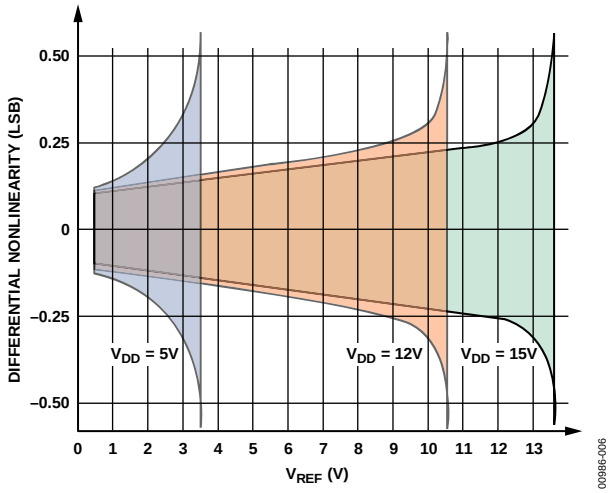


Figure 6. Differential Nonlinearity vs. V_{REF}

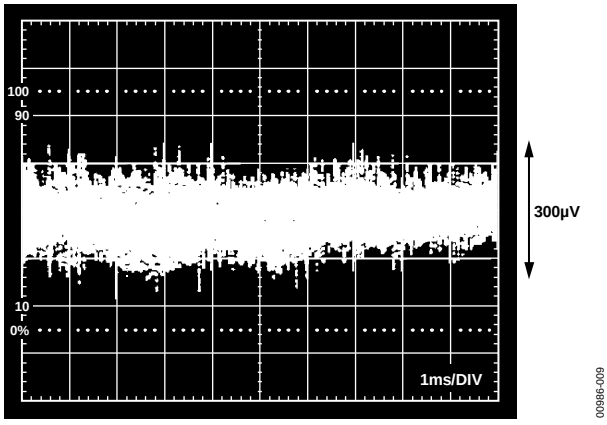


Figure 9. Broadband Noise

TERMINOLOGY

Total Unadjusted Error
Total unadjusted error is a comprehensive specification that includes full-scale error, relative accuracy, and zero code error. Maximum output voltage is V_{REF} − 1 LSB (ideal), where 1 LSB (ideal) is $V_{REF}/256$. The LSB size varies over the V_{REF} range. Therefore, the zero code error, relative to the LSB size, increases as V_{REF} decreases. Accordingly, the total unadjusted error, which includes the zero code error, also varies in terms of LSB over the V_{REF} range. As a result, total unadjusted error is specified for a fixed reference voltage of 10 V.

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after allowing for zero code error and full-scale error and is normally expressed in LSB or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum over the operating temperature range ensures monotonicity.

Digital Feedthrough
Digital feedthrough is the glitch impulse transferred to the output of the DAC due to a change in its digital input code. It is specified in nV sec and is measured at V_{REF} = 0 V.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter. It is specified in nV sec and is measured at V_{REF} = 0 V.

AC Feedthrough
AC feedthrough is the proportion of reference input signal that appears at the output of a converter when that DAC is loaded with all 0s.

Channel-to-Channel Isolation
Channel-to-channel isolation is the proportion of input signal from the reference of one DAC (loaded with all 1s) that appears at the output of one of the other three DACs (loaded with all 0s) The figure given is the worst case for the three other outputs and is expressed as a ratio in dB.

Full-Scale Error
Full-scale error is defined as

FSE = Measured Value − Zero Code Error − Ideal Value

CIRCUIT INFORMATION

DIGITAL-TO-ANALOG SECTION

The AD7225 contains four identical, 8-bit voltage mode digital-to-analog converters. Each DAC has a separate reference input. The output voltages from the converters have the same polarity as the reference voltages, allowing single-supply operation. A novel DAC switch pair arrangement on the AD7225 allows a reference voltage range from 2 V to 12.5 V on each reference input.

Each DAC consists of a highly stable, thin-film, R-2R ladder and eight high speed NMOS, single-pole, double-throw switches. The simplified circuit diagram for Channel A is shown in Figure 10. Note that AGND is common to all four DACs.

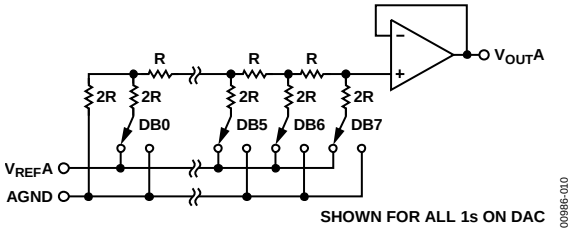


Figure 10. Digital-to-Analog Simplified Circuit Diagram

The input impedance at any of the reference inputs is code dependent and can vary from 11 kΩ minimum to infinity. The lowest input impedance at any reference input occurs when that DAC is loaded with Digital Code 01010101. Therefore, it is important that the reference presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminals is also code dependent and typically varies from 15 pF to 35 pF.

Each $V_{OUT}x$ pin can be considered a digitally programmable voltage source with an output voltage of

$$V_{OUTX} = D_X \times V_{REFX}$$

where D_X is a fractional representation of the digital input code and can vary from 0 to 255/256.

The output impedance is that of the output buffer amplifier.

OP AMP SECTION

Each voltage mode DAC output is buffered by a unity gain noninverting CMOS amplifier. This buffer amplifier is capable of developing 10 V across a 2 kΩ load and can drive capacitive loads of 3300 pF.

The AD7225 can be operated single or dual supply; operating with dual supplies results in enhanced performance in some parameters that cannot be achieved with single-supply operation. In single-supply operation (V_{SS} = 0 V = AGND), the sink capability of the amplifier, which is normally 400 μA, is reduced as the output voltage nears AGND. The full sink capability of 400 μA is maintained over the full output voltage range by tying V_{SS} to −5 V. This is shown in Figure 11.

Settling time for negative-going output signals approaching AGND is similarly affected by V_{SS}. Negative-going settling time for single-supply operation is longer than for dual-supply operation. Positive-going settling time is not affected by V_{SS}.

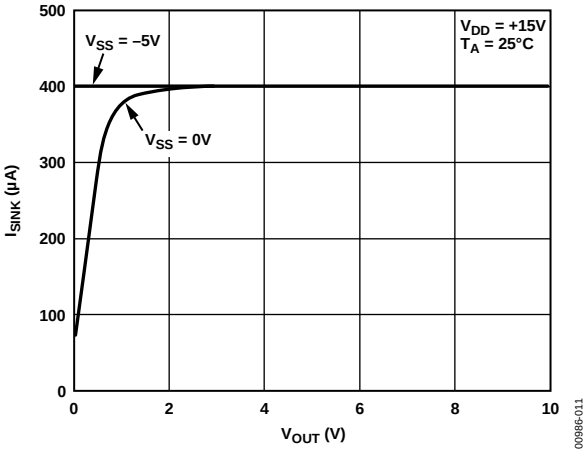


Figure 11. Variation of I_{SINK} with V_{OUT}

Additionally, the negative V_{SS} gives more headroom to the output amplifiers, which results in better zero code performance and improved slew rate at the output than can be obtained in the single-supply mode.

DIGITAL INPUTS SECTION

The AD7225 digital inputs are compatible with either TTL or 5 V CMOS levels. All logic inputs are static protected MOS gates with typical input currents of less than 1 nA. Internal input protection is achieved by an on-chip distributed diode between DGND and each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

INTERFACE LOGIC INFORMATION

The AD7225 contains two registers per DAC, an input register and a DAC register. The A0 and A1 address lines select which input register accepts data from the input port. When the $\overline{WR}$ signal is low, the input latches of the selected DAC are transparent. The data is latched into the addressed input register on the rising edge of $\overline{WR}$. Table 5 shows the addressing for the input registers on the AD7225.

Table 5. AD7225 Addressing

A1	A0	Selected Input Register
Low	Low	DAC A
Low	High	DAC B
High	Low	DAC C
High	High	DAC D

Only the data held in the DAC register determines the analog output of the converter. The $\overline{LDAC}$ signal is common to all four DACs and controls the transfer of information from the input registers to the DAC registers. Data is latched into all four DAC registers simultaneously on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ signal is level triggered and therefore the DAC registers can be made transparent by tying $\overline{LDAC}$ low (in this case, the outputs of the converters respond to the data held in their respective input latches). $\overline{LDAC}$ is an asynchronous signal and is independent of $\overline{WR}$. This is useful in many applications. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa), care must be taken to ensure that incorrect data is not latched through to the output. If $\overline{LDAC}$ is activated prior to the rising edge of $\overline{WR}$ (or $\overline{WR}$ occurs during $\overline{LDAC}$), $\overline{LDAC}$ must stay low for t_6 or longer after $\overline{WR}$ goes high to ensure correct data is latched through to the output. Table 6 shows the truth table for AD7225 operation. Figure 12 shows the input control logic for the part; the write cycle timing diagram is given in Figure 13.

Table 6. Truth Table

$\overline{WR}$	$\overline{LDAC}$	Function
High	High	No operation. Device not selected.
Low	High	Input register of selected DAC transparent.
↓	High	Input register of selected DAC latched.
High	Low	All four DAC registers Transparent (that is, outputs respond to data held in respective input registers). Input registers are latched.
High	↓	All four DAC registers latched.
Low	Low	DAC registers and selected input register transparent output follows input data for selected channel.

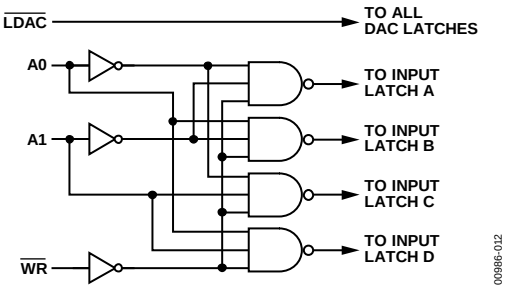


Figure 12. Input Control Logic

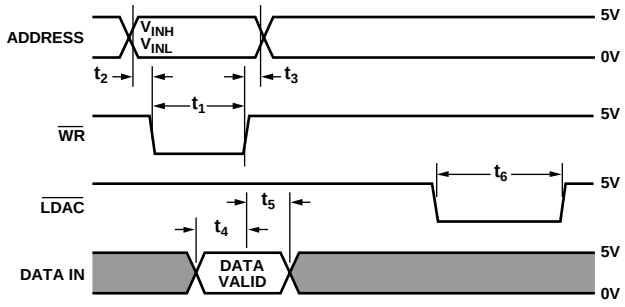


Figure 13. Write Cycle Timing Diagram

GROUND MANAGEMENT AND LAYOUT

Because the AD7225 contains four reference inputs that can be driven from ac sources (see the AC Reference Signal section), careful layout and grounding is important to minimize analog crosstalk between the four channels. The dynamic performance of the four DACs depends on the optimum choice of board layout. Figure 14 shows the relationship between input frequency and channel-to-channel isolation. Figure 15 shows a printed circuit board layout that minimizes crosstalk and feedthrough. The four input signals are screened by AGND. V_{REF} was limited to between 2 V and 3.24 V to avoid slew rate limiting effects from the output amplifier during measurements.

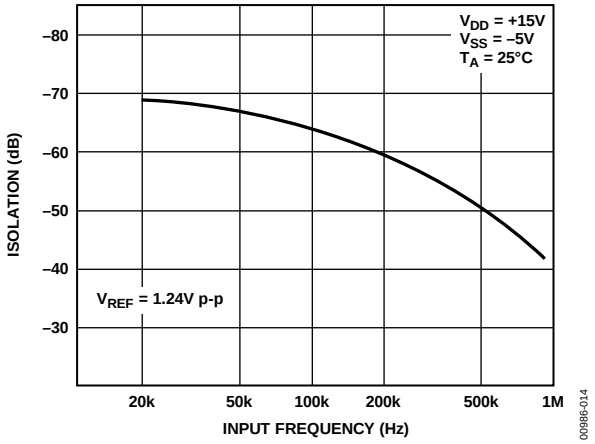


Figure 14. Channel-to-Channel Isolation

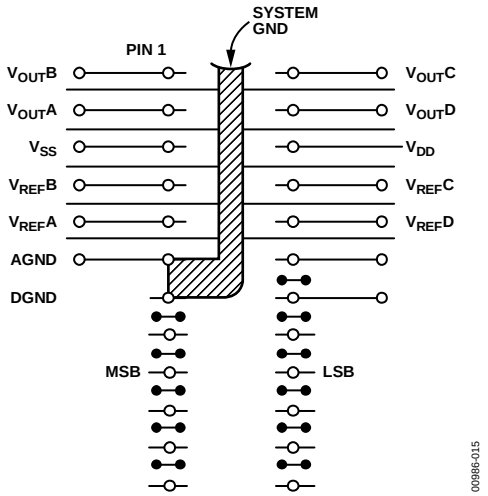


Figure 15. Suggested PCB Layout for AD7225, Component Side (Top View)

SPECIFICATION RANGES

For the AD7225 to operate to rated specifications, its input reference voltage must be at least 4 V below the V_{DD} power supply voltage. This voltage differential is the overhead voltage required by the output amplifiers.

The AD7225 is specified to operate over a V_{DD} range from 12 V ± 5% to 15 V ± 10% (that is, from 11.4 V to 16.5 V) with a V_{SS} of −5 V ± 10%. Operation is also specified for a single 15 V ± 5% V_{DD} supply. Applying a V_{SS} of −5 V results in improved zero-code error, improved output sink capability with outputs near AGND, and improved negative-going settling time.

Performance is specified over a wide range of reference voltages from 2 V to (V_{DD} − 4 V) with dual supplies. This allows a range of standard reference generators to be used, such as the AD780, a 2.5 V band gap reference, and the AD584, a precision 10 V reference. Note that an output voltage range of 0 V to 10 V requires a nominal 15 V ± 5% power supply voltage.

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for each channel of the AD7225, with the output voltage having the same positive polarity as $V_{REF}x$. The AD7225 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see the Op Amp Section, which outlines the advantages of having negative V_{SS}). Connections for the unipolar output operation are shown in Figure 16. The voltage at any of the reference inputs must never be negative with respect to DGND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table 7.

Note,

$$1\,LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$$

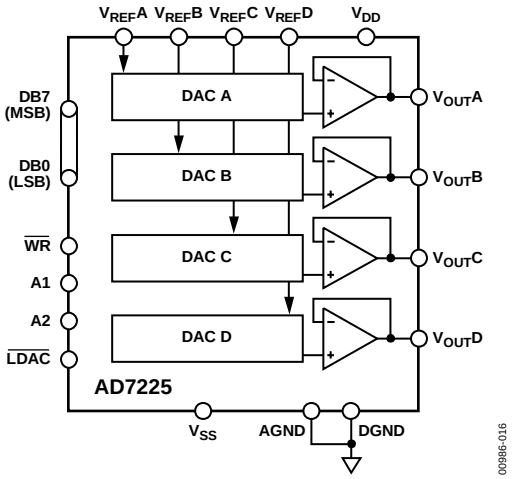


Figure 16. Unipolar Output Circuit

Table 7. Unipolar Code Table

DAC Latch Contents		
MSB	**LSB**	**Analog Output**
1111	1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000	0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000	0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111	1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000	0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000	0000	0 V

BIPOLAR OUTPUT OPERATION

Each of the DACs of the AD7225 can be individually configured to provide bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 17 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A (DAC Channel A) of the AD7225. In this case,

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \times \left(D_A V_{REF}\right) - \left(\frac{R2}{R1}\right) \times \left(V_{REF}\right)$$

With *R1 = R2*

$$V_{OUT} = \left(2D_A - 1\right) \times \left(V_{REF}\right)$$

where D_A is a fractional representation of the digital word in Latch A ($0 \le D_A \le 255/256$).

Mismatch between R1 and R2 causes gain and offset errors and, therefore, these resistors must match and track over temperature. The AD7225 can be operated in single supply or from positive/negative supplies. Table 8 shows the digital code vs. output voltage relationship for the circuit of Figure 17 with R1 = R2.

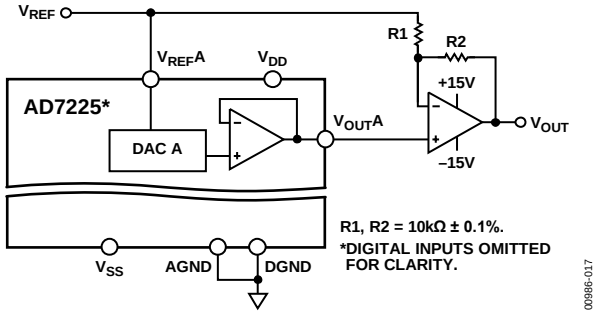


Figure 17. Bipolar Output Circuit

Table 8. Bipolar (Offset Binary) Code Table

DAC Latch Contents		
MSB	**LSB**	**Analog Output**
1111	1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000	0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000	0000	0 V
0111	1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000	0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000	0000	$-V_{REF}\left(\frac{128}{128}\right) = 1 - V_{REF}$

AGND BIAS

The AD7225 AGND pin can be biased above system ground (AD7225 DGND) to provide an offset zero analog output voltage level. Figure 18 shows a circuit configuration to achieve this for DAC Channel A of the AD7225. The output voltage, $V_{OUT}A$, can be expressed as:

$$V_{OUT}A = V_{BIAS} + D_A(V_{IN})$$

where D_A is a fractional representation of the digital word in DAC Latch A ($0 \le D_A \le 255/256$).

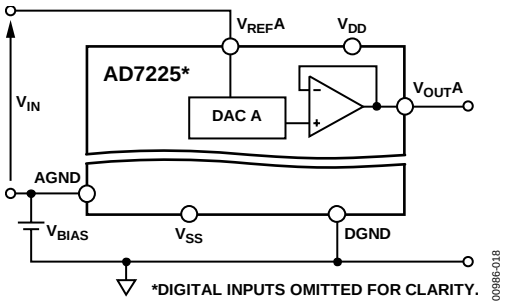


Figure 18. AGND Bias Circuit

For a given V_{IN}, increasing AGND above system ground reduces the effective $V_{DD} - V_{REF}$, which must be at least 4 V to ensure specified operation. Note that, because the AGND pin is common to all four DACs, this method biases up the output voltages of all the DACs in the AD7225. Note that V_{DD} and V_{SS} of the AD7225 should be referenced to DGND.

AC REFERENCE SIGNAL

In some applications, it may be desirable to have ac reference signals. The AD7225 has multiplying capability within the upper (V_{DD} – 4 V) and lower (2 V) limits of reference voltage when operated with dual supplies. Therefore, ac signals need to be ac-coupled and biased up before being applied to the reference inputs. Figure 19 shows a sine wave signal applied to $V_{REF}A$. For input signal frequencies up to 50 kHz, the output distortion typically remains less than 0.1%. The typical 3 dB bandwidth figure for small signal inputs is 800 kHz.

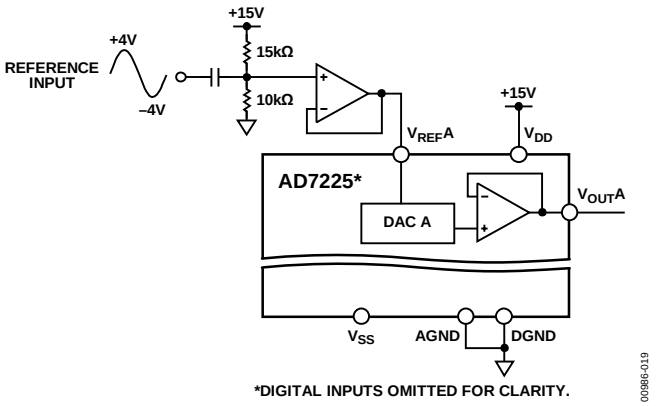


Figure 19. Applying an AC Signal to the AD7225

APPLICATIONS INFORMATION

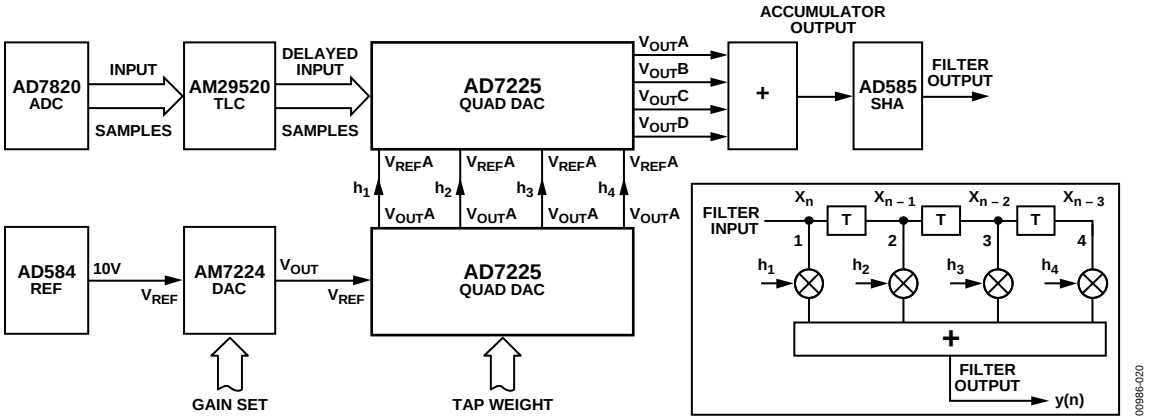


Figure 20. Programmable Transversal Filter

PROGRAMMABLE TRANSVERSAL FILTER

A discrete time filter can be described by either multiplication in the frequency domain or by convolution in the time domain:

$$Y(\omega) = H(\omega)X(\omega) \text{ or } y_n = \sum_{k=1}^{N} h_k X_{n-k+1}$$

The convolution sum can be implemented using the special structure known as the transversal filter (see Figure 21). It consists of an N-stage delay line with N taps weighted by N coefficients, the resulting products being accumulated to form the output. The tap weights or coefficients h_k are the nonzero elements of the impulse response and therefore determine the filter transfer function. A particular filter frequency response is realized by setting the coefficients to the appropriate values. This property leads to the implementation of transversal filters whose frequency response is programmable.

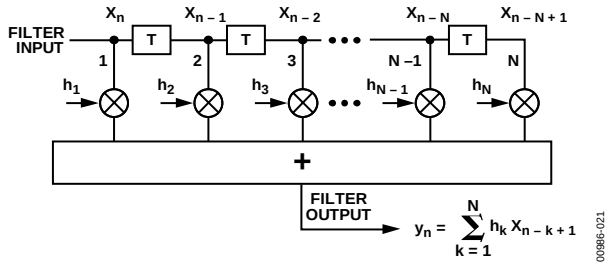


Figure 21. Transversal Filter

A four-tap programmable transversal filter can be implemented using the AD7225 (see Figure 20). The input signal is first sampled and converted to allow the tapped delay line function to be provided by the AM29520. The multiplication of delayed input samples by fixed, programmable up weights is accomplished by the AD7225, the four coefficients or reference inputs being set by the digital codes stored in the AD7226. The resultant products are accumulated to yield the convolution sum output sample, which is held by the AD585.

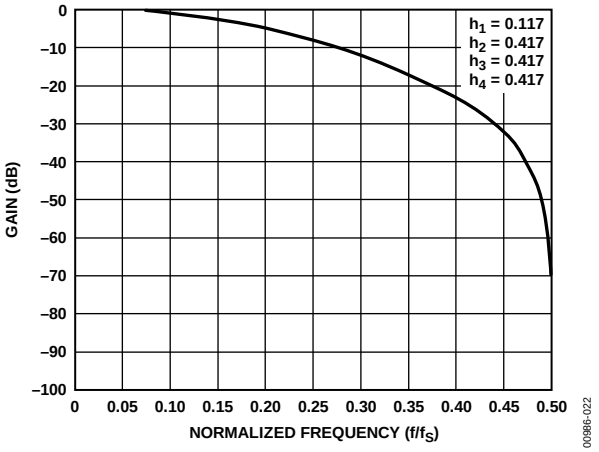


Figure 22. Predicted (Theoretical) Response

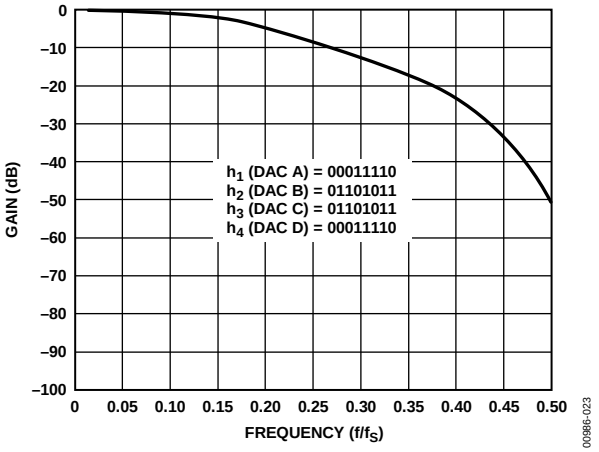


Figure 23. Actual Response

Low-pass, band-pass, and high-pass filters can be synthesized using this arrangement. The particular up weights needed for any desired transfer function can be obtained using the standard Remez exchange algorithm. Figure 22 shows the theoretical low-pass frequency response produced by a four-tap transversal filter with the coefficients indicated. Although the theoretical prediction does not take into account the quantization of the input samples and the truncation of the coefficients, neverthe-

less, there exists a good correlation with the actual performance of the transversal filter (see Figure 23).

DIGITAL WORD MULTIPLICATION

Because each DAC of the AD7225 has a separate reference input, the output of one DAC can be used as the reference input for another. This means that multiplication of digital words can be performed (with the result given in analog form). For example, if the output from DAC A is applied to $V_{REF}B$, then the output from DAC B, $V_{OUT}B$, can be expressed as:

$$V_{OUT}B = D_A \times D_B \times V_{REF}A$$

where D_A and D_B are the fractional representations of the digital words in DAC Latch A and DAC Latch B, respectively.

If $D_A = D_B = D$, the result is $D^2 \times V_{REF}A$.

In this manner, the four DACs can be used on their own or in conjunction with an external summing amplifier to generate complex waveforms. Figure 24 shows one such application. In this case, the output waveform, Y, is represented by

$$Y = -(x^4 + 2x^3 + 3x^2 + 2x + 4) \times V_{IN}$$

where x is the digital code that is applied to all four DAC latches.

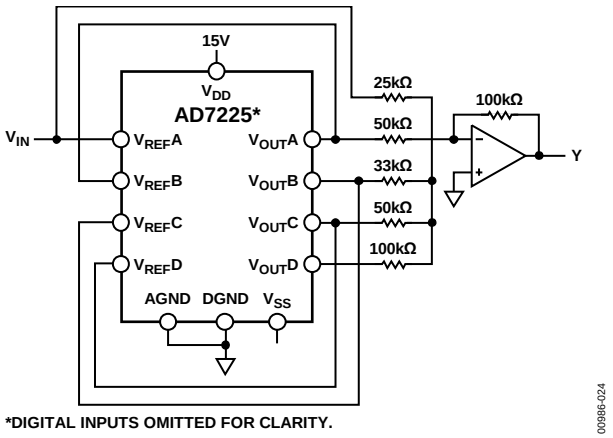


Figure 24. Complex Waveform Generation

MICROPROCESSER INTERFACE

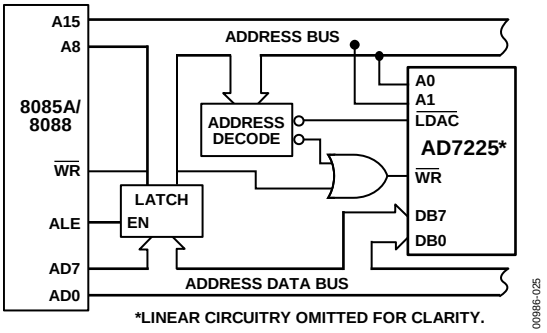


Figure 25. AD7225-to-8085A/8088 Interface, Double-Buffered Mode

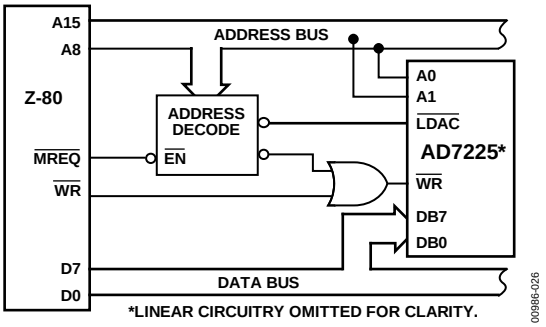


Figure 26. AD7225-to-Z-80 Interface, Double-Buffered Mode

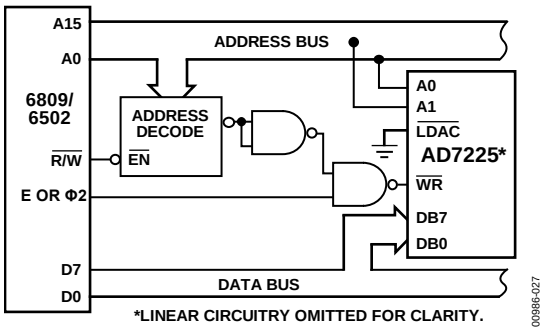


Figure 27. AD7225-to-6809/6502 Interface, Single-Buffered Mode

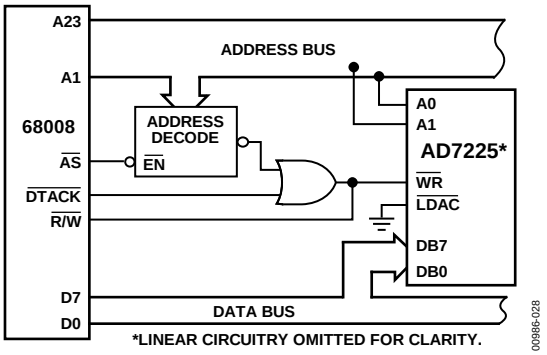


Figure 28. AD7225-to-68008 Interface, Single-Buffered Mode

V_{SS} GENERATION

Operating the AD7225 from dual supplies results in enhanced performance over single-supply operation on a number of parameters as previously outlined. Some applications may require this enhanced performance, but may only have a single power supply rail available. The circuit of Figure 29 shows a method of generating a negative voltage using one CD4049, operated from a V_{DD} of 15 V. Two inverters of the hex inverter chip are used as an oscillator. The other four inverters are in parallel and used as buffers for higher output current. The square wave output is level translated to a negative-going signal, then rectified and filtered. The circuit configuration shown provides an output voltage of −5.1 V for current loadings in the range of 0.5 mA to 9 mA. This satisfies the AD7225 I_{SS} requirement over the commercial operating temperature range.

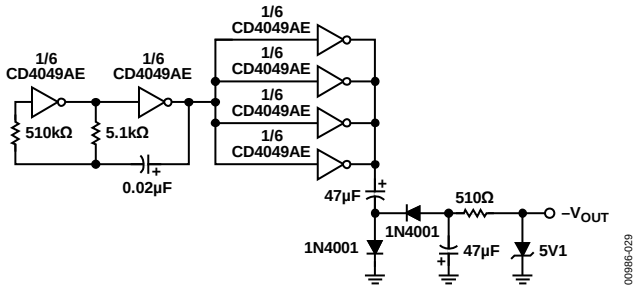
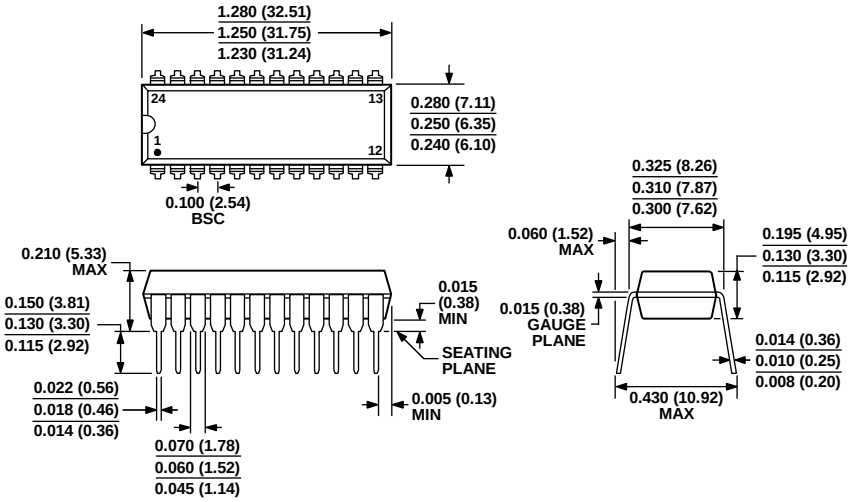


Figure 29. V_{SS} Generation Circuit

OUTLINE DIMENSIONS



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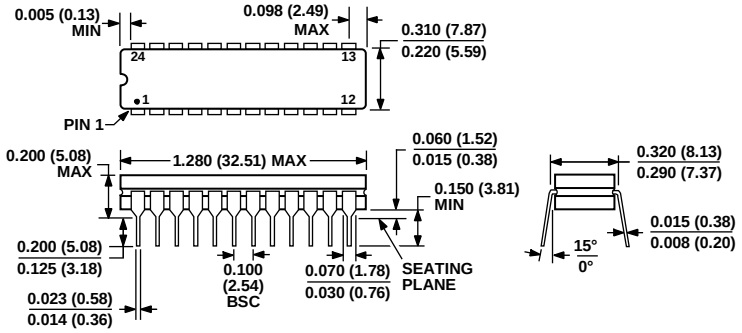
071006-A

Figure 30. 24-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-24-1)
Dimensions shown in inches and (millimeters)



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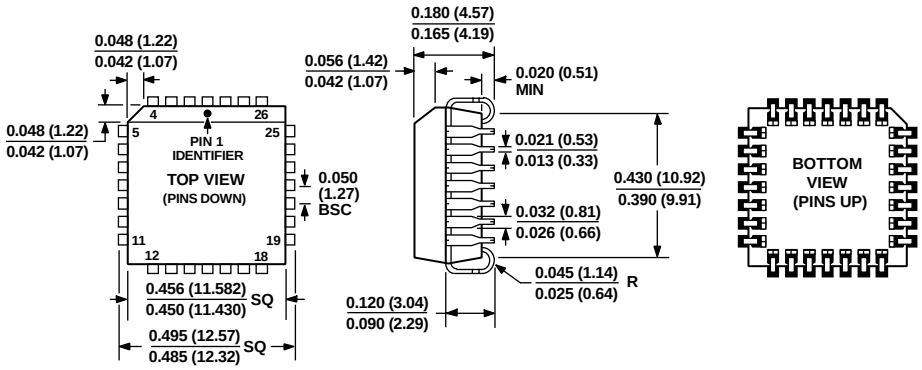
100808-A

Figure 31. 24-Lead Ceramic Dual In-Line Package [CERDIP]
Narrow Body
(Q-24-1)
Dimensions shown in inches and (millimeters)



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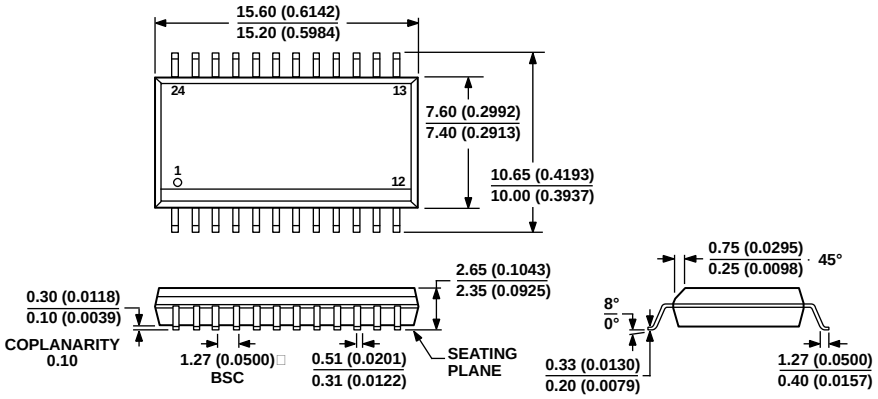
042508-A

Figure 32. 28-Lead Plastic Leaded Chip Carrier [PLCC]
(P-28)
Dimensions shown in inches and (millimeters)



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06-07-2006-A

Figure 33. 24-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-24)
Dimensions shown in millimeters and (inches)

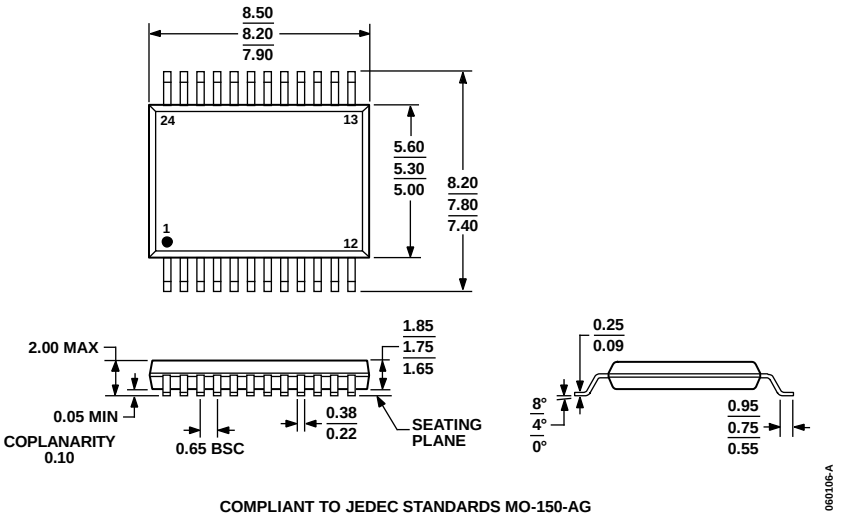

Figure 34. 24-Lead Shrink Small Outline Package [SSOP]
(RS-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Total Unadjusted Error	Package Description	Package Option
AD7225BQ	–40°C to +85°C	±2 LSB	24-Lead CERDIP	Q-24-1
AD7225BRS	–40°C to +85°C	±2 LSB	24-Lead SSOP	RS-24
AD7225BRS-REEL	–40°C to +85°C	±2 LSB	24-Lead SSOP	RS-24
AD7225BRSZ	–40°C to +85°C	±2 LSB	24-Lead SSOP	RS-24
AD7225CRS	–40°C to +85°C	±1 LSB	24-Lead SSOP	RS-24
AD7225CRS-REEL	–40°C to +85°C	±1 LSB	24-Lead SSOP	RS-24
AD7225CRSZ	–40°C to +85°C	±1 LSB	24-Lead SSOP	RS-24
AD7225CRSZ-RL	–40°C to +85°C	±1 LSB	24-Lead SSOP	RS-24
AD7225KN	–40°C to +85°C	±2 LSB	24-Lead PDIP	N-24-1
AD7225KNZ	–40°C to +85°C	±2 LSB	24-Lead PDIP	N-24-1
AD7225KP	–40°C to +85°C	±2 LSB	28-Lead PLCC	P-28
AD7225KP-REEL	–40°C to +85°C	±2 LSB	28-Lead PLCC	P-28
AD7225KPZ	–40°C to +85°C	±2 LSB	28-Lead PLCC	P-28
AD7225KR	–40°C to +85°C	±2 LSB	24-Lead SOIC_W	RW-24
AD7225KR-REEL	–40°C to +85°C	±2 LSB	24-Lead SOIC_W	RW-24
AD7225KRZ	–40°C to +85°C	±2 LSB	24-Lead SOIC_W	RW-24
AD7225KRZ-REEL	–40°C to +85°C	±2 LSB	24-Lead SOIC_W	RW-24
AD7225LN	–40°C to +85°C	±1 LSB	24-Lead PDIP	N-24-1
AD7225LNZ	–40°C to +85°C	±1 LSB	24-Lead PDIP	N-24-1
AD7225LP	–40°C to +85°C	±1 LSB	28-Lead PLCC	P-28
AD7225LP-REEL	–40°C to +85°C	±1 LSB	28-Lead PLCC	P-28
AD7225LPZ	–40°C to +85°C	±1 LSB	28-Lead PLCC	P-28
AD7225LPZ-REEL	–40°C to +85°C	±1 LSB	28-Lead PLCC	P-28
AD7225LR	–40°C to +85°C	±1 LSB	24-Lead SOIC_W	RW-24
AD7225LR-REEL	–40°C to +85°C	±1 LSB	24-Lead SOIC_W	RW-24
AD7225LRZ	–40°C to +85°C	±1 LSB	24-Lead SOIC_W	RW-24
AD7225LRZ-REEL	–40°C to +85°C	±1 LSB	24-Lead SOIC_W	RW-24

[1] To order MIL-STD-883 processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2] Z = RoHS Compliant Part.

NOTES

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