THE DATASHEET OF

SI8421-B-IS

Si8410/20/21

SINGLE AND DUAL-CHANNEL DIGITAL ISOLATORS

Features

- High-speed operation
  - DC – 150 Mbps
- Low propagation delay
  - <10 ns
- Wide Operating Supply Voltage: 2.375–5.5 V
- Low power
  - I1 + I2 < 12 mA/channel at 100 Mbps
- Precise timing
  - 2 ns pulse width distortion
  - 1 ns channel-channel matching
  - 2 ns pulse width skew
- 2500 V_{RMS} isolation
- Transient Immunity
  - >25 kV/µs
- DC correct
- No start-up initialization required
- <10 µs Startup Time
- High temperature operation
  - 125 °C at 100 Mbps
  - 100 °C at 150 Mbps
- Narrow body SOIC-8 package

Applications

- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power factor correction systems

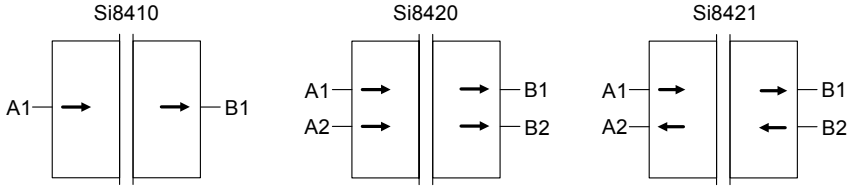
Safety Regulatory Approvals

- UL recognition:2500 Vrms for 1 Minute per UL1577
- CSA component acceptance notice
- IEC certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)

Description

The Silicon Laboratories family of digital isolators are CMOS devices that employ an RF coupler to transmit digital information across an isolation barrier. Very high speed operation at low power levels is achieved. These parts are available in an 8-pin narrow-body SOIC package. Three speed grade options (1, 10, and 150 Mbps) are available and achieve typical propagation delays of less than 10 ns.

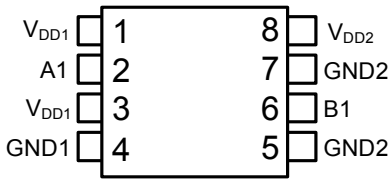
Block Diagram



Pin Assignments

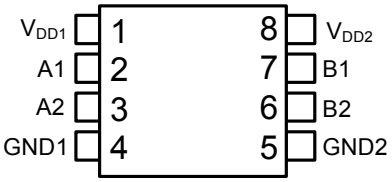
Narrow Body SOIC

Si841x



Top View

Si842x



Top View

U.S. Patent #6,262,600
U.S. Patent #6,525,566
U.S. Patent #6,873,065
U.S. Patent #7,075,329
U.S. Patent #7,302,247
U.S. Patent #7,376,212
Other Patents Pending

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1. Electrical Specifications

Table 1. Electrical Characteristics
(V_{DD1} = 5 V, V_{DD2} = 5 V, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
DC Supply Current (All inputs 0 V or at Supply)						
Si8410-A,-B,-C, V_{DD1}		All inputs 0 DC	—	7	10	mA
Si8410-A,-B,-C, V_{DD2}		All inputs 0 DC	—	3	5	mA
Si8410-A,-B,-C, V_{DD1}		All inputs 1 DC	—	9	14	mA
Si8410-A,-B,-C, V_{DD2}		All inputs 1 DC	—	3	5	mA
Si8420-A,-B,-C, V_{DD1}		All inputs 0 DC	—	7	10	mA
Si8420-A,-B,-C, V_{DD2}		All inputs 0 DC	—	4	7	mA
Si8420-A,-B,-C, V_{DD1}		All inputs 1 DC	—	11	15	mA
Si8420-A,-B,-C, V_{DD2}		All inputs 1 DC	—	4	6	mA
Si8421-A,-B,-C, V_{DD1}		All inputs 0 DC	—	9	12	mA
Si8421-A,-B,-C, V_{DD2}		All inputs 0 DC	—	9	12	mA
Si8421-A,-B,-C, V_{DD1}		All inputs 1 DC	—	10	14	mA
Si8421-A,-B,-C, V_{DD2}		All inputs 1 DC	—	10	14	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8410-B,-C, V_{DD1}			—	8	12	mA
Si8410-B,-C, V_{DD2}			—	5	7	mA
Si8420-B,-C, V_{DD1}			—	9	13	mA
Si8420-B,-C, V_{DD2}			—	9	12	mA
Si8421-B,-C, V_{DD1}			—	12	16	mA
Si8421-B,-C, V_{DD2}			—	12	16	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8410-C, V_{DD1}			—	8	12	mA
Si8410-C, V_{DD2}			—	15	22	mA
Si8420-C, V_{DD1}			—	9	13	mA
Si8420-C, V_{DD2}			—	30	39	mA
Si8421-C, V_{DD1}			—	21	27	mA
Si8421-C, V_{DD2}			—	21	27	mA

Table 1. Electrical Characteristics (Continued)
(V_{DD1} = 5 V, V_{DD2} = 5 V, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
Si841x/2x-A						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	1000	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	25	40	75	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	30	ns
Propagation Delay Skew[1]	$t_{PSK(P-P)}$		—	—	50	ns
Channel-Channel Skew	t_{PSK}		—	—	40	ns
Si841x/2x-B						
Maximum Data Rate			0	—	10	Mbps
Minimum Pulse Width			—	—	100	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	10	20	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	7.5	ns
Propagation Delay Skew[1]	$t_{PSK(P-P)}$		—	—	25	ns
Channel-Channel Skew	t_{PSK}		—	—	5	ns
Si841x/2x-C						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.6	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	4	6.5	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	3.5	ns
Propagation Delay Skew[1]	$t_{PSK(P-P)}$		—	—	5.5	ns
Channel-Channel Skew	t_{PSK}		—	—	3	ns

Table 1. Electrical Characteristics (Continued)
(V_{DD1} = 5 V, V_{DD2} = 5 V, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
For All Models						
Output Rise Time	t_r	C_L = 15 pF	—	2	—	ns
Output Fall Time	t_f	C_L = 15 pF	—	2	—	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	25	30	—	kV/µs
Start-up Time[2]	t_{SU}		—	3	—	µs

Notes:
1. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
2. Start-up time is the time period from the application of power to valid data at the output.

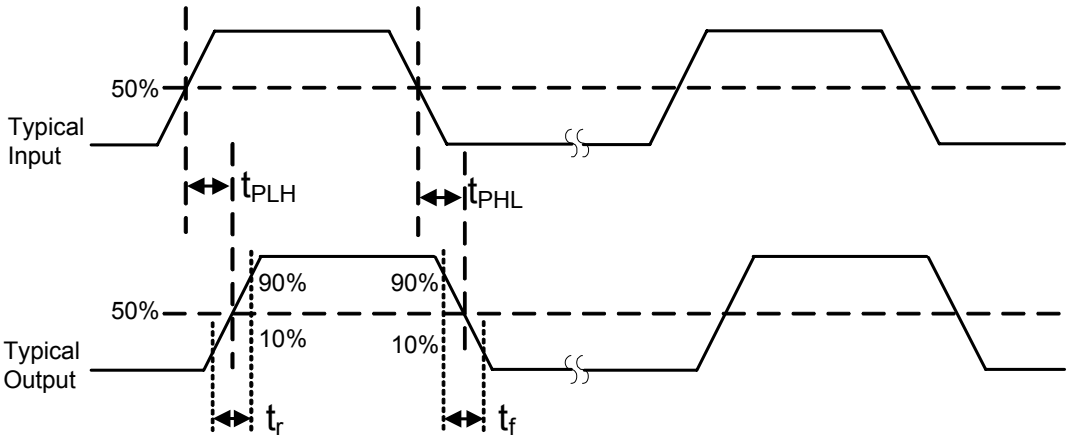


Figure 1. Propagation Delay Timing

Table 2. Electrical Characteristics
(V_{DD1} = 3.3 V, V_{DD2} = 3.3 V, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8410-A,-B,-C, V_{DD1}		All inputs 0 DC	—	6	9	mA
Si8410-A,-B,-C, V_{DD2}		All inputs 0 DC	—	2	4	mA
Si8410-A,-B,-C, V_{DD1}		All inputs 1 DC	—	8	13	mA
Si8410-A,-B,-C, V_{DD2}		All inputs 1 DC	—	2	4	mA
Si8420-A,-B,-C, V_{DD1}		All inputs 0 DC	—	7	9	mA
Si8420-A,-B,-C, V_{DD2}		All inputs 0 DC	—	4	6	mA
Si8420-A,-B,-C, V_{DD1}		All inputs 1 DC	—	10	14	mA
Si8420-A,-B,-C, V_{DD2}		All inputs 1 DC	—	4	6	mA
Si8421-A,-B,-C, V_{DD1}		All inputs 0 DC	—	8	11	mA
Si8421-A,-B,-C, V_{DD2}		All inputs 0 DC	—	8	11	mA
Si8421-A,-B,-C, V_{DD1}		All inputs 1 DC	—	9	13	mA
Si8421-A,-B,-C, V_{DD2}		All inputs 1 DC	—	9	13	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8410-B,-C, V_{DD1}			—	7	11	mA
Si8410-B,-C, V_{DD2}			—	4	6	mA
Si8420-B,-C, V_{DD1}			—	8	12	mA
Si8420-B,-C, V_{DD2}			—	8	12	mA
Si8421-B,-C, V_{DD1}			—	10	14	mA
Si8421-B,-C, V_{DD2}			—	10	14	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8410-C, V_{DD1}			—	7	11	mA
Si8410-C, V_{DD2}			—	10	16	mA
Si8420-C, V_{DD1}			—	8	12	mA
Si8420-C, V_{DD2}			—	20	26	mA
Si8421-C, V_{DD1}			—	17	21	mA
Si8421-C, V_{DD2}			—	17	21	mA

Table 2. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V, V_{DD2} = 3.3 V, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
Si841x/2x-A						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	1000	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	25	40	75	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	30	ns
Propagation Delay Skew[1]	$t_{PSK(P-P)}$		—	—	50	ns
Channel-Channel Skew	t_{PSK}		—	—	40	ns
Si841x/2x-B						
Maximum Data Rate			0	—	10	Mbps
Minimum Pulse Width			—	—	100	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	10	20	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	7.5	ns
Propagation Delay Skew[1]	$t_{PSK(P-P)}$		—	—	25	ns
Channel-Channel Skew	t_{PSK}		—	—	5	ns
Si841x/2x-C						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.6	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	4	7.5	10	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	3.5	ns
Propagation Delay Skew[1]	$t_{PSK(P-P)}$		—	—	5.5	ns
Channel-Channel Skew	t_{PSK}		—	—	3	ns

Table 2. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V, V_{DD2} = 3.3 V, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
For All Models						
Output Rise Time	t_r	C_L = 15 pF	—	2	—	ns
Output Fall Time	t_f	C_L = 15 pF	—	2	—	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	25	30	—	kV/µs
Start-up Time[2]	t_{SU}		—	3	—	µs

Notes:
1. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
2. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics
(V_{DD1} = 2.5 V, V_{DD2} = 2.5 V, T_A = –40 to 100 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8410-A,-B,-C, V_{DD1}		All inputs 0 DC	—	5	7	mA
Si8410-A,-B,-C, V_{DD2}		All inputs 0 DC	—	2	3	mA
Si8410-A,-B,-C, V_{DD1}		All inputs 1 DC	—	7	9	mA
Si8410-A,-B,-C, V_{DD2}		All inputs 1 DC	—	2	3	mA
Si8420-A,-B,-C, V_{DD1}		All inputs 0 DC	—	6	7	mA
Si8420-A,-B,-C, V_{DD2}		All inputs 0 DC	—	4	5	mA
Si8420-A,-B,-C, V_{DD1}		All inputs 1 DC	—	9	11	mA
Si8420-A,-B,-C, V_{DD2}		All inputs 1 DC	—	3	5	mA
Si8421-A,-B,-C, V_{DD1}		All inputs 0 DC	—	7	9	mA
Si8421-A,-B,-C, V_{DD2}		All inputs 0 DC	—	7	9	mA
Si8421-A,-B,-C, V_{DD1}		All inputs 1 DC	—	8	10	mA
Si8421-A,-B,-C, V_{DD2}		All inputs 1 DC	—	8	10	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8410-B,-C, V_{DD1}			—	6	8	mA
Si8410-B,-C, V_{DD2}			—	3	5	mA
Si8420-B,-C, V_{DD1}			—	7	9	mA
Si8420-B,-C, V_{DD2}			—	6	8	mA
Si8421-B,-C, V_{DD1}			—	8	11	mA
Si8421-B,-C, V_{DD2}			—	8	11	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8410-C, V_{DD1}			—	6	8	mA
Si8410-C, V_{DD2}			—	7	10	mA
Si8420-C, V_{DD1}			—	7	9	mA
Si8420-C, V_{DD2}			—	12	15	mA
Si8421-C, V_{DD1}			—	12	15	mA
Si8421-C, V_{DD2}			—	12	15	mA

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 2.5 V, V_{DD2} = 2.5 V, T_A = –40 to 100 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
Si841x/2x-A						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	1000	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	25	40	75	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	30	ns
Propagation Delay Skew[1]	$t_{PSK(P-P)}$		—	—	50	ns
Channel-Channel Skew	t_{PSK}		—	—	40	ns
Si841x/2x-B						
Maximum Data Rate			0	—	10	Mbps
Minimum Pulse Width			—	—	100	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	10	20	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	7.5	ns
Propagation Delay Skew[1]	$t_{PSK(P-P)}$		—	—	25	ns
Channel-Channel Skew	t_{PSK}		—	—	5	ns
Si841x/2x-C						
Maximum Data Rate			0	—	100	Mbps
Minimum Pulse Width			—	—	10	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	5	10	17	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	7	ns
Propagation Delay Skew[1]	$t_{PSK(P-P)}$		—	—	12	ns
Channel-Channel Skew	t_{PSK}		—	—	4	ns

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 2.5 V, V_{DD2} = 2.5 V, T_A = –40 to 100 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
For All Models						
Output Rise Time	t_r	C_L = 15 pF	—	2	—	ns
Output Fall Time	t_f	C_L = 15 pF	—	2	—	ns
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V	25	30	—	kV/µs
Start-up Time[2]	t_{SU}		—	3	—	µs

Notes:
1. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
2. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature	T_{STG}	–65	—	150	C°
Operating Temperature	T_A	–40	—	125	C°
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	—	6	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	L_O	—	—	10	mA
Lead Solder Temperature (10s)		—	—	260	C°
Maximum Isolation Voltage		—	—	4000	V_{DC}

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.

Table 5. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	100 Mbps, 15 pF, 5 V	–40	25	125	C°
		150 Mbps, 15 pF, 5 V	0	25	100	C°
Supply Voltage	V_{DD1}		2.375	—	5.5	V
	V_{DD2}		2.375	—	5.5	V

***Note:** The maximum ambient temperature is dependent upon data frequency, output loading, the number of operating channels, and supply voltage.

Table 6. Regulatory Information

CSA
The Si84xx is certified under CSA Component Acceptance Notice. For more details, see File 232873.
VDE
The Si84xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
UL
The Si84xx is certified under UL1577 component recognition program to provide basic insulation to 2500 V_{RMS} (1 minute). It is production tested $\geq$ 3000 V_{RMS} for 1 second. For more details, see File E257455.

Table 7. Insulation and Safety-related Specifications

Parameter	Symbol	Test Condition	Value	Unit
Minimum Air Gap (Clearance)	L(IO1)		5.0 min	mm
Minimum External Tracking (Creepage)	L(IO2)		4.60	mm
Minimum Internal Gap (Internal Clearance)			0.008 min	mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN IEC 60112/VDE 0303 Part 1	>175	V
Resistance (Input-Output)[1]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	1.4	pF
Input Capacitance[2]	C_I		4.0	pF

Notes:
1. To determine resistance and capacitance, the Si84xx is converted into a 2-terminal device. Pins 1–4 are shorted together to form the first terminal and pins 5–8 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 8. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Conditions	Specification
Basic isolation group	Material Group	IIIa
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II

Table 9. IEC 60747-5-2 Insulation Characteristics*

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	V peak
Input to Output Test Voltage	V_{PR}	Method a After Environmental Tests Subgroup 1 (V_{IORM} x 1.6 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	896	V peak
		Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1050	
		After Input and/or Safety Test Subgroup 2/3 (V_{IORM} x 1.2 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	672	
Highest Allowable Overvoltage (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}		4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** The Si84xx is suitable for basic electrical isolation a climate classification of 40/125/21.

Table 10. IEC Safety Limiting Values

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Case Temperature	T_S		—	—	150	°C
Safety input, output, or supply current	I_S	θ_{JA} = 210 °C/W, V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	—	—	105	mA

***Note:** Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 2.

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IC Junction-to-Case Thermal Resistance	θ_{JC}	Thermocouple located at center of package	—	100	—	°C/W
IC Junction-to-Air Thermal Resistance	θ_{JA}		—	210	—	°C/W
Device Power Dissipation*	P_D		—	—	250	mW

***Note:** The Si8420-C-IS is tested with V_{DD1} = V_{DD2} = 5.5 V, T_J = 150 °C, C_L = 15 pF, input a 150 Mbps 50% duty cycle square wave.

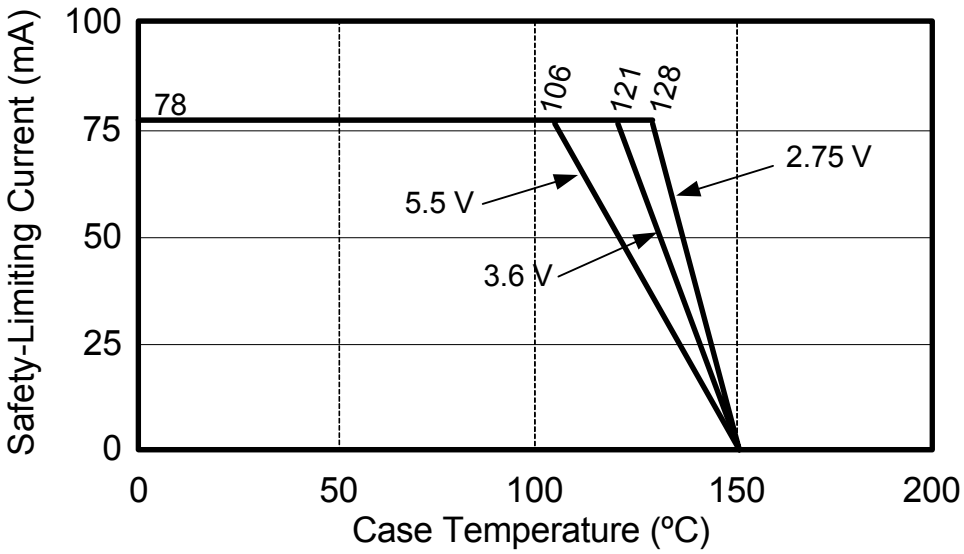


Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

2. Typical Performance Characteristics

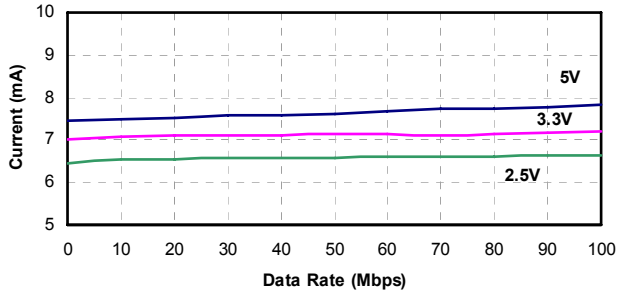


Figure 3. Si8410 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation

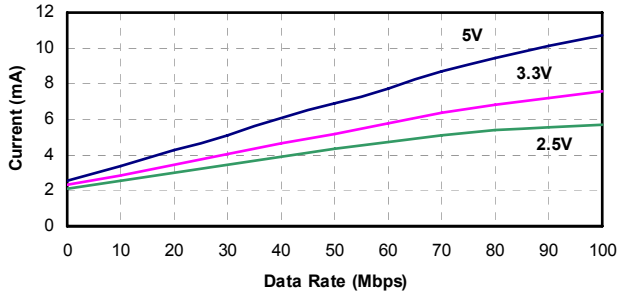


Figure 4. Si8410 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

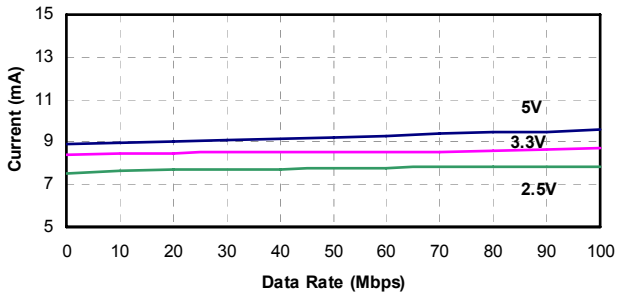


Figure 5. Si8420 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation

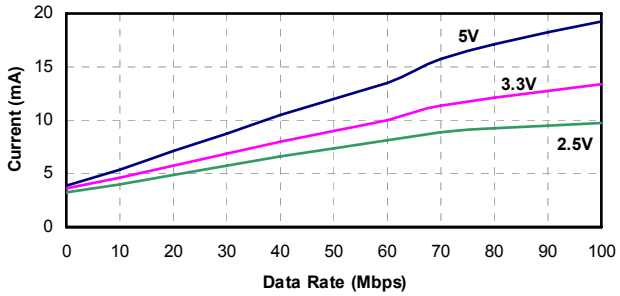


Figure 6. Si8420 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

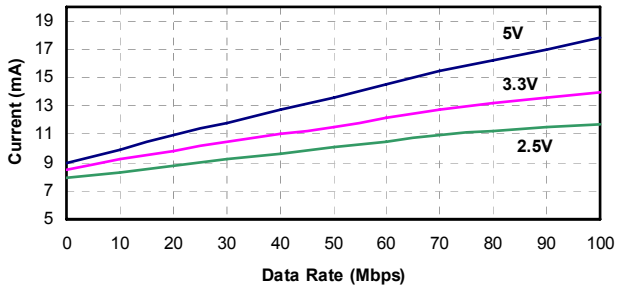


Figure 7. Si8421 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

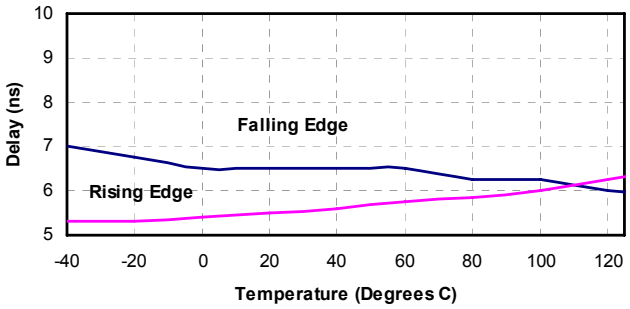


Figure 8. Propagation Delay vs. Temperature 5 V Operation

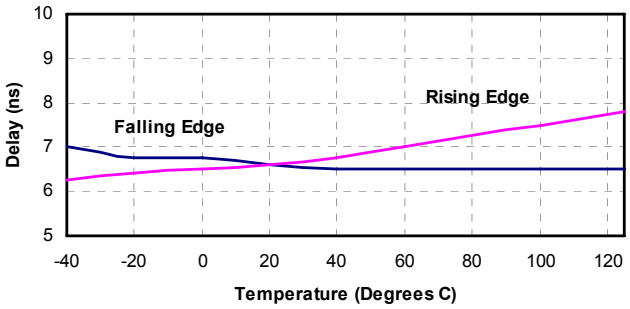


Figure 9. Propagation Delay vs. Temperature 3.3 V Operation

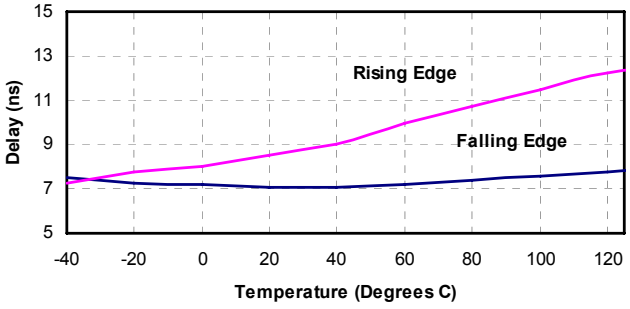


Figure 10. Propagation Delay vs. Temperature 2.5 V Operation

3. Application Information

3.1. Theory of Operation

The operation of an Si841x or Si842x channel is analogous to that of an opto coupler, except that an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at startup. A simplified block diagram for a single Si8410 channel is shown in Figure 11. A channel consists of an RF transmitter and receiver separated by a transformer.

Referring to the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying and applies the resulting waveform to the primary of the transformer. The receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver.

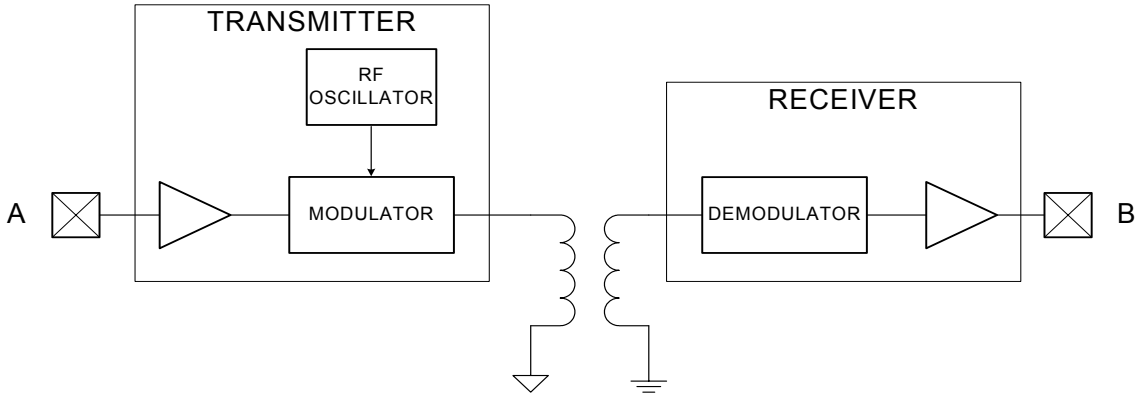


Figure 11. Simplified Channel Diagram

3.2. Eye Diagram

Figure 12 illustrates an eye-diagram taken on an Si8410. The test used an Anritsu (MP1763C) Pulse Pattern Generator for the data source. The output of the generator's clock and data from an Si8410 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that very low pulse width distortion and very little jitter were exhibited.

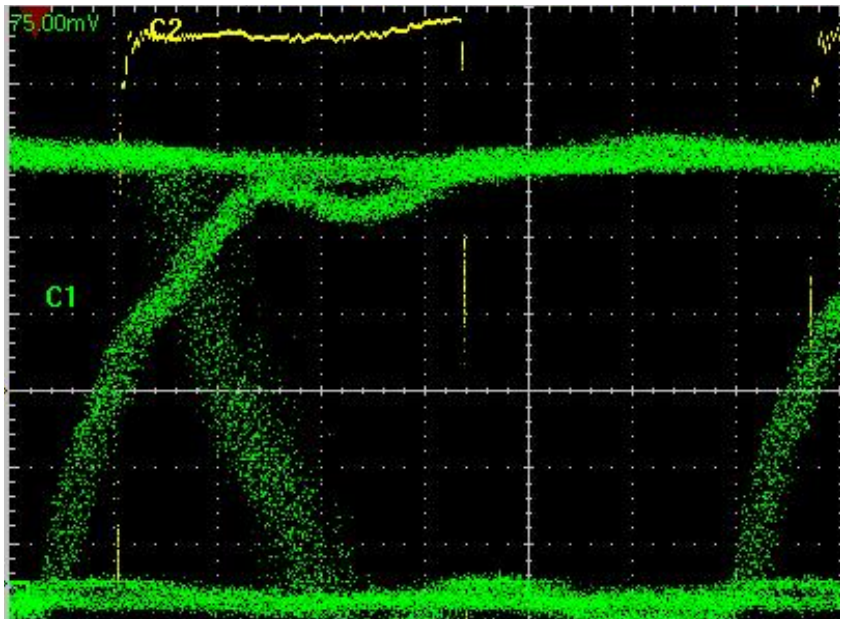


Figure 12. Eye Diagram

4. Layout Recommendations

Dielectric isolation is a set of specifications produced by safety regulatory agencies from around the world, which describes the physical construction of electrical equipment that derives power from high-voltage power systems, such as 100–240 V_{AC} systems or industrial power. The dielectric test (or HIPOT test) given in the safety specifications places a very high voltage between the input power pins of a product and the user circuits and the user-touchable surfaces of the product. For the IEC relating to products deriving their power from the 220–240 V power grids, the test voltage is 2500 V_{AC} (or 3750 V_{DC}, the peak equivalent voltage).

There are two terms described in the safety specifications:

- Creepage—the distance along the insulating surface an arc may travel.
- Clearance—the shortest distance through air that an arc may travel.

Figure 13 illustrates the accepted method of providing the proper creepage distance along the surface. For a 220–240 V application, this distance is 8 mm, and the wide-body SOIC package must be used. There must be no copper traces within this 8 mm exclusion area, and the surface should have a conformal coating, such as solder resist. The digital isolator chip must straddle this exclusion area.

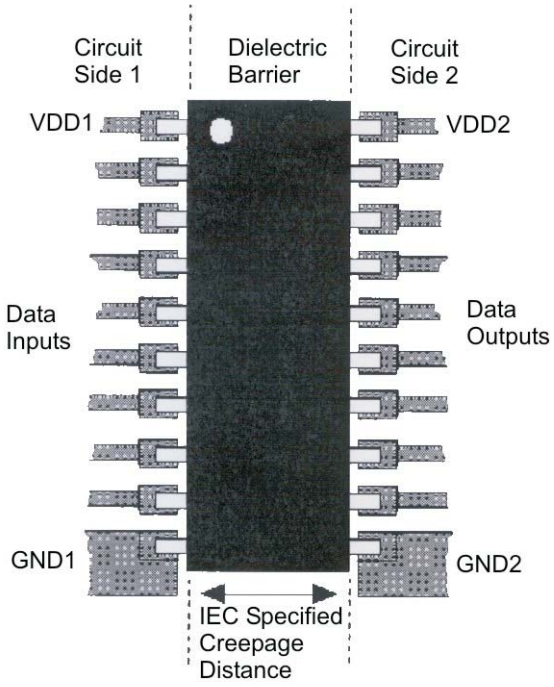


Figure 13. Creepage Distance

4.1. Supply Bypass

The Si841x and Si842x families require a 0.1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package.

4.2. Input and Output Characteristics

The Si841x and Si842x inputs and outputs are standard CMOS drivers/receivers. Table 12 details powered and unpowered operation of the Si84xx.

Table 12. Si84xx Operation Table

V_I Input[1,4]	VDDI State[1,2,3]	VDDO State[1,2,3]	V_O Output[1,4]	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X	UP	P	L	Upon the transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X	P	UP	L	Upon the transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.

Notes:
1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals.
2. Powered (P) state is defined as 2.375 V < VDD < 5.5 V.
3. Unpowered (UP) state is defined as VDD = 0 V.
4. X = not applicable; H = Logic High; L = Logic Low.

4.3. RF Radiated Emissions

The Si841x and Si842x families use an RF carrier frequency of approximately 2.1 GHz. This will result in a small amount of radiated emissions at this frequency and its harmonics. The radiation is not from the IC chip but, rather, is due to a small amount of RF energy driving the isolated ground planes, which can act as a dipole antenna.

The unshielded Si8410 evaluation board passes FCC requirements. Table 13 shows measured emissions compared to FCC requirements.

Radiated emissions can be reduced if the circuit board is enclosed in a shielded enclosure or if the PCB is a less efficient antenna.

Table 13. Radiated Emissions

Frequency (GHz)	Measured (dBµV/m)	FCC Spec (dBµV/m)	Compared to Spec (dB)
2.094	70.0	74.0	–4.0
2.168	68.3	74.0	–5.7
4.210	61.9	74.0	–12.1
4.337	60.7	74.0	–13.3
6.315	58.3	74.0	–15.7
6.505	60.7	74.0	–13.3
8.672	45.6	74.0	–28.4

4.4. RF Immunity and Common Mode Transient Immunity

The Si841x and Si842x families have very high common mode transient immunity while transmitting data. This is typically measured by applying a square pulse with very fast rise/fall times between the isolated grounds. Measurements show no failures up to 30 kV/µs. During a high surge event, the output may glitch low for up to 20–30 ns, but the output corrects immediately after the surge event.

The Si841x and Si842x families pass the industrial requirements of CISPR24 for RF immunity of 3 V/m using an unshielded evaluation board. As shown in Figure 14, the isolated ground planes form a parasitic dipole antenna, while Figure 15 shows the RMS common mode voltage versus frequency above which the Si841x becomes susceptible to data corruption. To avoid compromising data, care must be taken to keep RF common-mode voltage below the envelope specified in Figure 15. The PCB should be laid-out to not act as an efficient antenna for the RF frequency of interest. RF susceptibility is also significantly reduced when the end system is housed in a metal enclosure, or otherwise shielded.

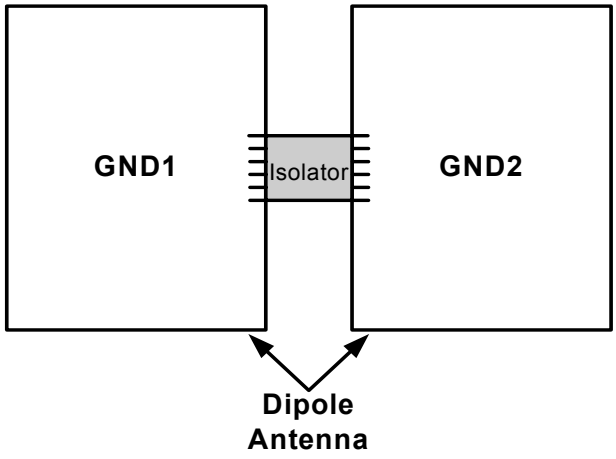


Figure 14. Dipole Antenna

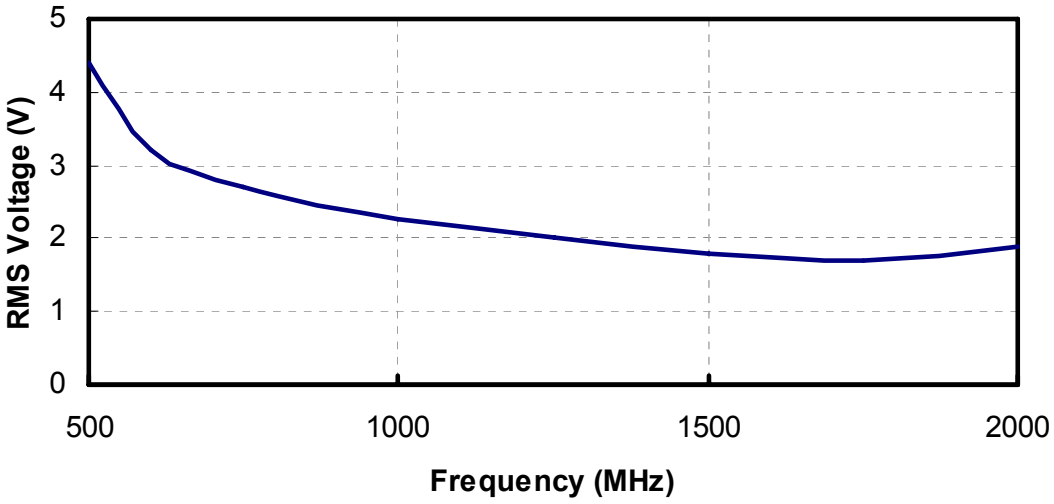
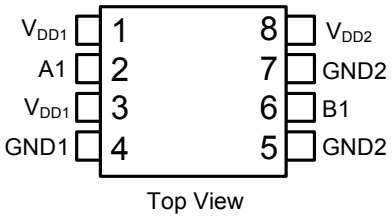


Figure 15. RMS Common Mode Voltage vs. Frequency

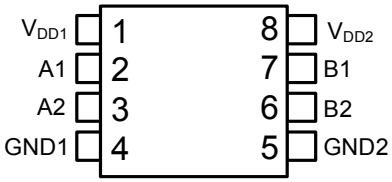
5. Pin Descriptions

Si841x



Top View

Si842x



Top View

Narrow Body SOIC

Name	SOIC-8 Pin# Si8410	SOIC-8 Pin# Si8420/21	Type	Description
V_{DD1}	1,3	1	Supply	Side 1 power supply.
GND1	4	4	Ground	Side 1 ground.
A1	2	2	Digital I/O	Side 1 digital input or output.
A2	NA	3	Digital I/O	Side 1 digital input or output.
B1	6	7	Digital I/O	Side 2 digital input or output.
B2	NA	6	Digital I/O	Side 2 digital input or output.
V_{DD2}	8	8	Supply	Side 2 power supply.
GND2	5,7	5	Ground	Side 2 ground.

6. Ordering Guide

Ordering Part Number	Number of Inputs V_{DD1} Side	Number of Inputs V_{DD2} Side	Maximum Data Rate	Temperature	Package Type
Si8410-A-IS	1	0	1	–40 to 125 °C	SOIC-8
Si8410-B-IS	1	0	10	–40 to 125 °C	SOIC-8
Si8410-C-IS	1	0	150	–40 to 125 °C	SOIC-8
Si8420-A-IS	2	0	1	–40 to 125 °C	SOIC-8
Si8420-B-IS	2	0	10	–40 to 125 °C	SOIC-8
Si8420-C-IS	2	0	150	–40 to 125 °C	SOIC-8
Si8421-A-IS	1	1	1	–40 to 125 °C	SOIC-8
Si8421-B-IS	1	1	10	–40 to 125 °C	SOIC-8
Si8421-C-IS	1	1	150	–40 to 125 °C	SOIC-8

Note: All packages are Pb-free and RoHS Compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.

7. Package Outline: 8-Pin SOIC

Figure 16 illustrates the package details for the Si84xx. Table 14 lists the values for the dimensions shown in the illustration.

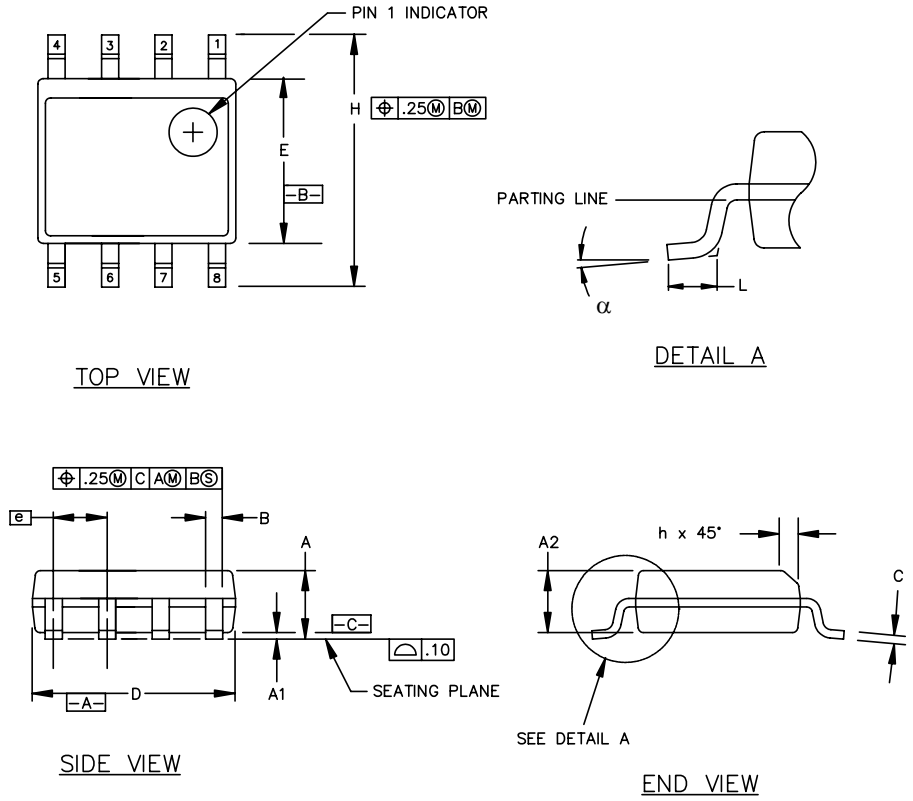


Figure 16. 8-pin Small Outline Integrated Circuit (SOIC) Package

Table 14. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
∝	0°	8°

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.11

- Changed MSL2 to MSL3 in the "6. Ordering Guide" on page 24.
- Added pertinent patent numbers.

NOTES:

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