



**THE DATASHEET OF  
SN74LV161ADR**



# SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

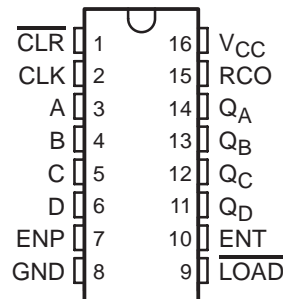
SCLS404F – APRIL 1998 – REVISED DECEMBER 2005

- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 9.5 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

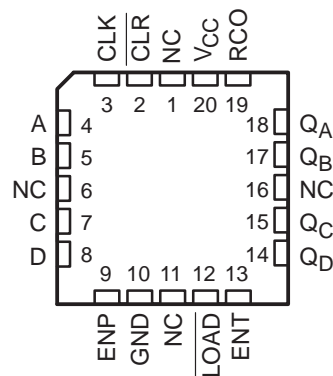
## description/ordering information

The 'LV161A devices are 4-bit synchronous binary counters designed for 2-V to 5.5-V  $V_{CC}$  operation.

SN54LV161A . . . J OR W PACKAGE  
SN74LV161A . . . D, DB, DGV, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LV161A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube of 40	SN74LV161AD	LV161A
		Reel of 2500	SN74LV161ADR	
	SOP – NS	Reel of 2000	SN74LV161ANSR	74LV161A
	SSOP – DB	Reel of 2000	SN74LV161ADBR	LV161A
	TSSOP – PW	Tube of 90	SN74LV161APW	LV161A
		Reel of 2000	SN74LV161APWR	
Reel of 250		SN74LV161APWT		
TVSOP – DGV	Reel of 2000	SN74LV161ADGVR	LV161A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV161AJ	SNJ54LV161AJ
	CFP – W	Tube of 150	SNJ54LV161AW	SNJ54LV161AW
	LCCC – FK	Tube of 55	SNJ54LV161AFK	SNJ54LV161AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2005, Texas Instruments Incorporated

# SN54LV161A, SN74LV161A

## 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS404F – APRIL 1998 – REVISED DECEMBER 2005

### description/ordering information (continued)

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that normally are associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'LV161A devices is asynchronous. A low level at the clear ( $\overline{\text{CLR}}$ ) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ( $\overline{\text{LOAD}}$ ), or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry output (RCO). Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with  $Q_A$  high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or  $\overline{\text{LOAD}}$ ) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

These devices are fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE

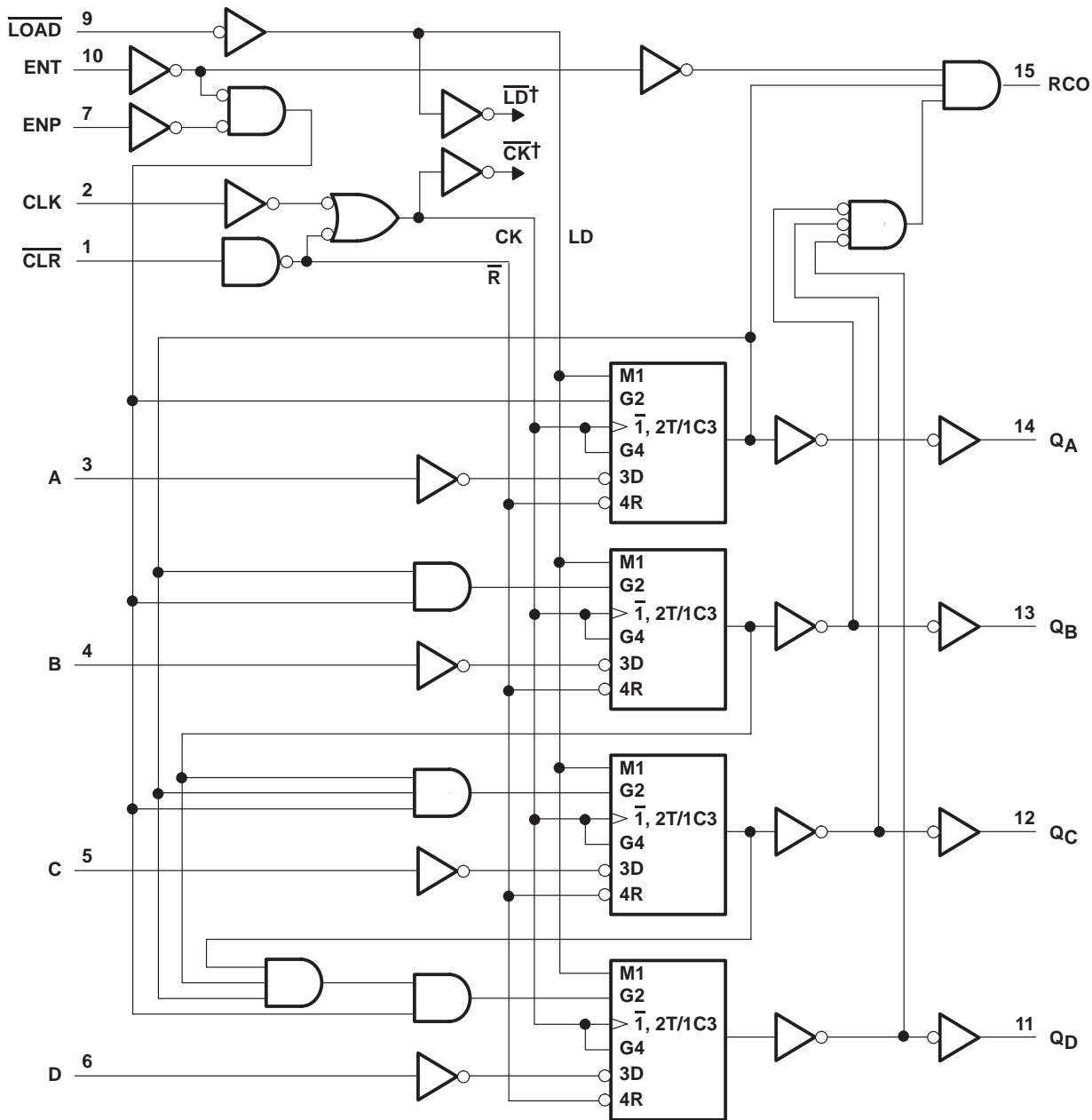
INPUTS					OUTPUTS				FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{LOAD}}$	ENP	ENT	CLK	QA	QB	QC	QD	
L	X	X	X	X	L	L	L	L	Reset to "0"
H	L	X	X	↑	A	B	C	D	Preset Data
H	H	X	L	↑	No Change				No Count
H	H	L	X	↑	No Change				No Count
H	H	H	H	↑	Count up				Count
H	X	X	X	↑	No Change				No Count



# SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS404F – APRIL 1998 – REVISED DECEMBER 2005

## logic diagram (positive logic)



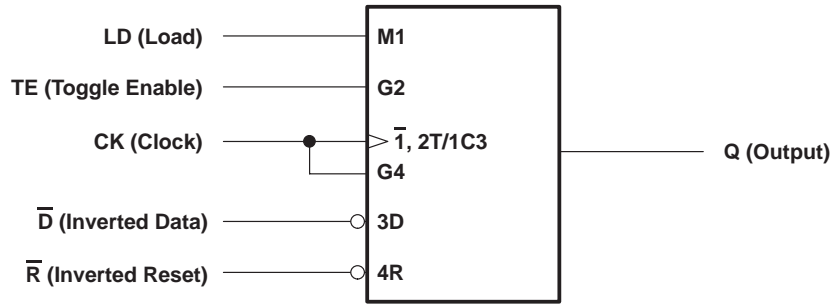
† For simplicity, routing of complementary signals  $\overline{LD}$  and  $\overline{CK}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

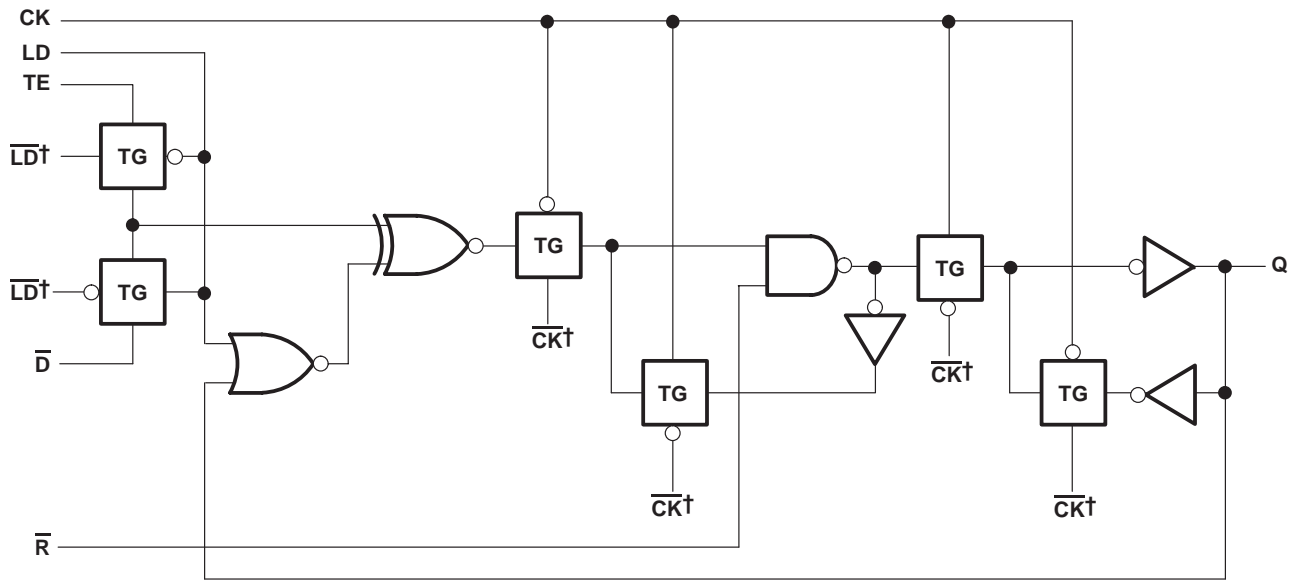
# SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS404F – APRIL 1998 – REVISED DECEMBER 2005

## logic symbol, each D/T flip-flop



## logic diagram, each D/T flip-flop (positive logic)

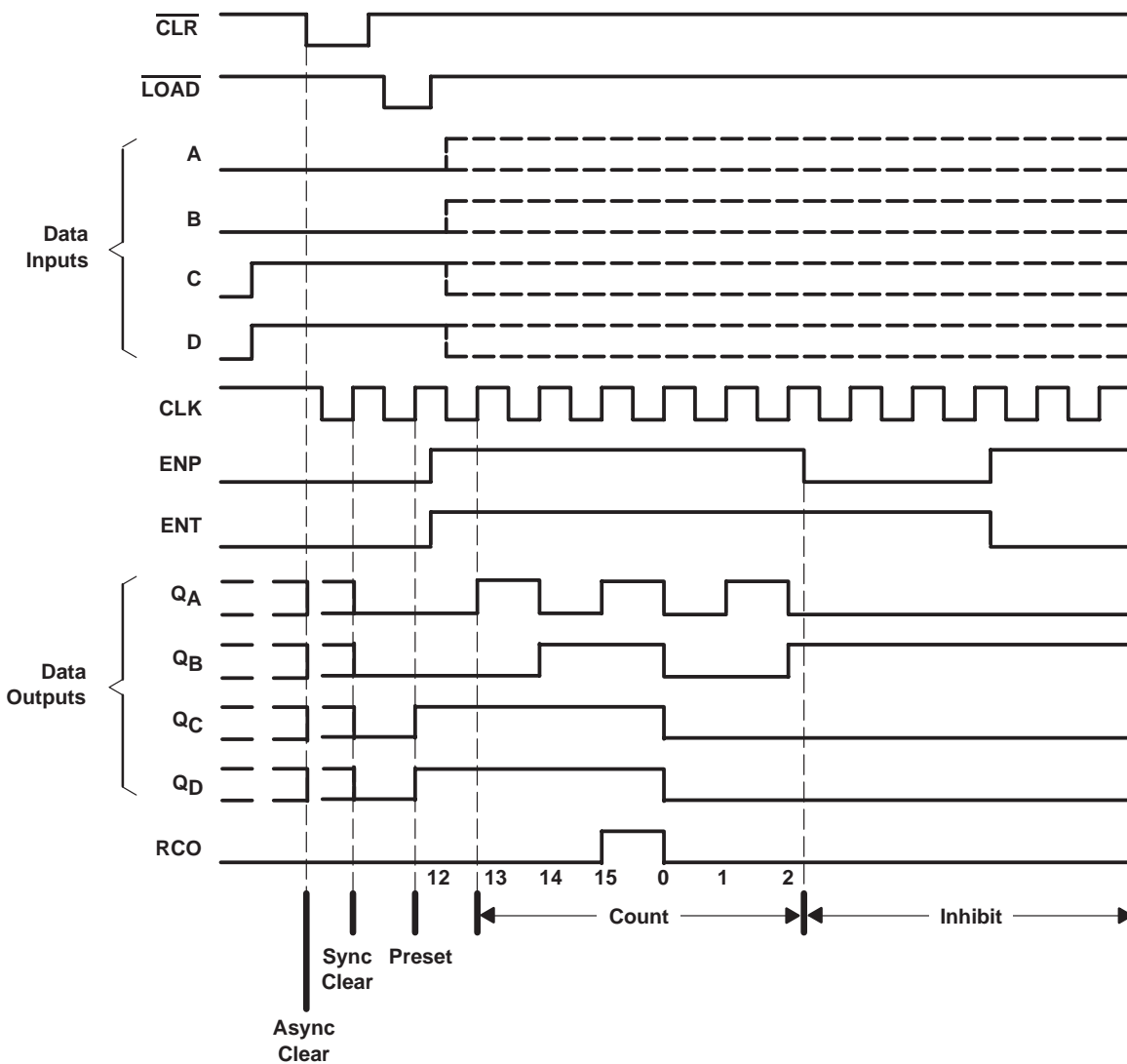


† The origins of  $\overline{LD}$  and  $\overline{CK}$  are shown in the overall logic diagram of the device.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



# SN54LV161A, SN74LV161A

## 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS404F – APRIL 1998 – REVISED DECEMBER 2005

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range applied in high or low state, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Voltage range applied to any output in the power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package .....	73°C/W
DB package .....	82°C/W
DGV package .....	120°C/W
NS package .....	64°C/W
PW package .....	108°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
  2. This value is limited to 5.5 V maximum.
  3. The package thermal impedance is calculated in accordance with JESD 51-7.



# SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS404F – APRIL 1998 – REVISED DECEMBER 2005

## recommended operating conditions (see Note 4)

		SN54LV161A		SN74LV161A		UNIT	
		MIN	MAX	MIN	MAX		
V <sub>CC</sub>	Supply voltage	2	5.5	2	5.5	V	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	1.5		V	
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7			
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7			
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	0.5		V	
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3			
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3			
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3			
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50	-50	μA	
		V <sub>CC</sub> = 2.3 V to 2.7 V		-2	-2	mA	
		V <sub>CC</sub> = 3 V to 3.6 V		-6	-6		
		V <sub>CC</sub> = 4.5 V to 5.5 V		-12	-12		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	50	μA	
		V <sub>CC</sub> = 2.3 V to 2.7 V		2	2	mA	
		V <sub>CC</sub> = 3 V to 3.6 V		6	6		
		V <sub>CC</sub> = 4.5 V to 5.5 V		12	12		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V	0	100	0	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0	20	0	20	
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV161A			SN74LV161A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1			V <sub>CC</sub> -0.1		V	
	I <sub>OH</sub> = -2 mA	2.3 V	2		2				
	I <sub>OH</sub> = -6 mA	3 V	2.48		2.48				
	I <sub>OH</sub> = -12 mA	4.5 V	3.8		3.8				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V				0.1	0.1	V	
	I <sub>OL</sub> = 2 mA	2.3 V				0.4	0.4		
	I <sub>OL</sub> = 6 mA	3 V				0.44	0.44		
	I <sub>OL</sub> = 12 mA	4.5 V				0.55	0.55		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V				±1	±1	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V				20	20	μA	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0				5	5	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		1.8		1.8		pF	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



# SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS404F – APRIL 1998 – REVISED DECEMBER 2005

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV161A		SN74LV161A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLK high or low	7	7	7	7	ns	
		$\overline{\text{CLR}}$ low	7	7	7	7		
$t_{su}$	Setup time before CLK $\uparrow$	$\overline{\text{CLR}}$	4.5	4.5	4.5	ns		
		Data (A, B, C, and D)	7.5	8.5	8.5			
		ENP, ENT	9.5	11	11			
		$\overline{\text{LOAD}}$ low	10	11.5	11.5			
$t_h$	Hold time, all synchronous inputs after CLK $\uparrow$	1.5	1.5	1.5	1.5	ns		

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV161A		SN74LV161A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLK high or low	5	5	5	ns		
		$\overline{\text{CLR}}$ low	5	5	5			
$t_{su}$	Setup time before CLK $\uparrow$	$\overline{\text{CLR}}$	2.5	2.5	2.5	ns		
		Data (A, B, C, and D)	5.5	6.5	6.5			
		ENP, ENT	7.5	9	9			
		$\overline{\text{LOAD}}$ low	8	9.5	9.5			
$t_h$	Hold time, all synchronous inputs after CLK $\uparrow$	1	1	1	1	ns		

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV161A		SN74LV161A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLK high or low	5	5	5	ns		
		$\overline{\text{CLR}}$ low	5	5	5			
$t_{su}$	Setup time before CLK $\uparrow$	$\overline{\text{CLR}}$	1.5	1.5	1.5	ns		
		Data (A, B, C, and D)	4.5	4.5	4.5			
		ENP, ENT	5	6	6			
		$\overline{\text{LOAD}}$ low	5	6	6			
$t_h$	Hold time, all synchronous inputs after CLK $\uparrow$	1	1	1	1	ns		

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS404F – APRIL 1998 – REVISED DECEMBER 2005

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			$C_L = 15\text{ pF}$	50*	125*		40*		40		MHz
			$C_L = 50\text{ pF}$	30	95		25		25		
$t_{pd}$	CLK	Q	$C_L = 15\text{ pF}$	7.9*	16.2*		1*	19.5*	1	19.5	ns
		RCO (count mode)		8.9*	17*		1*	20.5*	1	20.5	
		RCO (preset mode)		11.9*	20.6*		1*	24.5*	1	24.5	
	ENT	8.3*		15.7*		1*	19*	1	19		
$t_{PHL}$	$\overline{\text{CLR}}$	Q		8.8*	17*		1*	20.5*	1	20.5	
		RCO		9.8*	16.6*		1*	20*	1	20	
$t_{pd}$	CLK	Q	$C_L = 50\text{ pF}$	10.5	19.2		1	22.5	1	22.5	ns
		RCO (count mode)		11.7	20		1	23.5	1	23.5	
		RCO (preset mode)		14.5	23.6		1	27.5	1	27.5	
	ENT	11		18.7		1	22	1	22		
$t_{PHL}$	$\overline{\text{CLR}}$	Q		11.4	20		1	23.5	1	23.5	
		RCO		12.6	19.6		1	23	1	23	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



# SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS404F – APRIL 1998 – REVISED DECEMBER 2005

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}^*$	80*	165*		70*		70		MHz
			$C_L = 50\text{ pF}$	55	125		50		50		
$t_{\text{pd}}^*$	CLK	Q	$C_L = 15\text{ pF}$	6	12.8		1*	15*	1	15	ns
		RCO (count mode)		6.7	13.6		1*	16*	1	16	
		RCO (preset mode)		8.6	17.2		1*	20*	1	20	
	ENT	RCO		6.2	12.3		1*	14.5*	1	14.5	
$t_{\text{PHL}}^*$	$\overline{\text{CLR}}$	Q		6.5	13.6		1*	16*	1	16	
		RCO		7.2	13.2		1*	15.5*	1	15.5	
$t_{\text{pd}}$	CLK	Q	$C_L = 50\text{ pF}$	7.8	16.3		1	18.5	1	18.5	ns
		RCO (count mode)		8.7	17.1		1	19.5	1	19.5	
		RCO (preset mode)		10.6	20.7		1	23.5	1	23.5	
	ENT	RCO		8.3	15.8		1	18	1	18	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q		8.4	17.1		1	19.5	1	19.5	
		RCO		9.2	16.7		1	19	1	19	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

# SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS404F – APRIL 1998 – REVISED DECEMBER 2005

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	135*	220		115*		115		MHz
			$C_L = 50\text{ pF}$	95	165		85		85		
$t_{\text{pd}}$	CLK	Q	$C_L = 15\text{ pF}$	4.5*	8.1*	1*	9.5*	1	9.5	ns	
		RCO (count mode)		5.1*	8.1*	1*	9.5*	1	9.5		
		RCO (preset mode)		6.3*	10.3*	1*	12*	1	12		
	ENT	RCO		4.8*	8.1*	1*	9.5*	1	9.5		
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q		4.9*	9*	1*	10.5*	1	10.5		
		RCO		5.5*	8.6*	1*	10*	1	10		
$t_{\text{pd}}$	CLK	Q	$C_L = 50\text{ pF}$	5.9	10.1	1	11.5	1	11.5	ns	
		RCO (count mode)		6.6	10.1	1	11.5	1	11.5		
		RCO (preset mode)		7.8	12.3	1	14	1	14		
	ENT	RCO		6.1	10.1	1	11.5	1	11.5		
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q		6.3	11	1	12.5	1	12.5		
		RCO		6.9	10.6	1	12	1	12		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER		SN74LV161A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.2	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		3		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	23.6	pF
			5 V	25.8	

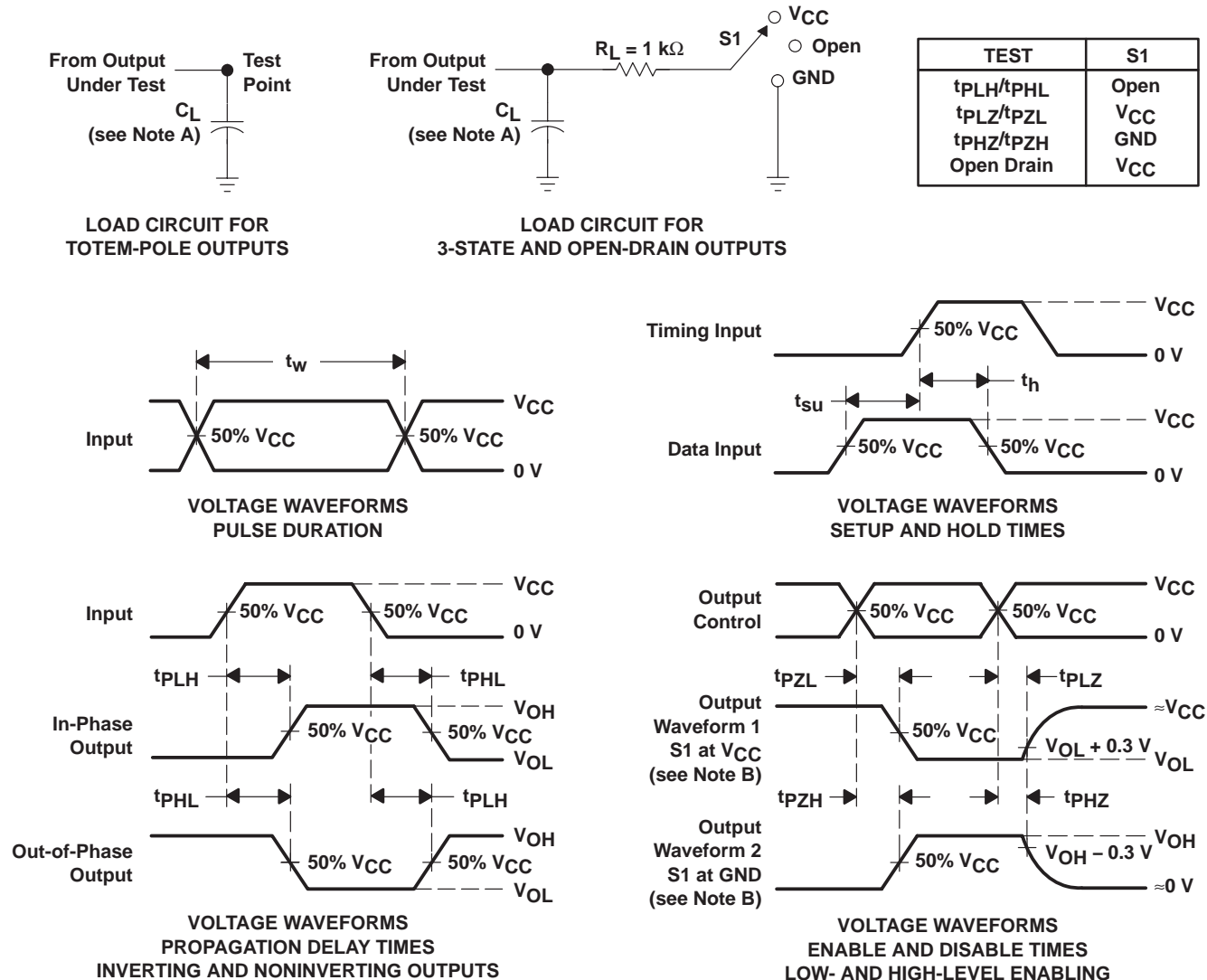
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



# SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS404F – APRIL 1998 – REVISED DECEMBER 2005

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV161AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161A	<a href="#">Samples</a>
SN74LV161ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161A	<a href="#">Samples</a>
SN74LV161ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161A	<a href="#">Samples</a>
SN74LV161ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161A	<a href="#">Samples</a>
SN74LV161ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV161A	<a href="#">Samples</a>
SN74LV161APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161A	<a href="#">Samples</a>
SN74LV161APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161A	<a href="#">Samples</a>
SN74LV161APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161A	<a href="#">Samples</a>
SN74LV161APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161A	<a href="#">Samples</a>
SN74LV161APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV161A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV161ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV161ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV161ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV161APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV161APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV161ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV161ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV161ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LV161APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV161APWT	TSSOP	PW	16	250	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



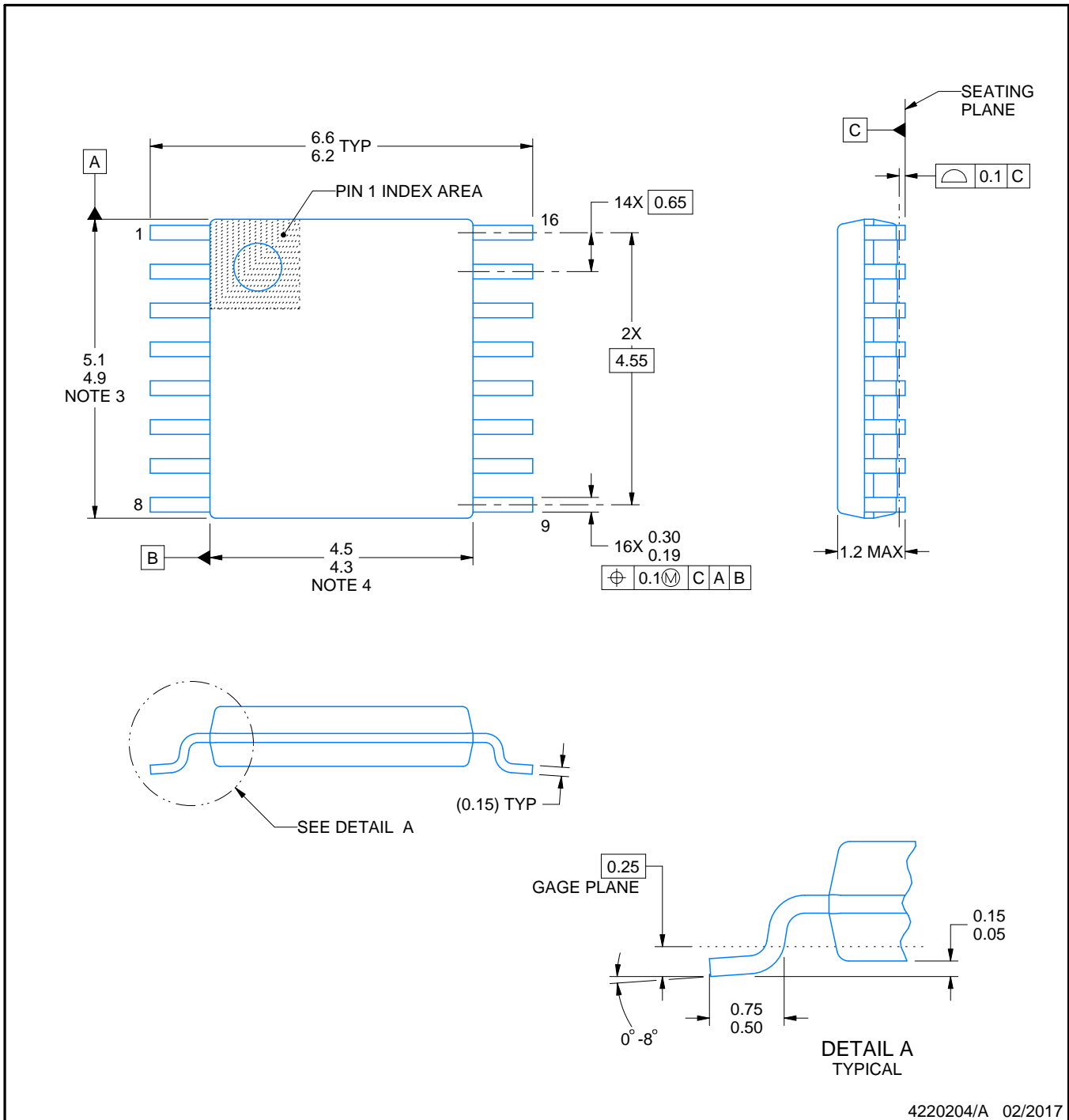
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2018, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SN74LV161ADR on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management