



# THE DATASHEET OF TPIC6273DWRG4



# TPIC6273 POWER LOGIC OCTAL D-TYPE LATCH

SLIS011A – APRIL 1992 – REVISED OCTOBER 1995

- Low  $r_{DS(on)}$  . . . 1.3  $\Omega$  Typ
- Avalanche Energy . . . 75 mJ
- Eight Power DMOS Transistor Outputs of 250-mA Continuous Current
- 1.5-A Pulsed Current Per Output
- Output Clamp Voltage up to 45 V
- Low Power Consumption

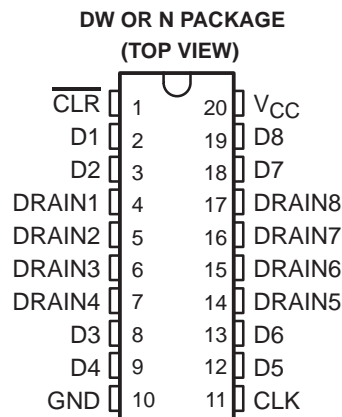
## description

The TPIC6273 is a monolithic high-voltage high-current power logic octal D-type latch with DMOS transistor outputs designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

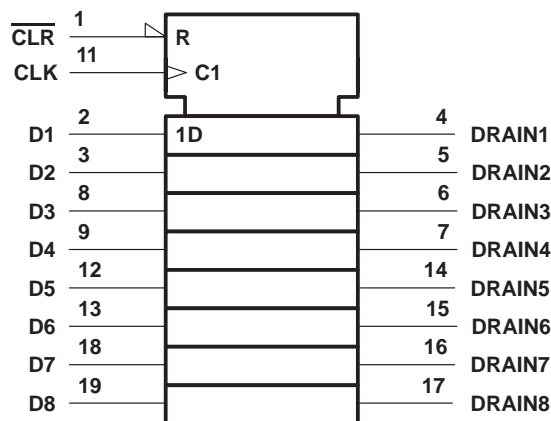
The TPIC6273 contains eight positive-edge-triggered D-type flip-flops with a direct clear input. Each flip-flop features an open-drain power DMOS transistor output.

When clear ( $\overline{CLR}$ ) is high, information at the D inputs meeting the setup time requirements is transferred to the DRAIN outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous  $\overline{CLR}$  is provided to turn all eight DMOS-transistor outputs off.

The TPIC6273 is characterized for operation over the operating case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .



## logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

**FUNCTION TABLE  
(each channel)**

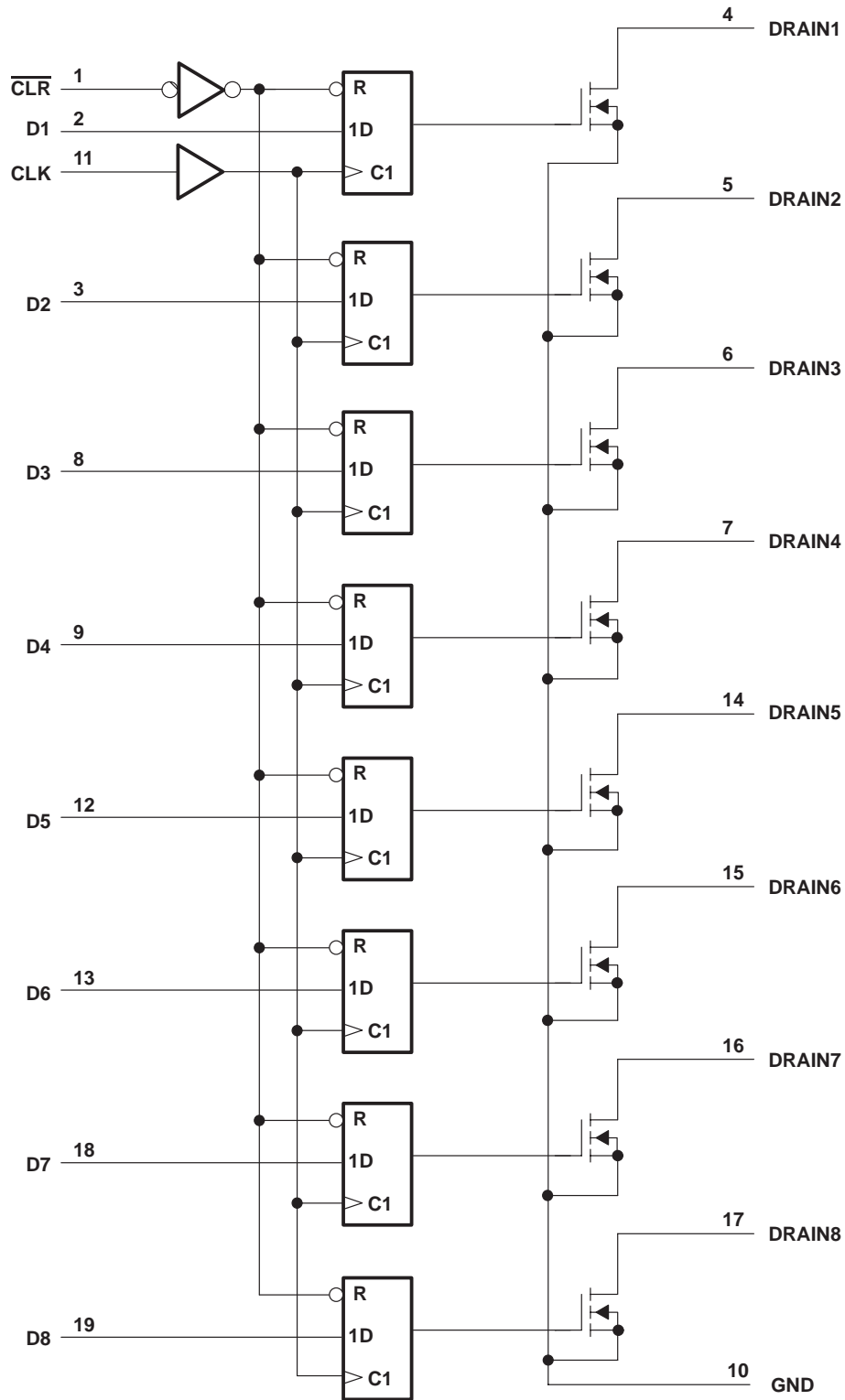
| INPUTS           |            |   | OUTPUT  |
|------------------|------------|---|---------|
| $\overline{CLR}$ | CLK        | D | DRAIN   |
| L                | X          | X | H       |
| H                | $\uparrow$ | H | L       |
| H                | $\uparrow$ | L | H       |
| H                | L          | X | Latched |

H = high level, L = low level, X = irrelevant

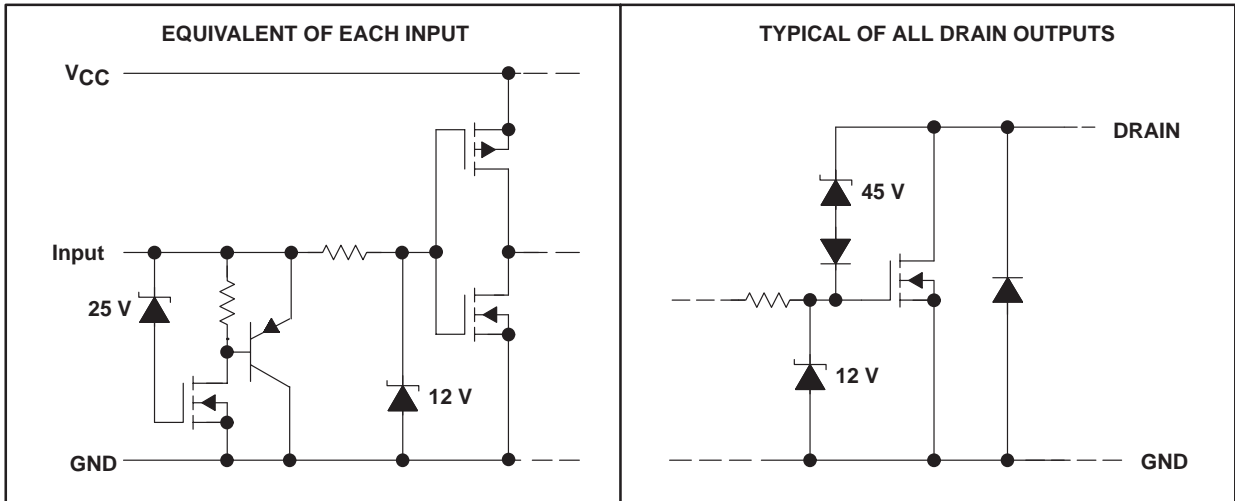
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## logic diagram (positive logic)



**schematic of inputs and outputs**



**absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†**

|   |                              |
|---|------------------------------|
| Logic supply voltage, $V_{CC}$ (see Note 1)   | 7 V                          |
| Logic input voltage range, $V_I$  | -0.3 V to 7 V                |
| Power DMOS drain-to-source voltage, $V_{DS}$ (see Note 2)   | 45 V                         |
| Continuous source-drain diode anode current   | 1 A                          |
| Pulsed source-drain diode anode current   | 2 A                          |
| Pulsed drain current, each output, all outputs on, $I_{Dn}$ , $T_A = 25^\circ\text{C}$ (see Note 3) | 750 mA                       |
| Continuous drain current, each output, all outputs on, $I_{Dn}$ , $T_A = 25^\circ\text{C}$          | 250 mA                       |
| Peak drain current single output, $I_{DM}$ , $T_A = 25^\circ\text{C}$ (see Note 3)                  | 2 A                          |
| Single-pulse avalanche energy, $E_{AS}$ (see Figure 4)  | 75 mJ                        |
| Avalanche current, $I_{AS}$ (see Note 4)  | 1 A                          |
| Continuous total power dissipation  | See Dissipation Rating Table |
| Operating virtual junction temperature range, $T_J$   | -40°C to 150°C               |
| Storage temperature range, $T_{stg}$  | -65°C to 150°C               |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds  | 260°C                        |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to GND.
  2. Each power DMOS source is internally connected to GND.
  3. Pulse duration  $\leq 100 \mu\text{s}$ , duty cycle  $\leq 2\%$
  4. DRAIN supply voltage = 15 V, starting junction temperature ( $T_{JS}$ ) = 25°C, L = 100 mH,  $I_{AS} = 1 \text{ A}$  (see Figure 4).

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 125^\circ\text{C}$<br>POWER RATING |
|---------|---|---|---|
| DW      | 1125 mW                                     | 9.0 mW/°C   | 225 mW                                    |
| N       | 1150 mW                                     | 9.2 mW/°C   | 230 mW                                    |

# TPIC6273

## POWER LOGIC OCTAL D-TYPE LATCH

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**recommended operating conditions over recommended operating temperature range (unless otherwise noted)**

|   | MIN           | MAX | UNIT             |
|---|---------------|-----|------------------|
| Logic supply voltage, $V_{CC}$  | 4.5           | 5.5 | V                |
| High-level input voltage, $V_{IH}$  | 0.85 $V_{CC}$ |     | V                |
| Low-level input voltage, $V_{IL}$   | 0.15 $V_{CC}$ |     | V                |
| Pulsed drain output current, $T_C = 25^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ (see Notes 3 and 5) | -1.8          | 1.5 | A                |
| Setup time, D high before $\text{CLK}\uparrow$ , $t_{SU}$ (see Figure 2)                          | 10            |     | ns               |
| Hold time, D high after $\text{CLK}\uparrow$ , $t_H$ (see Figure 2)                               | 15            |     | ns               |
| Pulse duration, $t_W$ (see Figure 2)  | 25            |     | ns               |
| Operating case temperature, $T_C$   | -40           | 125 | $^\circ\text{C}$ |

**electrical characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$  (unless otherwise noted)**

| PARAMETER  | TEST CONDITIONS  | MIN | TYP  | MAX | UNIT          |
|--|--|-----|------|-----|---------------|
| $V_{(BR)DSX}$ Drain-source breakdown voltage         | $I_D = 1\text{ mA}$  | 45  |      |     | V             |
| $V_{SD}$ Source-drain diode forward voltage          | $I_F = 250\text{ mA}$ , See Note 3   |     | 0.85 | 1   | V             |
| $I_{IH}$ High-level input current                    | $V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}$   |     |      | 1   | $\mu\text{A}$ |
| $I_{IL}$ Low-level input current                     | $V_{CC} = 5.5\text{ V}$ , $V_I = 0$  |     |      | -1  | $\mu\text{A}$ |
| $I_{CC}$ Logic supply current                        | $I_O = 0$ , All inputs low   |     | 15   | 100 | $\mu\text{A}$ |
| $I_N$ Nominal current                                | $V_{DS(on)} = 0.5\text{ V}$ ,<br>$I_N = I_D$ , $T_C = 85^\circ\text{C}$ See Notes 5, 6, and 7                        |     | 250  |     | mA            |
| $I_{DSX}$ Off-state drain current                    | $V_{DS} = 40\text{ V}$   |     | 0.05 | 1   | $\mu\text{A}$ |
|  | $V_{DS} = 40\text{ V}$ , $T_C = 125^\circ\text{C}$   |     | 0.15 | 5   |               |
| $r_{DS(on)}$ Static drain-source on-state resistance | $I_D = 250\text{ mA}$ , $V_{CC} = 4.5\text{ V}$  |     | 1.3  | 2   | $\Omega$      |
|  | $I_D = 250\text{ mA}$ , $T_C = 125^\circ\text{C}$ ,<br>$V_{CC} = 4.5\text{ V}$ See Notes 5 and 6 and Figures 8 and 9 |     | 2    | 3.2 |               |
|  | $I_D = 500\text{ mA}$ , $V_{CC} = 4.5\text{ V}$  |     | 1.3  | 2   |               |

**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$**

| PARAMETER   | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |    |
|---|---|-----|-----|-----|------|----|
| $t_{PLH}$ Propagation delay time, low-to-high-level output from CLK | $C_L = 30\text{ pF}$ , $I_D = 250\text{ mA}$ ,<br>See Figures 1, 2, and 10                    |     | 625 |     | ns   |    |
| $t_{PHL}$ Propagation delay time, high-to-low-level output from CLK |   |     | 150 |     | ns   |    |
| $t_r$ Rise time, drain output                                       |   |     |     | 675 |      | ns |
| $t_f$ Fall time, drain output                                       |   |     |     | 400 |      | ns |
| $t_a$ Reverse-recovery-current rise time                            | $I_F = 250\text{ mA}$ , $di/dt = 20\text{ A}/\mu\text{s}$ ,<br>See Notes 5 and 6 and Figure 3 |     | 100 |     | ns   |    |
| $t_{rr}$ Reverse-recovery time                                      |   |     | 300 |     |      |    |

- NOTES: 3. Pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 2\%$   
5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.  
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at  $T_C = 85^\circ\text{C}$ .

**thermal resistance**

| PARAMETER   | TEST CONDITIONS | MIN                            | MAX | UNIT                      |
|---|-----------------|--------------------------------|-----|---------------------------|
| $R_{\theta JA}$ Thermal resistance, junction-to-ambient | DW package      |                                | 111 | $^\circ\text{C}/\text{W}$ |
|   | N package       | All 8 outputs with equal power | 108 |                           |



PARAMETER MEASUREMENT INFORMATION

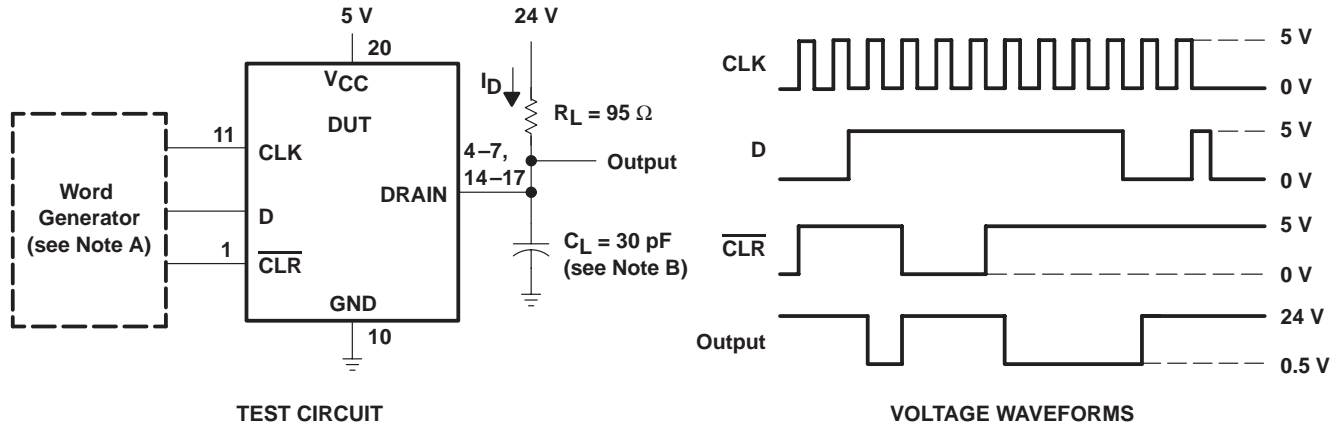


Figure 1. Resistive Load Normal Operation

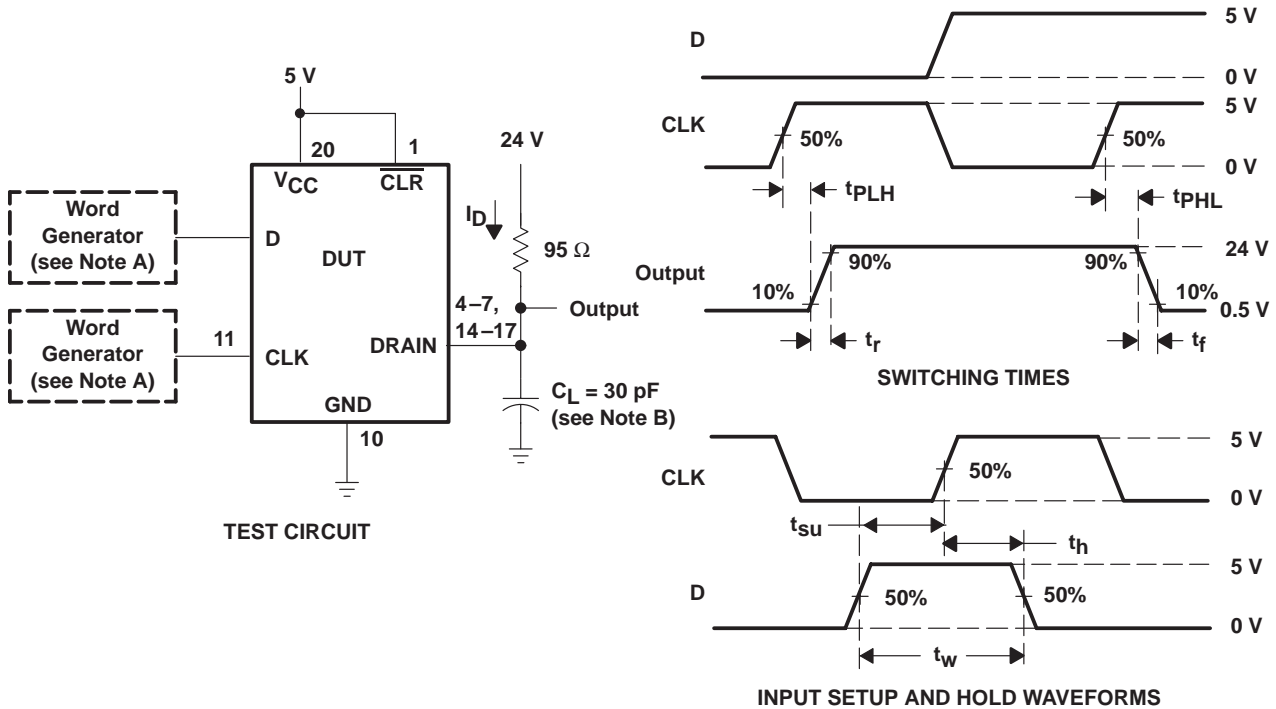


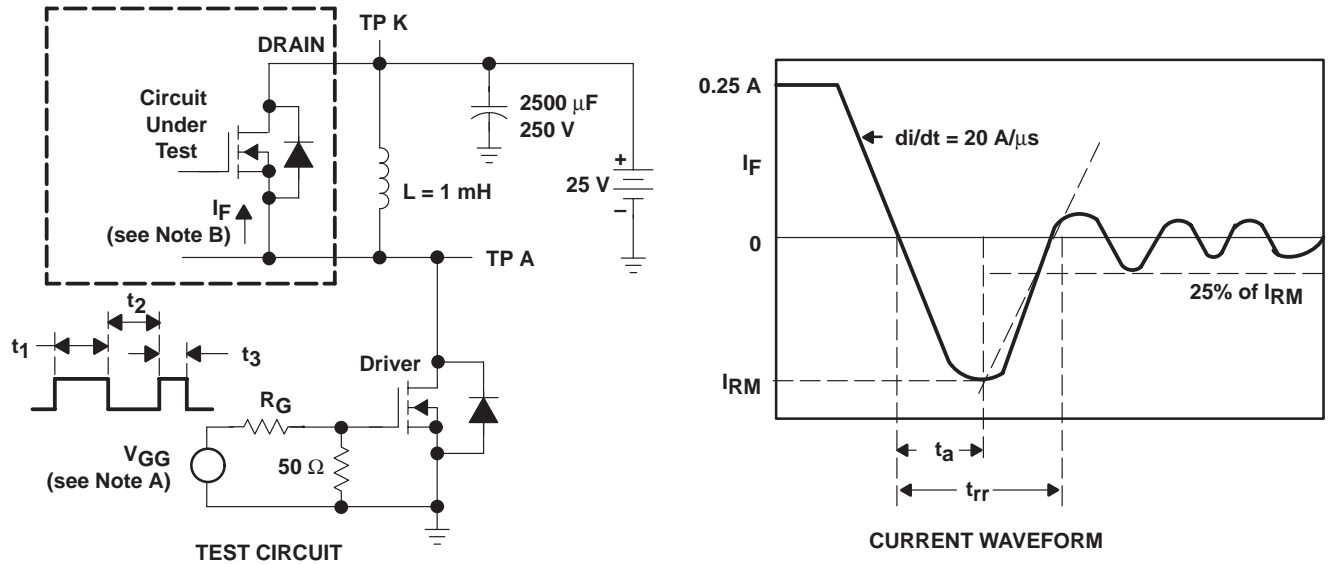
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $t_w = 300$  ns, pulsed repetition rate (PRR) = 5 KHz,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

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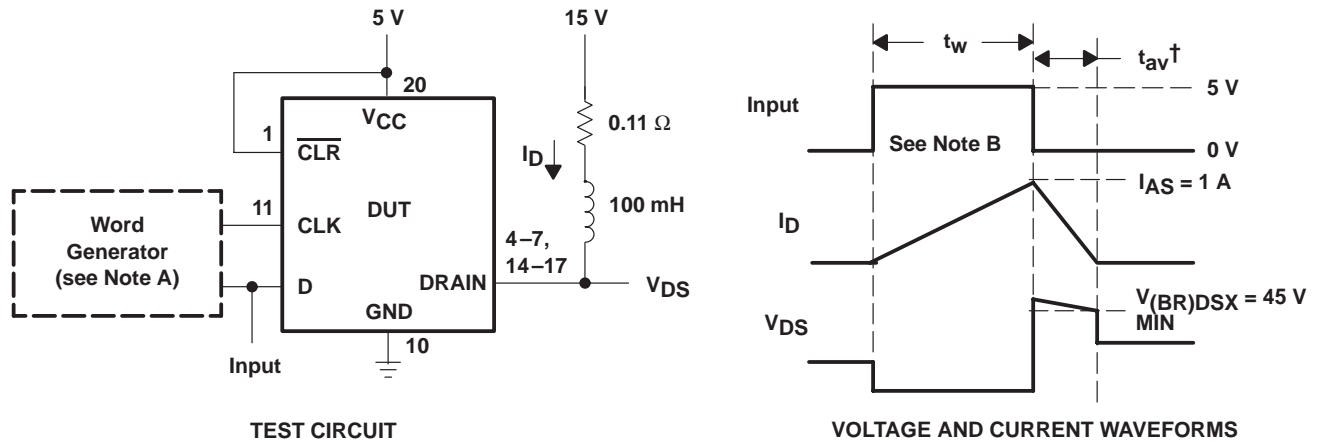
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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The  $V_{GG}$  amplitude and  $R_G$  are adjusted for  $di/dt = 20 \text{ A}/\mu\text{s}$ . A  $V_{GG}$  double-pulse train is used to set  $I_F = 0.25 \text{ A}$ , where  $t_1 = 10 \mu\text{s}$ ,  $t_2 = 7 \mu\text{s}$ , and  $t_3 = 3 \mu\text{s}$ .  
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



† Non-JEDEC symbol for avalanche ftime.

- NOTES: A. The word generator A has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
B. Input pulse duration,  $t_w$ , is increased until peak current  $I_{AS} = 1 \text{ A}$ .  
Energy test is defined as  $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 75 \text{ mJ}$ , where  $t_{av}$  = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT  
vs  
TIME DURATION OF AVALANCHE

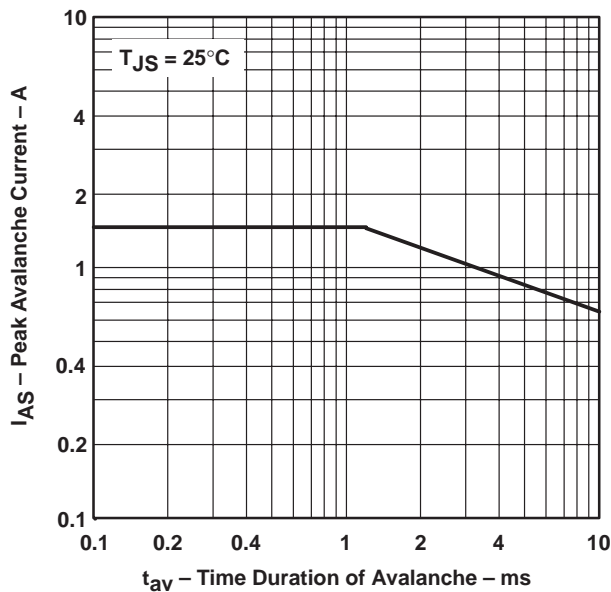


Figure 5

MAXIMUM CONTINUOUS  
DRAIN CURRENT OF EACH OUTPUT  
vs  
NUMBER OF OUTPUTS CONDUCTING  
SIMULTANEOUSLY

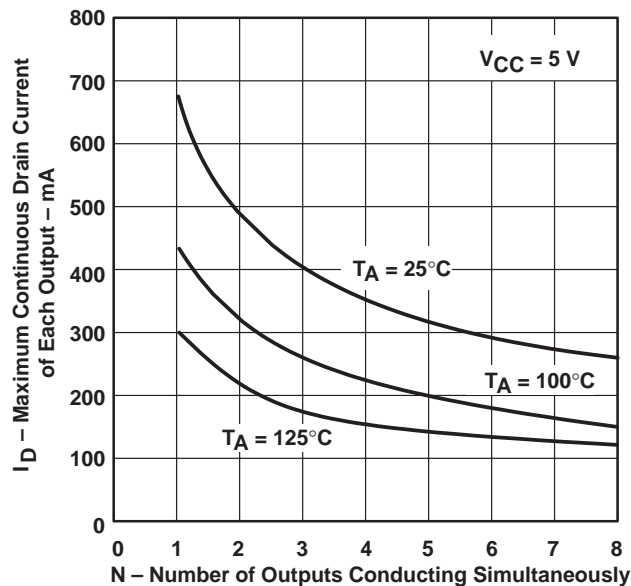


Figure 6

MAXIMUM PEAK DRAIN CURRENT  
OF EACH OUTPUT  
vs  
NUMBER OF OUTPUTS CONDUCTING  
SIMULTANEOUSLY

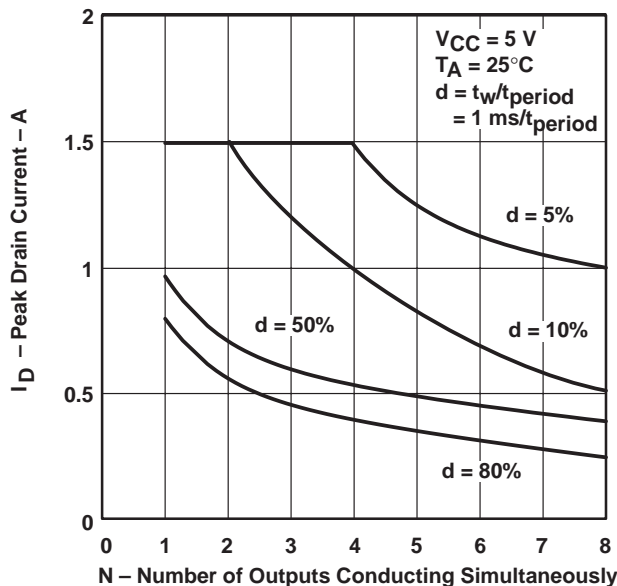


Figure 7

# TPIC6273 POWER LOGIC OCTAL D-TYPE LATCH

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## TYPICAL CHARACTERISTICS

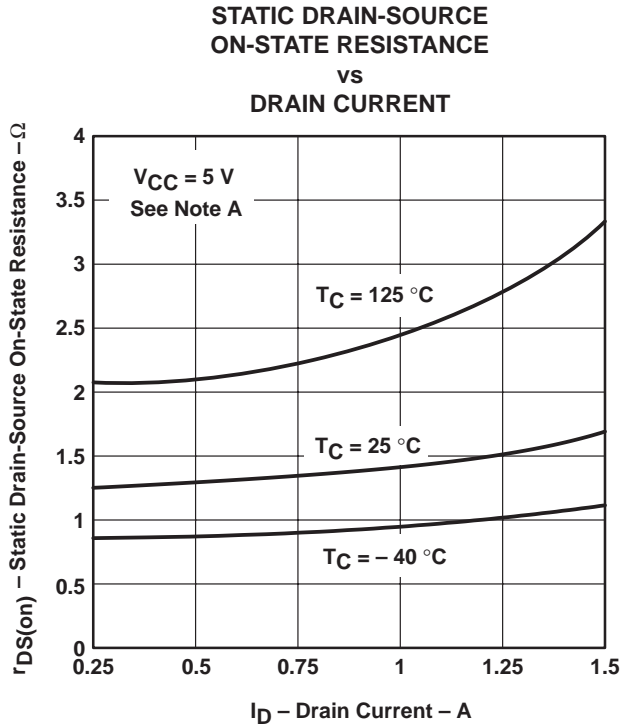


Figure 8

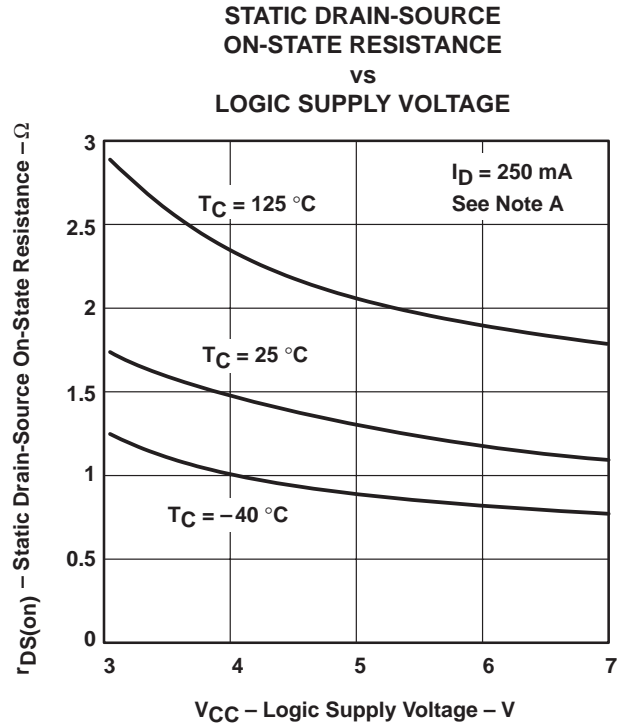


Figure 9

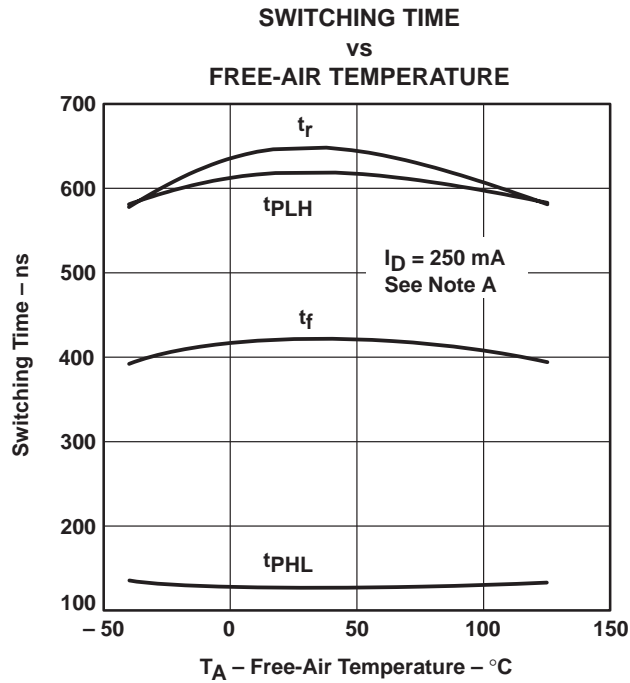


Figure 10

NOTE A: Technique should limit  $T_J - T_C$  to 10 $^{\circ}C$  maximum.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPIC6273DW       | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | TPIC6273                | <a href="#">Samples</a> |
| TPIC6273DWG4     | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TPIC6273                | <a href="#">Samples</a> |
| TPIC6273DWR      | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | TPIC6273                | <a href="#">Samples</a> |
| TPIC6273DWRG4    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | TPIC6273                | <a href="#">Samples</a> |
| TPIC6273N        | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -40 to 125   | TPIC6273N               | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPIC6273DWR   | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| TPIC6273DWRG4 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPIC6273DWR   | SOIC         | DW              | 20   | 2000 | 350.0       | 350.0      | 43.0        |
| TPIC6273DWRG4 | SOIC         | DW              | 20   | 2000 | 350.0       | 350.0      | 43.0        |

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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