



**THE DATASHEET OF
CY74FCT245CTQCT**



CY54FCT245T, CY74FCT245T 8-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS

SCCS018B – MAY 1994 – REVISED NOVEMBER 2001

- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT245T
 - 48-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT245T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current
- 3-State Outputs

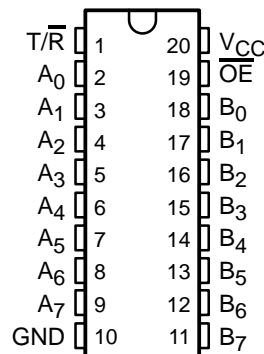
description

The 'FCT245T devices contain eight noninverting bidirectional buffers with 3-state outputs and are intended for bus-oriented applications.

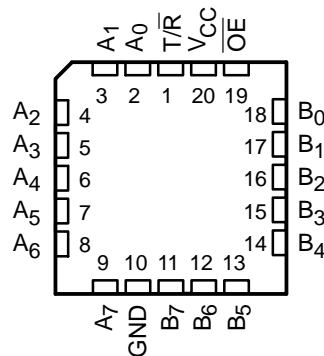
The transmit/receive (T/\bar{R}) input determines the direction of data flow through these bidirectional transceivers. Transmit (active high) enables data from A ports to B ports. The output enable (\overline{OE}), when high, disables both the A and B ports by putting them in the high-impedance state.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

CY54FCT245T . . . D PACKAGE
CY74FCT245T . . . P, Q, OR SO PACKAGE
(TOP VIEW)



CY54FCT245T . . . L PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CY54FCT245T, CY74FCT245T
8-BIT TRANSCEIVERS
WITH 3-STATE OUTPUTS

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ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	3.8	CY74FCT245DTQCT	FCT245D
	QSOP – Q	Tape and reel	4.1	CY74FCT245CTQCT	FCT245C
	SOIC – SO	Tube	4.1	CY74FCT245CTSOC	FCT245C
		Tape and reel	4.1	CY74FCT245CTSOCT	
	DIP – P	Tube	4.6	CY74FCT245ATPC	CY74FCT245ATPC
	QSOP – Q	Tape and reel	4.6	CY74FCT245ATQCT	FCT245A
	SOIC – SO	Tube	4.6	CY74FCT245ATSOC	FCT245A
		Tape and reel	4.6	CY74FCT245ATSOCT	
	QSOP – Q	Tape and reel	7	CY74FCT245TQCT	FCT245
SOIC – SO	Tube	7	CY74FCT245TSOC	FCT245	
	Tape and reel	7	CY74FCT245TSOCT		
-55°C to 125°C	CDIP – D	Tube	4.5	CY54FCT245CTDMB	
	LCC – L	Tube	4.5	CY54FCT245CTLMB	
	CDIP – D	Tube	4.9	CY54FCT245ATDMB	
	LCC – L	Tube	4.9	CY54FCT245ATLMB	
	CDIP – D	Tube	7.5	CY54FCT245TDMB	
	LCC – L	Tube	7.5	CY54FCT245TLMB	

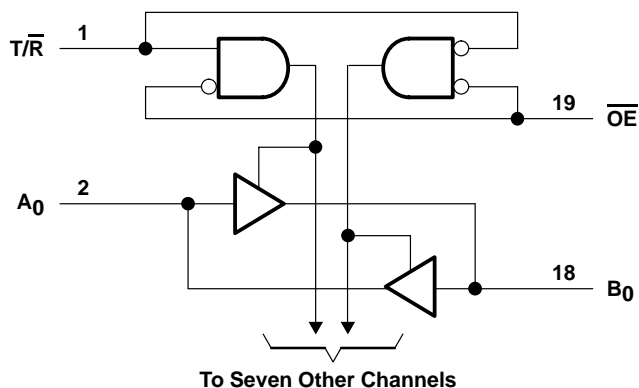
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	T/R	
L	L	B data to bus A
L	H	A data to bus B
H	X	Z

H = High logic level, L = Low logic level,
 X = Don't care, Z = High-impedance state

logic diagram (positive logic)



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CY54FCT245T, CY74FCT245T
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WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT245T			CY74FCT245T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _{IN} = -18 mA	-0.7	-1.2					V
	V _{CC} = 4.75 V, I _{IN} = -18 mA				-0.7	-1.2		
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -12 mA	2.4	3.3					V
	V _{CC} = 4.75 V	I _{OH} = -32 mA			2			
		I _{OH} = -15 mA			2.4	3.3		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA	0.3	0.55					V
	V _{CC} = 4.75 V, I _{OL} = 64 mA				0.3	0.55		
V _{hys}	All inputs	0.2			0.2			V
I _I	V _{CC} = 5.5 V, V _{IN} = V _{CC}			5				μA
	V _{CC} = 5.25 V, V _{IN} = V _{CC}					5		
I _{IH}	V _{CC} = 5.5 V, V _{IN} = 2.7 V			±1				μA
	V _{CC} = 5.25 V, V _{IN} = 2.7 V					±1		
I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.5 V			±1				μA
	V _{CC} = 5.25 V, V _{IN} = 0.5 V					±1		
I _{OZH}	V _{CC} = 5.5 V, V _{OUT} = 2.7 V			10				μA
	V _{CC} = 5.25 V, V _{OUT} = 2.7 V					10		
I _{OZL}	V _{CC} = 5.5 V, V _{OUT} = 0.5 V			-10				μA
	V _{CC} = 5.25 V, V _{OUT} = 0.5 V					-10		
I _{OS} ‡	V _{CC} = 5.5 V, V _{OUT} = 0 V	-60	-120	-225				mA
	V _{CC} = 5.25 V, V _{OUT} = 0 V				-60	-120	-225	
I _{off}	V _{CC} = 0 V, V _{OUT} = 4.5 V			±1			±1	μA
I _{CC}	V _{CC} = 5.5 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V	0.1	0.2					mA
	V _{CC} = 5.25 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V				0.1	0.2		
ΔI _{CC}	V _{CC} = 5.5 V, V _{IN} = 3.4 V [§] , f ₁ = 0, Outputs open	0.5	2					mA
	V _{CC} = 5.25 V, V _{IN} = 3.4 V [§] , f ₁ = 0, Outputs open				0.5	2		
I _{CCD} ¶	V _{CC} = 5.5 V, One input switching at 50% duty cycle, Outputs open, T/R or OE = GND and V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V	0.06	0.12					mA/ MHz
	V _{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, T/R or OE = GND and V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V				0.06	0.12		

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.



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WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT245T		CY74FCT245T		UNIT
				MIN	TYP†	MAX	MIN	
I _C #	V _{CC} = 5.5 V, Outputs open, T/R or OE = GND	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	0.7	1.4			mA
			V _{IN} = 3.4 V or GND	1.2	3.4			
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} – 0.2 V	1.3	2.6			
			V _{IN} = 3.4 V or GND	3.3	10.6			
	V _{CC} = 5.25 V, Outputs open, T/R or OE = GND	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			0.7	1.4	
			V _{IN} = 3.4 V or GND			1.2	3.4	
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} – 0.2 V			1.3	2.6	
			V _{IN} = 3.4 V or GND			3.3	10.6	
C _i				5	10	5	10	pF
C _o				9	12	9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

I_C = I_{CC} + ΔI_{CC} × D_H × N_T + I_{CCD} (f₀/2 + f₁ × N₁)

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f₁ = Input signal frequency

N₁ = Number of inputs changing at f₁

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

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switching characteristics over operating free-air temperature range (see Figure 1)

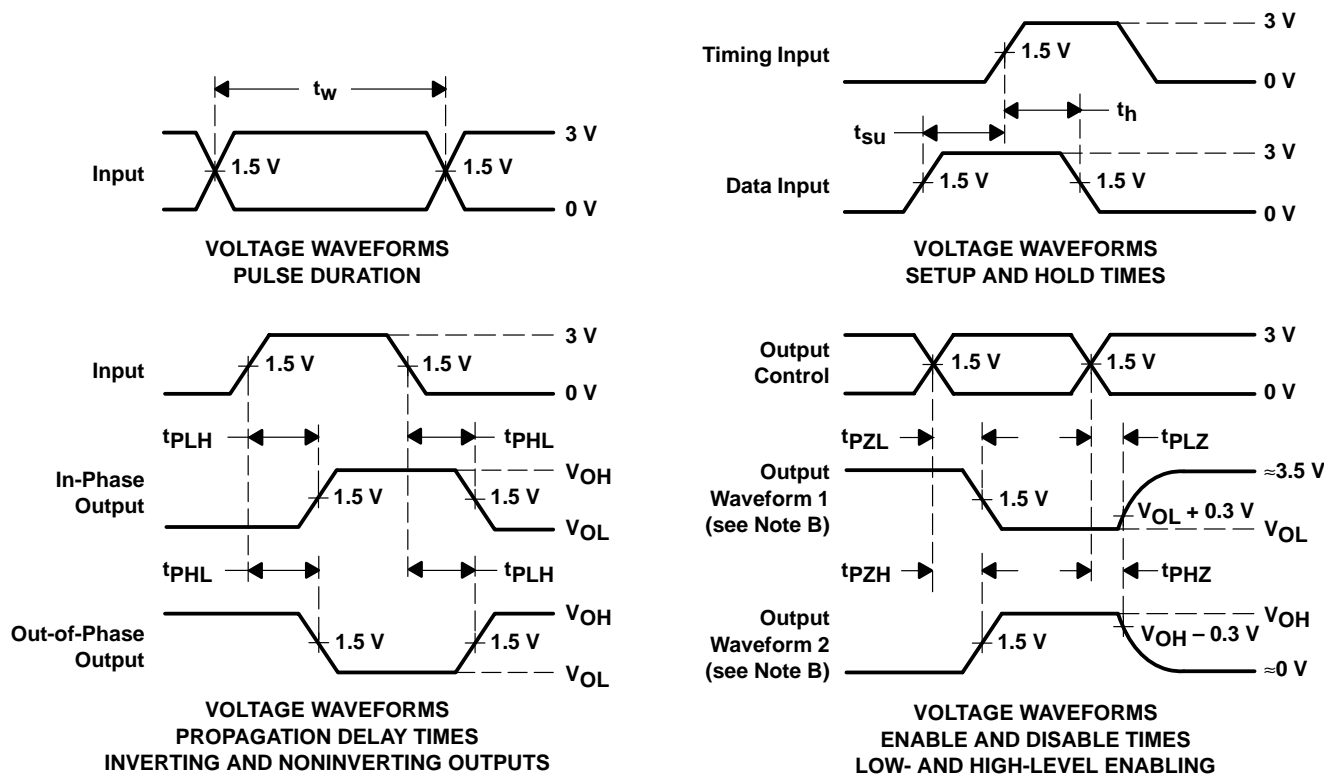
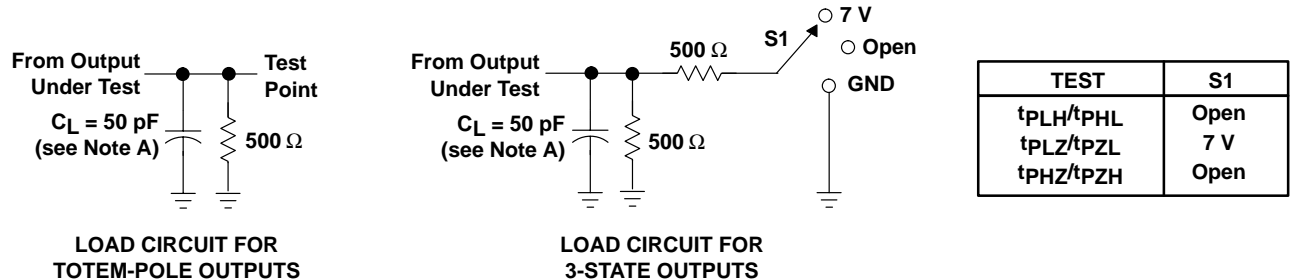
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT245T		CY54FCT245AT		CY54FCT245CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	1.5	7.5	1.5	4.9	1.5	4.5	ns
t _{PHL}			1.5	7.5	1.5	4.9	1.5	4.5	
t _{PZH}	\overline{OE} or T/ \overline{R}	A or B	1.5	10	1.5	6.5	1.5	6.2	ns
t _{PZL}			1.5	10	1.5	6.5	1.5	6.2	
t _{PHZ}	\overline{OE} or T/ \overline{R}	A or B	1.5	10	1.5	6	1.5	5.2	ns
t _{PLZ}			1.5	10	1.5	6	1.5	5.2	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT245T		CY74FCT245AT		CY74FCT245CT		CY74FCT245DT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	1.5	7	1.5	4.6	1.5	4.1	1.5	3.8	ns
t _{PHL}			1.5	7	1.5	4.6	1.5	4.1	1.5	3.8	
t _{PZH}	\overline{OE} or T/ \overline{R}	A or B	1.5	9.5	1.5	6.2	1.5	5.8	1.5	5	ns
t _{PZL}			1.5	9.5	1.5	6.2	1.5	5.8	1.5	5	
t _{PHZ}	\overline{OE} or T/ \overline{R}	A or B	1.5	7.5	1.5	5	1.5	4.8	1.5	4.3	ns
t _{PLZ}			1.5	7.5	1.5	5	1.5	4.8	1.5	4.3	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9221401M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9221401M2A CY54FCT 245TLMB	Samples
5962-9221401MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9221401MR A	Samples
5962-9221403M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9221403M2A	Samples
5962-9221403MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9221403MR A CY54FCT245ATDM B	Samples
5962-9221405M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9221405M2A CY54FCT 245CTLMB	Samples
5962-9221405MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9221405MR A	Samples
CY54FCT245ATDMB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9221403MR A CY54FCT245ATDM B	Samples
CY54FCT245CTLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9221405M2A CY54FCT 245CTLMB	Samples
CY54FCT245TLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9221401M2A CY54FCT 245TLMB	Samples
CY74FCT245ATPC	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	CY74FCT245ATPC	Samples
CY74FCT245ATPCE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	CY74FCT245ATPC	Samples
CY74FCT245ATQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT245ATQCTE4	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245A	Samples
CY74FCT245ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245A	Samples
CY74FCT245ATSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245A	Samples
CY74FCT245CTQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245C	Samples
CY74FCT245CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245C	Samples
CY74FCT245TQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245	Samples
CY74FCT245TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245	Samples
CY74FCT245TSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245	Samples
CY74FCT245TSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT245ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT245ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT245CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT245TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT245TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT245ATQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT245ATSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT245CTQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT245TQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT245TSOCT	SOIC	DW	20	2000	367.0	367.0	45.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

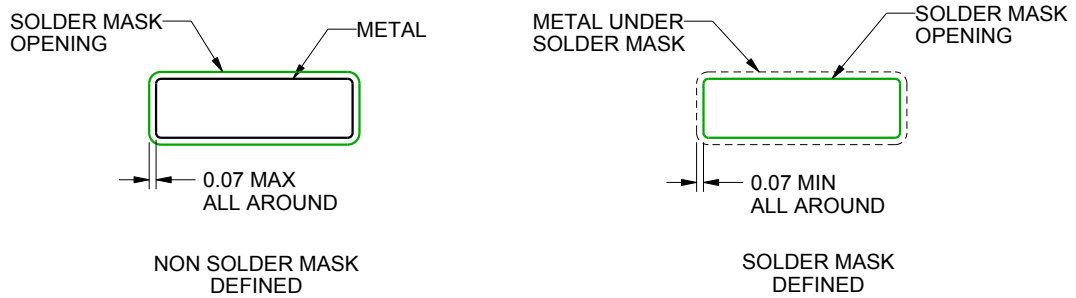
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

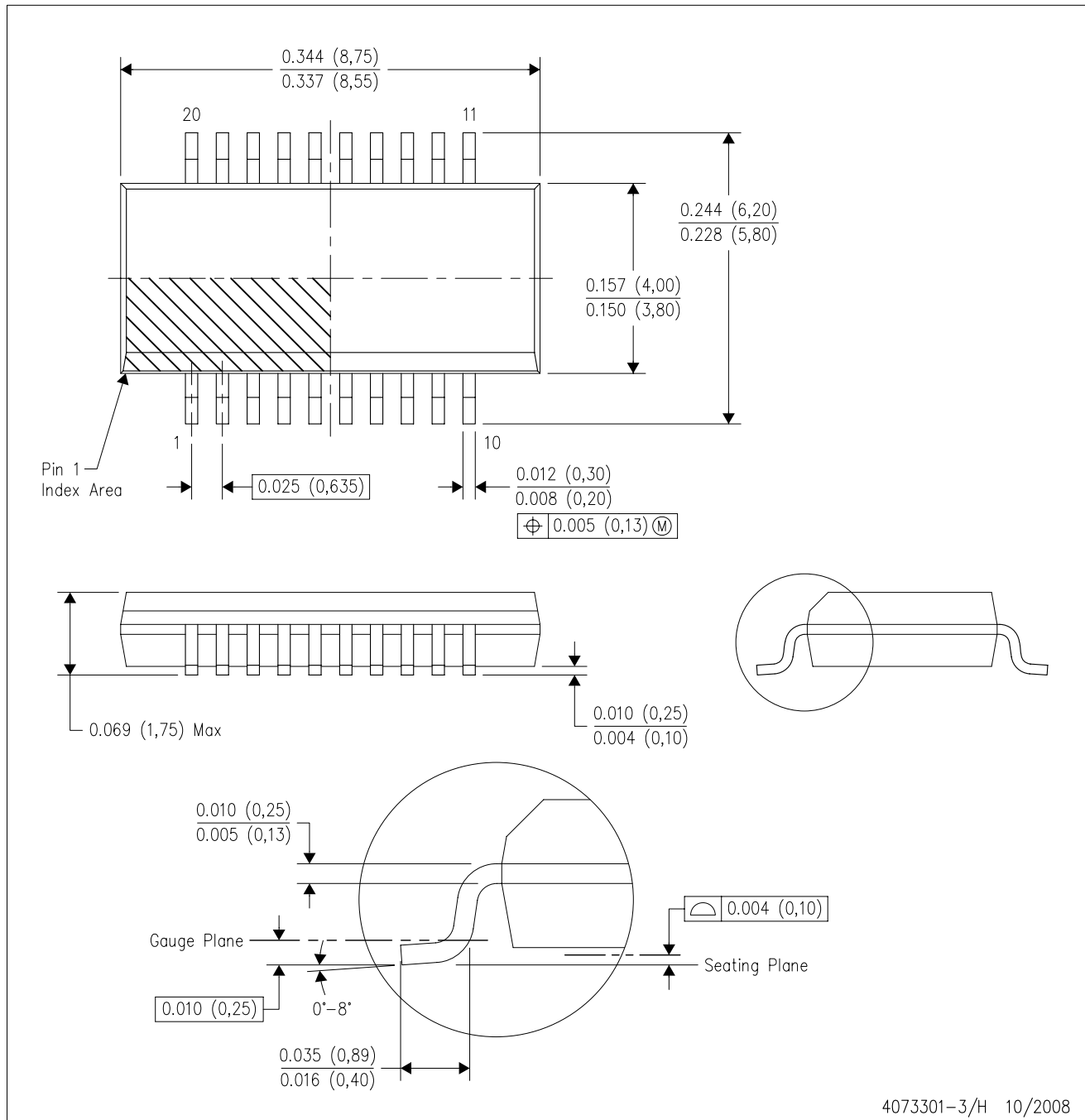


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

DBQ (R-PDSO-G20)

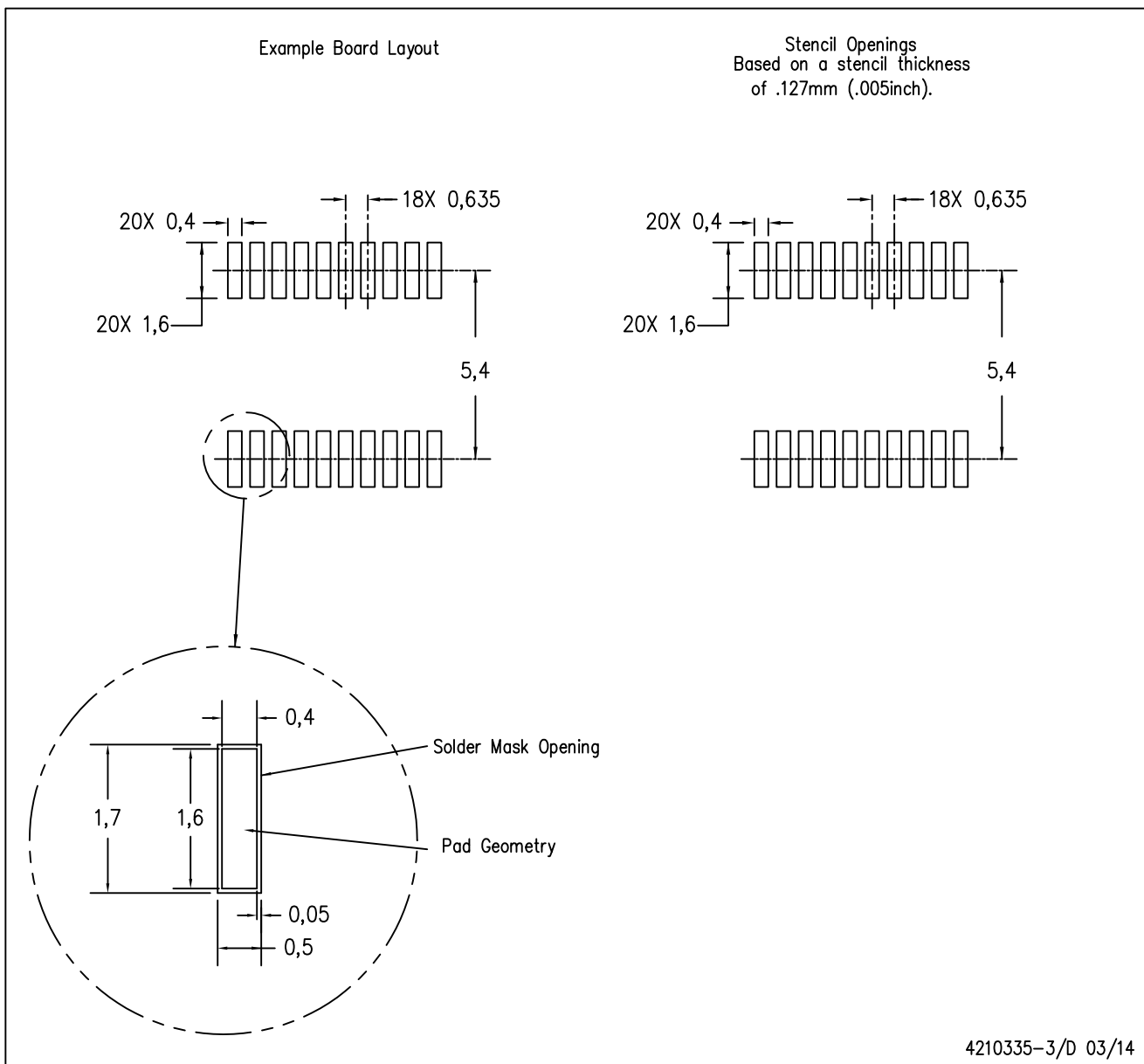
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AD.

DBQ (R-PDSO-G20)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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