

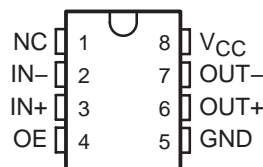


# THE DATASHEET OF TL712CP



- Operates From a Single 5-V Supply
- 0-V to 5.5-V Common-Mode Input Voltage Range
- Self-Biased Inputs
- Complementary 3-State Outputs
- Enable Capability
- Hysteresis . . . 5 mV Typ
- Response Times . . . 25 ns Typ

D, P, PS, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

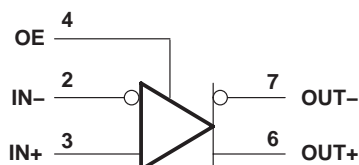
The TL712 is a high-speed comparator fabricated with bipolar Schottky process technology. The circuit has differential analog inputs and complementary 3-state TTL-compatible logic outputs with symmetrical switching characteristics. When the output enable (OE) is low, both outputs are in the high-impedance state. This device operates from a single 5-V supply and is useful as a disk memory read-chain data comparator.

## ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE†   |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|--------------|-----------------------|------------------|
| 0°C to 70°C    | PDIP (P)   | Tube of 50   | TL712CP               | TL712CP          |
|                | SOIC (D)   | Tube of 75   | TL712CD               | TL712C           |
|                |            | Reel of 2500 | TL712CDR              |                  |
|                | SOP (PS)   | Reel of 2000 | TL712CPSR             | T712             |
|                | TSSOP (PW) | Tube of 150  | TL712CPW              | T712             |
|                |            | Reel of 2000 | TL712CPWR             |                  |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## symbol (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**PRODUCTION DATA** information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

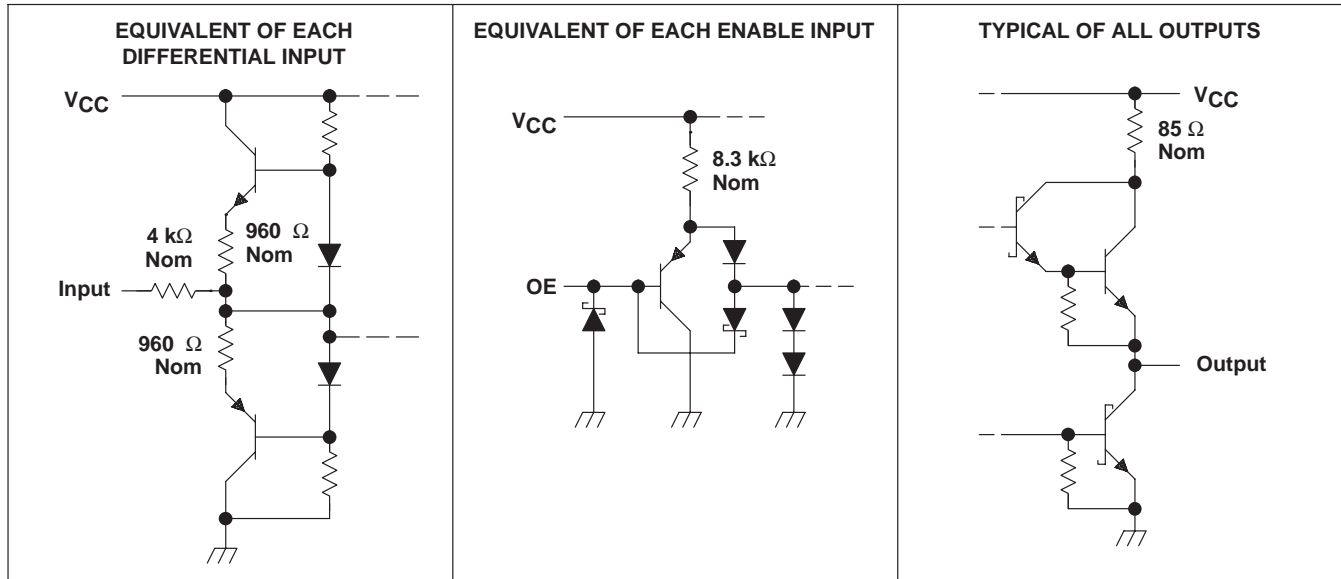
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

# TL712 DIFFERENTIAL COMPARATOR

SLCS002D – JUNE 1983 – REVISED AUGUST 2003

## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|   |                |
|---|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)                         | 7 V            |
| Differential input voltage, $V_{ID}$ (see Note 2)             | $\pm 25$ V     |
| Input voltage, $V_I$ , any differential input                 | $\pm 25$ V     |
| Output enable voltage   | 7 V            |
| Low-level output current, $I_{OL}$                            | 50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Notes 3 and 4): |                |
| D package   | 97°C/W         |
| P package   | 85°C/W         |
| PS package  | 95°C/W         |
| PW package  | 149°C/W        |
| Operating virtual junction temperature, $T_J$                 | 150°C          |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds  | 260°C          |
| Storage temperature range, $T_{stg}$                          | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the network ground.
  2. Differential voltage values are at  $IN+$  with respect to  $IN-$ .
  3. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A) / \theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  4. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions**

|   | MIN  | NOM | MAX  | UNIT |
|---|------|-----|------|------|
| V <sub>CC</sub> Supply voltage                | 4.75 | 5   | 5.25 | V    |
| V <sub>IC</sub> Common-mode input voltage     | 0    |     | 5.5  | V    |
| I <sub>OH</sub> High-level output current     |      |     | -1   | mA   |
| I <sub>OL</sub> Low-level output current      |      |     | 16   | mA   |
| T <sub>A</sub> Operating free-air temperature | 0    |     | 70   | °C   |

**electrical characteristics at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

| PARAMETER   | TEST CONDITIONS                                    | MIN               | TYP | MAX  | UNIT |
|---|--|-------------------|-----|------|------|
| V <sub>T</sub> Threshold voltage (V <sub>T+</sub> and V <sub>T-</sub> ) | V <sub>ICR</sub> = 0 to 5 V                        | -100 <sup>†</sup> |     | 100  | mV   |
| V <sub>hys</sub> Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )        |  |                   | 5   |      | mV   |
| V <sub>OH</sub> High-level output voltage                               | V <sub>ID</sub> = 100 mV, I <sub>OH</sub> = -1 mA  | 2.7               | 3.5 |      | V    |
| V <sub>OL</sub> Low-level output voltage                                | V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 16 mA |                   | 0.4 | 0.5  | V    |
| I <sub>OZ</sub> Off-state output current                                | V <sub>O</sub> = 2.4 V                             |                   |     | -20  | μA   |
| I <sub>I</sub> Enable current   | V <sub>I</sub> = 5.5 V                             |                   |     | 100  | μA   |
| I <sub>IH</sub> High-level enable current                               | V <sub>IH</sub> = 2.7 V                            |                   |     | 20   | μA   |
| I <sub>IL</sub> Low-level enable current                                | V <sub>IL</sub> = 0.4 V                            |                   |     | -360 | μA   |
| r <sub>i</sub> Differential input resistance                            |  | 4                 |     |      | kΩ   |
| r <sub>o</sub> Output resistance  |  |                   |     | 100  | Ω    |
| I <sub>OS</sub> Short-circuit output current                            |  | -15               |     | -85  | mA   |
| I <sub>CC</sub> Supply current  | V <sub>ID</sub> = 0, No load                       |                   | 17  | 20   | mA   |

<sup>†</sup> The algebraic convention, where the more-negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

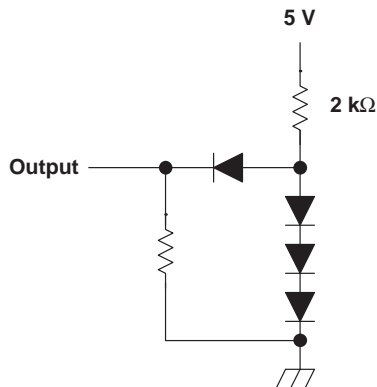
| PARAMETER   | TEST CONDITIONS                   | TYP | UNIT |
|---|-----------------------------------|-----|------|
| t <sub>PLH</sub> Propagation delay time, low-to-high-level output | TTL load, See Note 5 and Figure 1 | 25  | ns   |
| t <sub>PHL</sub> Propagation delay time, high-to-low-level output |                                   | 25  | ns   |

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive (105 mV total) and is the interval between the input step function and the instant when the output crosses 2.5 V.

# TL712 DIFFERENTIAL COMPARATOR

SLCS002D – JUNE 1983 – REVISED AUGUST 2003

## PARAMETER MEASUREMENT INFORMATION



NOTE A: All diodes are 1N4148 or equivalent.

Figure 1. TTL Output Load Circuit

## TYPICAL CHARACTERISTICS

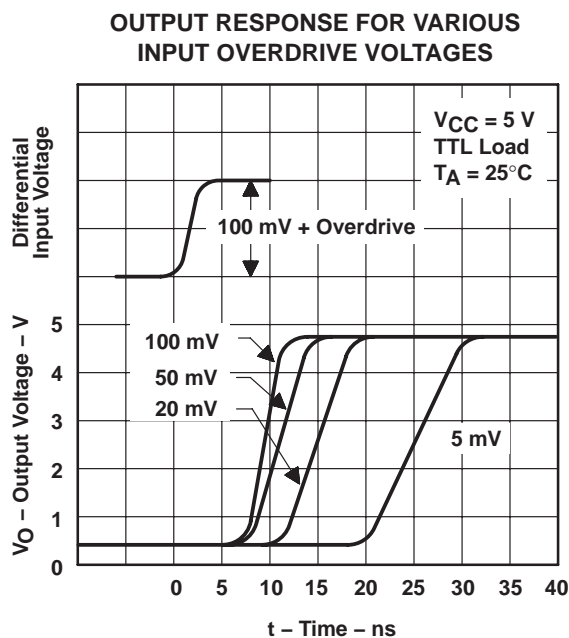


Figure 2

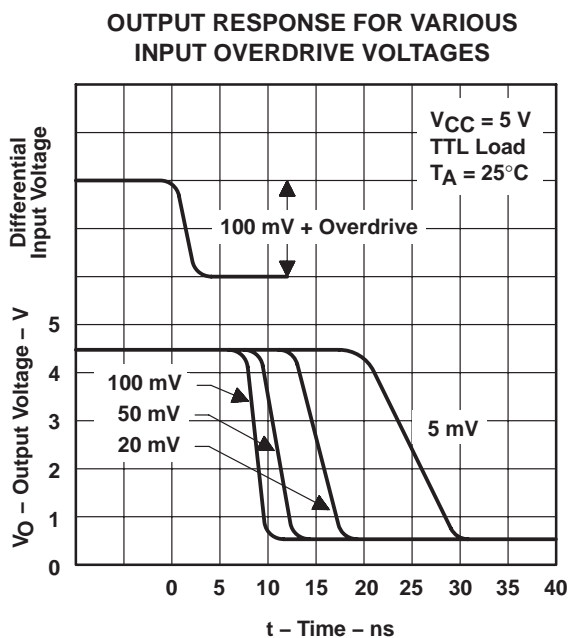


Figure 3

TYPICAL CHARACTERISTICS

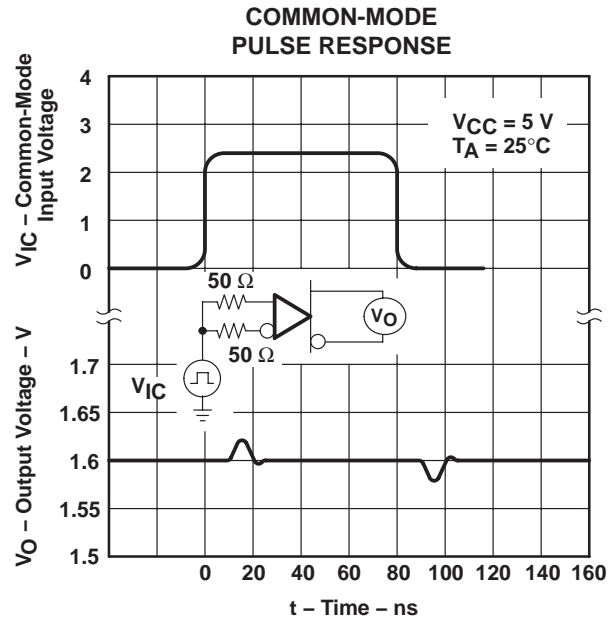


Figure 4

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL712CD          | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL712C                  | <a href="#">Samples</a> |
| TL712CDG4        | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL712C                  | <a href="#">Samples</a> |
| TL712CDR         | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL712C                  | <a href="#">Samples</a> |
| TL712CP          | ACTIVE        | PDIP         | P               | 8    | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL712CP                 | <a href="#">Samples</a> |
| TL712CPSR        | ACTIVE        | SO           | PS              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T712                    | <a href="#">Samples</a> |
| TL712CPSRG4      | ACTIVE        | SO           | PS              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T712                    | <a href="#">Samples</a> |
| TL712CPWR        | ACTIVE        | TSSOP        | PW              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T712                    | <a href="#">Samples</a> |
| TL712CPWRE4      | ACTIVE        | TSSOP        | PW              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T712                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

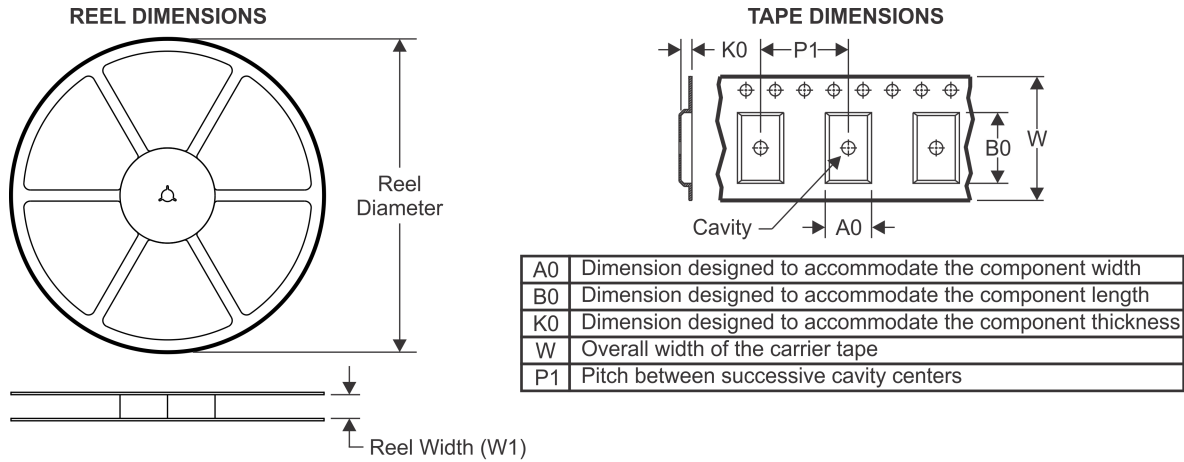
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL712CDR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL712CPWR | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL712CDR  | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TL712CPWR | TSSOP        | PW              | 8    | 2000 | 367.0       | 367.0      | 35.0        |



# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

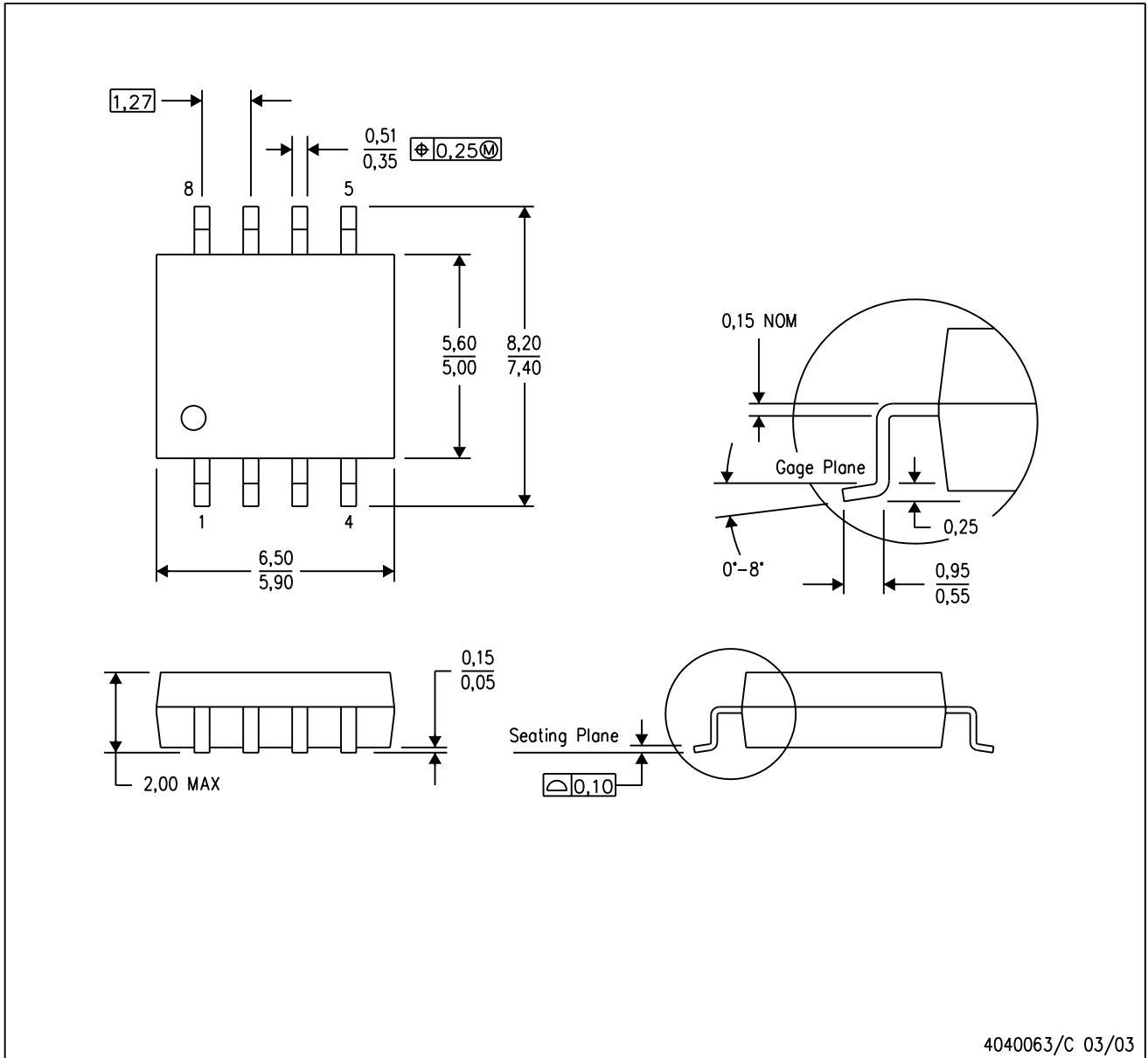
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

PS (R-PDSO-G8)

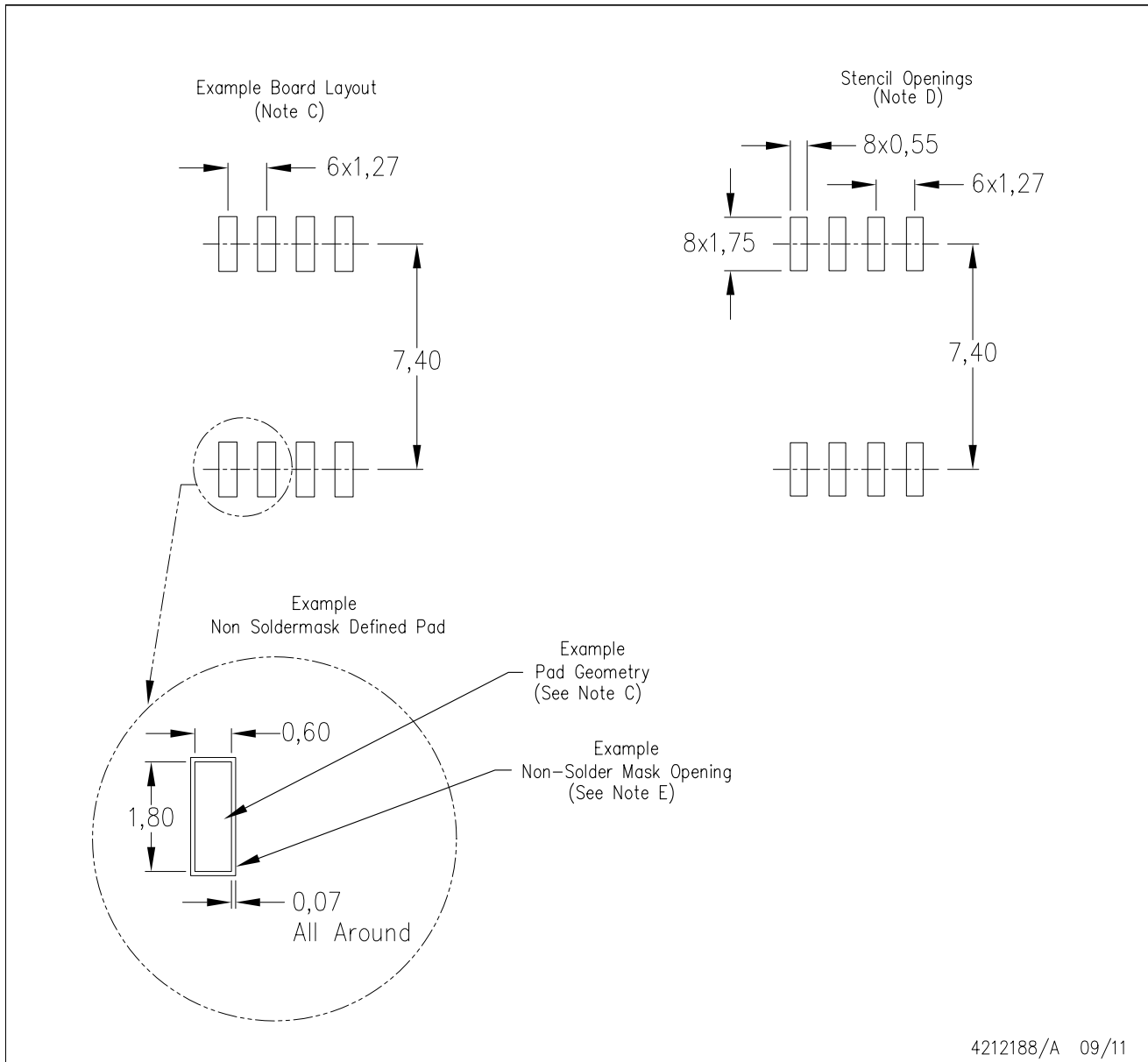
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

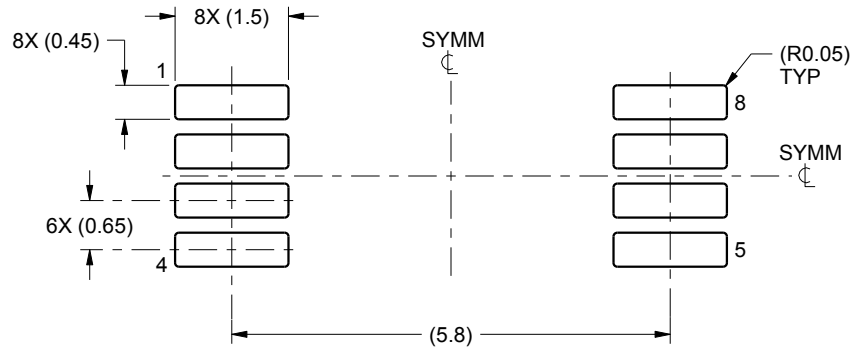


# EXAMPLE BOARD LAYOUT

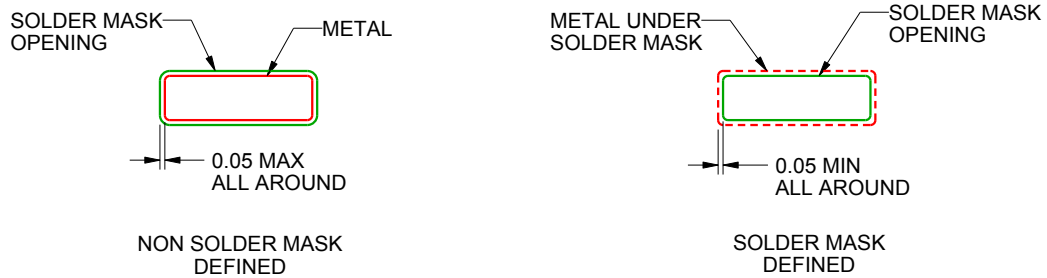
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View TL712CP](#) on WIN SOURCE

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management