



**THE DATASHEET OF  
MC74HCT04ADTR2G**



# MC74HCT04A

## Hex Inverter

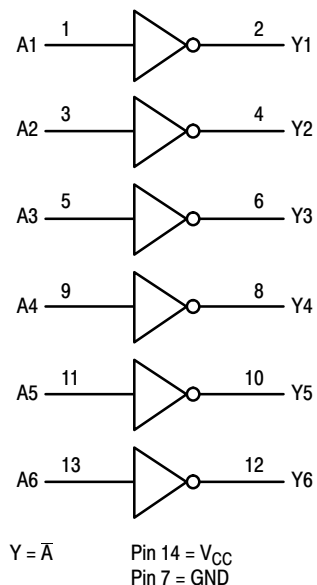
### With LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC74HCT04A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT04A is identical in pinout to the LS04.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1  $\mu$ A
- In Compliance With the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 48 FETs or 12 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### LOGIC DIAGRAM



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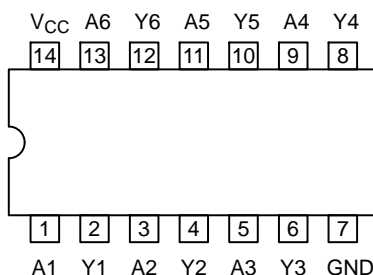


SOIC-14 NB  
D SUFFIX  
CASE 751A



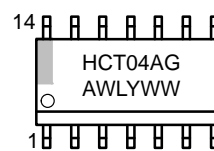
TSSOP-14  
DT SUFFIX  
CASE 948G

#### PIN ASSIGNMENT

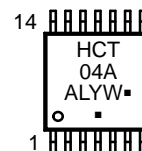


14-Lead (Top View)

#### MARKING DIAGRAMS



SOIC-14 NB



TSSOP-14

A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### FUNCTION TABLE

Inputs	Outputs
A	Y
L	H
H	L

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

# MC74HCT04A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air SOIC Package† TSSOP Package†	500 450	mW
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C  
TSSOP Package: -6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature Range, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise/Fall Time (Figure 1)	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	$V_{CC}$ V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1V$ $ I_{out}  \leq 20\mu A$	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1V$ $ I_{out}  \leq 20\mu A$	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \leq 20\mu A$	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out}  \leq 20\mu A$	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	4.5	0.26	0.33	0.40	$\mu A$
			5.5	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\mu A$	4.5	1	10	40	$\mu A$
			5.5	1	10	40	
$\Delta I_{CC}$	Additional Quiescent Supply Current	$V_{in} = 2.4V$ , Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0\mu A$	5.5	≥ -55°C	25 to 125°C		mA
				2.9	2.4		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

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## AC CHARACTERISTICS ( $V_{CC} = 5.0V \pm 10\%$ , $C_L = 50pF$ , Input $t_r = t_f = 6ns$ )

Symbol	Parameter	Guaranteed Limit			Unit
		-55 to 25°C	≤85°C	≤125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	15 17	19 21	22 26	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF

$C_{PD}$	Power Dissipation Capacitance (Per Inverter)*	Typical @ 25°C, $V_{CC} = 5.0 V$		pF
		22		

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

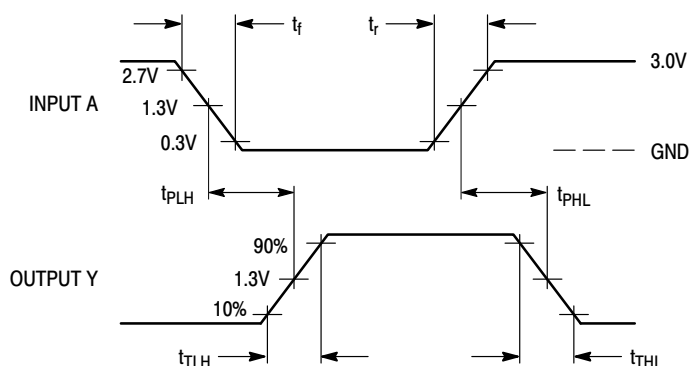
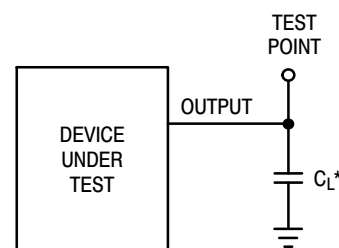


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit

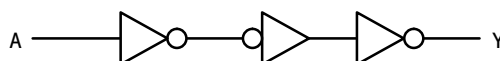


Figure 3. Expanded Logic Diagram  
(1/6 of the Device Shown)

## ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT04ADG	SOIC-14 NB (Pb-Free)	55 Units / Rail
MC74HCT04ADR2G	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
MC74HCT04ADTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV74HCT04ADG*	SOIC-14 NB (Pb-Free)	55 Units / Rail
NLV74HCT04ADR2G*	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
NLV74HCT04ADTR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

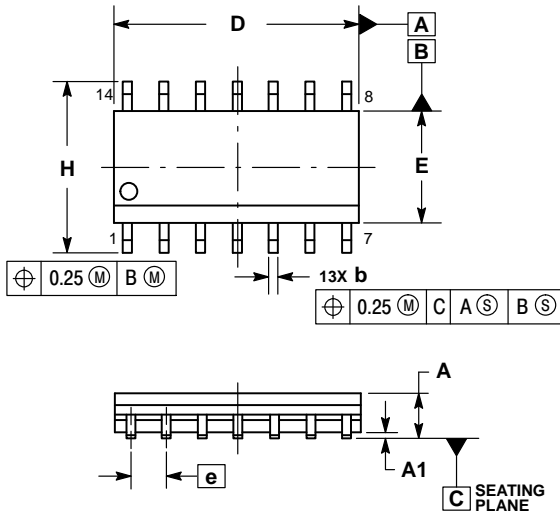
\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.



# MC74HCT04A

## PACKAGE DIMENSIONS

### SOIC-14 NB CASE 751A-03 ISSUE K

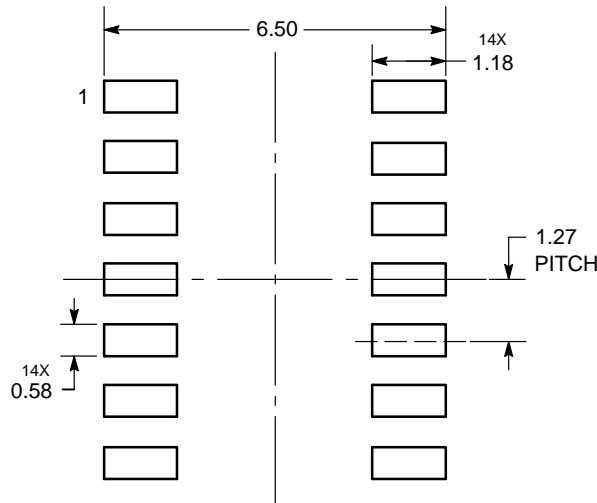


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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