

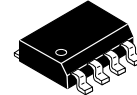
High-Side and Low-Side Gate Driver

FAN7382

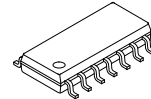
The FAN7382, a monolithic high and low side gate-drive IC, can drive MOSFETs and IGBTs that operate up to +600 V. onsemi's high-voltage process and commonmode noise canceling technique provides stable operation of the high-side driver under high-dv/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to $V_S = -9.8$ V (typical) for $V_{BS} = 15$ V. The input logic level is compatible with standard TTL-series logic gates. UVLO circuits for both channels prevent malfunction when V_{CC} or V_{BS} is lower than the specified threshold voltage. Output drivers typically source/sink 350 mA/650 mA, respectively, which is suitable for fluorescent lamp ballasts, PDP scan drivers, motor controls, etc.

Features

- Floating Channels Designed for Bootstrap Operation to +600 V
- Typically 350 mA/650 mA Sourcing/Sinking Current Driving Capability for Both Channels
- Common-Mode dv/dt Noise Canceling Circuit
- Extended Allowable Negative V_S Swing to -9.8 V for Signal Propagation at $V_{CC} = V_{BS} = 15$ V
- V_{CC} & V_{BS} Supply Range from 10 V to 20 V
- UVLO Functions for Both Channels
- TTL Compatible Input Logic Threshold Levels
- Matched Propagation Delay Below 50 ns
- Output In-phase with Input Signal
- These are Pb-Free Devices



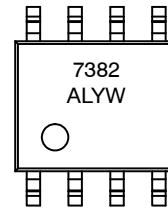
SOIC8
CASE 751EG



SOIC14 N
CASE 751ER

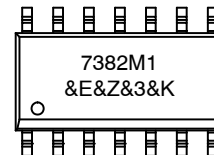
MARKING DIAGRAMS

SOIC8



7382 = Device Code
 A = Assembly Site
 L = Wafer Lot Number
 YW = Assembly Start Week

SOIC14 N



7382M1 = Device Code
 &E = Designates Space
 &Z = Assembly Location
 &3 = 3-Digit Date Code
 &K = 2-Digits Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

FAN7382

Typical Application Circuit

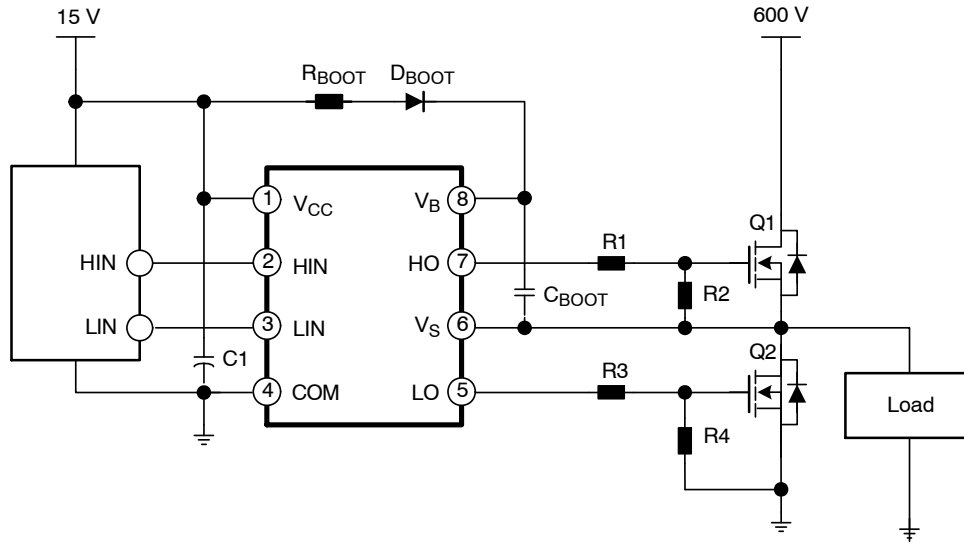


Figure 1. Application Circuit for Half-Bridge

Internal Block Diagram

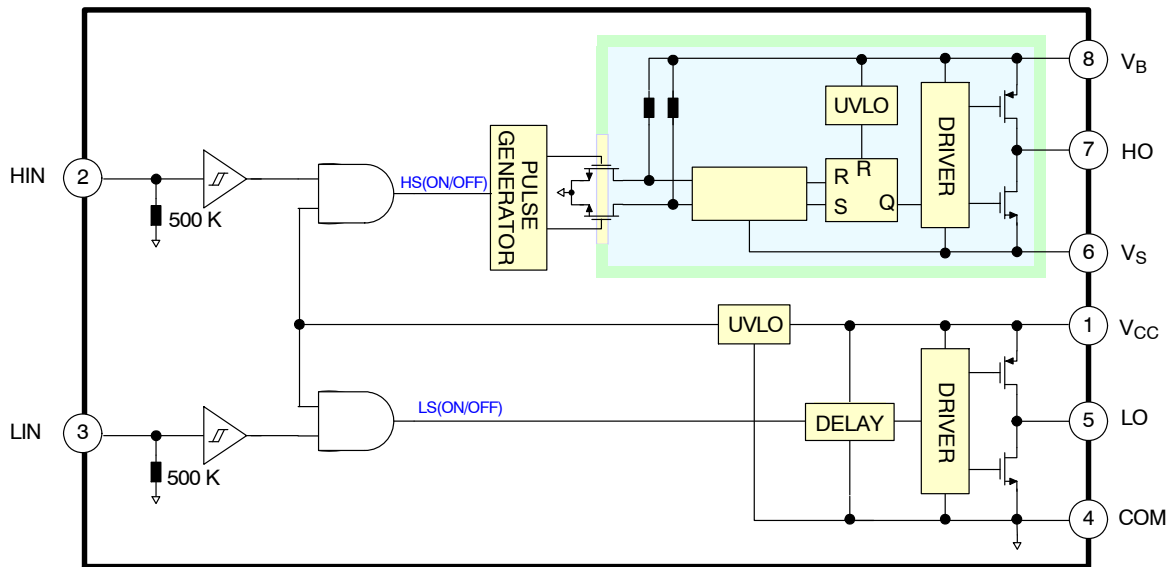


Figure 2. Functional Block Diagram

FAN7382

Pin Assignments

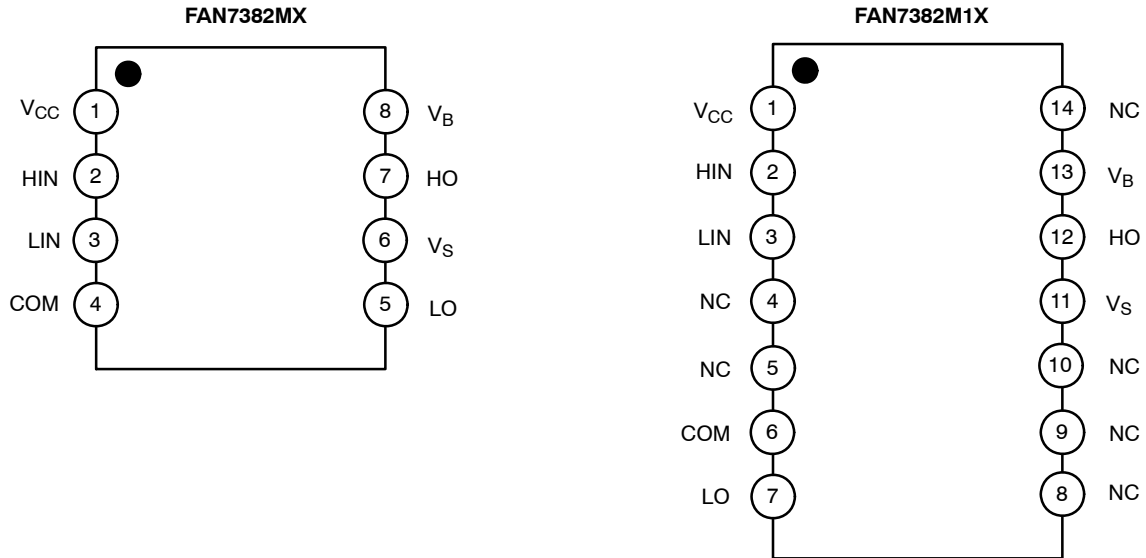


Figure 3. Pin Configuration (Top View)

PIN DEFINITIONS

Name	Description
V _{CC}	Low-Side Supply Voltage
HIN	Logic Input for High-Side Gate Driver Output
LIN	Logic Input for Low-Side Gate Driver Output
COM	Logic Ground and Low-Side Driver Return
LO	Low-Side Driver Output
V _S	High-Voltage Floating Supply Return
HO	High-Side Driver Output
V _B	High-Side Floating Supply

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
High-Side Offset Voltage	V_S	$V_B - 25$	$V_B + 0.3$	V
High-Side Floating Supply Voltage	V_B	-0.3	625	
High-Side Floating Output Voltage HO	V_{HO}	$V_S - 0.3$	$V_B + 0.3$	
Low-Side and Logic Fixed Supply Voltage	V_{CC}	-0.3	25	
Low-Side Output Voltage LO	V_{LO}	-0.3	$V_{CC} + 0.3$	
Logic Input Voltage (HIN, LIN)	V_{IN}	-0.3	$V_{CC} + 0.3$	
Logic Ground	COM	$V_{CC} - 25$	$V_{CC} + 0.3$	
Allowable Offset Voltage Slew Rate	dV_S/dt		50	V/ns
Power Dissipation	P_D (Notes 1, 2, 3)	SOIC8	0.625	W
		SOIC14 N	1.0	
Junction temperature	T_J		150	°C
Storage Temperature	T_{STG}		150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
2. Refer to the following standards:
 JESD51-2: Integral circuits thermal test method environmental conditions – natural convection
 JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
3. Do not exceed P_D under any circumstances.

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Thermal Resistance, Junction-to-Ambient	θ_{JA}	SOIC8	200	°C/W
		SOIC14 N	110	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply Voltage	V_B	$V_S + 10$	$V_S + 20$	V
High-Side Floating Supply Offset Voltage	V_S	$6 - V_{CC}$	600	V
High-Side (HO) Output Voltage	V_{HO}	V_S	V_B	V
Low-Side (LO) Output Voltage	V_{LO}	COM	V_{CC}	V
Logic Input Voltage (HIN, LIN)	V_{IN}	COM	V_{CC}	V
Low-Side Supply Voltage	V_{CC}	10	20	V
Ambient Temperature	T_A	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

FAN7382

ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC} , V_{BS}) = 15.0 V, T_A = 25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S and COM and are applicable to the respective outputs HO and LO.

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
V_{CC} and V_{BS} Supply Under-Voltage Positive Going Threshold		V_{CCUV+} V_{BSUV+}	8.2	9.2	10.0	V
V_{CC} and V_{BS} Supply Under-Voltage Negative Going Threshold		V_{CCUV-} V_{BSUV-}	7.6	8.7	9.6	V
V_{CC} Supply Under-Voltage Lockout Hysteresis		V_{CCUVH} V_{BSUVH}		0.6		V
Offset Supply Leakage Current	$V_B = V_S = 600$ V	I_{LK}			50	μ A
Quiescent V_{BS} Supply Current	$V_{IN} = 0$ V or 5 V	I_{QBS}		45	120	μ A
Quiescent V_{CC} Supply Current	$V_{IN} = 0$ V or 5 V	I_{QCC}		70	180	μ A
Operating V_{BS} Supply Current	$f_{IN} = 20$ kHz, rms value	I_{PBS}			600	μ A
Operating V_{CC} Supply Current	$f_{IN} = 20$ kHz, rms value	I_{PCC}			600	μ A
Logic "1" Input Voltage		V_{IH}	2.9			V
Logic "0" input voltage		V_{IL}			0.8	V
High-Level Output Voltage, $V_{BIAS} - V_O$	$I_O = 20$ mA	V_{OH}			1.0	V
Low-Level Output Voltage, V_O		V_{OL}			0.6	V
Logic "1" Input Bias Current	$V_{IN} = 5$ V	I_{IN+}		10	20	μ A
Logic "0" Input Bias Current	$V_{IN} = 0$ V	I_{IN-}		1.0	2.0	μ A
Output High Short-Circuit Pulsed Current	$V_O = 0$ V, $V_{IN} = 5$ V with $PW < 10$ μ s	I_{O+}	250	350		mA
Output Low Short-Circuit Pulsed Current	$V_O = 15$ V, $V_{IN} = 0$ V with $PW < 10$ μ s	I_{O-}	500	650		mA
Allowable Negative V_S Pin Voltage for HIN Signal Propagation to HO		V_S		-9.8	-7.0	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC} , V_{BS}) = 15.0 V, V_S = COM, C_L = 1000 pF and, T_A = 25°C, unless otherwise specified.

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Turn-On Propagation Delay	$V_S = 0$ V	t_{on}	100	170	300	ns
Turn-Off Propagation Delay	$V_S = 0$ V or 600 V (Note 4)	t_{off}	100	200	300	ns
Turn-On Rise Time		t_r	20	60	140	ns
Turn-Off Fall Time		t_f		30	80	ns
Delay Matching, HS & LS Turn-On/Off		MT			50	ns

4. This parameter guaranteed by design.

TYPICAL CHARACTERISTICS

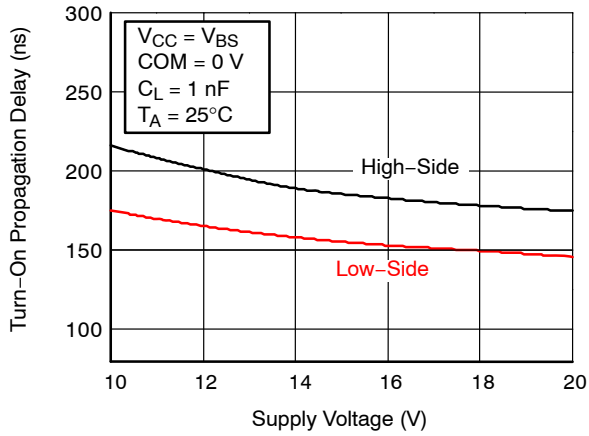


Figure 4. Turn-On Propagation Delay vs. Supply Voltage

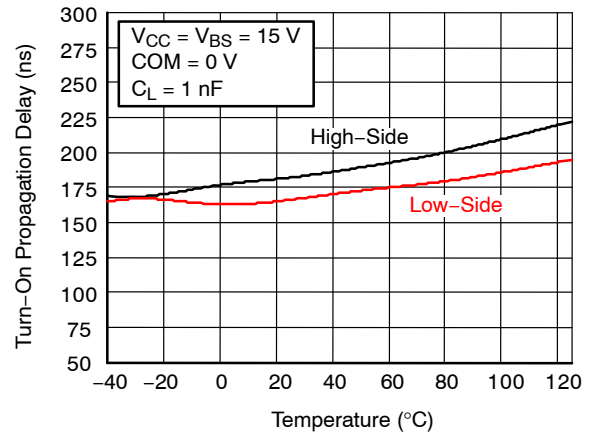


Figure 5. Turn-On Propagation Delay vs. Temperature

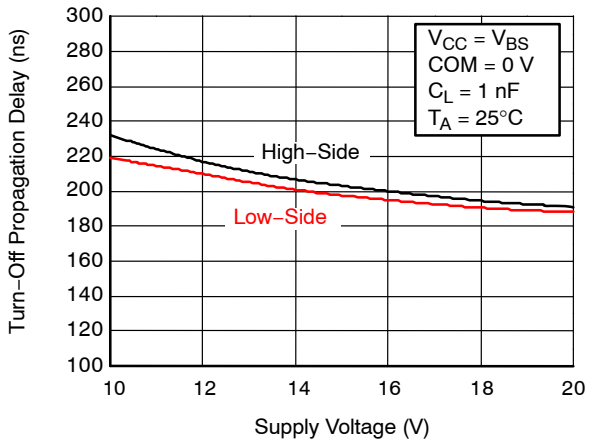


Figure 6. Turn-Off Propagation Delay vs. Supply Voltage

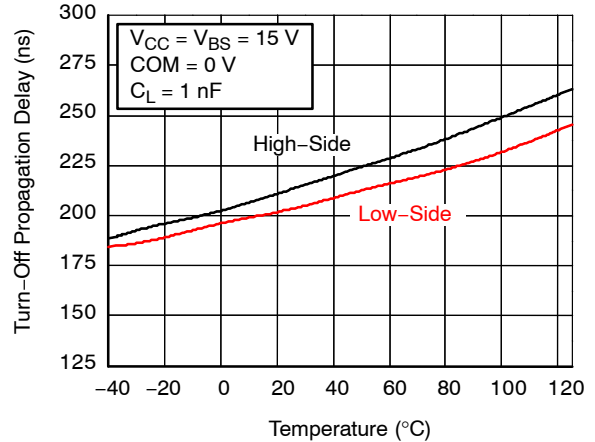


Figure 7. Turn-Off Propagation Delay vs. Temperature

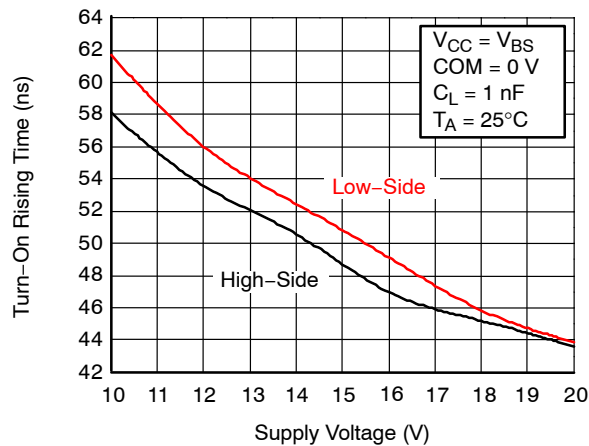


Figure 8. Turn-On Rising Time vs. Supply Voltage

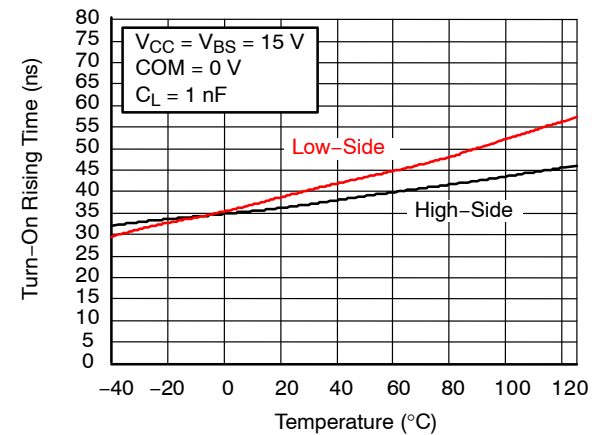


Figure 9. Turn-On Rising Time vs. Temperature

TYPICAL CHARACTERISTICS (continued)

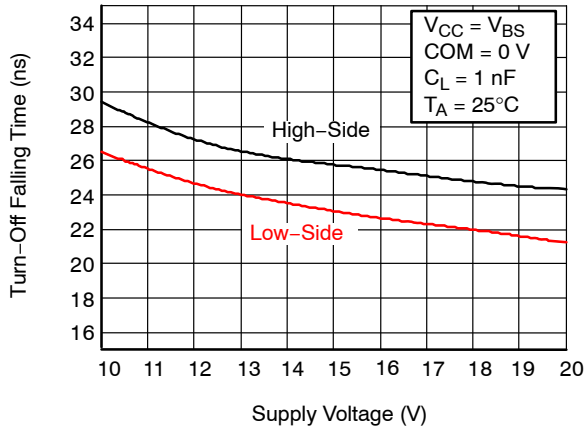


Figure 10. Turn-Off Falling Time vs. Supply Voltage

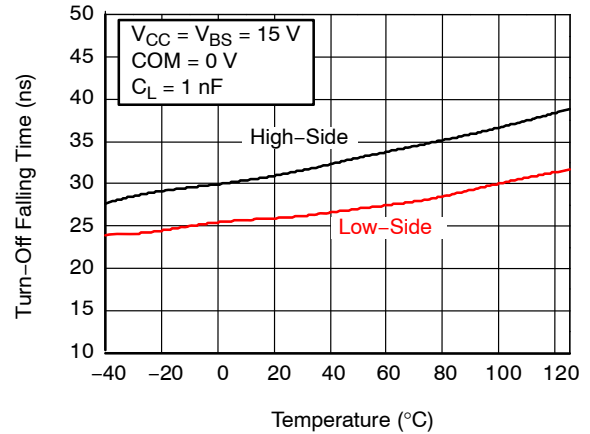


Figure 11. Turn-Off Falling Time vs. Temperature

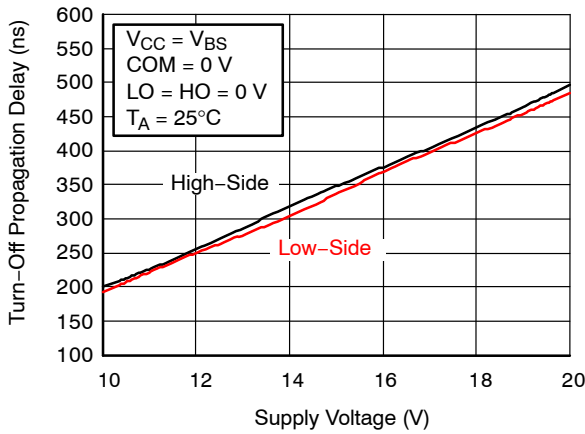


Figure 12. Output Sourcing Current vs. Supply Voltage

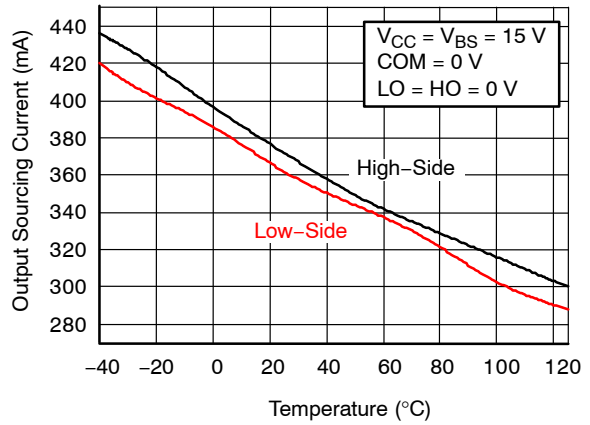


Figure 13. Output Sourcing Current vs. Temperature

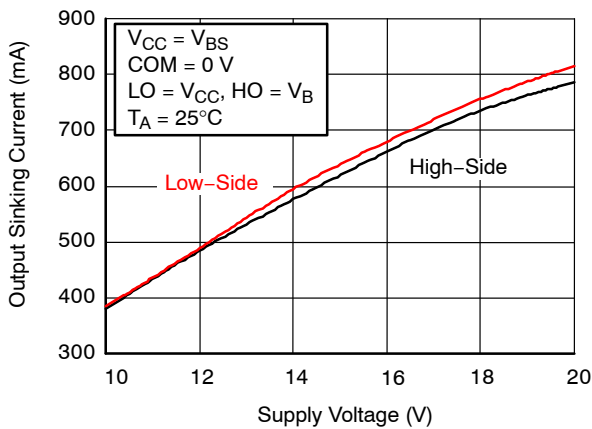


Figure 14. Output Sinking Current vs. Supply Voltage

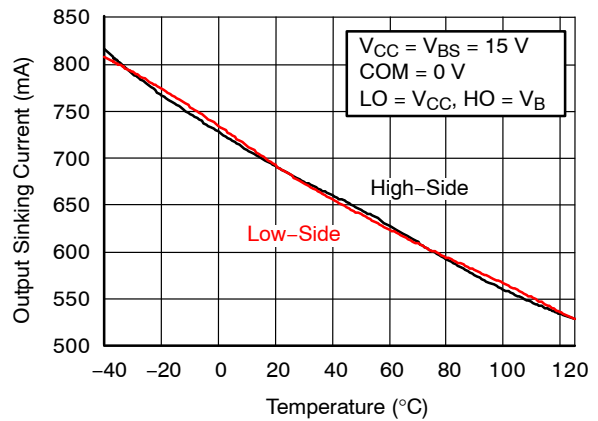


Figure 15. Output Sinking Current vs. Temperature

TYPICAL CHARACTERISTICS (continued)

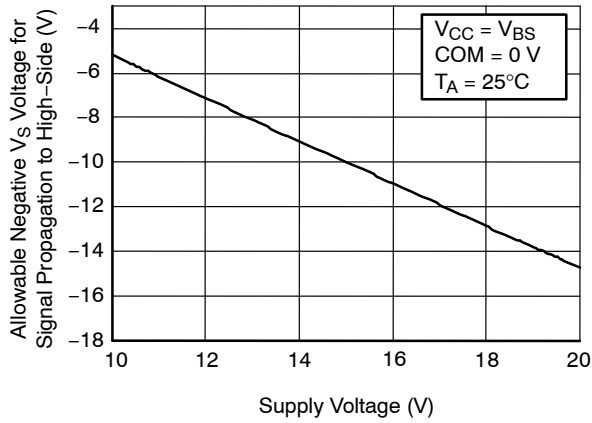


Figure 16. Allowable Negative V_S Voltage for Signal Propagation to High Side vs. Supply Voltage

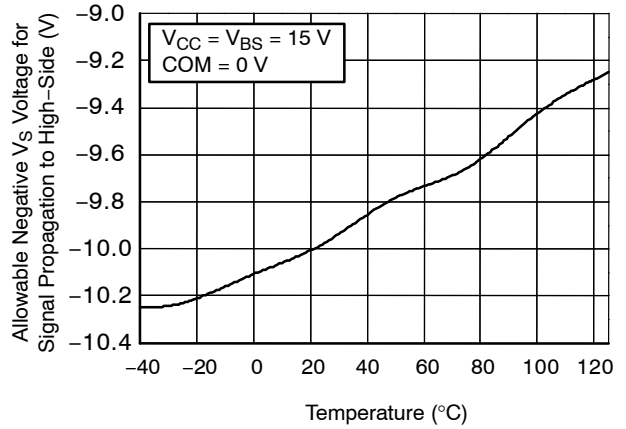


Figure 17. Allowable Negative V_S Voltage for Signal Propagation to High Side vs. Temperature

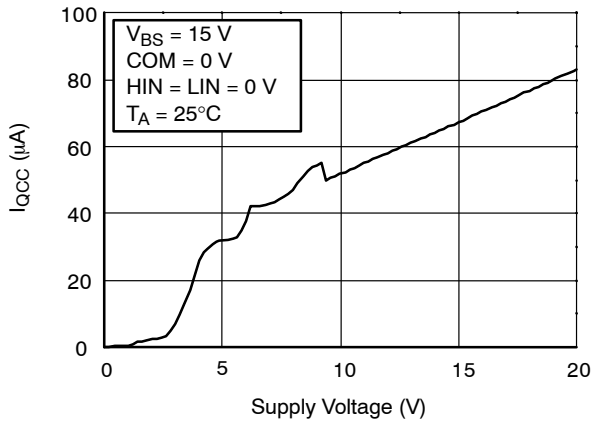


Figure 18. I_{QCC} vs. Supply Voltage

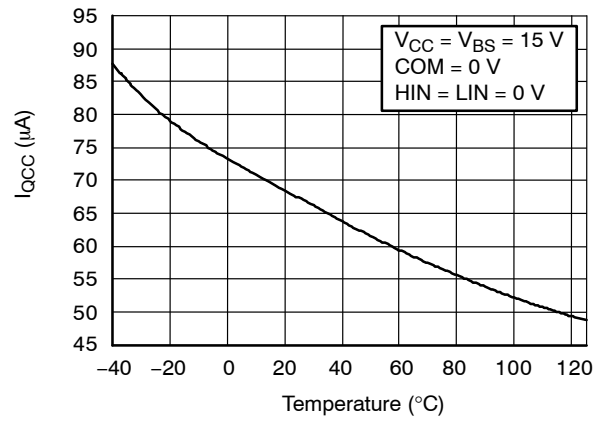


Figure 19. I_{QCC} vs. Temperature

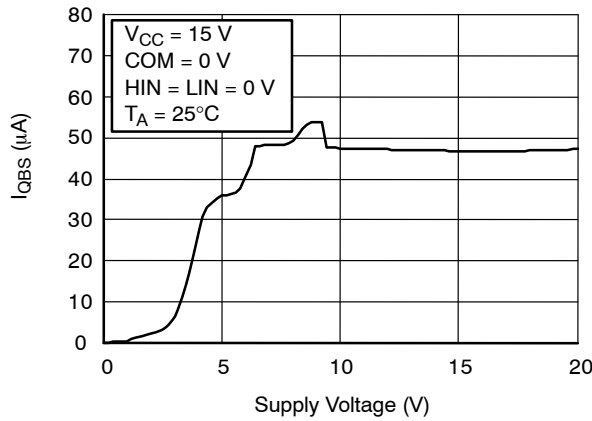


Figure 20. I_{QBS} vs. Supply Voltage

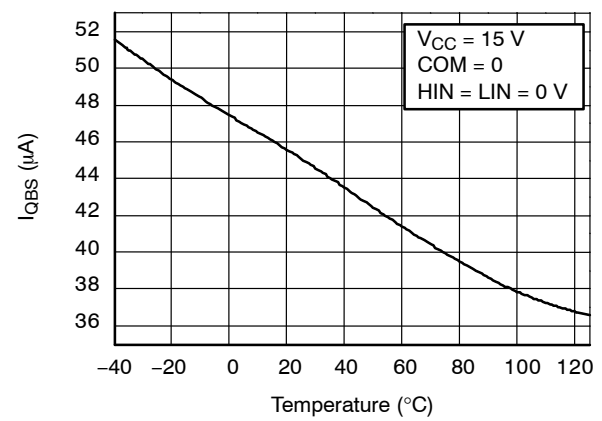


Figure 21. I_{QBS} vs. Temperature

TYPICAL CHARACTERISTICS (continued)

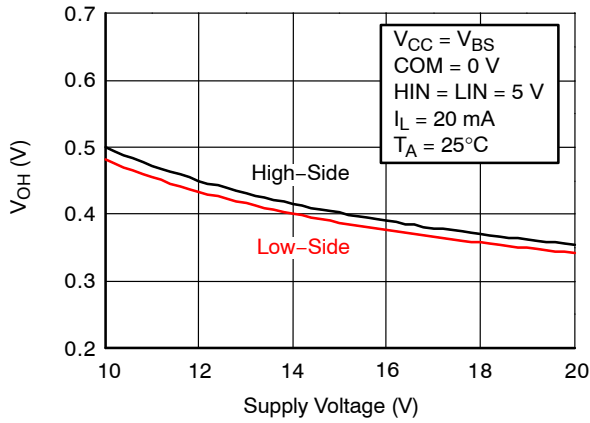


Figure 22. High-Level Output Voltage vs. Supply Voltage

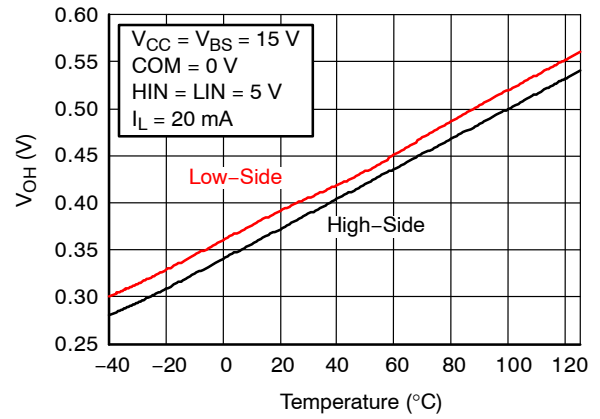


Figure 23. High-Level Output Voltage vs. Temperature

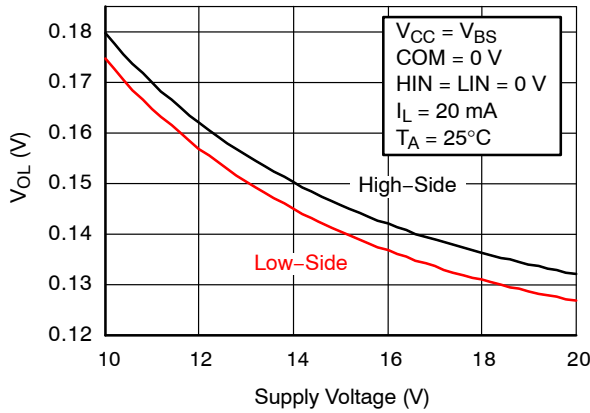


Figure 24. Low-Level Output Voltage vs. Supply Voltage

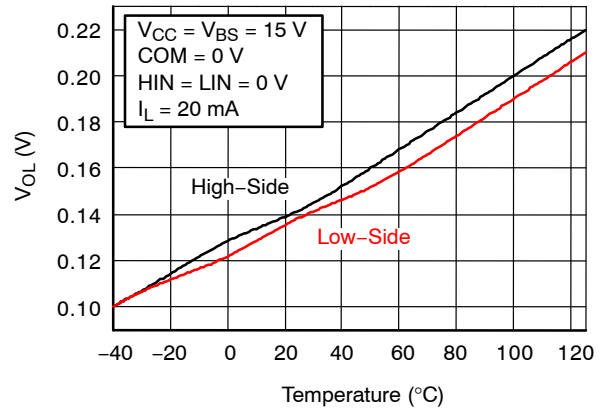


Figure 25. Low-Level Output Voltage vs. Temperature

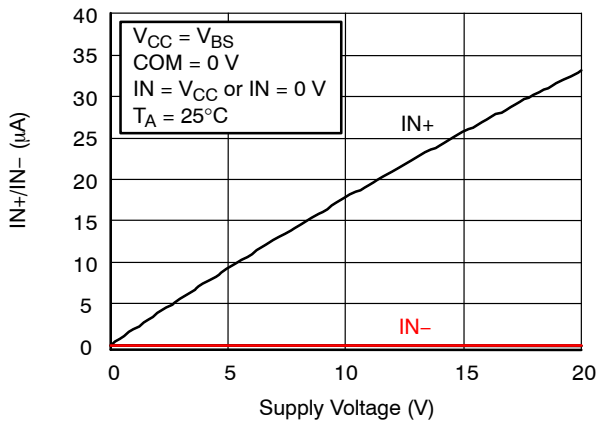


Figure 26. Input Bias Current vs. Supply Voltage

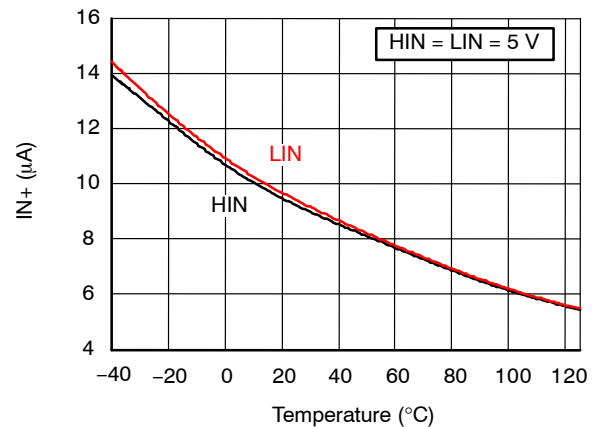


Figure 27. Input Bias Current vs. Temperature

TYPICAL CHARACTERISTICS (continued)

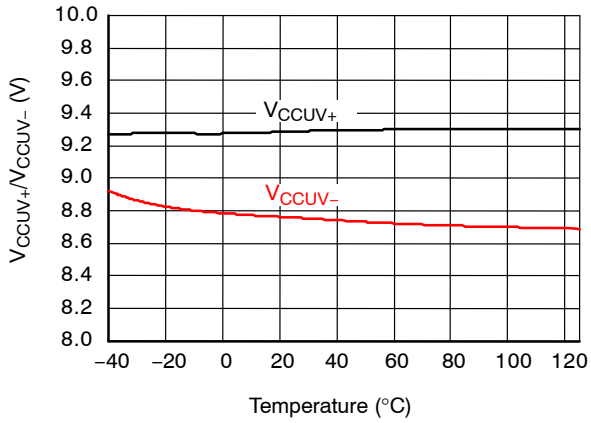


Figure 28. V_{CC} UVLO Threshold Voltage vs. Temperature

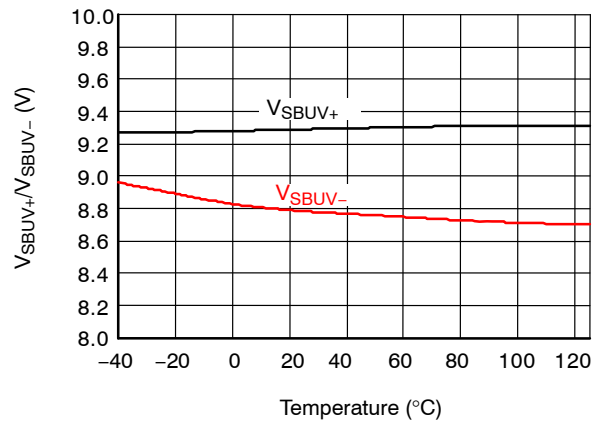


Figure 29. V_{BS} UVLO Threshold Voltage vs. Temperature

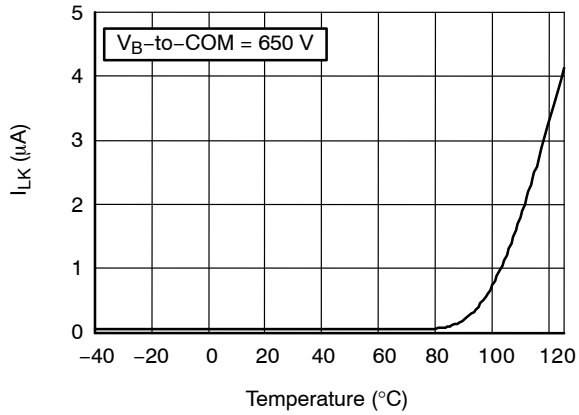


Figure 30. V_B to COM Leakage Current vs. Temperature

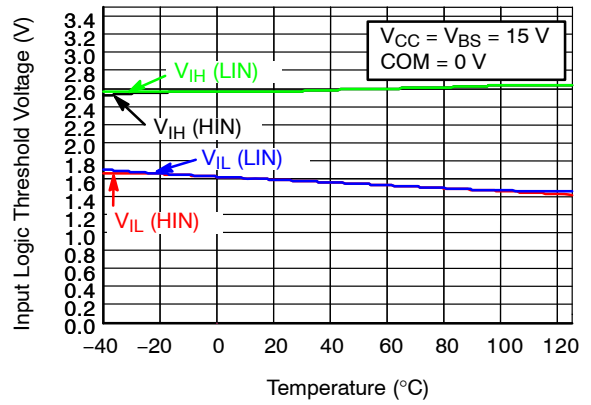


Figure 31. Input Logic Threshold Voltage vs. Temperature

TYPICAL CHARACTERISTICS (continued)

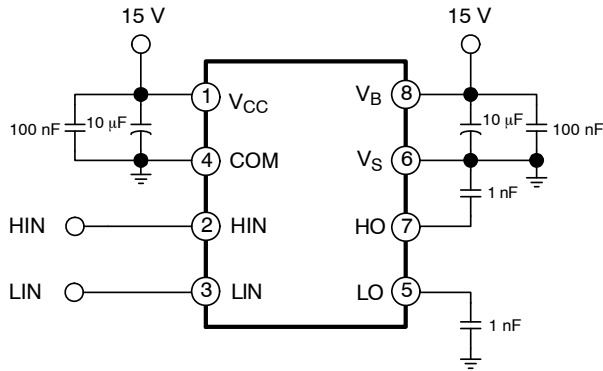


Figure 32. Switching Time Test Circuit

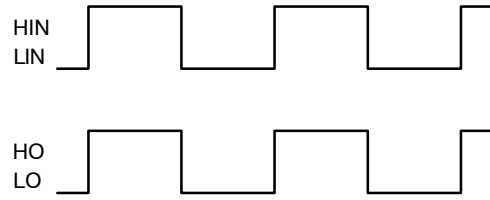


Figure 33. Input / Output Timing Diagram

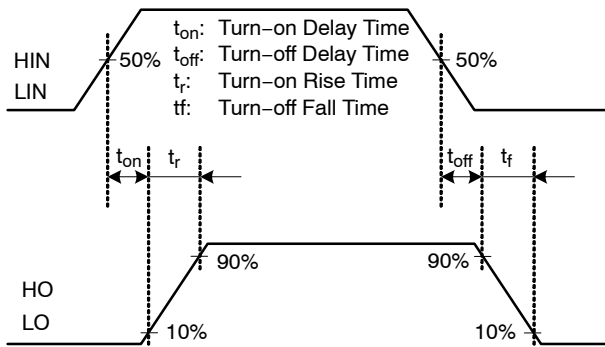


Figure 34. Switching Time Waveform Definition

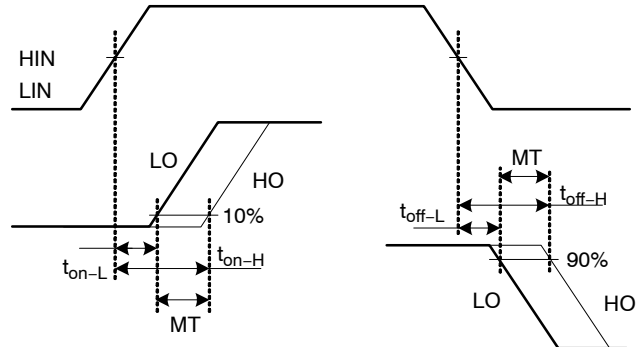


Figure 35. Delay Matching Waveform Definition

FAN7382

ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Shipping [†]
FAN7382MX (Note 5)	-40°C ~125°C	SOIC8 (Pb-Free)	3000 / Tape & Reel
FAN7382M1X (Note 5)		SOIC14 N (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

5. These devices passed wave soldering test by JESD22A-111.

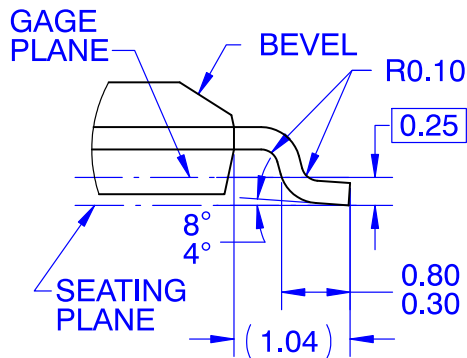
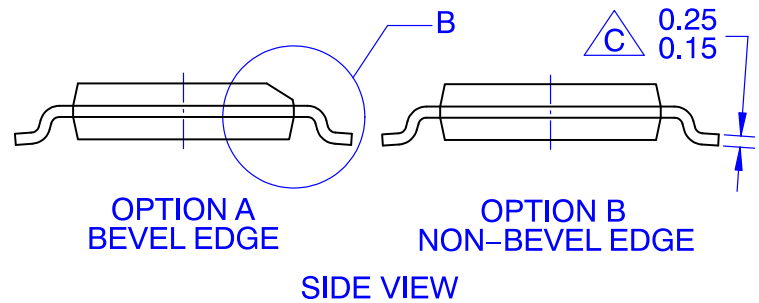
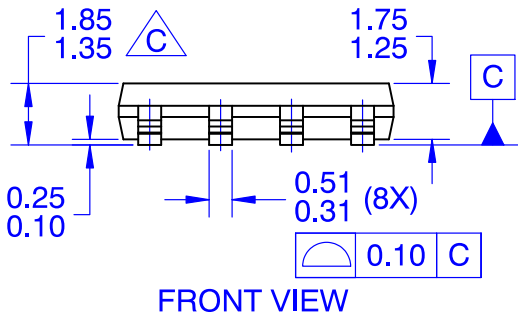
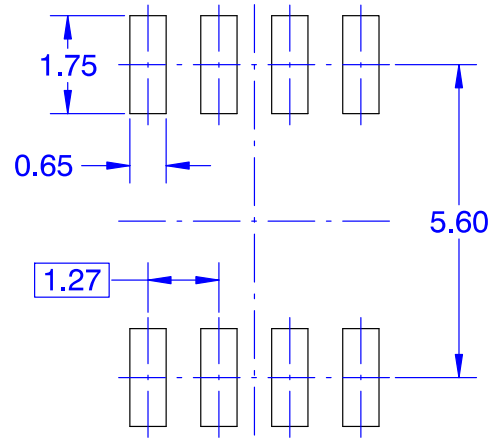
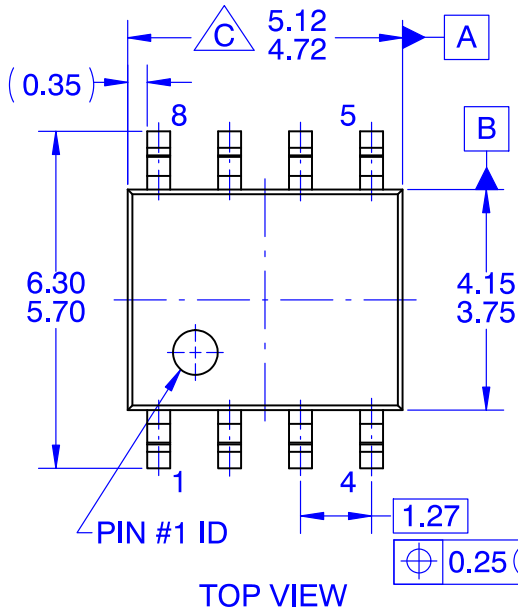
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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ISSUE O

DATE 30 SEP 2016



NOTES: UNLESS OTHERWISE SPECIFIED

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- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C** OUT OF JEDEC STANDARD VALUE
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- E. LAND PATTERN AS PER IPC SOIC127P600X175-8M

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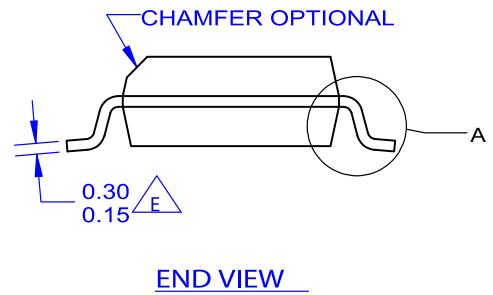
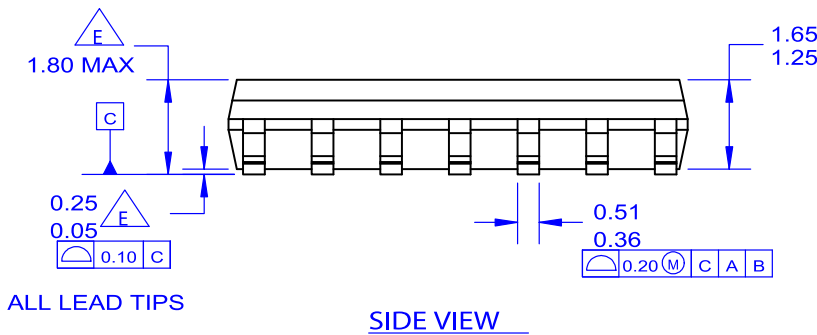
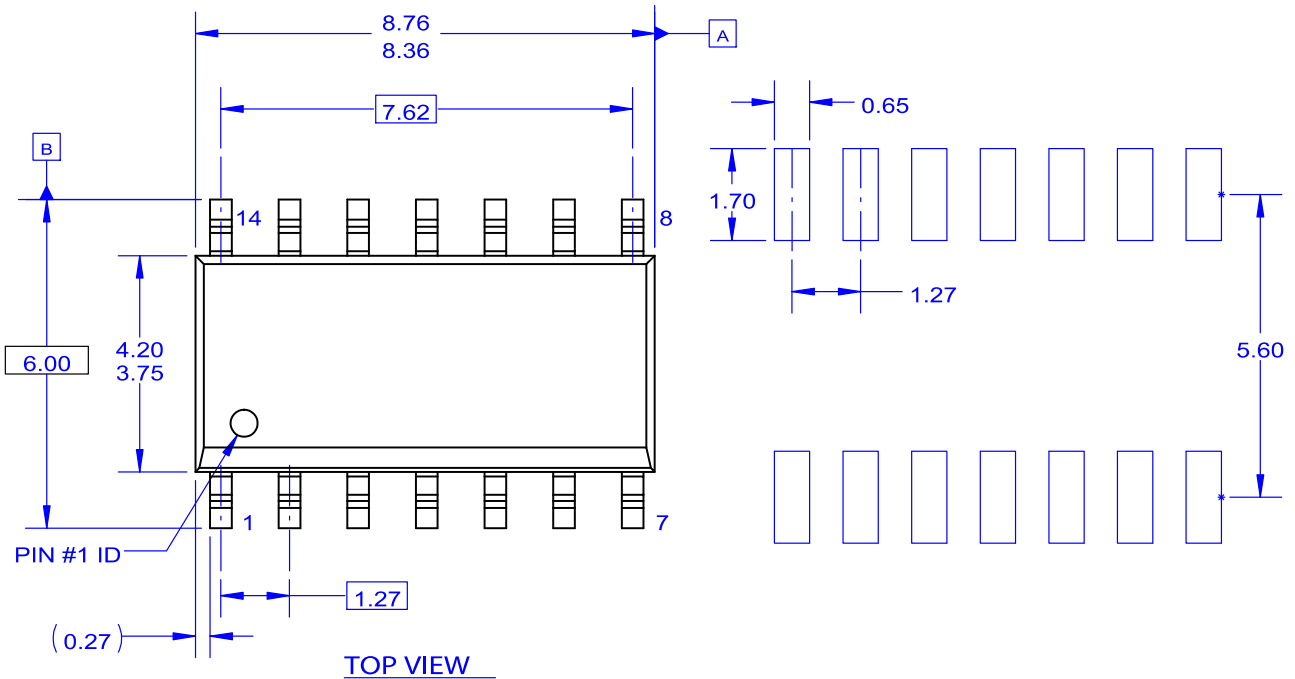
PACKAGE DIMENSIONS

ON Semiconductor®



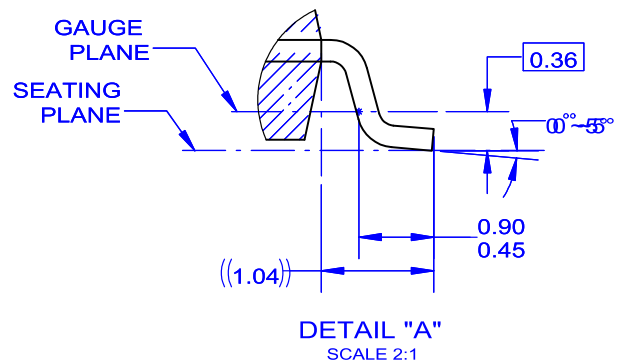
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DATE 31 DEC 2016



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