



**THE DATASHEET OF
MC100EL91DWR2**



MC100EL91

5 V Triple PECL Input to -5 V ECL Output Translator

Description

The MC100EL91 is a triple PECL input to ECL output translator. The device receives standard voltage differential PECL signals, determined by the V_{CC} supply level, and translates them to differential -5 V ECL output signals. (For translation of LVPECL to -3.3 V ECL output, see MC100LVEL91.)

To accomplish the level translation, the EL91 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via 0.01 μF capacitors.

Under open input conditions, the \bar{D} input will be biased at $V_{CC}/2$ and the D input will be pulled to GND. This condition will force the Q output to a low, ensuring stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

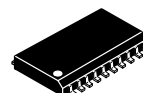
Features

- 670 ps Typical Propagation Delay
- ESD Protection: > 2 kV Human Body Model
- The 100 Series Contains Temperature Compensation
- Operating Range:
 - ◆ $V_{CC} = 4.75 \text{ V to } 5.5 \text{ V}$
 - ◆ $V_{EE} = -4.2 \text{ V to } -5.5 \text{ V}$; GND = 0 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at GND
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level: 3 (Pb-Free)
 - ◆ For Additional Information, see Application Note [AND8003/D](#)
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 282 devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



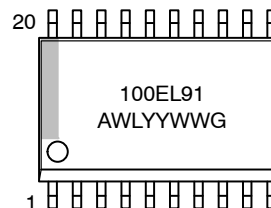
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SOIC-20 WB
DW SUFFIX
CASE 751D-05

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|-------------------------|------------------|
| MC100EL91DWG | SOIC-20 WB (Pb-Free) | 38 Units/Tube |
| MC100EL91DWR2G | SOIC-20 WB (Pb-Free) | 1000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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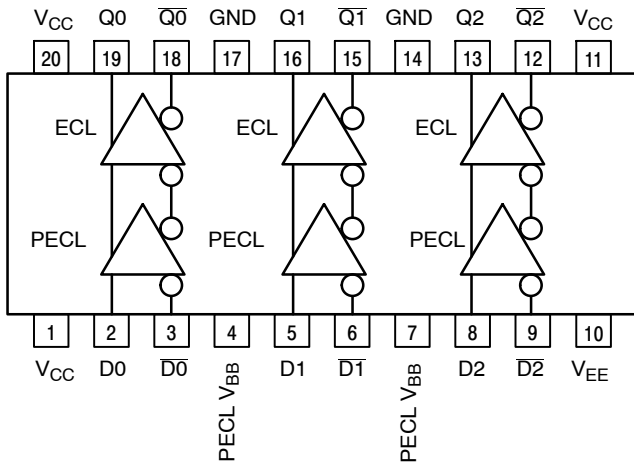


Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|---------------------|-------------------------------|
| Dn, \overline{Dn} | PECL Inputs |
| Qn, \overline{Qn} | ECL Outputs |
| PECL V_{BB} | PECL Reference Voltage Output |
| V_{CC} | Positive Supply |
| V_{EE} | Negative Supply |
| GND | Ground |

**All V_{CC} pins are tied together on the die.

Warning: All V_{CC} , V_{EE} , and GND pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View) and Logic Diagram

Table 2. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------|--|--------------------------------------|-------------------|-------------|-----------------------------|
| V_{CC} | PECL Power Supply | GND = 0 V | | 8 to 0 | V |
| V_{EE} | NECL Power Supply | GND = 0 V | | -8 to 0 | V |
| V_I | PECL Input Voltage | GND = 0 V | $V_I \leq V_{CC}$ | 6 to 0 | V |
| I_{out} | Output Current | Continuous Surge | | 50 100 | mA |
| I_{BB} | PECL V_{BB} Sink/Source | | | ± 0.5 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}\text{C}$ |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | SOIC-20 WB | 90 60 | $^{\circ}\text{C}/\text{W}$ |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC-20 WB | 30 to 35 | $^{\circ}\text{C}/\text{W}$ |
| T_{sol} | Wave Solder (Pb-Free) | <2 to 3 sec @ 248 $^{\circ}\text{C}$ | | 265 | $^{\circ}\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 3. PECL INPUT DC CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$; $V_{EE} = -5.0\text{ V}$; $GND = 0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|---------------|---|------------|-----|------------|------------|-----|------------|------------|-----|------------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{CC} | V_{CC} Power Supply Current | | | 11 | | 6 | 11 | | | 11 | mA |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3835 | | 4120 | 3835 | | 4120 | 3835 | | 4120 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3190 | | 3525 | 3190 | | 3525 | 3190 | | 3525 | mV |
| PECL V_{BB} | Output Voltage Reference | 3.62 | | 3.74 | 3.62 | | 3.74 | 3.62 | | 3.74 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 2) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$ | 1.3 1.5 | | 4.8 4.8 | 1.2 1.4 | | 4.8 4.8 | 1.2 1.4 | | 4.8 4.8 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input parameters vary 1:1 with V_{CC} . $V_{CC} = +4.75\text{ V}$ to $+5.2\text{ V}$, $V_{EE} = -4.20\text{ V}$ to -5.5 V .
2. V_{IHCMR} min varies 1:1 with GND . V_{IHCMR} max varies 1:1 with V_{CC} .

Table 4. NECL OUTPUT DC CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$ to 5.0 V ; $V_{EE} = -5.0\text{ V}$; $GND = 0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|----------|-------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | V_{EE} Power Supply Current | | | 28 | | 22 | 28 | | | 30 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | -1085 | -1005 | -880 | -1025 | -955 | -880 | -1025 | -955 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Output parameters vary 1:1 with GND . $V_{CC} = +4.75\text{ V}$ to $+5.2\text{ V}$, $V_{EE} = -4.20\text{ V}$ to -5.5 V .
2. Outputs are terminated through a $50\ \Omega$ resistor to $GND - 2.0\text{ V}$

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Table 5. AC CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$; $V_{EE} = -5.0\text{ V}$; $GND = 0\text{ V}$ (Note 4))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|------------------------|--|------------|------------|------------|------------|------------|------------|------------|------------|------------|---------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Toggle Frequency | | 700 | | | 700 | | | 700 | | MHz |
| t_{PLH} t_{PHL} | Propagation Delay D to Q Differential Single-Ended. | 540 490 | 640 640 | 740 790 | 570 520 | 670 670 | 770 820 | 610 560 | 710 710 | 810 860 | ps |
| t_{SKEW} | Skew Output-to-Output (Note 1) Part-to-Part (Differential) (Note 1) Cycle (Differential) (Note 2) | | 40 25 | 100 200 | | 40 25 | 100 200 | | 40 25 | 100 200 | ps |
| t_{JITTER} | Random Clock Jitter @ 700 MHz | | 1.2 | | | 1.2 | | | 1.2 | | pS(RMS) |
| V_{PP} | Input Swing (Note 3) | 200 | | 1000 | 200 | | 1000 | 200 | | 1000 | mV |
| t_r t_f | Output Rise/Fall Times Q (20% - 80%) | 270 | 400 | 530 | 270 | 400 | 530 | 270 | 400 | 530 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
2. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
3. $V_{PP}(\text{min})$ is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 .
4. $V_{CC} = +4.75\text{ V}$ to $+5.2\text{ V}$, $V_{EE} = -4.20\text{ V}$ to -5.5 V . Outputs are terminated through a $50\ \Omega$ resistor to $GND - 2.0\text{ V}$.

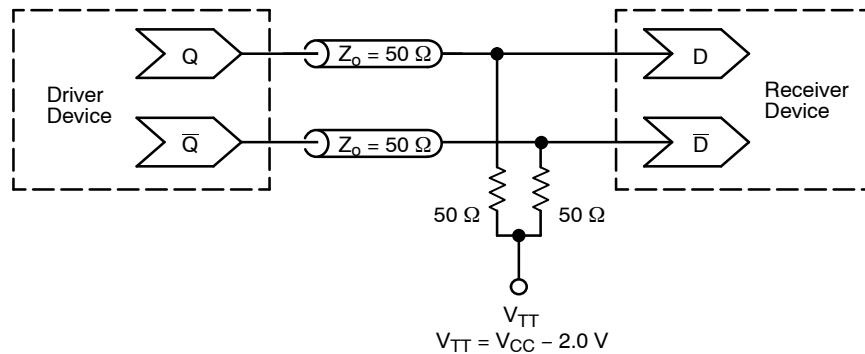
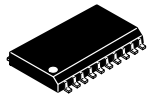


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

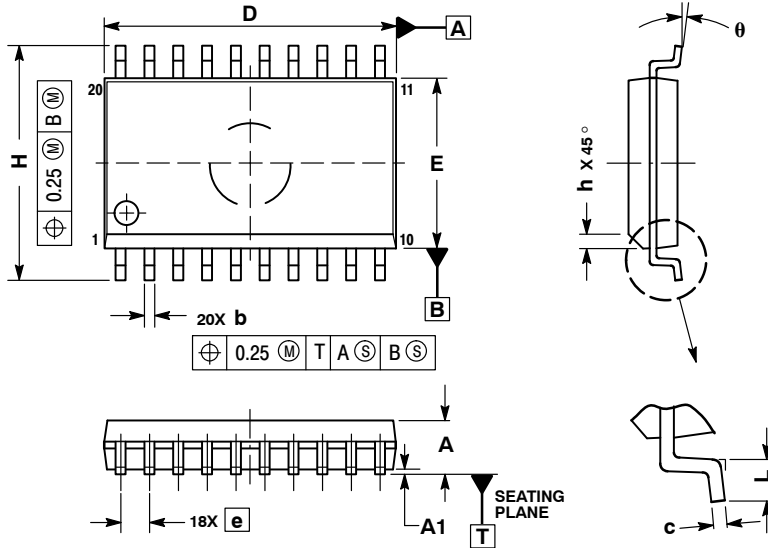
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

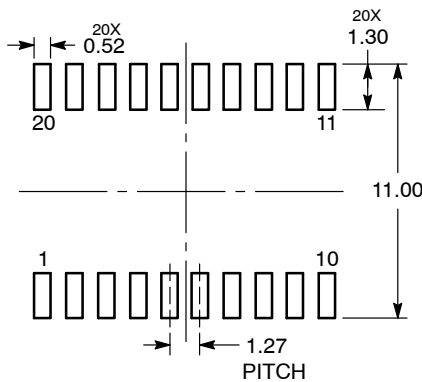


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

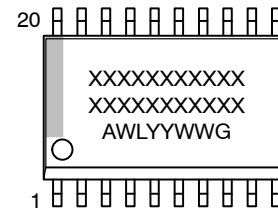
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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|------------------|-------------|--|
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