# THE DATASHEET OF

# MC14021BDR2

# MC14014B, MC14021B

# 8-Bit Static Shift Register

The MC14014B and MC14021B 8−bit static shift registers are constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel−to−serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

### Features

- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation
- “Q” Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- MC14014B Pin−for−Pin Replacement for CD4014B
- MC14021B Pin−for−Pin Replacement for CD4021B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

**MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage Range | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage Range (DC or Transient) | −0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient) per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package (Note 1) | 500 | mW |
| $T_A$ | Ambient Temperature Range | −55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8−Second Soldering) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Package: –7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

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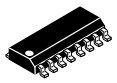
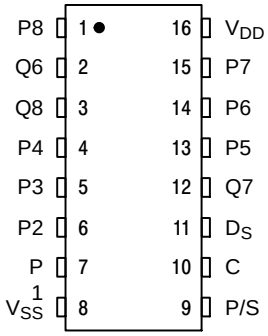
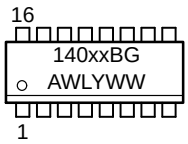


**SOIC−16**
**D SUFFIX**
**CASE 751B**

### PIN ASSIGNMENT




### MARKING DIAGRAM




xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Indicator

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

## TRUTH TABLE

**SERIAL OPERATION:**

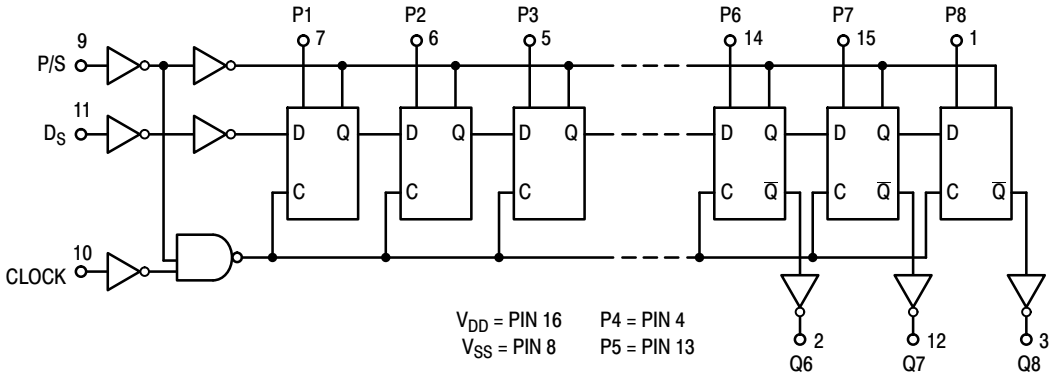
| t | Clock | $D_S$ | P/S | Q6 t=n+6 | Q7 t=n+7 | Q8 t=n+8 |
|---|---|---|---|---|---|---|
| n | ↗ | 0 | 0 | 0 | ? | ? |
| n+1 | ↗ | 1 | 0 | 1 | 0 | ? |
| n+2 | ↗ | 0 | 0 | 0 | 1 | 0 |
| n+3 | ↗ | 1 | 0 | 1 | 0 | 1 |
| | ↘ | X | 0 | Q6 | Q7 | Q8 |

**PARALLEL OPERATION:**

| Clock | | $D_S$ | P/S | $P_n$ | $*Q_n$ |
|---|---|---|---|---|---|
| MC14014B | MC14021B | | | | |
| ↗ | X | X | 1 | 0 | 0 |
| ↗ | X | X | 1 | 1 | 1 |

*Q6, Q7, & Q8 are available externally
X = Don't Care

## LOGIC DIAGRAM



**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | −55°C Min | −55°C Max | 25°C Min | 25°C Typ (Note 2) | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage “0” Level | $V_{OL}$ | 5.0 | − | 0.05 | − | 0 | 0.05 | − | 0.05 | Vdc |
| $V_{in}$ = $V_{DD}$ or 0 | | 10 | − | 0.05 | − | 0 | 0.05 | − | 0.05 | |
| | | 15 | − | 0.05 | − | 0 | 0.05 | − | 0.05 | |
| $V_{in}$ = 0 or $V_{DD}$ “1” Level | $V_{OH}$ | 5.0 | 4.95 | − | 4.95 | 5.0 | − | 4.95 | − | Vdc |
| | | 10 | 9.95 | − | 9.95 | 10 | − | 9.95 | − | |
| | | 15 | 14.95 | − | 14.95 | 15 | − | 14.95 | − | |
| Input Voltage “0” Level | $V_{IL}$ | | | | | | | | | Vdc |
| ($V_O$ = 4.5 or 0.5 Vdc) | | 5.0 | − | 1.5 | − | 2.25 | 1.5 | − | 1.5 | |
| ($V_O$ = 9.0 or 1.0 Vdc) | | 10 | − | 3.0 | − | 4.50 | 3.0 | − | 3.0 | |
| ($V_O$ = 13.5 or 1.5 Vdc) | | 15 | − | 4.0 | − | 6.75 | 4.0 | − | 4.0 | |
| ($V_O$ = 0.5 or 4.5 Vdc) “1” Level | $V_{IH}$ | 5.0 | 3.5 | − | 3.5 | 2.75 | − | 3.5 | − | Vdc |
| ($V_O$ = 1.0 or 9.0 Vdc) | | 10 | 7.0 | − | 7.0 | 5.50 | − | 7.0 | − | |
| ($V_O$ = 1.5 or 13.5 Vdc) | | 15 | 11 | − | 11 | 8.25 | − | 11 | − | |
| Output Drive Current | $I_{OH}$ | | | | | | | | | mAdc |
| ($V_{OH}$ = 2.5 Vdc) Source | | 5.0 | –3.0 | − | –2.4 | –4.2 | − | –1.7 | − | |
| ($V_{OH}$ = 4.6 Vdc) | | 5.0 | –0.64 | − | –0.51 | –0.88 | − | −0.36 | − | |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | –1.6 | − | −1.3 | –2.25 | − | –0.9 | − | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | –4.2 | − | −3.4 | −8.8 | − | −2.4 | − | |
| ($V_{OL}$ = 0.4 Vdc) Sink | $I_{OL}$ | 5.0 | 0.64 | − | 0.51 | 0.88 | − | 0.36 | − | mAdc |
| ($V_{OL}$ = 0.5 Vdc) | | 10 | 1.6 | − | 1.3 | 2.25 | − | 0.9 | − | |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 4.2 | − | 3.4 | 8.8 | − | 2.4 | − | |
| Input Current | $I_{in}$ | 15 | − | ±0.1 | − | ±0.00001 | ±0.1 | − | ±1.0 | μAdc |
| Input Capacitance ($V_{in}$ = 0) | $C_{in}$ | − | − | − | − | 5.0 | 7.5 | − | − | pF |
| Quiescent Current (Per Package) | $I_{DD}$ | 5.0 | − | 5.0 | − | 0.005 | 5.0 | − | 150 | μAdc |
| | | 10 | − | 10 | − | 0.010 | 10 | − | 300 | |
| | | 15 | − | 15 | − | 0.015 | 15 | − | 600 | |
| Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) ($C_L$ = 50 pF on all outputs, all buffers switching) | $I_T$ | 5.0 | $I_T$ = (0.75 μA/kHz) f + $I_{DD}$ | | | | | | | μAdc |
| | | 10 | $I_T$ = (1.50 μA/kHz) f + $I_{DD}$ | | | | | | | |
| | | 15 | $I_T$ = (2.25 μA/kHz) f + $I_{DD}$ | | | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

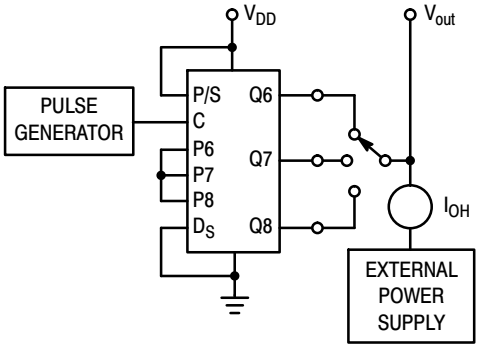
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: $I_T$ is in μA (per package), $C_L$ in pF, V = ($V_{DD}$ − $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.0015.

**SWITCHING CHARACTERISTICS** (Note 5) ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ Vdc | Min | Typ (Note 6) | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time | $t_{TLH}$, | | | | | ns |
| $t_{TLH}$, $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns | $t_{THL}$ | 5.0 | – | 100 | 200 | |
| $t_{TLH}$, $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns | | 10 | – | 50 | 100 | |
| $t_{TLH}$, $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns | | 15 | – | 40 | 80 | |
| Propagation Delay Time (Clock to Q, P/S to Q) | $t_{PLH}$, | | | | | ns |
| $t_{PHL}$, $t_{PLH}$ = (1.7 ns/pF) $C_L$ + 315 ns | $t_{PHL}$ | 5.0 | – | 400 | 800 | |
| $t_{PHL}$, $t_{PLH}$ = (0.66 ns/pF) $C_L$ + 137 ns | | 10 | – | 170 | 340 | |
| $t_{PHL}$, $t_{PLH}$ = (0.5 ns/pF) $C_L$ + 90 ns | | 15 | – | 115 | 230 | |
| Clock Pulse Width | $t_{WH}$ | 5.0 | 400 | 150 | – | ns |
| | | 10 | 175 | 75 | – | |
| | | 15 | 135 | 40 | – | |
| Clock Frequency | $f_{cl}$ | 5.0 | – | 3.0 | 1.5 | MHz |
| | | 10 | – | 6.0 | 3.0 | |
| | | 15 | – | 8.0 | 4.0 | |
| Parallel/Serial Control Pulse Width | $t_{WH}$ | 5.0 | 400 | 150 | – | ns |
| | | 10 | 175 | 75 | – | |
| | | 15 | 135 | 40 | – | |
| Setup Time | $t_{su}$ | 5.0 | 200 | 100 | – | ns |
| P/S to Clock | | 10 | 100 | 50 | – | |
| | | 15 | 80 | 40 | – | |
| Hold Time | $t_h$ | 5.0 | 20 | – 2.5 | – | ns |
| Clock to P/S | | 10 | 20 | – 10 | – | |
| | | 15 | 25 | 0 | – | |
| Setup Time | $t_{su}$ | 5.0 | 350 | 150 | – | ns |
| Data (Parallel or Serial) to | | 10 | 80 | 50 | – | |
| Clock or P/S | | 15 | 60 | 30 | – | |
| Hold Time | $t_h$ | 5.0 | 45 | 0 | – | ns |
| Clock to $D_S$ | | 10 | 35 | 0 | – | |
| | | 15 | 35 | 5 | – | |
| Hold Time | $t_h$ | 5.0 | 50 | 25 | – | ns |
| Clock to $P_n$ | | 10 | 45 | 20 | – | |
| | | 15 | 45 | 20 | – | |
| Input Clock Rise Time | $t_{r(cl)}$ | 5.0 | – | – | 15 | μs |
| | | 10 | – | – | 5 | |
| | | 15 | – | – | 4 | |

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.




Preset output under test to a logic “1” level.

**Figure 1. Output Source Current Test Circuit**

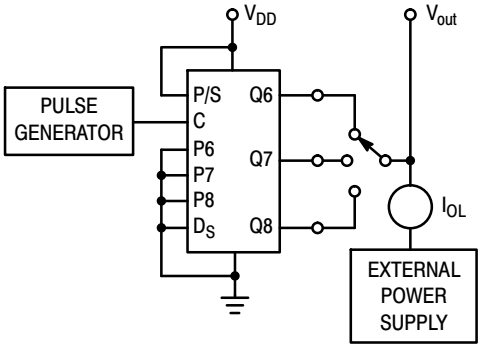



**Figure 2. Output Sink Current Test Circuit**

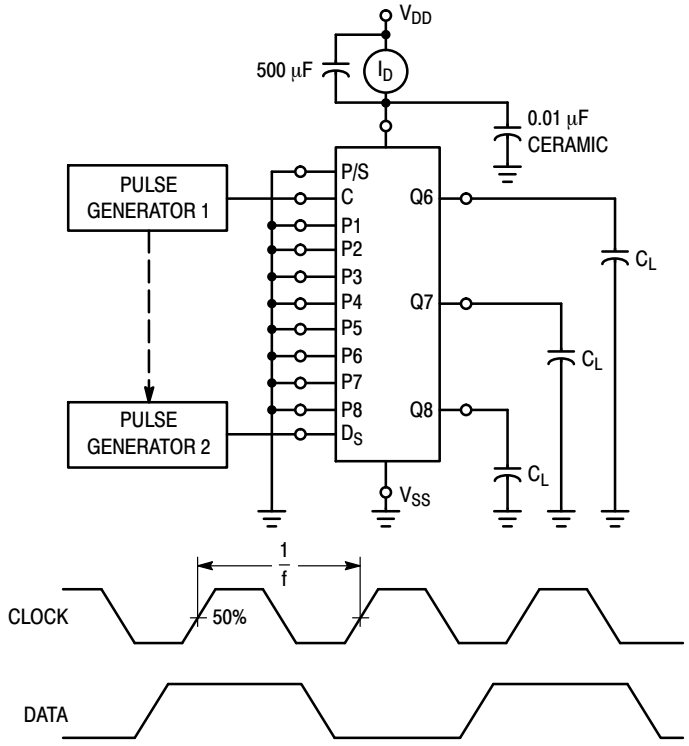



**Figure 3. Power Dissipation Test Circuit and Waveform**

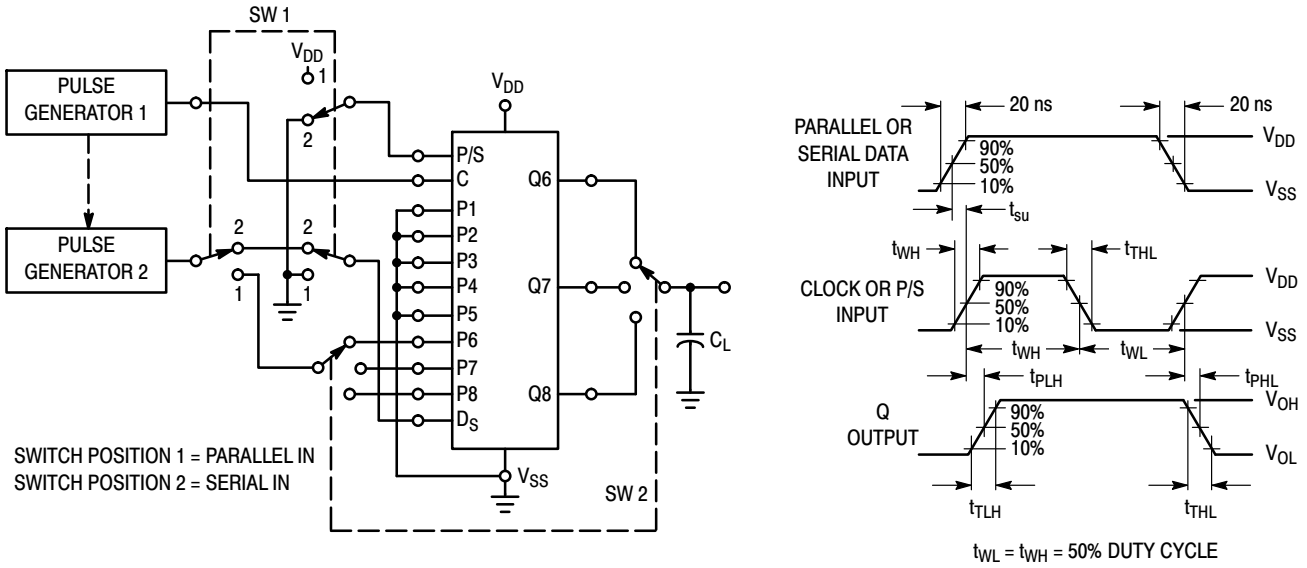



**Figure 4. Switching Time Test Circuit and Waveforms**

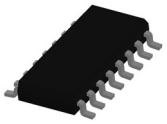
**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC14014BDG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC14014BDR2G | SOIC−16 (Pb−Free) | 2500 Units / Tape & Reel |
| NLV14014BDR2G* | SOIC−16 (Pb−Free) | 2500 Units / Tape & Reel |
| MC14021BDG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC14021BDR2G | SOIC−16 (Pb−Free) | 2500 Units / Tape & Reel |
| NLV14021BDR2G* | SOIC−16 (Pb−Free) | 2500 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

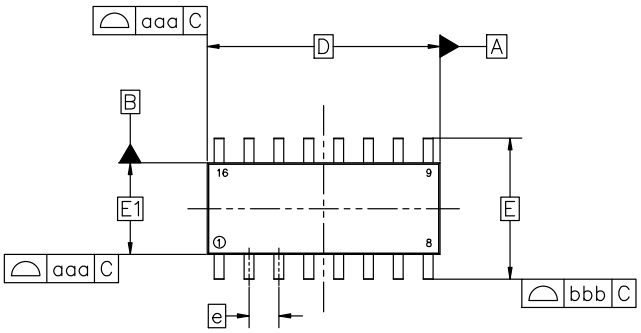
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



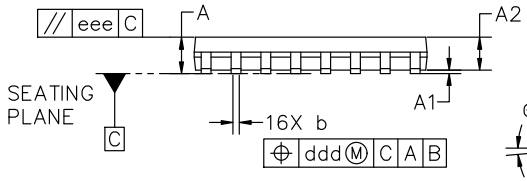
**SOIC−16 9.90x3.90x1.50 1.27P**
CASE 751B
ISSUE L

DATE 29 MAY 2024

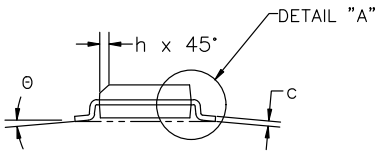
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.




TOP VIEW

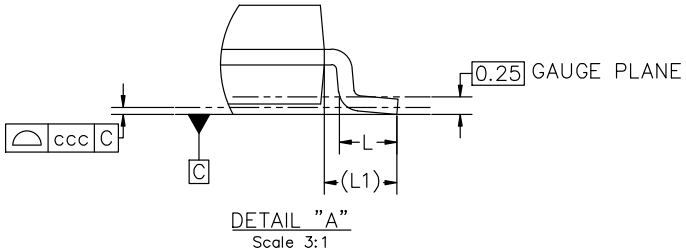



SIDE VIEW

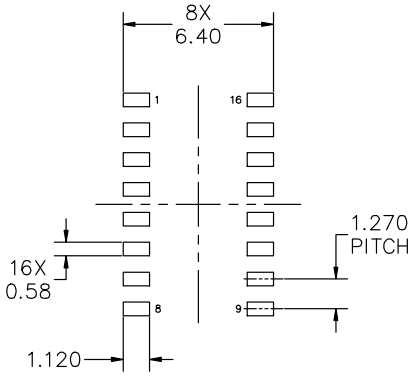



END VIEW

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 1.35 | 1.55 | 1.75 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 1.35 | 1.50 | 1.65 |
| b | 0.35 | 0.42 | 0.49 |
| c | 0.19 | 0.22 | 0.25 |
| D | 9.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |
| h | 0.25 | −−− | 0.50 |
| L | 0.40 | 0.83 | 1.25 |
| L1 | 1.05 REF | | |
| θ | 0° | −−− | 7° |
| TOLERANCE OF FORM AND POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.25 | | |
| eee | 0.10 | | |




DETAIL "A"
Scale 3:1




RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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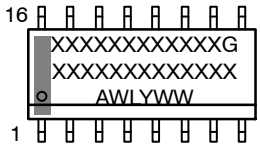
|---|---|---|
| DESCRIPTION: | SOIC−16 9.90X3.90X1.50 1.27P | PAGE 1 OF 2 |

**SOIC−16 9.90x3.90x1.50 1.27P**
CASE 751B
ISSUE L

DATE 29 MAY 2024

**GENERIC**
**MARKING DIAGRAM***




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| STYLE 1: | | STYLE 2: | | STYLE 3: | | STYLE 4: | |
|---|---|---|---|---|---|---|---|
| PIN 1. | COLLECTOR | PIN 1. | CATHODE | PIN 1. | COLLECTOR, DYE #1 | PIN 1. | COLLECTOR, DYE #1 |
| 2. | BASE | 2. | ANODE | 2. | BASE, #1 | 2. | COLLECTOR, #1 |
| 3. | EMITTER | 3. | NO CONNECTION | 3. | EMITTER, #1 | 3. | COLLECTOR, #2 |
| 4. | NO CONNECTION | 4. | CATHODE | 4. | COLLECTOR, #1 | 4. | COLLECTOR, #2 |
| 5. | EMITTER | 5. | CATHODE | 5. | COLLECTOR, #2 | 5. | COLLECTOR, #3 |
| 6. | BASE | 6. | NO CONNECTION | 6. | BASE, #2 | 6. | COLLECTOR, #3 |
| 7. | COLLECTOR | 7. | ANODE | 7. | EMITTER, #2 | 7. | COLLECTOR, #4 |
| 8. | COLLECTOR | 8. | CATHODE | 8. | COLLECTOR, #2 | 8. | COLLECTOR, #4 |
| 9. | BASE | 9. | CATHODE | 9. | COLLECTOR, #3 | 9. | BASE, #4 |
| 10. | EMITTER | 10. | ANODE | 10. | BASE, #3 | 10. | EMITTER, #4 |
| 11. | NO CONNECTION | 11. | NO CONNECTION | 11. | EMITTER, #3 | 11. | BASE, #3 |
| 12. | EMITTER | 12. | CATHODE | 12. | COLLECTOR, #3 | 12. | EMITTER, #3 |
| 13. | BASE | 13. | CATHODE | 13. | COLLECTOR, #4 | 13. | BASE, #2 |
| 14. | COLLECTOR | 14. | NO CONNECTION | 14. | BASE, #4 | 14. | EMITTER, #2 |
| 15. | EMITTER | 15. | ANODE | 15. | EMITTER, #4 | 15. | BASE, #1 |
| 16. | COLLECTOR | 16. | CATHODE | 16. | COLLECTOR, #4 | 16. | EMITTER, #1 |

| STYLE 5: | | STYLE 6: | | STYLE 7: | |
|---|---|---|---|---|---|
| PIN 1. | DRAIN, DYE #1 | PIN 1. | CATHODE | PIN 1. | SOURCE N-CH |
| 2. | DRAIN, #1 | 2. | CATHODE | 2. | COMMON DRAIN (OUTPUT) |
| 3. | DRAIN, #2 | 3. | CATHODE | 3. | COMMON DRAIN (OUTPUT) |
| 4. | DRAIN, #2 | 4. | CATHODE | 4. | GATE P-CH |
| 5. | DRAIN, #3 | 5. | CATHODE | 5. | COMMON DRAIN (OUTPUT) |
| 6. | DRAIN, #3 | 6. | CATHODE | 6. | COMMON DRAIN (OUTPUT) |
| 7. | DRAIN, #4 | 7. | CATHODE | 7. | COMMON DRAIN (OUTPUT) |
| 8. | DRAIN, #4 | 8. | CATHODE | 8. | SOURCE P-CH |
| 9. | GATE, #4 | 9. | ANODE | 9. | SOURCE P-CH |
| 10. | SOURCE, #4 | 10. | ANODE | 10. | COMMON DRAIN (OUTPUT) |
| 11. | GATE, #3 | 11. | ANODE | 11. | COMMON DRAIN (OUTPUT) |
| 12. | SOURCE, #3 | 12. | ANODE | 12. | COMMON DRAIN (OUTPUT) |
| 13. | GATE, #2 | 13. | ANODE | 13. | GATE N-CH |
| 14. | SOURCE, #2 | 14. | ANODE | 14. | COMMON DRAIN (OUTPUT) |
| 15. | GATE, #1 | 15. | ANODE | 15. | COMMON DRAIN (OUTPUT) |
| 16. | SOURCE, #1 | 16. | ANODE | 16. | SOURCE N-CH |

## ADDITIONAL INFORMATION

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**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales

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## Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management