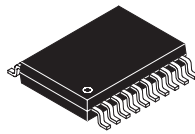




**THE DATASHEET OF  
TLV320AIC1106PW**





## PCM CODEC

### FEATURES

- Designed for Analog and Digital Wireless Handsets, Voice-Enabled Terminals, and Telecommunications Applications
- 2.7-V to 3.3-V Operation
- Selectable 13-Bit Linear or 8-Bit  $\mu$ -Law Companded Conversion
- Differential Microphone Input With External Gain Setting
- Differential Earphone Output Capable of Driving a 32- $\Omega$  to 8- $\Omega$  Load
- Programmable Volume Control in Linear Mode
- Microphone (MIC) and Earphone (EAR) Mute Functions
- Typical Power Dissipation of 0.03 mW in Power-Down Mode
- 2.048-MHz Master Clock Rate
- 300-Hz to 3.4-kHz Passband
- Low Profile 20-Terminal TSSOP Packaging

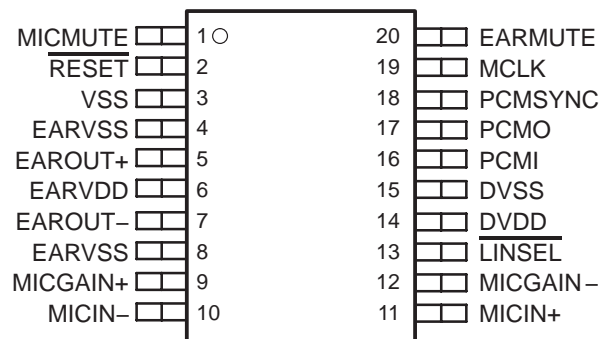
### APPLICATIONS

- Digital Handset
- Digital Headset
- Cordless Phones
- Digital PABX
- Digital Voice Recording

### DESCRIPTION

The TLV320AIC1106 PCM codec is designed to perform transmit encoding analog-to-digital (A/D) conversion, receive decoding digital-to-analog (D/A) conversion, and transmit and receive filtering for voice-band communications systems. The TLV320AIC1106 device operates in either the 13-bit linear or 8-bit companded ( $\mu$ -law) mode. The PCM codec generates its own internal clocks from a 2.048-MHz master clock input.

**PW PACKAGE  
(TOP VIEW)**

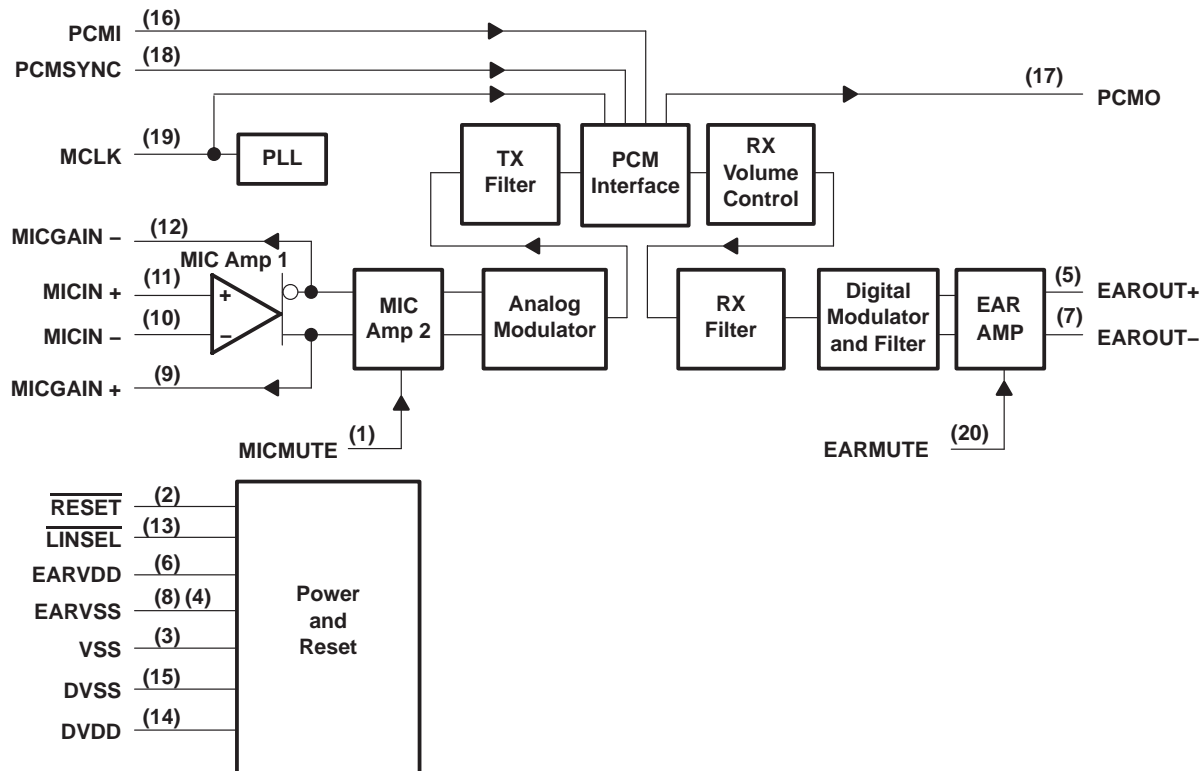


This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either  $V_{CC}$  or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



RX = Receive  
TX = Transmit

## detailed description

### power up/reset

An external reset must be applied to the active-low  $\overline{\text{RESET}}$  terminal while MCLK is active to ensure reset at power up.

### reference

A precision band-gap reference voltage is generated internally and supplies all required references to operate the transmit and receive channels.

### phase-locked loop

The phase-locked loop generates the internal clock frequency required for internal digital filters and modulators by phase-locking to 2.048-MHz master clock input.

### PCM interface

The PCM interface transmits and receives data at the PCMO and PCMI terminals, respectively. The data is transmitted or received at the MCLK speed once on each PCMSYN cycle. The PCMSYN can be driven by an external source that is derived from the master clock and used as an interrupt to the host controller.

### microphone input

The microphone input circuit consists of two differential input/differential output amplifiers (MIC Amp 1 and MIC Amp 2). MIC Amp 1 is a low-noise differential amplifier capable of an externally set gain. MIC Amp 2 is a differential amplifier with a fixed gain of 6 dB.

### analog modulator

The transmit channel modulator is a third-order sigma-delta design.

### transmit filter

The transmit filter is a digital filter designed to meet Consultative Committee on International Telegraphy and Telephony (CCITT) G.714 requirements. The TLV320AIC1106 device operates in either the 13-bit linear or 8-bit companded  $\mu$ -law mode.

### receive filter

The receive (RX) filter is a digital filter that meets CCITT G.714 requirements. The TLV320AIC1106 device operates in either the 13-bit linear or 8-bit  $\mu$ -law companded mode, which is selected at the  $\overline{\text{LINSEL}}$  input.

### receive volume control

In linear mode, the three least significant bits of the 16-bit PCMI data sample is used to control volume. The volume range is –18 dB to 3 dB in 3-dB steps.

### digital modulator and filter

The second-order digital modulator and filter convert the received digital PCM data to the analog output required by the earphone interface.

### earphone amplifiers

EAROUT is recommended for use as a differential output; however, it can be connected in single-ended topology as well. Clicks and pops are suppressed from the differential output.

Terminal Functions

| TERMINAL<br>TERMINAL | NO. | I/O | DESCRIPTION  |
|----------------------|-----|-----|--|
| EARVSS               | 4   | I   | Analog ground for EAROUT+                                |
| DVDD                 | 14  | I   | Digital positive power supply                            |
| DVSS                 | 15  | I   | Digital negative power supply                            |
| EARMUTE              | 20  | I   | Earphone mute  |
| EAROUT-              | 7   | O   | Earphone amplifier negative output                       |
| EAROUT+              | 5   | O   | Earphone amplifier positive output                       |
| EARVDD               | 6   | I   | Analog positive power supply for the earphone amplifiers |
| EARVSS               | 8   | I   | Analog ground for EAROUT-                                |
| LINSEL               | 13  | I   | Companding enable  |
| MCLK                 | 19  | I   | Master system clock input (2.048 MHz) (digital)          |
| MICGAIN+             | 9   | I   | Microphone gain positive feedback                        |
| MICGAIN-             | 12  | I   | Microphone gain negative feedback                        |
| MICMUTE              | 1   | I   | Microphone mute  |
| MICIN-               | 10  | I   | Microphone negative input (-)                            |
| MICIN+               | 11  | I   | Microphone positive input (+)                            |
| PCMI                 | 16  | I   | Receive PCM input  |
| PCMO                 | 17  | O   | Transmit PCM output                                      |
| PCMSYNC              | 18  | I   | PCM frame synchronization                                |
| RESET                | 2   | I   | Active-low reset   |
| VSS                  | 3   | I   | Ground return for band-gap internal reference            |

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, DVDD, EARVDD ..... -0.5 V to 3.6 V  
 Output voltage range, V<sub>O</sub> ..... -0.5 V to 3.6 V  
 Input voltage range, V<sub>I</sub> ..... -0.5 V to 3.6 V  
 Continuous total power dissipation ..... See Dissipation Rating Table  
 Operating free air temperature range, T<sub>A</sub> ..... -40°C to 85°C  
 Storage temperature range, T<sub>stg</sub> ..... -65°C to 150°C  
 Lead temperature 1,6 mm from case for 10 seconds ..... 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

| PACKAGE | T <sub>A</sub> ≤ 25°C<br>POWER RATING | DERATING FACTOR<br>ABOVE T <sub>A</sub> = 25°C | T <sub>A</sub> = 85°C<br>POWER RATING |
|---------|---------------------------------------|--|---------------------------------------|
| PW      | 680 W                                 | 6.8 W/°C                                       | 270 W                                 |

**recommended operating conditions (see Note 2)**

|  | MIN                   | NOM | MAX                   | UNIT |
|--|-----------------------|-----|-----------------------|------|
| Supply voltage, DVDD, EARVDD                               | 2.7                   |     | 3.3                   | V    |
| High-level input voltage, V <sub>IH</sub>                  | 0.7 × V <sub>DD</sub> |     |                       | V    |
| Low-level input voltage, V <sub>IL</sub>                   |                       |     | 0.3 × V <sub>DD</sub> | V    |
| Load impedance between EAROUT+ and EAROUT–, R <sub>L</sub> | 8 to 32               |     |                       | Ω    |
| Input voltage, MICIN                                       |                       |     | 0.9 × V <sub>DD</sub> | V    |
| Operating free-air temperature, T <sub>A</sub>             | –40                   |     | 85                    | °C   |

- NOTES: 1. To avoid possible damage and resulting reliability problems to these CMOS devices, follow the *power-on initialization* paragraph, described in the *Principles of Operations*.
2. Voltages are with respect to DVSS, and EARVSS.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)****supply current**

| PARAMETER       |                                     | TEST CONDITIONS              | MIN | TYP | MAX | UNIT |
|-----------------|-------------------------------------|------------------------------|-----|-----|-----|------|
| I <sub>DD</sub> | Supply current from V <sub>DD</sub> | Operating                    |     | 5   | 7   | mA   |
|                 |                                     | Power down, MCLK not present |     | 10  | 30  | μA   |
| t <sub>pu</sub> | Power-up time from power down       |                              |     |     | 10  | ms   |

**digital interface**

| PARAMETER       |   | TEST CONDITIONS                                  | MIN         | TYP | MAX | UNIT |
|-----------------|---|--|-------------|-----|-----|------|
| V <sub>OH</sub> | High-level output voltage, PCMO             | I <sub>OH</sub> = –3.2 mA, V <sub>DD</sub> = 3 V | DVDD – 0.25 |     |     | V    |
| V <sub>OL</sub> | Low-level output voltage, PCMO              | I <sub>OL</sub> = 3.2 mA, V <sub>DD</sub> = 3 V  |             |     | 0.2 | V    |
| I <sub>IH</sub> | High-level input current, any digital input | V <sub>I</sub> = 2.2 V to V <sub>DD</sub>        |             |     | 10  | μA   |
| I <sub>IL</sub> | Low-level input current, any digital input  | V <sub>I</sub> = 0 to 0.8 V                      |             |     | 10  | μA   |
| C <sub>I</sub>  | Input capacitance                           |  |             |     | 10  | pF   |
| C <sub>O</sub>  | Output capacitance                          |  |             |     | 20  | pF   |

**microphone interface**

| PARAMETER       |  | TEST CONDITIONS                      | MIN  | TYP | MAX | UNIT              |
|-----------------|--|--------------------------------------|------|-----|-----|-------------------|
| V <sub>IO</sub> | Input offset voltage                                   | See Note 3                           | –5   |     | 5   | mV                |
| I <sub>IB</sub> | Input bias current                                     |                                      | –250 |     | 250 | nA                |
| C <sub>i</sub>  | Input capacitance                                      |                                      |      | 5   |     | pF                |
| V <sub>n</sub>  | Microphone input referred noise, psophometric weighted | MIC Amp 1 gain = 23.5 dB, See Note 4 |      | 2.9 | 4   | μV <sub>rms</sub> |
|                 | MICMUTE  |                                      | –80  |     |     | dB                |

- NOTES: 3. Measured while MICIN+ and MICIN– are connected together. Less than a 0.5-mV offset results in 0 value code on PCMOUT.
4. Configured as shown in Figure 3.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**speaker interface**

| PARAMETER   |  | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|---|--|---|-----|-----|-----|------|
| Earphone AMP output power (see Note 5)                    |  | V <sub>DD</sub> = 2.7 V, fully differential, 8-Ω load, 3-dBm0 output, volume control = -3 dB, PCMI data input to -4 dB level  |     | 161 | 200 | mW   |
|   |  | V <sub>DD</sub> = 2.7 V, fully differential, 16-Ω load, 3-dBm0 output, volume control = -3 dB, PCMI data input to -2 dB level |     | 128 | 160 |      |
|   |  | V <sub>DD</sub> = 2.7 V, fully differential, 32-Ω load, 3-dBm0 output, volume control = -3 dB, PCMI data input to -1 dB level |     | 81  | 100 |      |
| I <sub>Omax</sub> Maximum output current for EAROUT (rms) |  | 3-dBm0 input, 8-Ω load  |     | 141 | 178 | mA   |
|   |  | 3-dBm0 input, 16-Ω load   |     | 90  | 112 |      |
|   |  | 3-dBm0 input, 32-Ω load   |     | 50  | 63  |      |
| EARMUTE   |  |   | -80 |     |     | dB   |

NOTE 5: Maximum power is with a load impedance of -20%, at 25°C.

**transmit gain and dynamic range, companded mode (μ-law) or linear mode selected (see Notes 6 and 7)**

| PARAMETER  | TEST CONDITIONS                                      | MIN  | TYP | MAX | UNIT             |
|--|--|------|-----|-----|------------------|
| Transmit reference-signal level (0dB)  | Differential, MIC Amp 1 configured for 23.5 dB gain  |      |     | 88  | mV <sub>pp</sub> |
| Overload-signal level (3 dBm0)   | Differential, MIC Amp 1 configured for 23.5 dB gain  |      |     | 124 | mV <sub>pp</sub> |
| Absolute gain error  | 0 dBm0 input signal, 2.7 V ≤ V <sub>DD</sub> ≤ 3.3 V | -1   |     | 1   | dB               |
| Gain error with input level relative to gain at -10 dBm0 MICIN, MICIN+ to PCMO | MICIN-, MICIN+ to PCMO at 3 dBm0 to -30 dBm0         | -0.5 |     | 0.5 | dB               |
|  | MICIN-, MICIN+ to PCMO at -31 dBm0 to -45 dBm0       | -1   |     | 1   |                  |
|  | MICIN-, MICIN+ to PCMO at -46 dBm0 to -55 dBm0       | -1.2 |     | 1.2 |                  |

NOTES: 6. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.

7. The reference signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 124-mV<sub>pp</sub>.

**transmit filter transfer, companded mode (μ-law) or linear mode selected**

| PARAMETER                                      | TEST CONDITIONS                    | MIN  | TYP | MAX | UNIT |
|--|------------------------------------|------|-----|-----|------|
| Gain relative to input signal gain at 1.02 kHz | f <sub>MIC</sub> < 100 Hz          | -0.5 |     | 0.5 | dB   |
|  | f <sub>MIC</sub> = 200 Hz          | -0.5 |     | 0.5 |      |
|  | f <sub>MIC</sub> = 300 Hz to 3 kHz | -0.5 |     | 0.5 |      |
|  | f <sub>MIC</sub> = 3.4 kHz         | -1.5 |     | 0   |      |
|  | f <sub>MIC</sub> = 4 kHz           |      |     | -14 |      |
|  | f <sub>MIC</sub> = 4.6 kHz         |      |     | -35 |      |
|  | f <sub>MIC</sub> = 8 kHz           |      |     | -47 |      |

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**transmit idle channel noise and distortion, companded mode ( $\mu$ -law) selected**

| PARAMETER  | TEST CONDITIONS                                    | MIN | TYP | MAX | UNIT              |
|--|--|-----|-----|-----|-------------------|
| Transmit idle channel noise, psophometrically weighted                           | MIC Amp 1 configured for 23.5-dB gain (see Note 8) |     | -80 | -70 | dBm <sub>0p</sub> |
| Transmit signal-to-distortion ratio with 1.02-kHz sine-wave input                | MICIN-, MICIN+ to PCMO at 3 dBm0                   | 27  |     |     | dBm0              |
|  | MICIN-, MICIN+ to PCMO at 0 dBm0                   | 30  |     |     |                   |
|  | MICIN-, MICIN+ to PCMO at -5 dBm0                  | 33  |     |     |                   |
|  | MICIN-, MICIN+ to PCMO at -10 dBm0                 | 36  |     |     |                   |
|  | MICIN-, MICIN+ to PCMO at -20 dBm0                 | 35  |     |     |                   |
|  | MICIN-, MICIN+ to PCMO at -30 dBm0                 | 26  |     |     |                   |
|  | MICIN-, MICIN+ to PCMO at -40 dBm0                 | 24  |     |     |                   |
| Intermodulation distortion, 2-tone CCITT method, composite power level, -13 dBm0 | CCITT G.712 (7.1), R2                              | 49  |     |     | dB                |
|  | CCITT G.712 (7.2), R2                              | 51  |     |     |                   |

NOTE 8: With recommended impedances and resistor tolerance of 1%

**transmit idle channel noise and distortion, linear mode selected**

| PARAMETER   | TEST CONDITIONS                                    | MIN | TYP | MAX | UNIT              |
|---|--|-----|-----|-----|-------------------|
| Transmit idle channel noise, psophometrically weighted                  | MIC Amp 1 configured for 23.5-dB gain (see Note 8) |     | -80 | -74 | dBm <sub>0p</sub> |
| Transmit signal-to-total distortion ratio with 1.02-kHz sine-wave input | MICIN-, MICIN+ to PCMO at 3 dBm0                   | 40  | 55  |     | dB                |
|   | MICIN-, MICIN+ to PCMO at 0 dBm0                   | 50  | 61  |     |                   |
|   | MICIN-, MICIN+ to PCMO at -5 dBm0                  | 52  | 62  |     |                   |
|   | MICIN-, MICIN+ to PCMO at -10 dBm0                 | 56  | 66  |     |                   |
|   | MICIN-, MICIN+ to PCMO at -20 dBm0                 | 52  | 68  |     |                   |
|   | MICIN-, MICIN+ to PCMO at -30 dBm0                 | 51  | 61  |     |                   |
|   | MICIN-, MICIN+ to PCMO at -40 dBm0                 | 43  | 59  |     |                   |
| MICIN-, MICIN+ to PCMO at -45 dBm0                                      | 38   | 55  |     |     |                   |

NOTE 8: With recommended impedances and resistor tolerance of 1%

**receive gain and dynamic range, linear or companded ( $\mu$ -law) mode selected (see Note 9)**

| PARAMETER   | TEST CONDITIONS   | MIN  | TYP  | MAX | UNIT            |
|---|---|------|------|-----|-----------------|
| Overload-signal level (3 dB)                              | Load = 8 $\Omega$ , volume control = -3 dB, PCMI data input to -4 dB level  |      | 3.2  |     | V <sub>pp</sub> |
|   | Load = 16 $\Omega$ , volume control = -3 dB, PCMI data input to -2 dB level |      | 4.05 |     |                 |
|   | Load = 32 $\Omega$ , volume control = -3 dB, PCMI data input to -1 dB level |      | 4.54 |     |                 |
| Absolute gain error                                       | 0 dBm0 input signal, $2.7 \text{ V} \leq V_{DD} \leq 3.3 \text{ V}$         | -1   |      | 1   | dB              |
| Gain error with output level relative to gain at -10 dBm0 | PCMI to EAROUT-, EAROUT+ at 3 dBm0 to -40 dBm0                              | -0.5 |      | 0.5 | dB              |
|   | PCMI to EAROUT-, EAROUT+ at -41 dBm0 to -50 dBm0                            | -1   |      | 1   |                 |
|   | PCMI to EAROUT-, EAROUT+ at -51 dBm0 to -55 dBm0                            | -1.2 |      | 1.2 |                 |

NOTE 9: 1020-Hz input signal at PCMI, output measured differentially between EAROUT- and EAROUT+

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

receive filter transfer, companded mode ( $\mu$ -law) or linear mode selected (MCLK = 2.048 MHz) (see Note 10)

| PARAMETER                                      | TEST CONDITIONS                       | MIN  | TYP | MAX | UNIT |
|--|---------------------------------------|------|-----|-----|------|
| Gain relative to input signal gain at 1.02-kHz | $f_{\text{EAROUT}} < 100$ Hz          |      |     | -15 | dB   |
|  | $f_{\text{EAROUT}} = 200$ Hz          |      |     | -5  |      |
|  | $f_{\text{EAROUT}} = 300$ Hz to 3 kHz | -0.5 |     | 0.5 |      |
|  | $f_{\text{EAROUT}} = 3.4$ kHz         | -1.5 |     | 0   |      |
|  | $f_{\text{EAROUT}} = 4$ kHz           |      |     | -14 |      |
|  | $f_{\text{EAROUT}} = 4.6$ kHz         |      |     | -35 |      |
|  | $f_{\text{EAROUT}} = 8$ kHz           |      |     | -47 |      |

NOTE 10: Volume control = -3 dB, PCMI data input to -1 dB level (32- $\Omega$  load)

receive idle channel noise and distortion, companded mode ( $\mu$ -law) selected (see Note 10)

| PARAMETER  | TEST CONDITIONS                      | MIN | TYP | MAX | UNIT |
|--|--------------------------------------|-----|-----|-----|------|
| Receive noise, C-message weighted                                | PCMI = 11111111 ( $\mu$ -law)        |     | -90 | -88 | dBm0 |
| Receive signal-to-distortion ratio with 1.02-kHz sine-wave input | PCMI to EAROUT-, EAROUT+ at 3 dBm0   | 21  |     |     | dB   |
|  | PCMI to EAROUT-, EAROUT+ at 0 dBm0   | 25  |     |     |      |
|  | PCMI to EAROUT-, EAROUT+ at -5 dBm0  | 36  |     |     |      |
|  | PCMI to EAROUT-, EAROUT+ at -10 dBm0 | 43  |     |     |      |
|  | PCMI to EAROUT-, EAROUT+ at -20 dBm0 | 40  |     |     |      |
|  | PCMI to EAROUT-, EAROUT+ at -30 dBm0 | 38  |     |     |      |
|  | PCMI to EAROUT-, EAROUT+ at -40 dBm0 | 28  |     |     |      |
|  | PCMI to EAROUT-, EAROUT+ at -45 dBm0 | 23  |     |     |      |

NOTE 10: Volume control = -3 dB, PCMI data input to -1 dB level (32- $\Omega$  load)

receive idle channel noise and distortion, linear mode selected (see Note 10)

| PARAMETER  | TEST CONDITIONS                      | MIN | TYP | MAX | UNIT |
|--|--------------------------------------|-----|-----|-----|------|
| Receive noise, (20-Hz to 20-kHz brickwall window)                                | PCMI = 00000000000000                |     | -83 | -78 | dBm0 |
| Receive signal-to-distortion ratio with 1.02-kHz sine-wave input (0-4 kHz)       | PCMI to EAROUT-, EAROUT+ at 3 dBm0   | 48  | 52  |     | dB   |
|  | PCMI to EAROUT-, EAROUT+ at 0 dBm0   | 51  | 56  |     |      |
|  | PCMI to EAROUT-, EAROUT+ at -5 dBm0  | 57  | 59  |     |      |
|  | PCMI to EAROUT-, EAROUT+ at -10 dBm0 | 55  | 62  |     |      |
|  | PCMI to EAROUT-, EAROUT+ at -20 dBm0 | 51  | 53  |     |      |
|  | PCMI to EAROUT-, EAROUT+ at -30 dBm0 | 45  | 47  |     |      |
|  | PCMI to EAROUT-, EAROUT+ at -40 dBm0 | 42  | 47  |     |      |
| Intermodulation distortion, 2-tone CCITT method, composite power level, -13 dBm0 | CCITT G.712 (7.1), R2                | 50  |     |     | dB   |
|  | CCITT G.712 (7.2), R2                | 54  |     |     |      |

NOTE 10: Volume control = -3 dB, PCMI data input to -1 dB level (32- $\Omega$  load)

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**power supply rejection**

| PARAMETER  | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-----|------|
| Supply voltage rejection, transmit channel               | MICIN-, MICIN+ = 0 V, $V_{DD} = 2.7\text{ V} + 100\text{ mV}_{pp}$ ,<br>f = 1 kHz, Resistor tolerance of 1%     |     | -74 | -50 | dB   |
| Supply voltage rejection, receive channel (differential) | PCM code = positive zero, $V_{DD} = 2.7\text{ V} + 100\text{ mV}_{pp}$ ,<br>f = 1 kHz, Resistor tolerance of 1% |     | -80 | -65 | dB   |

**crosstalk attenuation, linear mode selected**

| PARAMETER   | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|---|--|-----|-----|-----|------|
| Crosstalk attenuation, transmit-to-receive (differential) | MICIN-, MICIN+ = 0 dB, f = 300 Hz to 3400 Hz measured differentially between EAROUT- and EAROUT+ | 70  |     |     | dB   |
| Crosstalk attenuation, receive-to-transmit                | PCMI = 0 dBm0, f = 300 Hz to 3400 Hz measured at PCMO  | 70  |     |     | dB   |

**timing requirements**

**clock**

|                                    | MIN | NOM   | MAX | UNIT   |
|------------------------------------|-----|-------|-----|--------|
| $t_t$ Transition time, MCLK        |     |       | 10  | ns     |
| $f_{mclk}$ MCLK frequency          |     | 2.048 |     | MHz    |
| MCLK jitter                        |     |       | 37% |        |
| MCLK clock cycles per PCMSYN frame | 256 |       | 256 | cycles |

**transmit (see Figure 1)**

|  | MIN | MAX              | UNIT |
|--|-----|------------------|------|
| $t_{su}(PCMSYN)$ Setup time, PCMSYN high before MCLK ↓ | 20  | $t_c(MCLK) - 20$ | ns   |
| $t_h(PCMSYN)$ Hold time, PCMSYN high after MCLK ↓      | 20  | $t_c(MCLK) - 20$ |      |

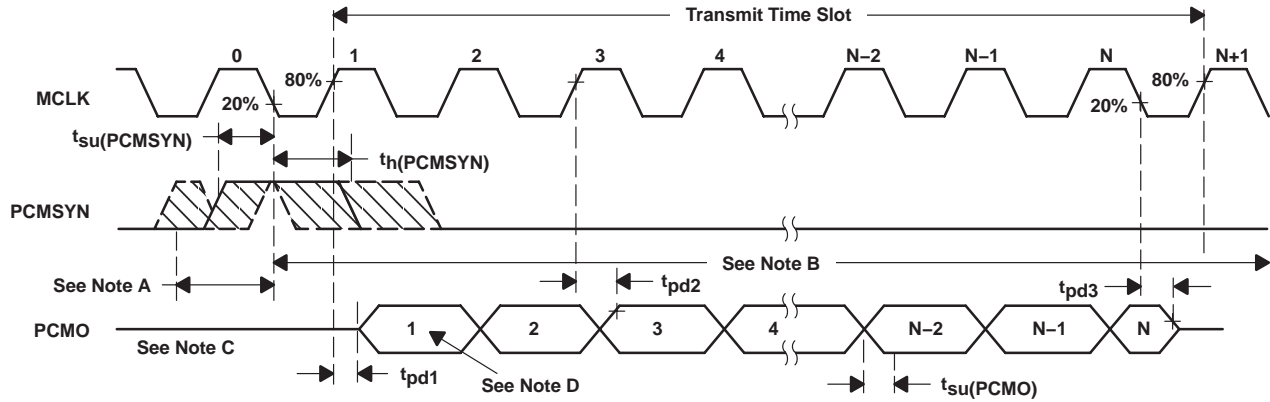
**receive (see Figure 2)**

|   | MIN | MAX              | UNIT |
|---|-----|------------------|------|
| $t_{su}(PCSYN)$ Setup time, PCMSYN high before MCLK ↓     | 20  | $t_c(MCLK) - 20$ | ns   |
| $t_h(PCSYN)$ Hold time, PCMSYN high after MCLK ↓          | 20  | $t_c(MCLK) - 20$ | ns   |
| $t_{su}(PCMI)$ Setup time, PCMI high or low before MCLK ↓ | 20  |                  | ns   |
| $t_h(PCMI)$ Hold time, PCMI high or low after MCLK ↓      | 20  |                  | ns   |

**switching characteristics over recommended operating conditions,  $C_L$  max = 10 pF (see Figure 1)**

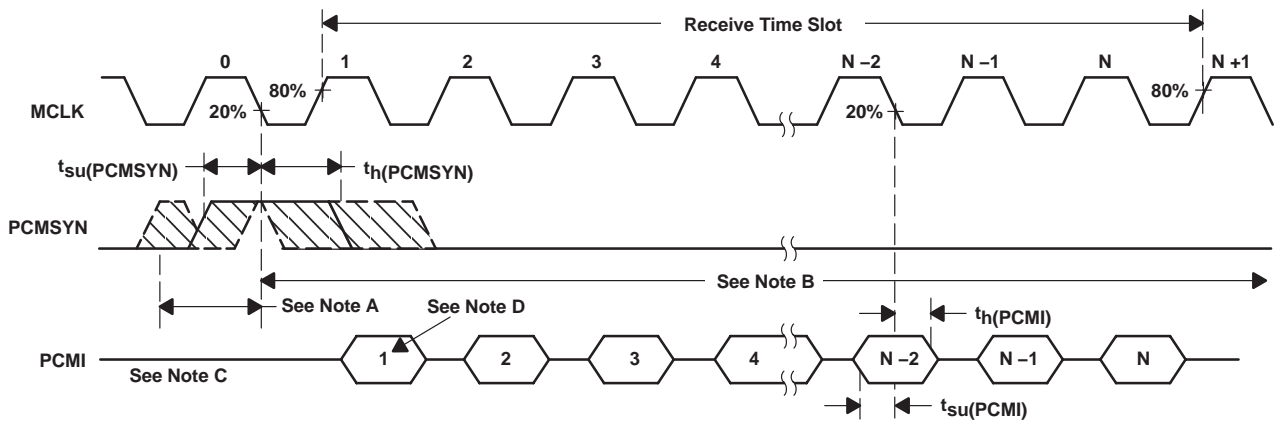
|  | MIN | MAX | UNIT |
|--|-----|-----|------|
| $t_{pd1}$ Propagation delay time, MCLK bit 1 high to PCMO bit 1 valid  |     | 35  | ns   |
| $t_{pd2}$ Propagation delay time, MCLK high to PCMO valid, bits 2 to n |     | 35  | ns   |
| $t_{pd3}$ Propagation delay time, MCLK bit n low to PCMO bit n Hi-Z    | 30  |     | ns   |

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. This window is allowed for PCMSYN high.  
 B. This window is allowed for PCMSYN low ( $t_h(PCMSYN)$  max determined by data collision considerations).  
 C. Transitions are measured at 50%.  
 D. Bit 1 = Most significant bit (MSB), Bit N = Least significant bit (LSB)

Figure 1. Transmit Timing Diagram



- NOTES: A. This window is allowed for PCMSYN high.  
 B. This window is allowed for PCMSYN low.  
 C. Transitions are measured at 50%.  
 D. Bit 1 = Most significant bit (MSB), Bit N = Least significant bit (LSB)

Figure 2. Receive Timing Diagram

## PRINCIPLES OF OPERATION

### power-up initialization

An external reset with a minimum pulse width of 500 ns must be applied to the active-low  $\overline{\text{RESET}}$  terminal with MCLK active to ensure reset upon power up.

**Table 1. Power-Up and Power-Down Power Consumption  
( $V_{DD} = 2.7$  V, Earphone Amplifier Loaded)**

| DEVICE STATUS | MAXIMUM POWER CONSUMPTION |
|---------------|---------------------------|
| Power up      | 16.2 mW                   |
| Power down    | 81 $\mu$ W                |

The loss of MCLK (no transition detected) automatically enters the device into a power-down state with PCMO in the high-impedance state. If an asynchronous power down occurs during a pulse code modulation (PCM) data transmit cycle, the PCM interface remains powered up until the PCM data is completely transferred.

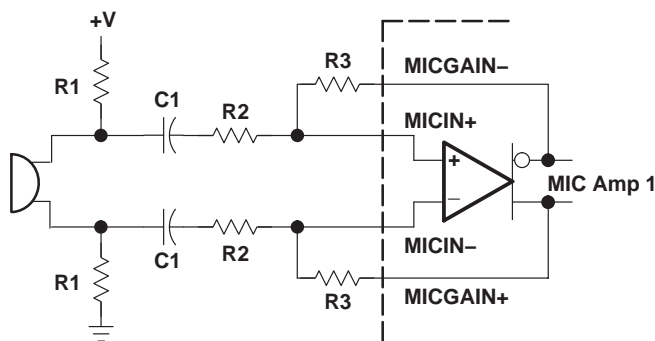
### conversion laws

The device can be programmed either for a 13-bit linear or 8-bit ( $\mu$ -law) companding mode. The companding operation approximates the CCITT G.711 recommendation. The linear mode operation uses a 13-bit twos complement format. Linear mode is selected with  $\overline{\text{LINSEL}}$  low.  $\overline{\text{LINSEL}}$  is high for companding.

### transmit operation

#### microphone input

The microphone input stage is a low-noise differential amplifier. The microphone must be capacitively coupled to the MICIN $^-$  and MICIN $^+$  terminals. Pre-amplifier (MIC Amp 1) gain is determined by selection of external resistors R2 and R3. To achieve the recommended gain setting of 23.5 dB for MIC Amp 1, resistor values of R2 = 34 k $\Omega$  and R3 = 510 k $\Omega$  are suggested. A 1% tolerance is recommended for all resistors to meet the specification. The recommended range for R2 is 34–100 k $\Omega$ . For values above 100 k $\Omega$ , the noise performance of the channel is degraded.



$$R1 = 2 \text{ k}\Omega$$

$$C1 = 0.22 \text{ }\mu\text{F}$$

$$\text{MIC Amp 1 Gain in dB} = 20 \log \left( \frac{R3}{R2} \right)$$

**Figure 3. Typical Microphone Interface**

**PRINCIPLES OF OPERATION**

**microphone mute function**

Transmit channel muting can be selected by setting MICMUTE high. Muting provides 80-dB attenuation of the input microphone signal.

**receive operation**

**earphone amplifier**

The analog signal is routed to the earphone amplifier differential output (EAROUT– or EAROUT+), which is capable of driving a load as low as 8 Ω. EAROUT is recommended for use as a differential output.

**earphone mute function**

Receive channel muting can be selected by setting the EARMUTE terminal to high.

**receive PCM data format**

- Companded mode: 8 bits are received, the MSB first
- Linear mode: 13 bits are received, the MSB first

**Table 2. Receive Data Bit Definitions**

| BIT NO. | COMPANDED MODE | LINEAR MODE |
|---------|----------------|-------------|
| 1       | CD7            | LD12        |
| 2       | CD6            | LD11        |
| 3       | CD5            | LD10        |
| 4       | CD4            | LD9         |
| 5       | CD3            | LD8         |
| 6       | CD2            | LD7         |
| 7       | CD1            | LD6         |
| 8       | CD0            | LD5         |
| 9       | –              | LD4         |
| 10      | –              | LD3         |
| 11      | –              | LD2         |
| 12      | –              | LD1         |
| 13      | –              | LD0         |
| 14      | –              | RXVOL2      |
| 15      | –              | RXVOL1      |
| 16      | –              | RXVOL0      |

---

## PRINCIPLES OF OPERATION

### receive volume control

In linear mode, RXVOL [2:0] PCM data bits are used for volume control according to Table 3. Volume control bits must be sent on PCMI for each 13-bit receive word. In companded mode, volume control is fixed at 0 dB.

**Table 3. Volume Control Bit Definition in Linear Mode**

| RXVOL [2:0] | GAIN SETTING |
|-------------|--------------|
| 000         | 3 dB         |
| 001         | 0 dB         |
| 010         | -3 dB        |
| 011         | -6 dB        |
| 100         | -9 dB        |
| 101         | -12 dB       |
| 110         | -15 dB       |
| 111         | -18 dB       |

### support section

The clock generator and control circuit uses the master clock input (MCLK) to generate internal clocks to drive internal counters, filters, and converters.

### clock frequencies and sample rates

A fixed PCMSYN rate of 8 kHz determines the sampling rate. The PCMSYN signal must be derived from the master clock. The divide ratio must be set to 256 for the device to work properly.

TYPICAL CHARACTERISTICS

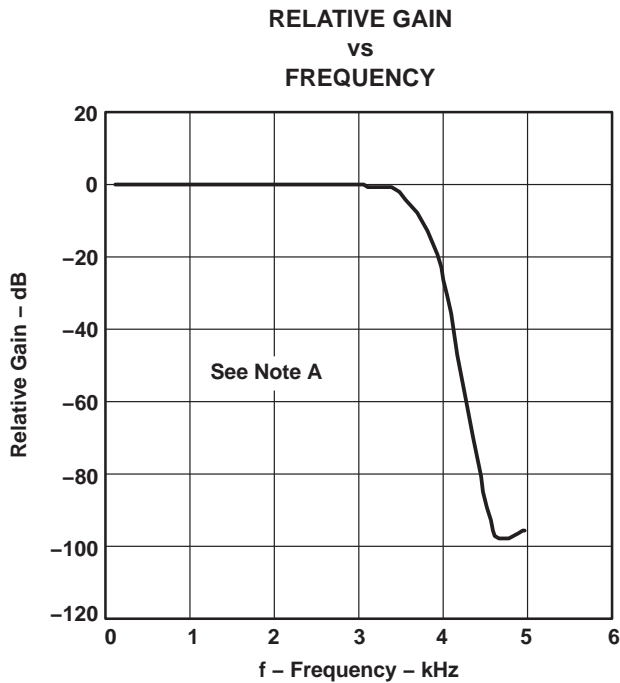


Figure 4

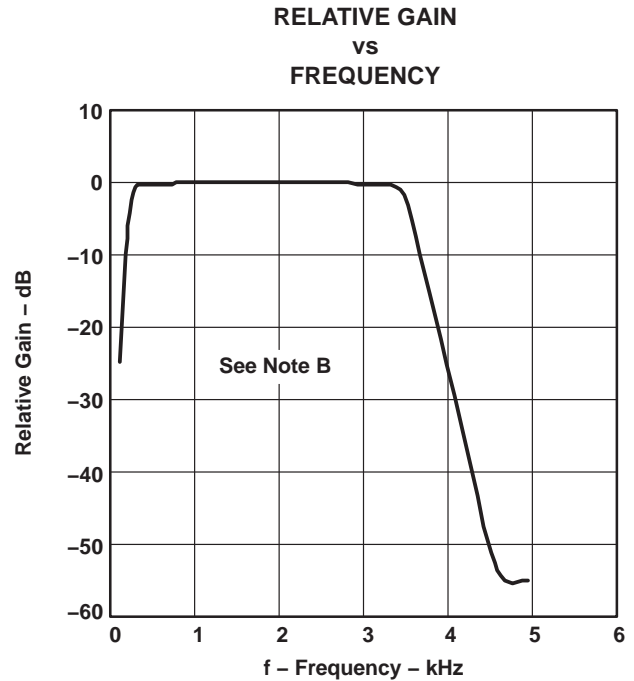


Figure 5

NOTES: A. Transmit channel frequency response shown relative to the gain at a 1.02-kHz input signal in linear mode.  
B. Receive channel frequency response shown relative to the gain at a 1.02-kHz input signal in linear mode.

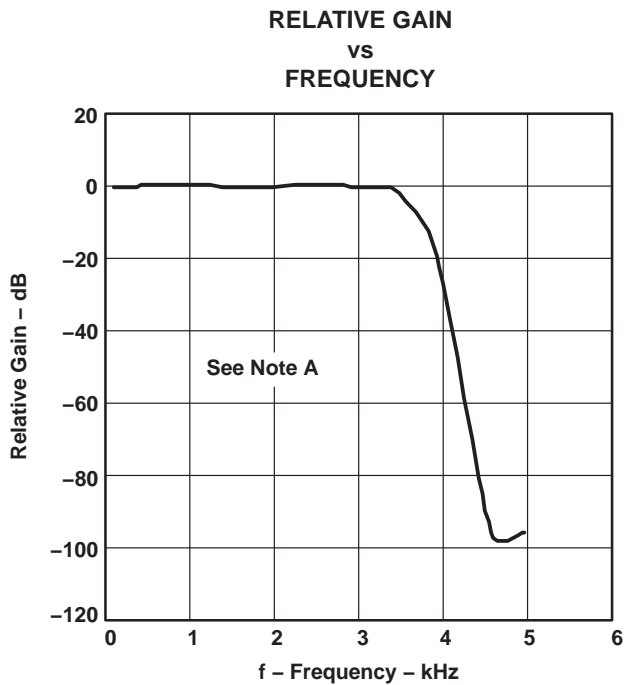


Figure 6

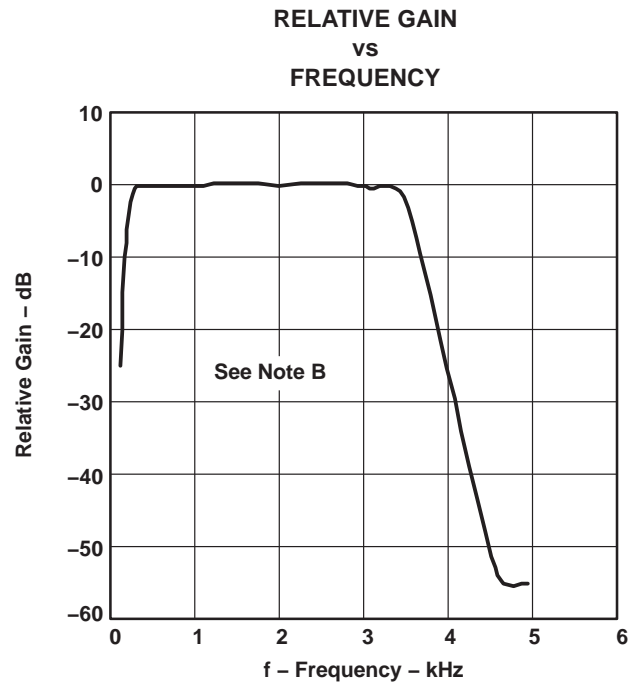
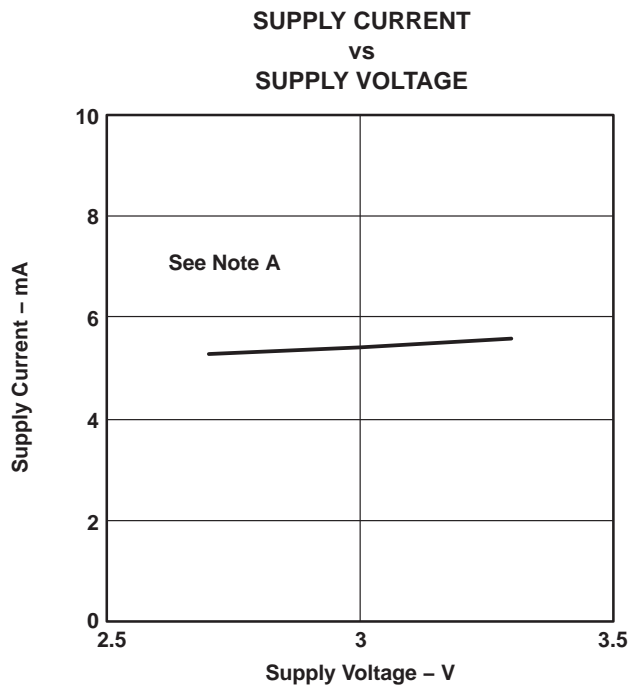


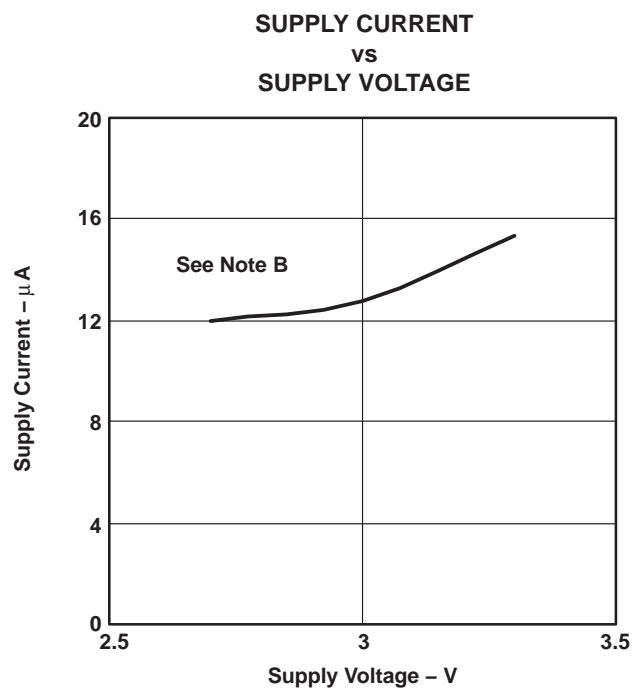
Figure 7

NOTES: A. Transmit channel frequency response shown relative to the gain at a 1.02-kHz input signal in  $\mu$ -Law mode.  
B. Receive channel frequency response shown relative to the gain at a 1.02-kHz input signal in  $\mu$ -Law mode.

TYPICAL CHARACTERISTICS



**Figure 8**



**Figure 9**

- NOTES: A. Supply current as a function of supply voltage in power-up mode.  
 B. Supply current as a function of supply voltage in power-down mode.

## PACKAGING INFORMATION

| Orderable Device   | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|--------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| TLV320AIC1106PW    | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | AIC1106                  | <a href="#">Samples</a> |
| TLV320AIC1106PWG4  | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | AIC1106                  | <a href="#">Samples</a> |
| TLV320AIC1106PWR   | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | AIC1106                  | <a href="#">Samples</a> |
| TLV320AIC1106PWRG4 | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | AIC1106                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV320AIC1106PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV320AIC1106PWR | TSSOP        | PW              | 20   | 2000 | 350.0       | 350.0      | 43.0        |

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