



**THE DATASHEET OF  
MC14016BDR2**



# Quad Analog Switch/ Quad Multiplexer

## MC14016B

The MC14016B quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

### Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise –  $12 \text{ nV}/\sqrt{\text{Cycle}}$ ,  $f \geq 1.0 \text{ kHz}$  typical
- Pin-for-Pin Replacements for CD4016B, CD4066B (Note Improved Transfer Characteristic Design Causes More Parasitic Coupling Capacitance than CD4016)
- For Lower  $R_{ON}$ , Use The HC4016 High-Speed CMOS Device or The MC14066B
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable\*
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient) per Control Pin	$\pm 10$	mA
$I_{SW}$	Switch Through Current	$\pm 25$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

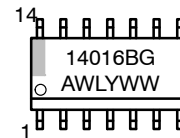
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



SOIC-14  
D SUFFIX  
CASE 751A

### MARKING DIAGRAM



A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Indicator

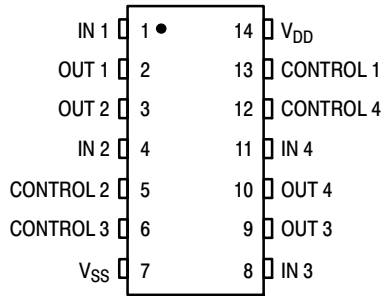
### ORDERING INFORMATION

Device	Package	Shipping†
MC14016BDG	SOIC-14 (Pb-Free)	55 Units / Tube
MC14016BDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV14016BDR2G*	SOIC-14 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

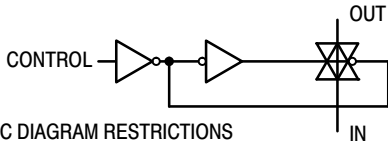
# MC14016B

## PIN ASSIGNMENT



## LOGIC DIAGRAM

(1/4 OF DEVICE SHOWN)

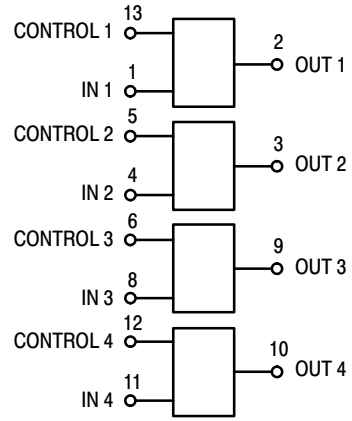


LOGIC DIAGRAM RESTRICTIONS

$$V_{SS} \leq V_{in} \leq V_{DD}$$

$$V_{SS} \leq V_{out} \leq V_{DD}$$

## BLOCK DIAGRAM



$V_{DD} = \text{PIN } 14$   
 $V_{SS} = \text{PIN } 7$

Control	Switch
0 = $V_{SS}$	Off
1 = $V_{DD}$	On

# MC14016B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Figure	Symbol	$V_{DD}$ Vdc	-55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Input Voltage Control Input	1	$V_{IL}$	5.0	-	-	-	1.5	0.9	-	-	Vdc
			10	-	-	-	1.5	0.9	-	-	
			15	-	-	-	1.5	0.9	-	-	
		$V_{IH}$	5.0	-	-	3.0	2.0	-	-	-	Vdc
			10	-	-	8.0	6.0	-	-	-	
			15	-	-	13	11	-	-	-	
Input Current Control	-	$I_{in}$	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	µAdc
Input Capacitance Control Switch Input Switch Output Feed Through	-	$C_{in}$	-	-	-	-	5.0	-	-	-	pF
			-	-	-	-	5.0	-	-	-	
			-	-	-	-	5.0	-	-	-	
			-	-	-	-	0.2	-	-	-	
Quiescent Current (Per Package) (Note 3)	2,3	$I_{DD}$	5.0	-	0.25	-	0.0005	0.25	-	7.5	µAdc
			10	-	0.5	-	0.0010	0.5	-	15	
			15	-	1.0	-	0.0015	1.0	-	30	
"ON" Resistance ( $V_C = V_{DD}$ , $R_L = 10\text{ k}\Omega$ )  ( $V_{in} = +10\text{ Vdc}$ ) ( $V_{in} = +0.25\text{ Vdc}$ , $V_{SS} = 0\text{ Vdc}$ ) ( $V_{in} = +5.6\text{ Vdc}$ )  ( $V_{in} = +15\text{ Vdc}$ ) ( $V_{in} = +0.25\text{ Vdc}$ , $V_{SS} = 0\text{ Vdc}$ ) ( $V_{in} = +9.3\text{ Vdc}$ )	4,5,6	$R_{ON}$	-	-	600	-	260	660	-	840	Ω
			-	-	600	-	310	660	-	840	
			10	-	600	-	310	660	-	840	
			-	-	360	-	260	400	-	520	
			-	-	360	-	260	400	-	520	
			15	-	360	-	300	400	-	520	
Δ "ON" Resistance Between any 2 circuits in a common package ( $V_C = V_{DD}$ ) ( $V_{in} = +5.0\text{ Vdc}$ , $V_{SS} = -5.0\text{ Vdc}$ ) ( $V_{in} = +7.5\text{ Vdc}$ , $V_{SS} = -7.5\text{ Vdc}$ )	-	$\Delta R_{ON}$	-	-	-	-	-	-	-	-	Ω
			5.0	-	-	-	15	-	-	-	
			7.5	-	-	-	10	-	-	-	
Input/Output Leakage Current ( $V_C = V_{SS}$ ) ( $V_{in} = +7.5$ , $V_{out} = -7.5\text{ Vdc}$ ) ( $V_{in} = -7.5$ , $V_{out} = +7.5\text{ Vdc}$ )	-	-	-	-	-	-	-	-	-	-	µAdc
			7.5	-	±0.1	-	±0.0015	±0.1	-	±1.0	
			7.5	-	±0.1	-	±0.0015	±0.1	-	±1.0	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: All unused inputs must be returned to  $V_{DD}$  or  $V_{SS}$  as appropriate for the circuit application.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. For voltage drops across the switch ( $\Delta V_{switch}$ ) > 600 mV (> 300 mV at high temperature), excessive  $V_{DD}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{DD}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.) Reference Figure 14.

# MC14016B

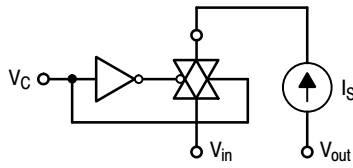
## ELECTRICAL CHARACTERISTICS (Note 4) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Figure	Symbol	$V_{DD}$ Vdc	Min	Typ (Note 5)	Max	Unit
Propagation Delay Time ( $V_{SS} = 0 \text{ Vdc}$ ) $V_{in}$ to $V_{out}$ ( $V_C = V_{DD}$ , $R_L = 10 \text{ k}\Omega$ )	7	$t_{PLH}$ ,	5.0	–	15	45	ns
		$t_{PHL}$	10 15	– –	7.0 6.0	20 15	
Control to Output ( $V_{in} \leq 10 \text{ Vdc}$ , $R_L = 10 \text{ k}\Omega$ )	8	$t_{PHZ}$ ,	5.0	–	34	120	ns
		$t_{PLZ}$ ,	10	–	20	110	
		$t_{PZH}$ ,	15	–	15	100	
		$t_{PZL}$					
Crosstalk, Control to Output ( $V_{SS} = 0 \text{ Vdc}$ ) ( $V_C = V_{DD}$ , $R_{in} = 10 \text{ k}\Omega$ , $R_{out} = 10 \text{ k}\Omega$ , $f = 1.0 \text{ kHz}$ )	9	–	5.0	–	30	–	mV
			10	–	50	–	
			15	–	100	–	
Crosstalk between any two switches ( $V_{SS} = 0 \text{ Vdc}$ ) ( $R_L = 1.0 \text{ k}\Omega$ , $f = 1.0 \text{ MHz}$ , crosstalk = $20 \log_{10} \frac{V_{out1}}{V_{out2}}$ )	–	–	5.0	–	–80	–	dB
Noise Voltage ( $V_{SS} = 0 \text{ Vdc}$ ) ( $V_C = V_{DD}$ , $f = 100 \text{ Hz}$ )  ( $V_C = V_{DD}$ , $f = 100 \text{ kHz}$ )	10,11	–	5.0	–	24	–	nV/ $\sqrt{\text{Cycle}}$
			10	–	25	–	
			15	–	30	–	
			5.0	–	12	–	
			10	–	12	–	
			15	–	15	–	
Second Harmonic Distortion ( $V_{SS} = -5.0 \text{ Vdc}$ ) ( $V_{in} = 1.77 \text{ Vdc}$ , RMS Centered @ $0.0 \text{ Vdc}$ , $R_L = 10 \text{ k}\Omega$ , $f = 1.0 \text{ kHz}$ )	–	–	5.0	–	0.16	–	%
Insertion Loss ( $V_C = V_{DD}$ , $V_{in} = 1.77 \text{ Vdc}$ , $V_{SS} = -5.0 \text{ Vdc}$ , RMS centered = $0.0 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )  $I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$ ( $R_L = 1.0 \text{ k}\Omega$ ) ( $R_L = 10 \text{ k}\Omega$ ) ( $R_L = 100 \text{ k}\Omega$ ) ( $R_L = 1.0 \text{ M}\Omega$ )	12	–	5.0	–	2.3	–	dB
				–	0.2	–	
				–	0.1	–	
				–	0.05	–	
				–			
Bandwidth ( $-3.0 \text{ dB}$ ) ( $V_C = V_{DD}$ , $V_{in} = 1.77 \text{ Vdc}$ , $V_{SS} = -5.0 \text{ Vdc}$ , RMS centered @ $0.0 \text{ Vdc}$ ) ( $R_L = 1.0 \text{ k}\Omega$ ) ( $R_L = 10 \text{ k}\Omega$ ) ( $R_L = 100 \text{ k}\Omega$ ) ( $R_L = 1.0 \text{ M}\Omega$ )	12,13	BW	5.0	–	54	–	MHz
				–	40	–	
				–	38	–	
				–	37	–	
				–			
OFF Channel Feedthrough Attenuation ( $V_{SS} = -5.0 \text{ Vdc}$ ) ( $V_C = V_{SS}$ , $20 \log_{10} \frac{V_{out}}{V_{in}} = -50 \text{ dB}$ ) ( $R_L = 1.0 \text{ k}\Omega$ ) ( $R_L = 10 \text{ k}\Omega$ ) ( $R_L = 100 \text{ k}\Omega$ ) ( $R_L = 1.0 \text{ M}\Omega$ )	–	–	5.0	–	1250	–	kHz
				–	140	–	
				–	18	–	
				–	2.0	–	
				–			
				–			

4. The formulas given are for typical characteristics only at  $25^\circ\text{C}$ .

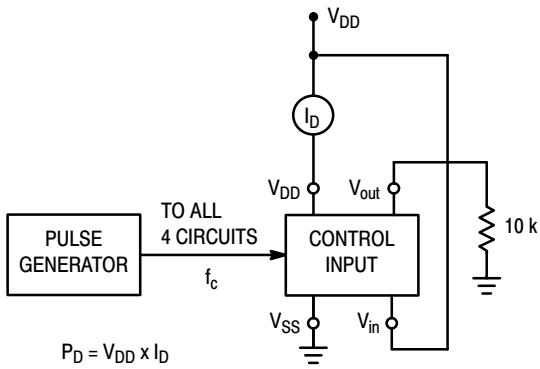
5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14016B

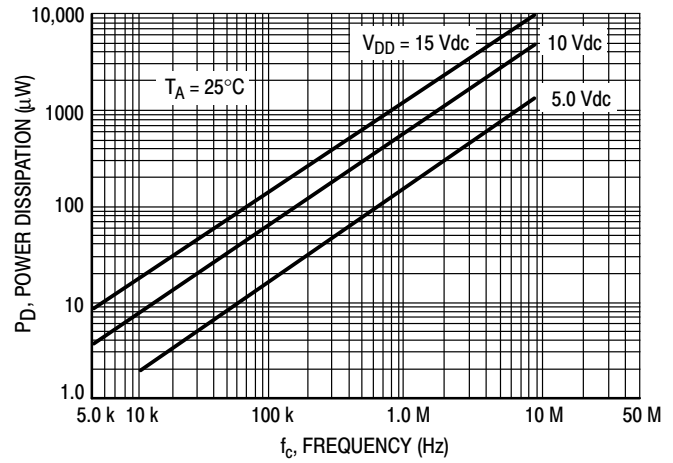


$V_{IL}$ :  $V_C$  is raised from  $V_{SS}$  until  $V_C = V_{IL}$ .  
 at  $V_C = V_{IL}$ :  $I_S = \pm 10 \mu A$  with  $V_{in} = V_{SS}$ ,  $V_{out} = V_{DD}$  or  $V_{in} = V_{DD}$ ,  $V_{out} = V_{SS}$ .  
 $V_{IH}$ : When  $V_C = V_{IH}$  to  $V_{DD}$ , the switch is ON and the  $R_{ON}$  specifications are met.

**Figure 1. Input Voltage Test Circuit**

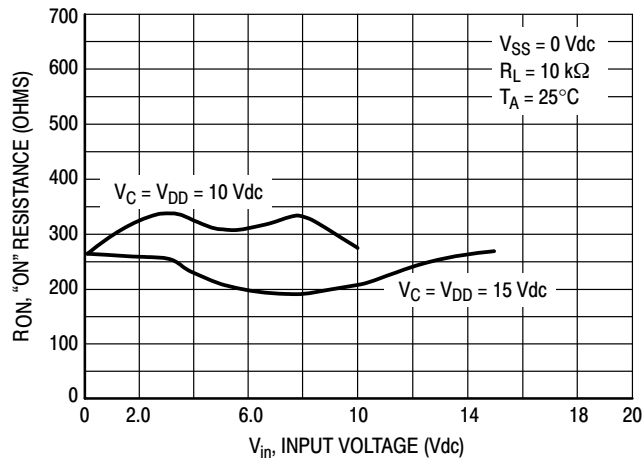


**Figure 2. Quiescent Power Dissipation Test Circuit**



**Figure 3. Typical Power Dissipation per Circuit (1/4 of device shown)**

## TYPICAL $R_{ON}$ VERSUS INPUT VOLTAGE



**Figure 4.  $V_{SS} = 0 V$**

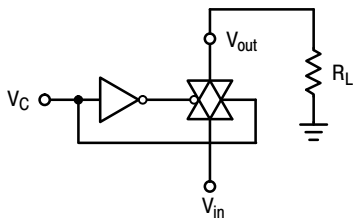


Figure 5.  $R_{ON}$  Characteristics Test Circuit

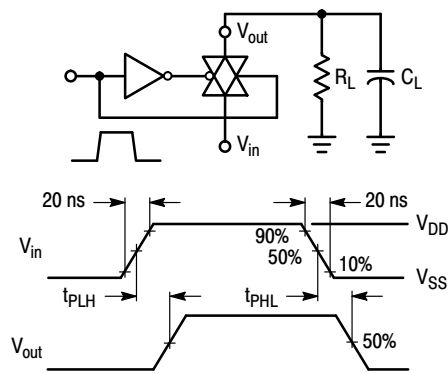


Figure 6. Propagation Delay Test Circuit and Waveforms

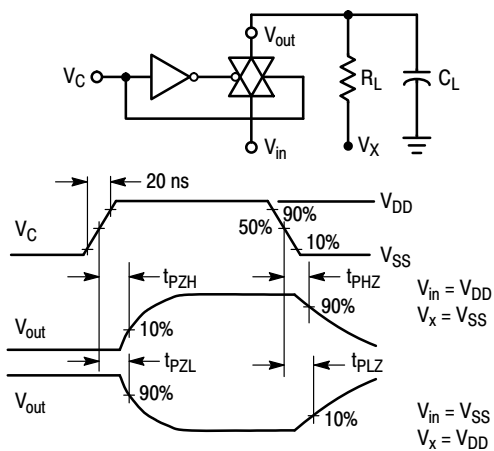


Figure 7. Turn-On Delay Time Test Circuit and Waveforms

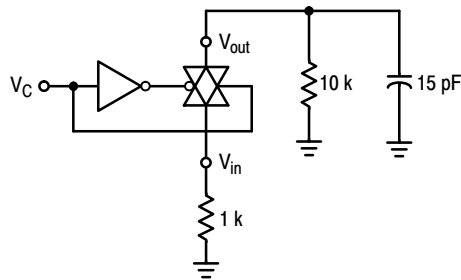


Figure 8. Crosstalk Test Circuit

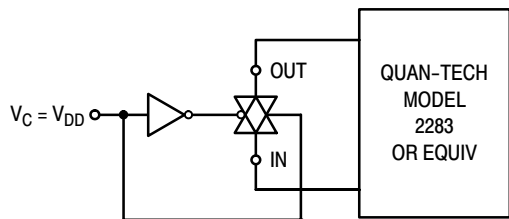


Figure 9. Noise Voltage Test Circuit

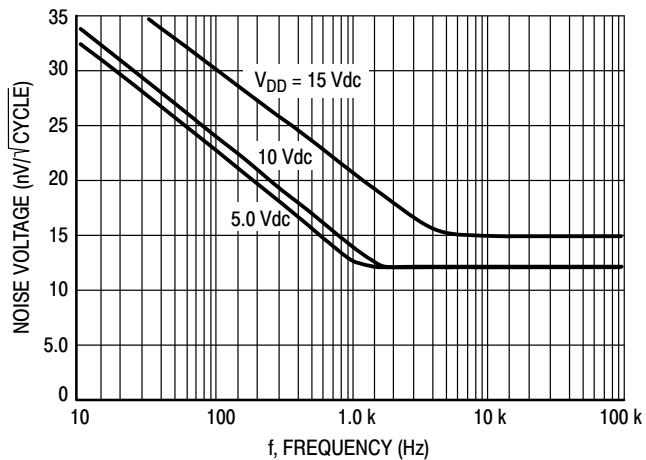
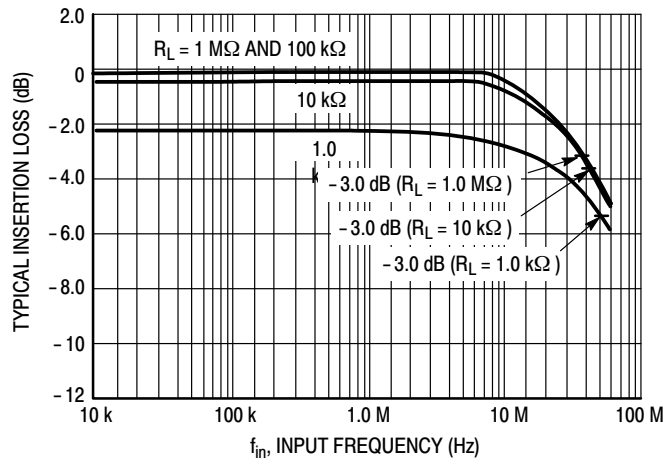
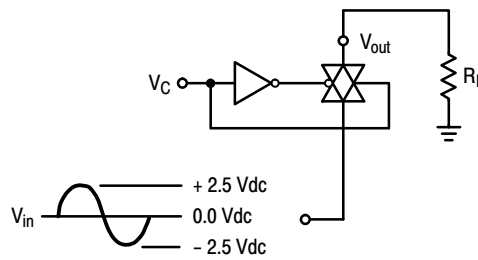


Figure 10. Typical Noise Characteristics

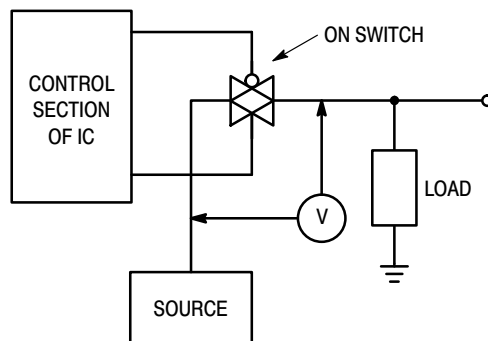
# MC14016B



**Figure 11. Typical Insertion Loss/Bandwidth Characteristics**



**Figure 12. Frequency Response Test Circuit**



**Figure 13.  $\Delta V$  Across Switch**

# MC14016B

## APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 V Digital Control signal is used to directly control a 5 V<sub>p-p</sub> analog signal.

The digital control logic levels are determined by V<sub>DD</sub> and V<sub>SS</sub>. The V<sub>DD</sub> voltage is the logic high voltage; the V<sub>SS</sub> voltage is logic low. For the example, V<sub>DD</sub> = +5 V logic high at the control inputs; V<sub>SS</sub> = GND = 0 V logic low.

The maximum analog signal level is determined by V<sub>DD</sub> and V<sub>SS</sub>. The analog voltage must not swing higher than V<sub>DD</sub> or lower than V<sub>SS</sub>.

The example shows a 5 V<sub>p-p</sub> signal which allows no margin at either peak. If voltage transients above V<sub>DD</sub> and/or below V<sub>SS</sub> are anticipated on the analog channels, external diodes (D<sub>x</sub>) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V<sub>DD</sub> and V<sub>SS</sub> is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V<sub>DD</sub> and V<sub>SS</sub>.

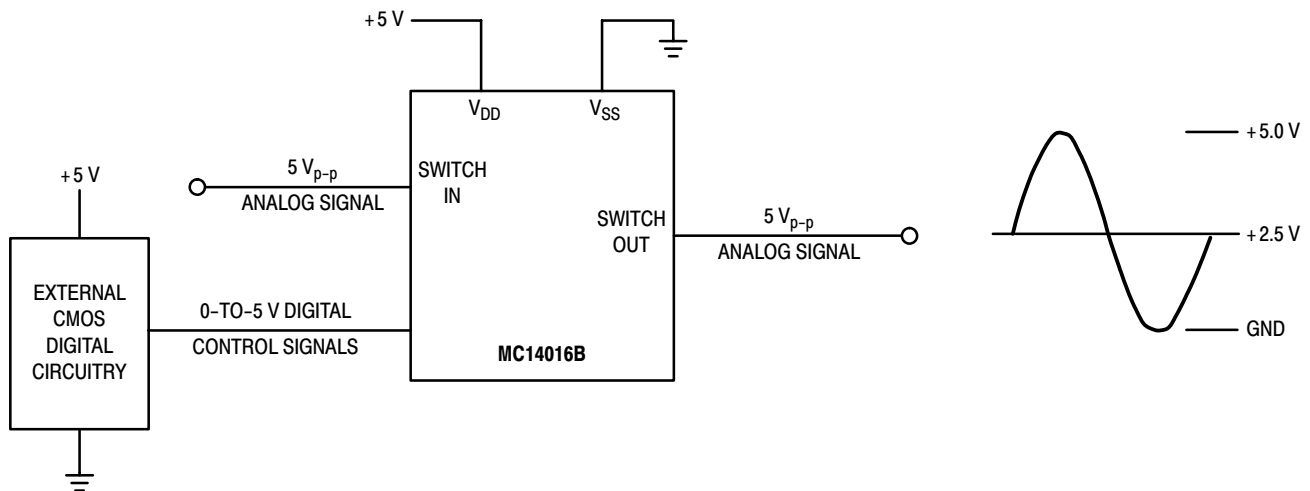
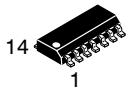


Figure A. Application Example



Figure B. External Germanium or Schottky Clipping Diodes

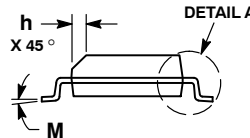
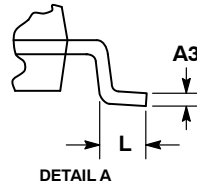
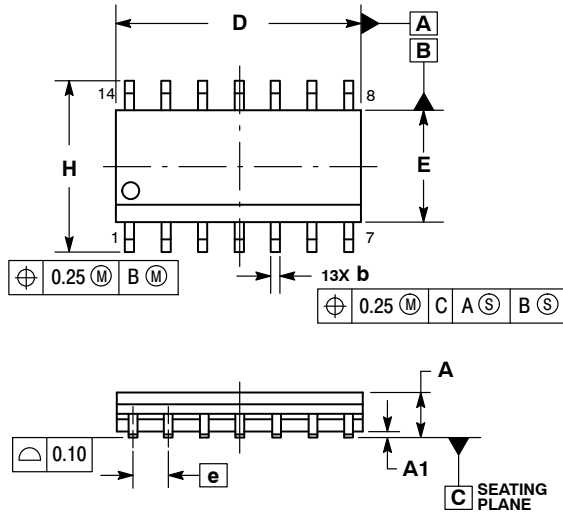
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

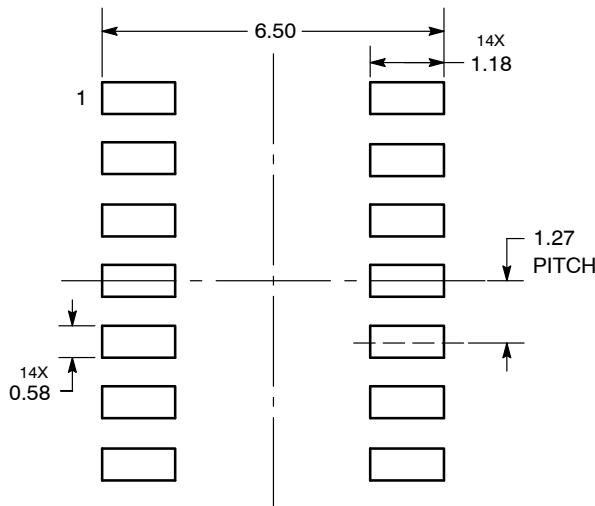


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

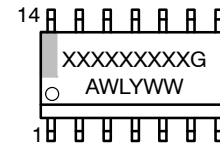
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

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