THE DATASHEET OF

ISO7142CCDBQR

www.win-source.net 0086-755-83957316

ISO7142CC 4242-V_{PK} Small-Footprint and Low-Power Quad Channel Digital Isolator

1 Features

- Maximum Signaling Rate: 50 Mbps (with 5-V Supplies)
- Robust Design With Integrated Noise Filter
- Low-Power Consumption, Typical I_{CC} per Channel (with 3.3-V Supplies):
  - 1.3 mA at 1 Mbps, 2.5 mA at 25 Mbps
- Wide Temperature Range: –55°C to 125°C
- 50 kV/µs Transient Immunity, Typical
- Long Life with SiO_2 Isolation Barrier
- Operates From 2.7-V, 3.3-V and 5-V Supply
- 2.7-V to 5.5-V Level Translation
- Small QSOP-16 Package
- Safety and Regulatory Approvals
  - 2500-V_{RMS} Isolation for 1 Minute per UL 1577
  - 4242-V_{PK} Isolation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards
  - CQC Certification per GB4943.1-2011

2 Applications

- General Purpose Isolation
- Industrial Automation
- Motor Control
- Solar Inverters

3 Description

ISO7142CC provides galvanic isolation up to 2500-V_{RMS} for 1 minute per UL and 4242-V_{PK} per VDE. ISO7142CC is a quad-channel isolator with two forward and two reverse-direction channels. This device is capable of maximum data rate of 50 Mbps with 5-V supplies and 40 Mbps with 3.3-V or 2.7-V supplies. ISO7142CC has integrated filters on the inputs to support noise-prone applications.

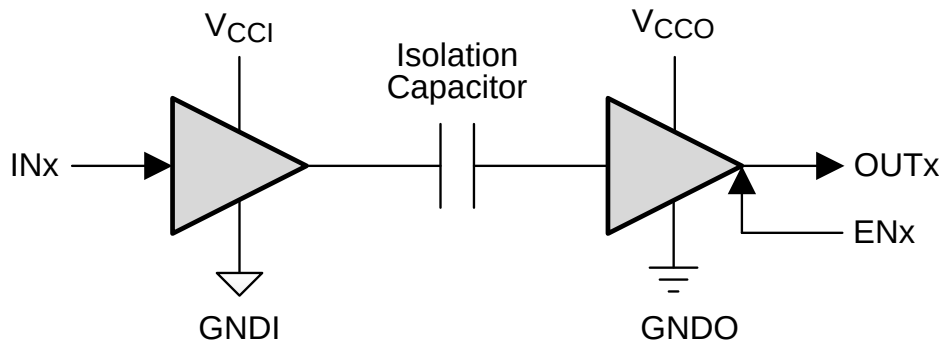
Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, this device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. This device has TTL input thresholds and can operate from 2.7-V, 3.3-V, and 5-V supplies.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7142CC	SSOP (16)	4.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



(1) V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

(2) V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2013) to Revision B	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed VDE Standard to DIN V VDE V 0884-10 (VDE V 0884-10)2006-12	1

Changes from Original (September 2013) to Revision A	Page
• Deleted the MIN value of –55°C from T_J in the RECOMMENDED OPERATING CONDITIONS table	4
• Changed the TYP value of C_I From: 3.5 To: 2 pF in the INSULATION AND SAFETY-RELATED SPECIFICATIONS table	13
• Changed the CSA column description for Basic Insulation	14
• Changed Figure 13	15

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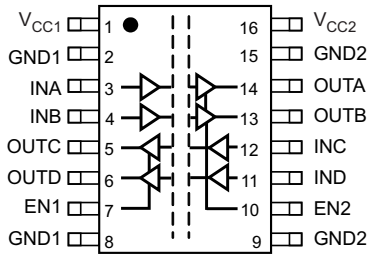
5 Pin Configuration and Functions

DBQ Package
16-Pin SSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2,8	—	Ground connection for V_{CC1}
GND2	9,15	—	Ground connection for V_{CC2}
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	12	I	Input, channel C
IND	11	I	Input, channel D
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	5	O	Output, channel C
OUTD	6	O	Output, channel D
V_{CC1}	1	—	Power supply, V_{CC1}
V_{CC2}	16	—	Power supply, V_{CC2}

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6 Specifications

6.1 Absolute Maximum Ratings[(1)]

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage[(2)]	–0.5	6	V
V	Voltage at INx, OUTx, ENx	–0.5	V_{CC} + 0.5[(3)]	V
I_O	Output current	-15	15	mA
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	2.7		5.5	V
I_{OH}	High-level output current (V_{CC} ≥ 3.0 V)	–4			mA
	High-level output current (V_{CC} < 3.0 V)	–2			
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V
t_{ui}	Input pulse duration (V_{CC} ≥ 4.5V)	20			ns
	Input pulse duration (V_{CC} < 4.5V)	25			
1 / t_{ui}	Signaling rate (V_{CC} ≥ 4.5V)	0		50	Mbps
	Signaling rate (V_{CC} < 4.5V)	0		40	
T_J	Junction temperature			136	°C
T_A	Ambient temperature	–55	25	125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		ISO7142CC DBQ (SSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	57.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics, 5 V

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 8	V_{CCO} (1) – 0.5			V
		I_{OH} = –20 µA; see Figure 8	V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 8			0.4	V
		I_{OL} = 20 µA; see Figure 8			0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			480		mV
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 11	25	70		kV/µs

(1) V_{CCI}= Supply voltage for the input channel; V_{CCO} = Supply voltage for the output channel

6.6 Electrical Characteristics, 3.3 V

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 8	V_{CCO} (1) – 0.5			V
		I_{OH} = –20 µA; see Figure 8	V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 8			0.4	V
		I_{OL} = 20 µA; see Figure 8			0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			460		mV
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 11	25	50		kV/µs

(1) V_{CCI}= Supply voltage for the input channel; V_{CCO} = Supply voltage for the output channel

6.7 Electrical Characteristics, 2.7 V

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 8	V_{CCO} (1) – 0.3			V
		I_{OH} = –20 µA; see Figure 8	V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 8			0.4	V
		I_{OL} = 20 µA; see Figure 8			0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			360		mV
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 11	25	45		kV/µs

(1) V_{CCI}= Supply voltage for the input channel; V_{CCO} = Supply voltage for the output channel

6.8 Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device power dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF Input a 25-MHz, 50% duty cycle square wave			170	mW

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6.9 Switching Characteristics, 5 V

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 8	15	21	38	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	See Figure 8			3.5	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction channels			1.5	ns
		Opposite-direction channels			6.5	
$t_{sk(pp)}$ (3)	Part-to-part skew time				14	ns
t_r	Output signal rise time	See Figure 8		2.5		ns
t_f	Output signal fall time	See Figure 8		2.1		ns
t_{PHZ}, t_{PLZ}	Disable propagation delay, high/low-to-high impedance output	See Figure 9		7	12	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	See Figure 9		6	12	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output	See Figure 9		12	23	us
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 10		8		µs
t_{GR}	Input glitch rejection time			9.5		ns

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals, and loads.

6.10 Switching Characteristics, 3.3 V

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 8	16	25	46	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	See Figure 8			3	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			2	ns
		Opposite-direction Channels			6.5	
$t_{sk(pp)}$ (3)	Part-to-part skew time				21	ns
t_r	Output signal rise time	See Figure 8		3		ns
t_f	Output signal fall time	See Figure 8		2.5		ns
t_{PHZ}, t_{PLZ}	Disable propagation delay, from high/low to high-impedance output	See Figure 9		9	14	ns
t_{PZH}	Enable propagation delay, from high-impedance to high output	See Figure 9		9	17	ns
t_{PZL}	Enable propagation delay, from high-impedance to low output	See Figure 9		12	24	us
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 10		7		µs
t_{GR}	Input glitch rejection time			11		ns

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.11 Switching Characteristics, 2.7 V

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 8	18	28	50	ns
PWD (1)	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$	See Figure 8			3	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			3	ns
		Opposite-direction Channels			8.5	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				24	ns
t_r	Output signal rise time	See Figure 8		3.5		ns
t_f	Output signal fall time	See Figure 8		2.8		ns
t_{PHZ}, t_{PLZ}	Disable propagation delay, from high/low to high-impedance output	See Figure 9		10	15	ns
t_{PZH}	Enable propagation delay, from high-impedance to high output	See Figure 9		10	19	ns
t_{PZL}	Enable propagation delay, from high-impedance to low output	See Figure 9		12	23	us
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 10		7		µs
t_{GR}	Input glitch rejection time			12		ns

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals, and loads.

6.12 Supply Current, 5 V

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0 V		0.8	1.6	mA
I_{CC1} , I_{CC2}	DC to 1 Mbps	DC Signal: $V_I = V_{CCI}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		3.3	5	
I_{CC1}, I_{CC2}	10 Mbps			4.9	7	
I_{CC1}, I_{CC2}	25 Mbps			7.3	10	
I_{CC1}, I_{CC2}	50 Mbps			11.1	14.5	

6.13 Supply Current, 3.3 V

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0 V		0.5	1	mA
I_{CC1}, I_{CC2}	DC to 1 Mbps	DC signal: $V_I = V_{CCI}$ or 0 V AC signal: All channels switching with square-wave clock input; C_L = 15 pF		2.5	4	
I_{CC1}, I_{CC2}	10 Mbps			3.5	5	
I_{CC1}, I_{CC2}	25 Mbps			5	7	
I_{CC1}, I_{CC2}	40 Mbps			6.5	10	

6.14 Supply Current, 2.7 V

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted.)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0 V		0.4	0.8	mA
I_{CC1}, I_{CC2}	DC to 1 Mbps	DC signal: $V_I = V_{CCI}$ or 0 V AC signal: All channels switching with square-wave clock input; C_L = 15 pF		2.2	3.5	
I_{CC1}, I_{CC2}	10 Mbps			3	4.2	
I_{CC1}, I_{CC2}	25 Mbps			4.2	5.5	
I_{CC1}, I_{CC2}	40 Mbps			5.4	7.5	

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6.15 Typical Characteristics

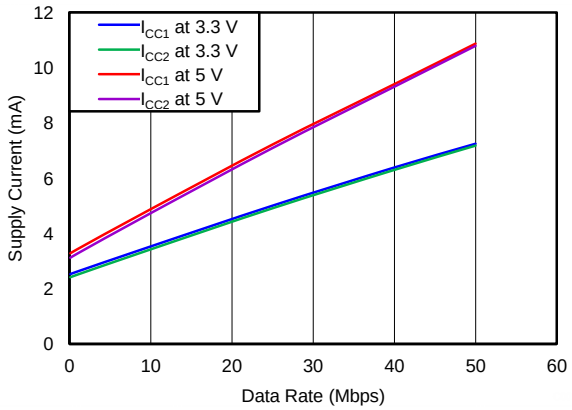

Figure 1. ISO7142 Supply Current for All Channels vs Data Rate

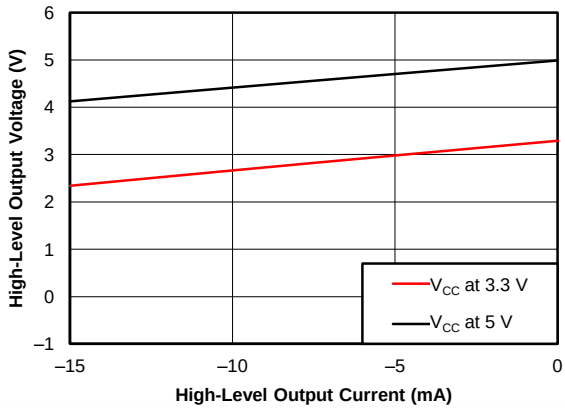

Figure 2. High-Level Output Voltage vs High-Level Output Current

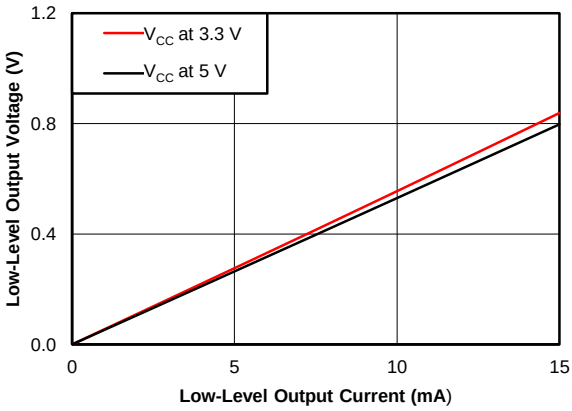

Figure 3. Low-Level Output Voltage vs Low-Level Output Current

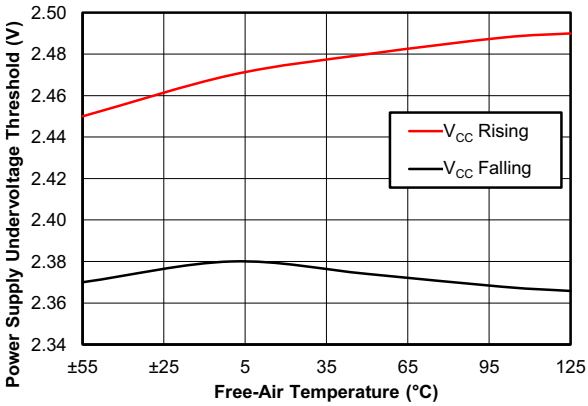

Figure 4. V_{CC} Undervoltage Threshold vs Free-Air Temperature

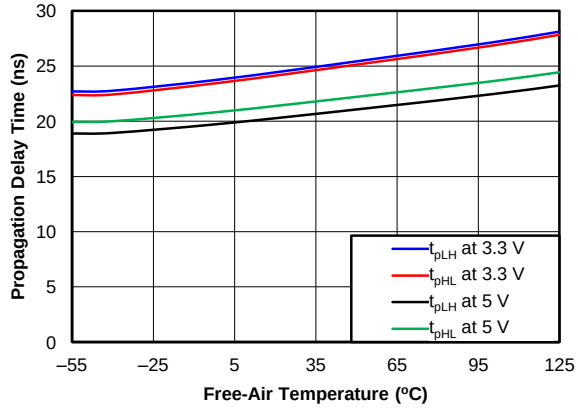

Figure 5. Propagation Delay Time vs Free-Air Temperature

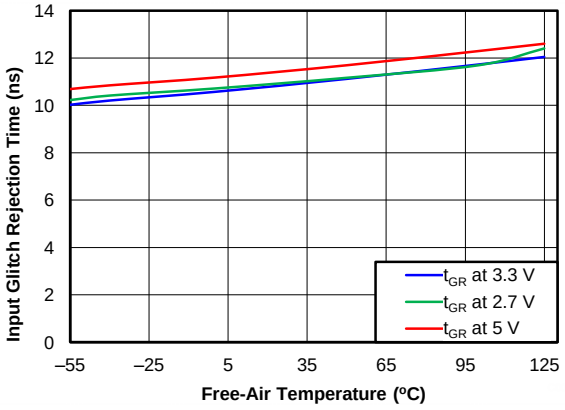

Figure 6. Input Glitch Rejection Time vs Free-Air Temperature

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Typical Characteristics (continued)

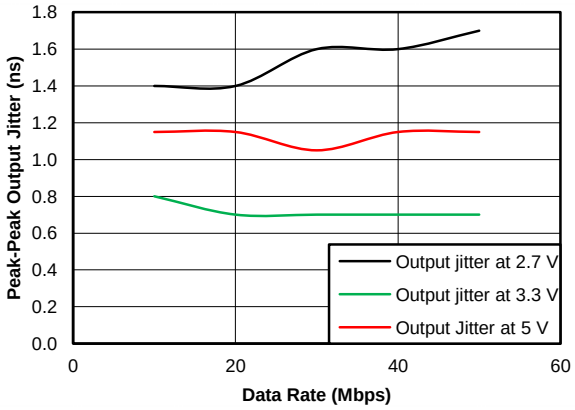
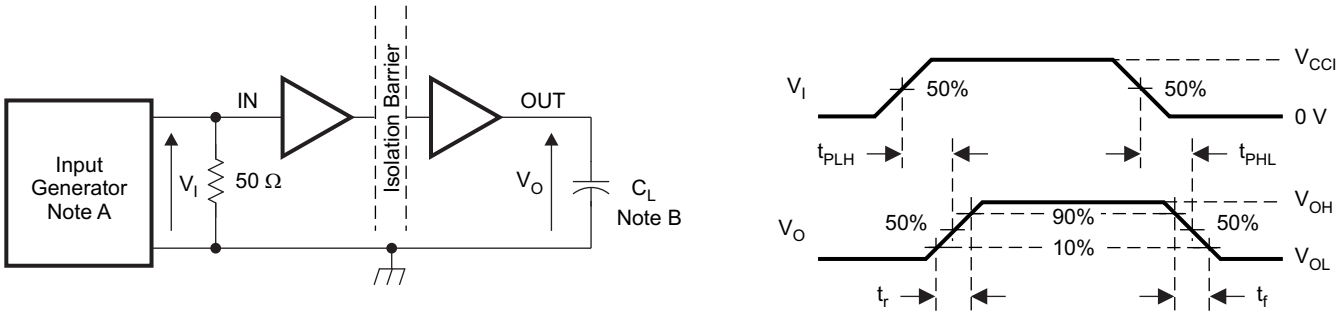


Figure 7. Peak-Peak Output Jitter vs Data Rate

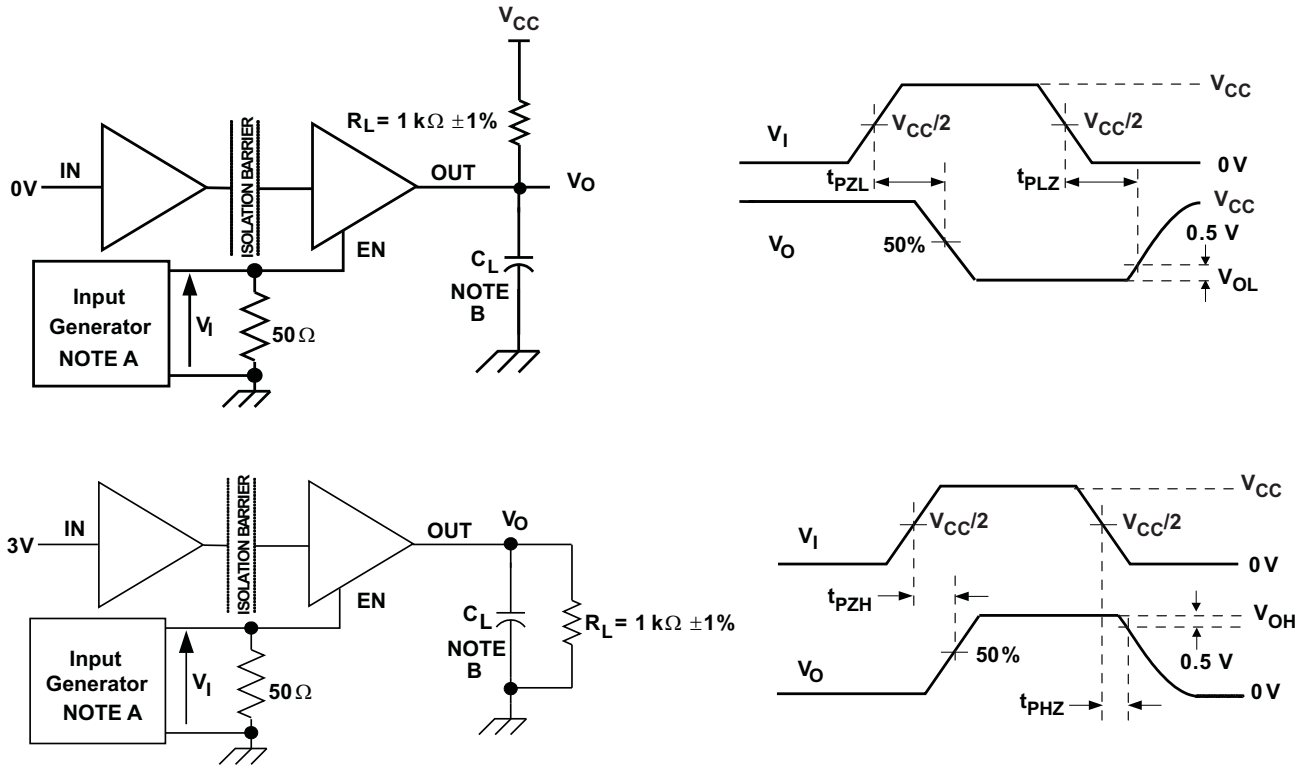
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate the input-generator signal. It is not needed in an actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 8. Switching-Characteristics Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 9. Enable/Disable Propagation Delay-Time Test Circuit and Waveform

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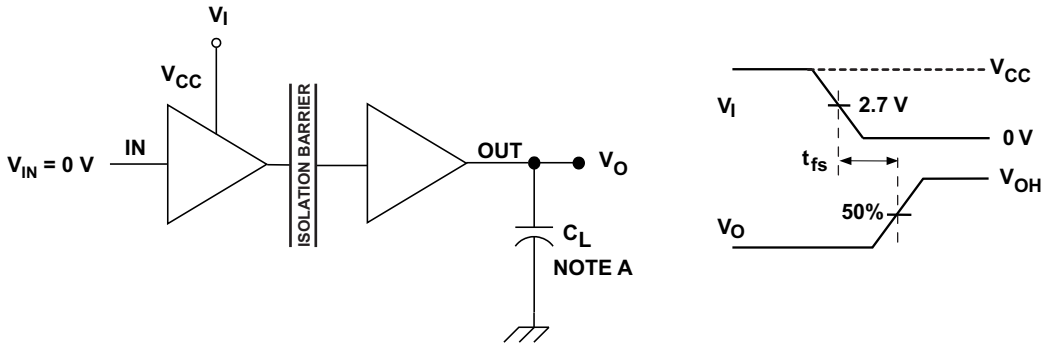
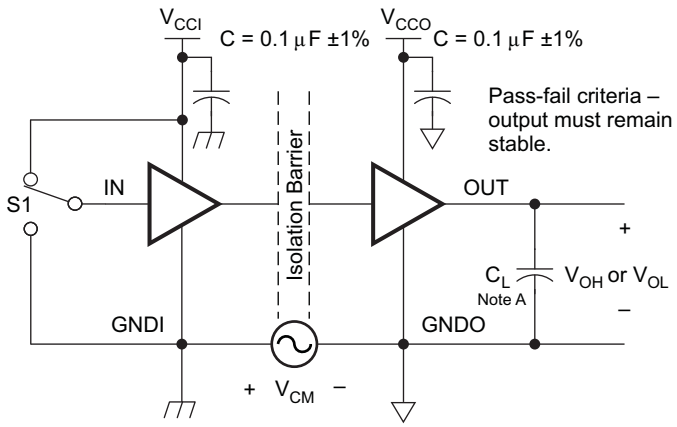
Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 10. Failsafe Delay-Time Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 11. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The isolator in Figure 12 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 50 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal through the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.2 Functional Block Diagram

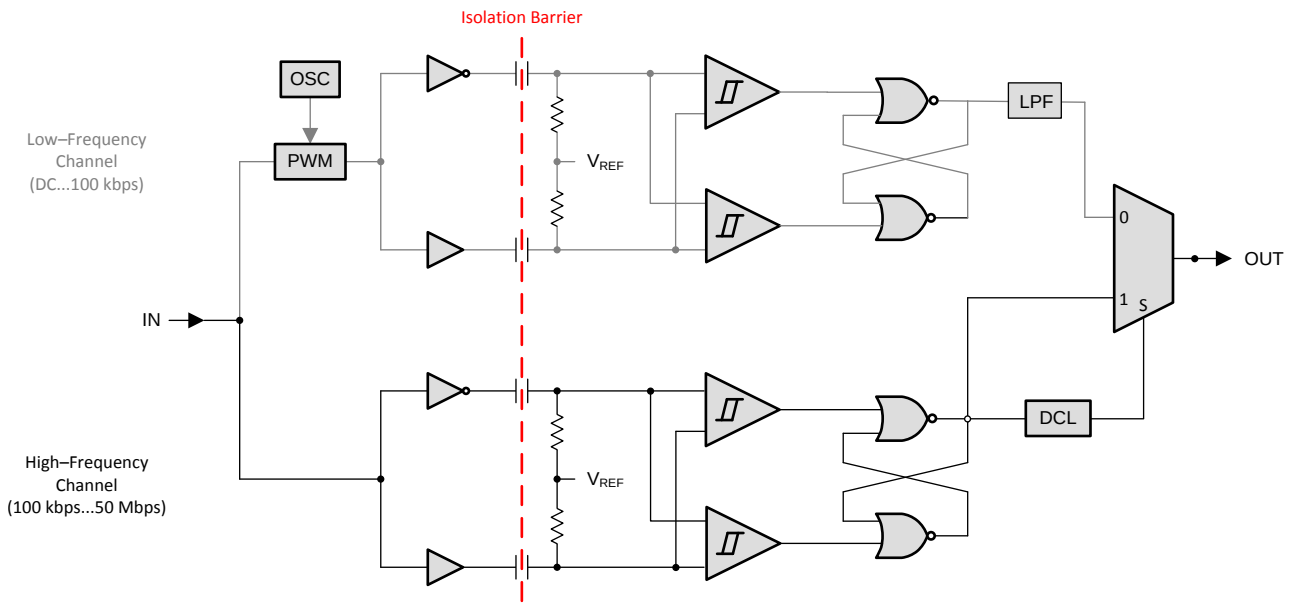


Figure 12. Conceptual Block Diagram of a Digital Capacitive Isolator

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8.3 Feature Description

8.3.1 Insulation and Safety-Related Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.014			mm
C_I (1)	Input capacitance	$V_I = V_{CC}/2 + 0.4 \sin(2\pi ft)$, f = 1 MHz, V_{CC} = 5 V		2		pF
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12						
V_{IOTM}	Maximum transient isolation voltage				4242	V_{PK}
V_{IORM}	Maximum working isolation voltage				566	V_{PK}
V_{PR}	Input-to-output test voltage	After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC			679	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 s, Partial discharge < 5 pC			906	
		Method b1, 100% production test, $V_{PR} = V_{IORM}$ x 1.875, t = 1 s, Partial discharge < 5 pC			1061	
L(I01)	Minimum air gap (clearance)	Shortest terminal to terminal distance through air	3.7			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal to terminal distance across the package surface	3.7			mm
	Pollution degree			2		
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112	≥400			V
R_{IO} (2)	Isolation resistance, input to output	V_{IO} = 500 V, T_A = 25°C		>10^{12}		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C		>10^{11}		
		V_{IO} = 500 V, T_S = 150°C		>10^{9}		
C_{IO} (2)	Barrier capacitance, input to output	$V_I = 0.4 \sin(2\pi ft)$, f = 1 MHz		2.4		pF
UL 1577						
V_{ISO}	Withstanding Isolation voltage	$V_{TEST} = V_{ISO}$= 2500 V_{RMS}, 60 sec (qualification); V_{TEST} = 1.2 * V_{ISO}= 3000 V_{RMS}, 1 sec (100% production)			2500	V_{RMS}

(1) Measured from input data pin to ground.
(2) All pins on each side of the barrier tied together creating a two-terminal device.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Material Group		II
Installation classification / Overvoltage Category for Basic Insulation	Rated mains voltage ≤ 150 V_{RMS}	I–IV
	Rated mains voltage ≤ 300 V_{RMS}	I–III

8.3.2 Regulatory Information

VDE	UL	CSA	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Certified under UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1	Certified according to GB 4943.1-2011
Basic Insulation; Maximum transient Isolation IsolatiIsolationvoltage, 4242 V_{PK} Maximum working isolation voltage, 566 V_{PK}	Single protection, 2500 V_{RMS} (1)	3000 V_{RMS} Isolation rating; 185 V_{RMS} Reinforced Insulation and 370 V_{RMS} Basic Insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2; 150 V_{RMS} Reinforced Insulation and 300 V_{RMS} Basic Insulation per CSA 61010-1-12 and IEC 61010-1 3rd Ed.	Basic Insulation, Altitude ≤ 5000m, Tropical climate, 250 V_{RMS} maximum working voltage.
File number: 40016131	File number: E181974	Master contract number: 220991	Certificate number: CQC14001109540

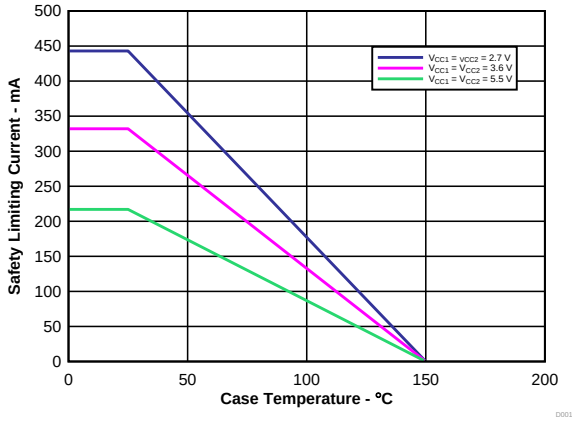
(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

8.3.3 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DBQ-16	θ_{JA} = 104.5°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			217	mA
			θ_{JA} = 104.5°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			332	
			θ_{JA} = 104.5°C/W, V_I = 2.7V, T_J = 150°C, T_A = 25°C			443	
T_S	Maximum safety temperature					150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.



NOTE: Thermal Derating Curve for Safety Limiting Current per VDE

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8.4 Device Functional Modes

Table 2. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)
PU	PU	H	H or open	H
		L	H or open	L
		X	L	Z
		Open	H or open	H
PD	PU	X	H or open	H
PD	PU	X	L	Z
X	PD	X	X	Undetermined

(1) V_{CCI} = Input-side Supply Voltage; V_{CCO} = Output-side Supply Voltage; PU = Powered Up (V_{CC} ≥ 2.7 V); PD = Powered Down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance

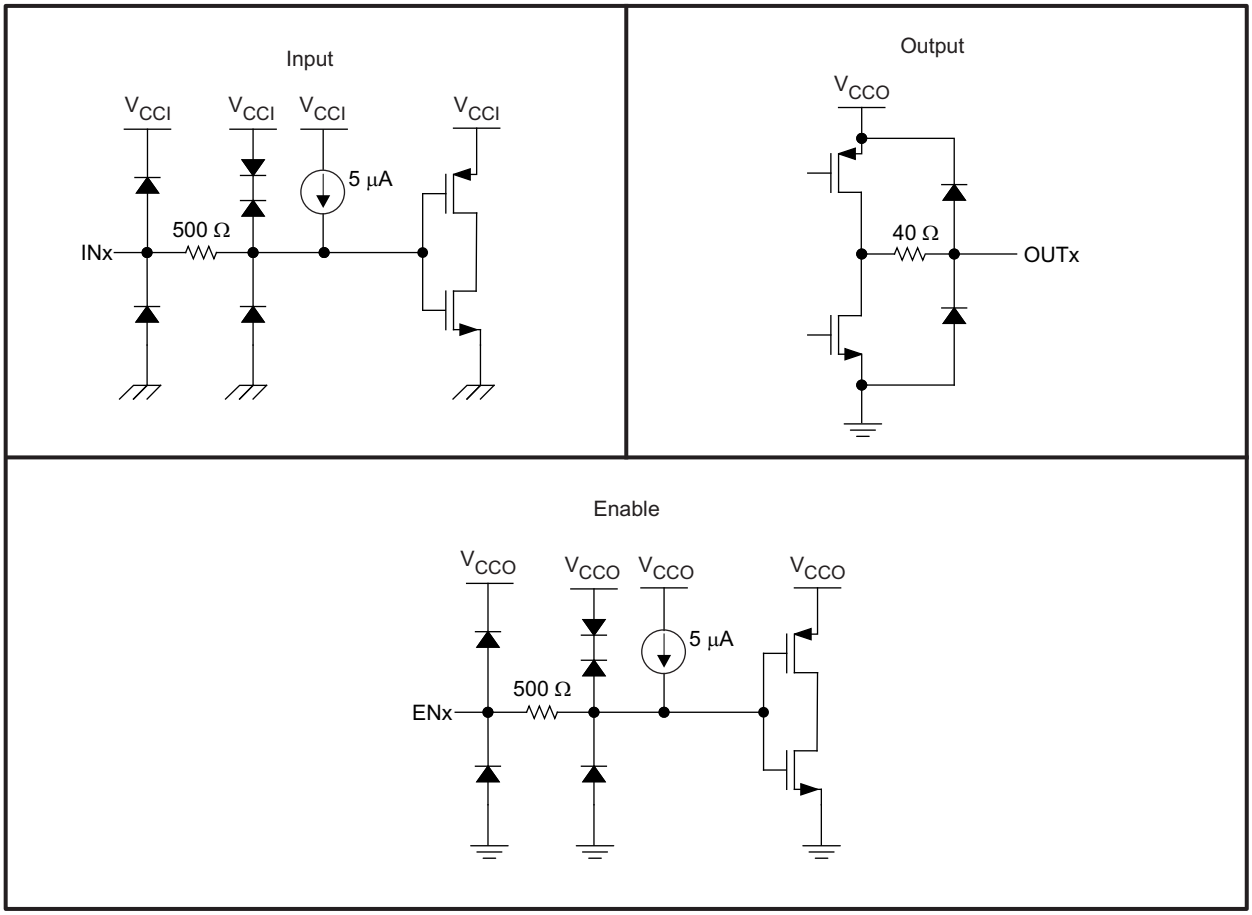

Figure 13. Device I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ISO7142CC uses single-ended TTL-logic switching technology. Its supply voltage range is from 2.7 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to note that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

Typical isolated RS-232 interface implementation is shown in Figure 14.

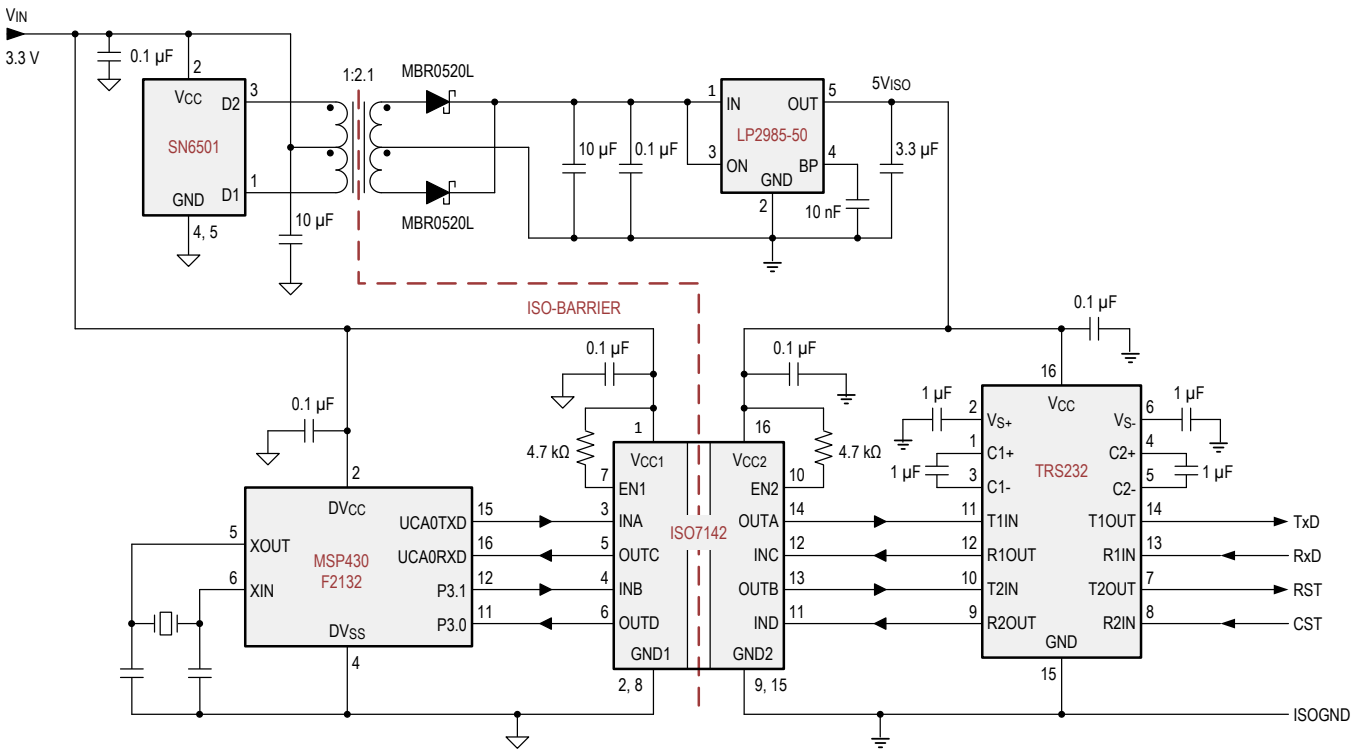

Figure 14. Typical Isolated RS-232 Application Circuit for ISO7142

9.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, ISO7142CC only requires two external bypass capacitors to operate.

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Typical Application (continued)

9.2.2 Detailed Design Procedure

Figure 15 shows the hookup of a typical ISO7142CC circuit. The only external components are two bypass capacitors.

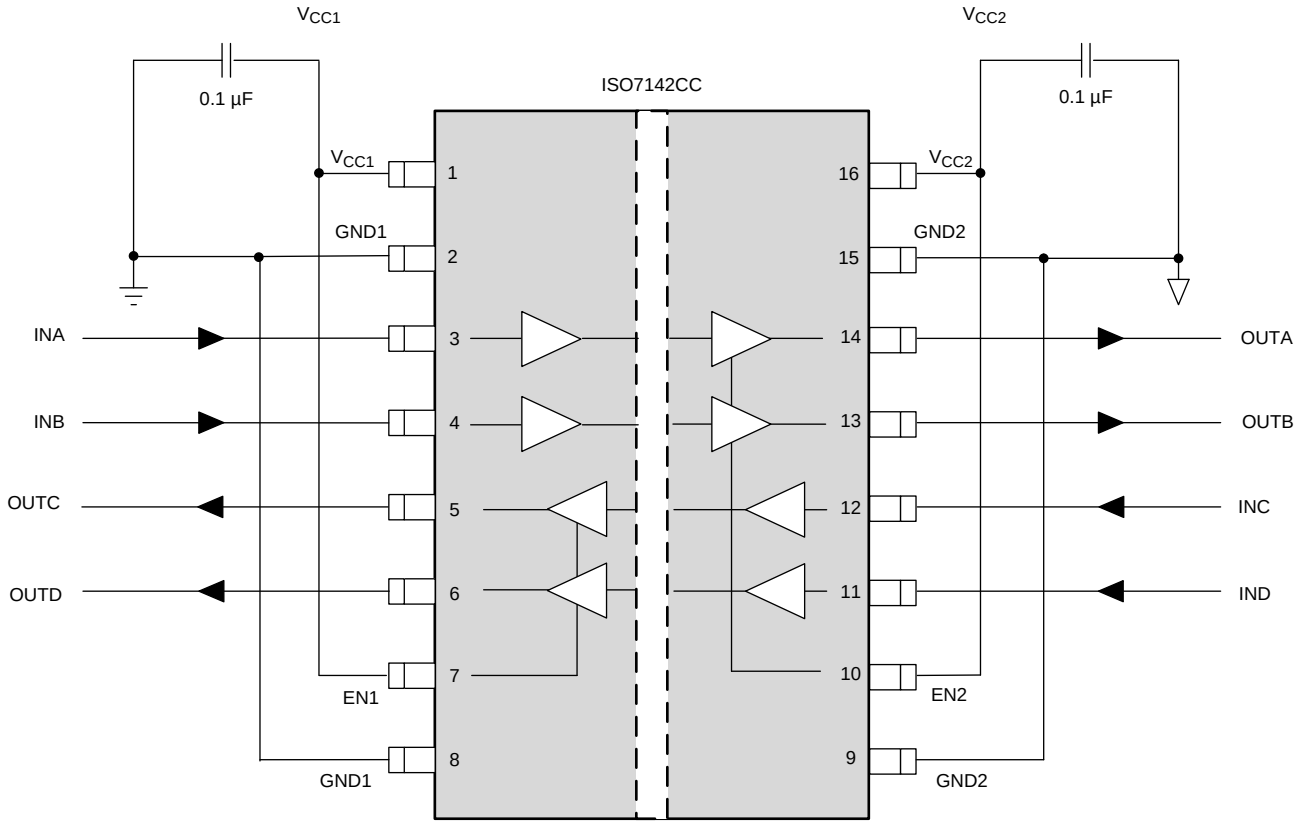

Figure 15. Typical ISO7142CC Circuit Hook-up

Typical Application (continued)

9.2.3 Application Curves

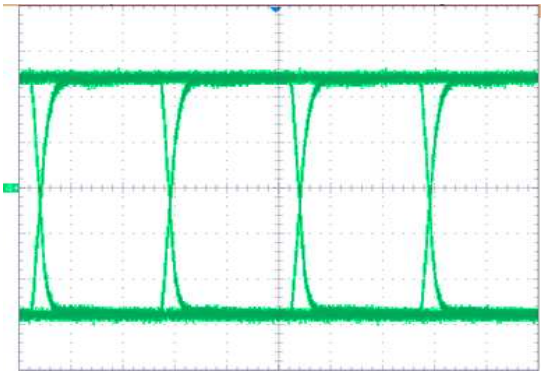

Figure 16. Typical Eye Diagram at 40 Mbps, PRBS 2^{16} - 1, 2.7-V Operation

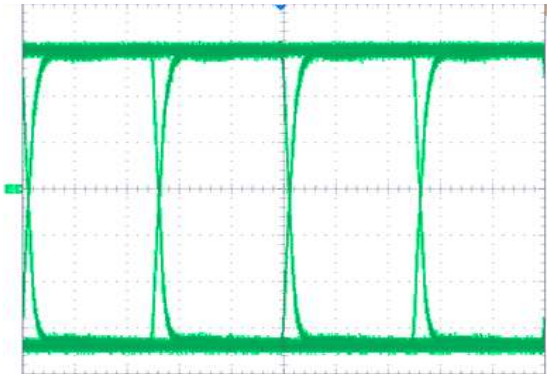

Figure 17. Typical Eye Diagram at 40 Mbps, PRBS 2^{16} - 1, 3.3-V Operation

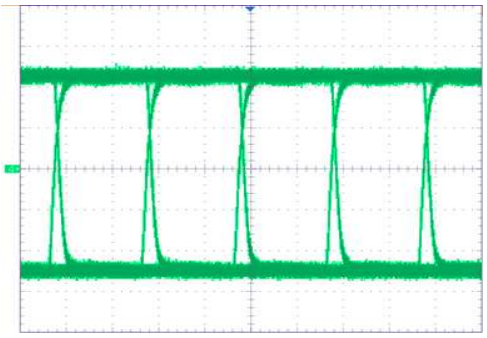

Figure 18. Typical Eye Diagram at 50 Mbps, PRBS 2^{16} - 1, 5-V Operation

10 Power Supply Recommendations

To help ensure reliable operation supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 datasheet (SLLSEA0).

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11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 19). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note, *Digital Isolator Design Guide*, SLLA284.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL 94 V-0 printed circuit board. This is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

11.2 Layout Example

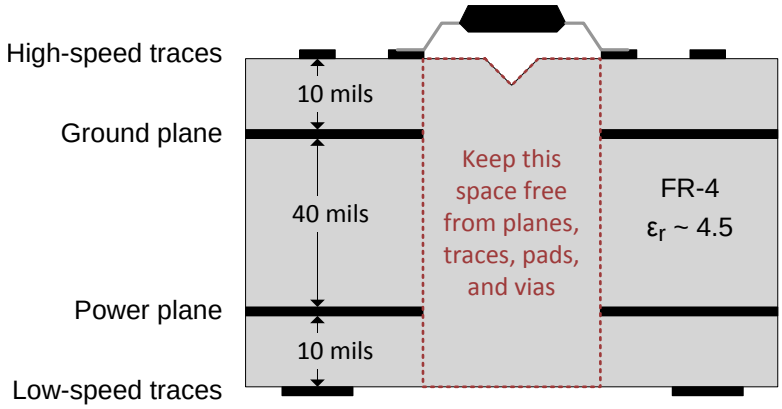

Figure 19. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Transformer Driver for Isolated Power Supplies*, SLLSEA0
- *Digital Isolator Design Guide*, SLLA284
- *Isolation Glossary* , SLLA353

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7142CCDBQ	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7142C	Samples
ISO7142CCDBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7142C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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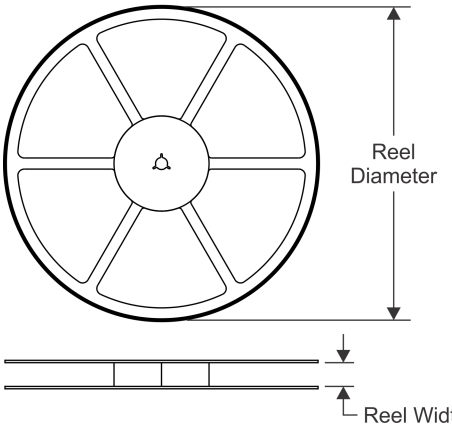
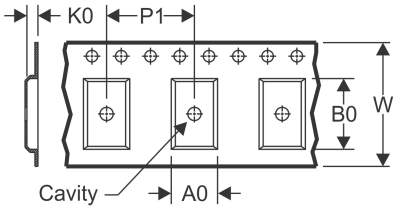
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

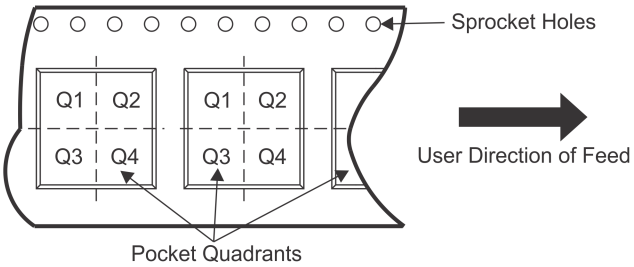


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

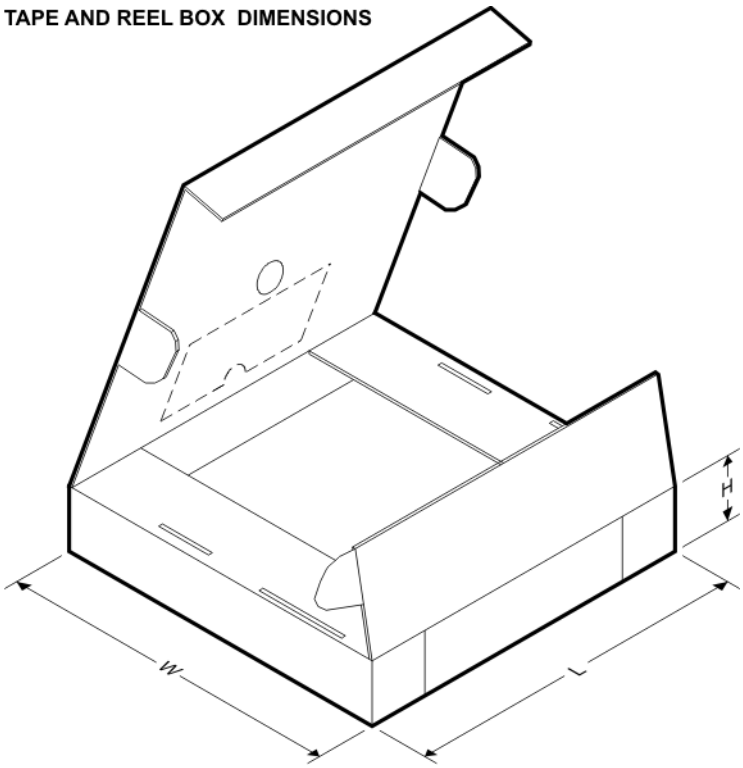
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7142CCDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

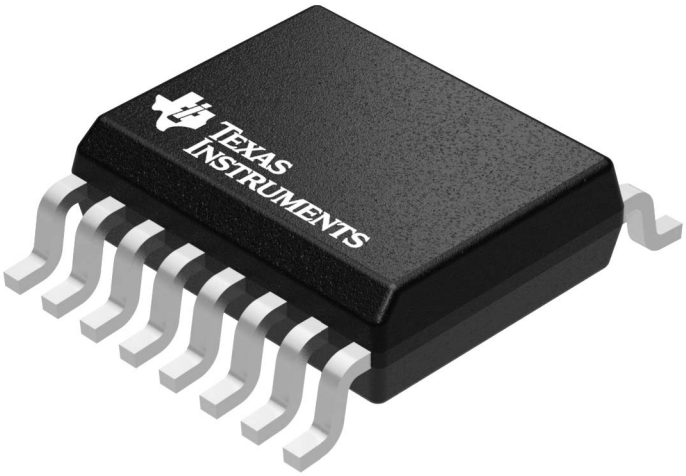


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7142CCDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0

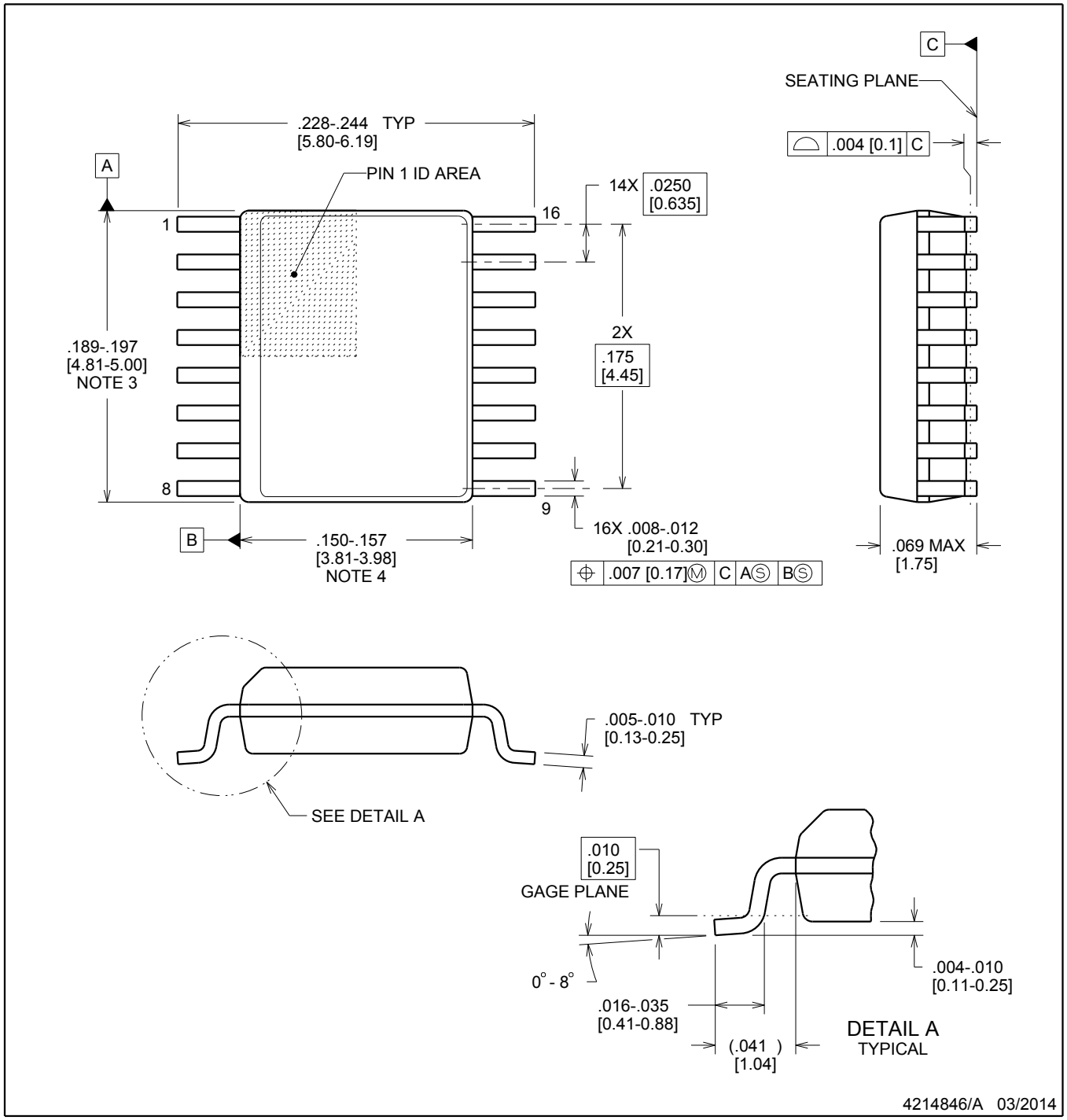
DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



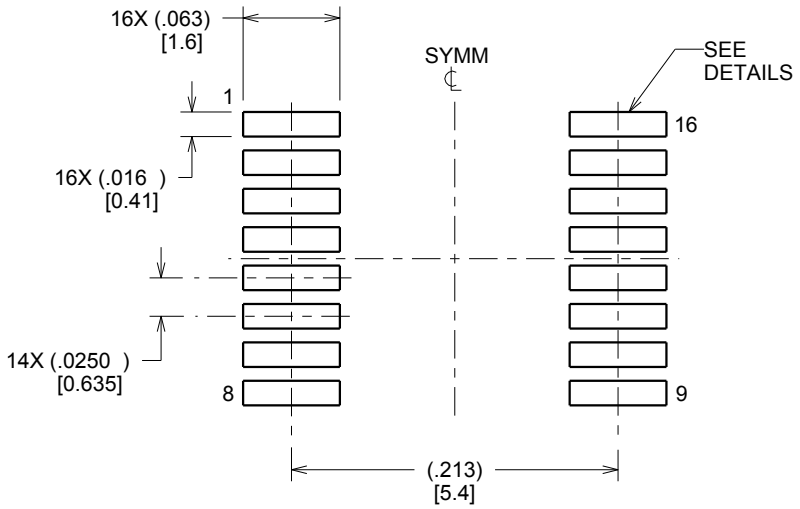
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073301-2/I

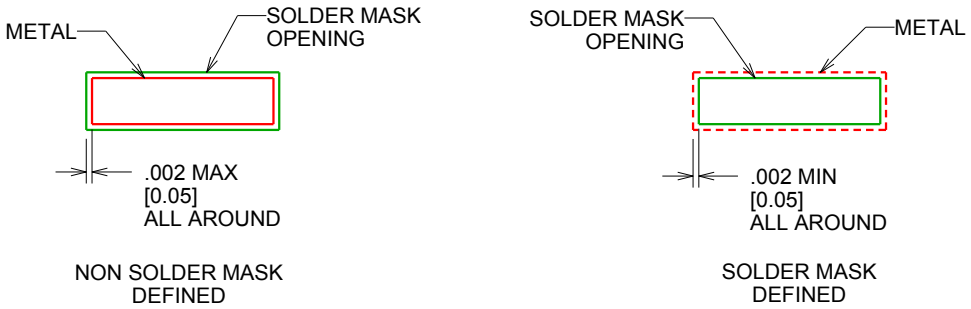


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

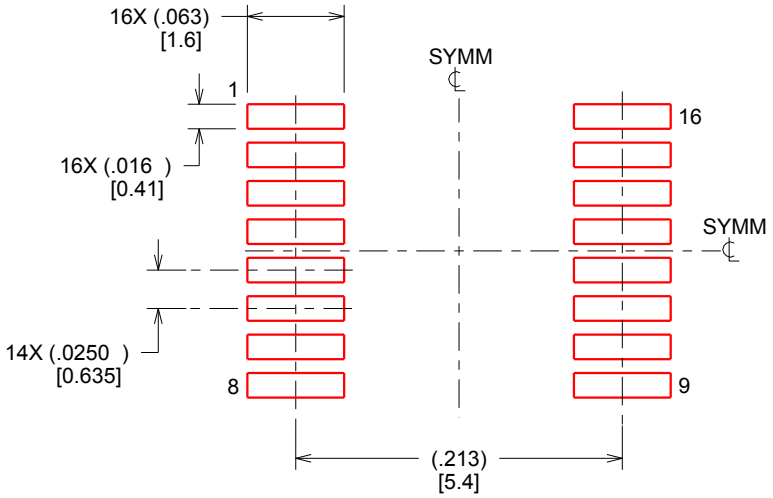


SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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