THE DATASHEET OF

TPS65721RSNR

TPS6572x Power Management IC (PMIC) With Battery Charger, One Step-Down Converter and One LDO

1 Features

- Battery Charger With Power Path Management
- 28-V Rated Power Path With:
  - 100-mA Input Current Limit
  - 500-mA Input Current Limit
- 300-mA Charge Current
- 200-mA Step-Down Converter for TPS65720
- 400-mA Step-Down Converter for TPS65721, TPS657201, TPS657202
- Up to 92% Efficiency
- V_{IN} Range for DCDC Converter From 2.3 V to 5.6 V
- 2.25-MHz Fixed Frequency Operation
- Power Save Mode at Light Load Current
- Output Voltage Accuracy in PWM Mode ±2%
- 100% Duty Cycle for Lowest Dropout
- 1 General Purpose 200-mA LDO
- V_{IN} Range for LDO From 1.8 V to 5.6 V
- I^2C Compatible Interface
- 4GPIOs
- Available in a 25-Ball DSBGA With 0.4-mm Pitch and in 4-mm × 4-mm 32-Pin WQFN Package

2 Applications

- Bluetooth Headsets
- Handheld Equipment
- Wearables, Smart Watches
- Portable Accessories

3 Description

The TPS6572x device is a small power management unit targeted for Bluetooth headsets or other portable low-power consumer-end equipments. The device contains an USB friendly Lithium-Ion battery charger, a highly efficient step-down converter, a low-dropout linear regulator, and additional supporting functions. The device is controlled by an I^2C interface. Several settings can be customized by the use of nonvolatile memory which is factory programmed.

The 2.25-MHz step-down converter enters a low-power mode at light load for maximum efficiency across the widest possible range of load currents. For low-noise applications the devices can be forced into fixed-frequency PWM mode using the I^2C-compatible interface.

The device allows the use of small inductors and capacitors to achieve a small solution size. The TPS65720 provides an output current of up to 200 mA on the DC-DC converter while TPS657201, TPS657202, and TPS65721 provide up to 400 mA. The TPS6572x also integrates one 200-mA LDO. The LDO operates with an input voltage range from 1.8 V to 5.6 V, thus allowing it to be supplied from the output of the step-down converter or directly from the system voltage.

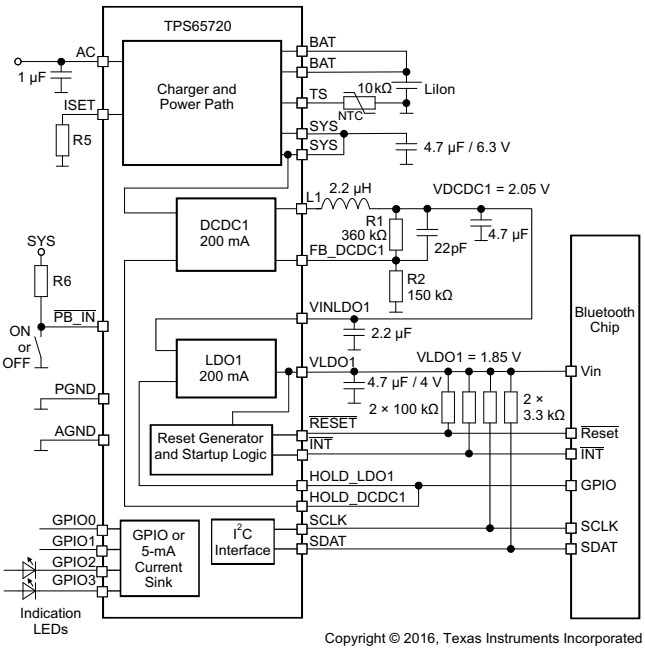
The TPS65720, TPS657201, and TPS657202 come in a small 25-ball 2-mm × 2-mm wafer chip scale package (DSBGA) with 0.4-mm ball pitch or a 4-mm × 4-mm WQFN package with a 0.4-mm pitch (TPS65721).

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65720x	DSBGA (25)	2.11 mm × 2.11 mm
TPS65721	WQFN (32)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2016) to Revision C — **Page**

- Changed the title of the data sheet ... 1
- Changed the *Electrostatic Discharge Caution* statement ... 57

Changes from Revision A (September 2015) to Revision B — **Page**

- Changed *Timer Fault*, To: *Charger Fault*, and Bit <TIMER_FAULT> = 1 To: Bit <CH_FAULT> = 1 ... 24
- *IRMASK0 Register Address: 0Dh (read/write)* , Changed B4 From: M_TIMER_FAULT To: Reserved ... 44
- *IR0 Register Address: 10h (read only)* , Changed B4 From: TIMER_FAULT To: Reserved ... 45
- *IR0 Register Address: 10h (read only)* , Changed B4 From: Rising edge of TIMER_FAULT To: Reserved ... 45

Changes from Original (October 2009) to Revision A — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added the TPS657202 and the TPS65721 devices to the data sheet ... 1

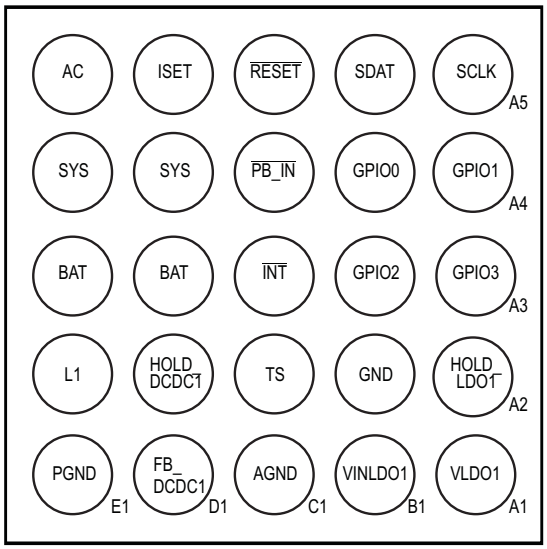
5 Device Options

PART NUMBER(1)	SIZE FOR DSBGA PACKAGE	OPTION
TPS65720	D = 2105 μm ±25 μm E = 2105 μm ±25 μm	DCDC1 externally adjustable LDO1 default 1.85 V AC input current limit = 500 mA
TPS657201	D = 2105 μm ±25 μm E = 2105 μm ±25 μm	DCDC1 default 1.85 V LDO1 default 1.85 V analog multiplexer (TS_OUT) AC input current limit = 500 mA
TPS657202	D = 2105 μm ±25 μm E = 2105 μm ±25 μm	DCDC1 default 1.90 V LDO1 default 2.85 V analog multiplexer (TS_OUT) AC input current limit = 100 mA
TPS65721	—	DCDC1 externally adjustable LDO1 externally adjustable AC input current limit = 500 mA

(1) The RSN and YFF package is available in tape and reel. Add R suffix (TPS65720YFFR; TPS65721RSNR) to order quantities of 3000 parts per reel. Add T suffix (TPS65720YFFT; TPS65721RSNT) to order quantities of 250 parts per reel.

6 Pin Configuration and Functions

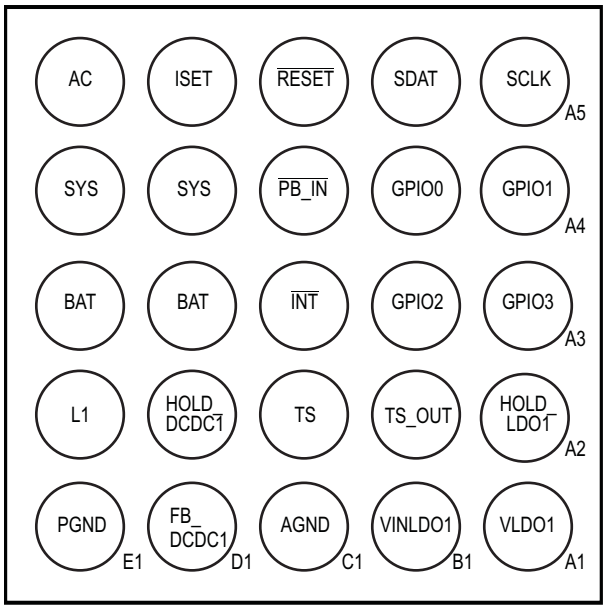
YFF Package
25-Pin DSBGA
Bottom View



Pin Functions—DSBGA (TPS65720)

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	VLDO1	O	Output voltage of LDO1
A2	HOLD_LDO1	I	Power-on input for LDO1. When pulled HIGH, LDO1 is kept enabled after $\overline{\text{PB\_IN}}$ was released HIGH.
A3	GPIO3	I/O	General purpose I/O or 5-mA current sink
A4	GPIO1	I/O	General purpose I/O
A5	SCLK	I	Clock input for the I^2C interface
B1	VINLDO1	I	Input voltage for LDO1
B2	GND	—	Connect to AGND and PGND
B3	GPIO2	I/O	General purpose I/O or 5-mA current sink
B4	GPIO0	I/O	General purpose I/O
B5	SDAT	I/O	Data line for the I^2C interface
C1	AGND	—	Analog ground
C2	TS	I	Connect a thermistor from this pin to GND for battery temperature
C3	$\overline{\text{INT}}$	O	Open-drain interrupt output
C4	$\overline{\text{PB\_IN}}$	I	Push button input; Turns on DCDC1 and LDO1 if pulled to GND.
C5	$\overline{\text{RESET}}$	O	Open-drain output of the reset generator; This output goes active LOW when the output voltage of LDO1 falls 8% below its target voltage.
D1	FB_DCDC1	I	Feedback input of step-down converter
D2	HOLD_DCDC1	I	Power-On input for DCDC1 converter. When pulled HIGH, the DC-DC converter is kept enabled after $\overline{\text{PB\_IN}}$ was released HIGH.
D3	BAT	I/O	Connect to battery + terminal
D4	SYS	O	System voltage; output of the power path manager. Power input for step-down converter DCDC1
D5	ISET	I	Connect a resistor from this pin to GND to set fast charge current
E1	PGND	—	Power ground
E2	L1	O	Switch output of step-down converter
E3	BAT	I/O	Connect to battery + terminal
E4	SYS	O	System voltage; output of the power path manager. Power input for step-down converter DCDC1
E5	AC	I	Input power for power manager, connect to external DC supply.

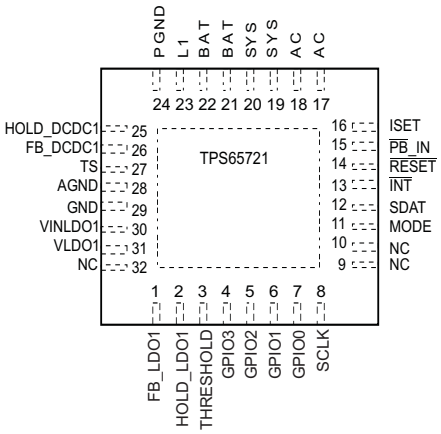
YFF Package
25-Pin DSBGA
Bottom View



Pin Functions—DSBGA (TPS657201, TPS657202)

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	VLDO1	O	Output voltage of LDO1
A2	HOLD_LDO1	I	Power-on input for LDO1. When pulled HIGH, LDO1 is kept enabled after $\overline{\text{PB\_IN}}$ was released HIGH.
A3	GPIO3	I/O	General purpose I/O or 5-mA current sink
A4	GPIO1	I/O	General purpose I/O
A5	SCLK	I	Clock input for the I^2C interface
B1	VINLDO1	I	Input voltage for LDO1
B2	VBAT/TS_OUT	O	Output of battery temperature and battery voltage monitor
B3	GPIO2	I/O	General purpose I/O or 5-mA current sink
B4	GPIO0	I/O	General purpose I/O
B5	SDAT	I/O	Data line for the I^2C interface
C1	AGND	—	Analog ground
C2	TS	I	Connect a thermistor from this pin to GND for battery temperature
C3	$\overline{\text{INT}}$	O	Open-drain interrupt output
C4	$\overline{\text{PB\_IN}}$	I	Push button input; Turns on DCDC1 and LDO1 if pulled to GND.
C5	$\overline{\text{RESET}}$	O	Open-drain output of the reset generator; This output goes active LOW when the output voltage of LDO1 falls 8% below its target voltage.
D1	FB_DCDC1	I	Feedback input of step-down converter
D2	HOLD_DCDC1	I	Power-on input for DCDC1 converter. When pulled HIGH, the DC-DC converter is kept enabled after $\overline{\text{PB\_IN}}$ was released HIGH.
D3	BAT	I/O	Connect to battery + terminal
D4	SYS	O	System voltage; output of the power path manager. Power input for step-down converter DCDC1
D5	ISET	I	Connect a resistor from this pin to GND to set fast charge current
E1	PGND	—	Power ground
E2	L1	O	Switch output of step-down converter
E3	BAT	I/O	Connect to battery + terminal
E4	SYS	O	System voltage; output of the power path manager. Power input for step-down converter DCDC1
E5	AC	I	Input power for power manager, connect to external DC supply.

RSN Package
32-Pin WQFN With Thermal Pad
Top View



Pin Functions—WQFN (TPS65721)

PIN		I/O	DESCRIPTION
NAME	NO.		
AC	17, 18	I	Input power for power manager, connect to external DC supply.
AGND	28	—	Analog ground
BAT	21, 22	I/O	Connect to battery + terminal
FB_DCDC1	26	I	Feedback input of step-down converter
FB_LDO1	1	I	Feedback input for LDO1
GND	29	—	Connect to AGND and PGND
GPIO0	7	I/O	General purpose I/O
GPIO1	6	I/O	General purpose I/O
GPIO2	5	I/O	General purpose I/O or 5-mA current source
GPIO3	4	I/O	General purpose I/O or 5-mA current source
HOLD_DCDC1	25	I	Power-on input for DCDC1 converter. When pulled HIGH, the DC-DC converter is kept enabled after $\overline{\text{PB\_IN}}$ was released HIGH.
HOLD_LDO1	2	I	Power-on input for LDO1. When pulled HIGH, LDO1 is kept enabled after $\overline{\text{PB\_IN}}$ was released HIGH.
$\overline{\text{INT}}$	13	O	Open-drain interrupt output
ISET	16	I	Connect a resistor from this pin to GND to set fast charge current
L1	23	O	Switch output of step-down converter
MODE	11	I	Pull HIGH to force the DCDC1 converter to PWM mode.
$\overline{\text{PB\_IN}}$	15	I	Push button input; Turns on DCDC1 and LDO1 if pulled to GND.
PGND	24	—	Power ground
$\overline{\text{RESET}}$	14	O	Open-drain output of the reset generator; This output goes active LOW when the input voltage at pin THRESHOLD falls below the threshold voltage.
SCLK	8	I	Clock input for the I^2C interface
SDAT	12	I/O	Data line for the I^2C interface
SYS	19, 20	O	System voltage; output of the power path manager. Power input for step-down converter DCDC1
THRESHOLD	3	I	Input voltage to the reset comparator. When the input voltage falls below the threshold, the $\overline{\text{RESET}}$ output is actively pulled LOW.
TS	27	I	Connect a thermistor from this pin to GND for battery temperature
VINLDO1	30	I	Input voltage for LDO1
VLDO1	31	O	Output voltage from LDO1
ThermalPad	—	—	Connect to GND

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	All pins except A/PGND, AC, GPIOx pins with respect to AGND	–0.3	7	V
	GPIOx pins with respect to AGND	–0.3	VSYS	V
	AC pin with respect to AGND	–0.3	28	V
Voltage range on pin VLDO1, FB_LDO1, TS_OUT, TS with respect to AGND		–0.3	3.6	V
Current	AC, BAT, SYS, L1, VLDO1, VINLDO1, PGND		600	mA
	GPIOx, AGND		20	mA
	All other pins		3	mA
Continuous total power dissipation		See *Dissipation Ratings*		
Operating free-air temperature, T_A		–40	85	°C
Maximum junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{AC}	Input voltage at AC pin	4.35		28	V
V_{SYS}	Voltage at SYS pin	2.2		5.6	V
I_{INUSB}	Input current at AC			500	mA
I_{OUTSYS}	Output current at SYS			400	mA
I_{BAT}	Average current into and out of BAT pin			300	mA
$V_{INDCDC1}$	Input voltage for step-down converter DCDC1	2.3		5.6	V
V_{DCDC1}	Output voltage for DCDC1 step-down converter; externally adjustable	0.6		$V_{INDCDC1}$	V
$I_{OUTDCDC1}$	Output current at L			400	mA
L	Inductor at L(1)	2.2	3.3	4.7	µH
V_{INLDO1}	Input voltage for LDO1	1.8		VSYS	V
V_{LDO1}	Output voltage for LDO1	0.8		3.3	V
I_{LDO1}	Output current at LDO1			200	mA
C_{INAC}	Input capacitor at AC(1)	0.1		1	µF
C_{BAT}	Capacitor at BAT(1)	0.1		4.7	µF
C_{SYS}	Capacitor at SYS(1)	4.7		10	µF
$C_{INDCDC1}$	Input capacitor at $V_{INDCDC1}$(1); if connected to SYS, only one 4.7-µF capacitor required for SYS and CINDCDC1	4.7			µF
$C_{OUTDCDC1}$	Output capacitor at V_{DCDC1}(1)	4.7	10	22	µF
C_{INLDO1}	Input capacitor at VINLDO1(1)	2.2			µF
$C_{OUTLDO1}$	Output capacitor at LDO1(1)	2.2			µF

(1) See *Application and Implementation* for more details.

Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
R_{ISET}	Minimum R_{ISET} value for proper operation; lower values may trigger the short circuit protection on ISET	700			Ω
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPS65720 YFF (DSBGA) 25 PINS	TPS65721 RSN (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	37.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	28.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.3	8.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.3	8.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{SYS} = 3.6 V, V_{DCDC1} = 2.05 V, PFM mode, L = 3.3 µH, $C_{OUTDCDC1}$ = 4.7 µF, V_{INLDO1} = 2.05 V, V_{LDO1} = 1.85 V, T_A = –40°C to 85°C typical values apply in a temperature range of 10°C to 35°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Operating quiescent current when only DCDC1 converter is enabled	DCDC1 enabled, IOUT = 0 mA. PFM mode enabled; device not switching		36	45	µA
		DCDC1 enabled, IOUT = 0 mA. PWM mode		2.8		mA
I_Q	Operating quiescent current when LDO1 and DCDC1 are enabled	Current into BAT pin (PFM mode)		33	50	µA
		Current into VINLDO1		13	18	µA
I_{SD}	Shutdown current after voltage was applied to BAT but device never enabled before (shipping mode)	For VINLDO1 = 0 V (LDO1 supplied by DCDC1); powered by VBAT = 3.6 V		4	13	µA
	Shutdown current after first power-up	For VINLDO1 = 0 V (LDO1 supplied by DCDC1); powered by VBAT = 3.6 V		12	17	µA
	Shutdown current after first power-up	For VINLDO1 ≠ 0 V (LDO1 supplied by SYS); powered by VBAT = 3.6 V		12	18	µA
SDAT, SCLK, $\overline{PB\_IN}$, HOLD, GPIO0 TO GPIO3, $\overline{INT}$, $\overline{RESET}$, THRESHOLD						
V_{IH}	High-level input voltage for SCLK, SDAT, GPIOx, HOLD_DCDC1, HOLD_LDO1, $\overline{PB\_IN}$	GPIOs configured as input	1.2		VSYS	V
V_{IL}	Low-level input voltage for SCLK, SDAT, GPIOx, HOLD_DCDC1, HOLD_LDO1, $\overline{PB\_IN}$	GPIOs configured as input	0		0.4	V
V_{OL}	Low-level output voltage for SDAT, GPIOx, $\overline{INT}$, $\overline{RESET}$	GPIOs configured as output; I_o = 1 mA; no internal pull-up	0		0.4	V
I_{OL}	Sink current for GPIO2, GPIO3	GPIO2, GPIO3 configured as current sink; V_{OL} = 0.4 V ; for T_J = 0°C to 85°C	–20%	5	20%	mA
	Sink current for GPIOx	GPIOx configured as open-drain output ; output = LOW			3	mA
V_{OL}	Minimum voltage for proper current regulation from GPIO2 or GPIO3 to GND if programmed as a current sink	I_O = 5 mA; current sink turned on	0.4			V
$V_{RESET-falling}$	LDO1 out of regulation reset voltage	Falling edge; $\overline{RESET}$ is asserted LOW for TPS65720, TPS657201, TPS657202	VLDO1, nom-13%		VLDO1, nom-7%	V
$V_{RESET-rising}$		Rising edge; $\overline{RESET}$ is released HIGH for TPS65720, TPS657201, TPS657202 after T_{RESET}		VLDO1, nom-4%		V
$V_{THRESHOLD\_down}$	Threshold voltage for reset input	Falling voltage; WQFN package only	–3%	570	3%	mV
$V_{THRESHOLD\_hys}$	Hysteresis on THRESHOLD	Rising voltage; WQFN package only		30		mV
I_{LKG}	Input leakage current	$\overline{PB\_IN}$, SDAT, SCLK, GPIOx configured as output, $\overline{INT}$, $\overline{RESET}$, output high impedance			0.2	µA

Electrical Characteristics (continued)

V_{SYS} = 3.6 V, V_{DCDC1} = 2.05 V, PFM mode, L = 3.3 µH, $C_{OUTDCDC1}$ = 4.7 µF, V_{INLDO1} = 2.05 V, V_{LDO1} = 1.85 V, T_A = –40°C to 85°C typical values apply in a temperature range of 10°C to 35°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STEP-DOWN CONVERTER						
V_{SYS}	Input voltage for DCDC1		2.3		5.6	V
UVLO	Internal undervoltage lockout threshold hysteresis	V_{SYS} falling	2.15	2.2	2.25	V
		V_{SYS} rising		120		mV
POWER SWITCH						
$R_{DS(ON)}$	High-side MOSFET ON-resistance	V_{SYS} = $V_{INDCDC1}$ = 3.6 V, YFF package		350	600	mΩ
		V_{SYS} = $V_{INDCDC1}$ = 3.6 V, RSN package		400	650	
I_{LK_HS}	High-side MOSFET leakage current	V_{DS} = 5.6 V			1	µA
$R_{DS(ON)}$	Low-side MOSFET ON-resistance	$V_{INDCDC1/2}$ = 3.6 V, YFF package		300	500	mΩ
		$V_{INDCDC1/2}$ = 3.6 V, RSN package		350	550	mΩ
I_{LK_LS}	Low-side MOSFET leakage current	VDS = 5.6 V			1	µA
I_{LIMF}	Forward current limit high-side and low-side MOSFET	2.3 V ≤ V_{IN} ≤ 5.6 V, TPS65720	425	600	775	mA
		2.3 V ≤ V_{IN} ≤ 5.6 V, TPS65721, TPS657201, TPS657202	625	850	1150	mA
I_O	DC output current	V_{SYS} > 2.7 V; TPS65720			200	mA
		V_{SYS} > 2.7 V; TPS65721, TPS657201, TPS657202			400	
OUTPUT						
V_{OUT}	Output voltage range		0.6		Vin	V
V_{FB}	Feedback voltage	for TPS65720, TPS65721		0.6		V
V_{OUT}	Default output voltage for TPS657201			1.85		V
V_{OUT}	Default output voltage for TPS657202			1.90		V
I_{FB}	FB pin input current for externally adjustable version	External resistor-divider			0.1	µA
I_{FB}	FB pin input current for TPS657201, TPS657202	Internal resistor-divider			5	µA
V_{OUT}	DC output voltage accuracy (1)	V_{IN} = 2.3 V to 5.6 V; PFM operation, 0 mA < I_{OUT} < I_{OUTMAX}		1%	3%	
		V_{IN} = 2.3 V to 5.6 V, PWM operation, 0 mA < I_{OUT} < I_{OUTMAX}	–2%		2%	
	DC output voltage load regulation	PWM operation		0.5		%/A
$V_{PGOOD\text{-}falling}$	PGOOD threshold at falling output voltage	<PGOODZ_DCDC1> is set to 1	VDCDC1, nom-14%		VDCDC1, nom-7%	V
$V_{PGOOD\text{-}rising}$	PGOOD threshold at rising output voltage	<PGOODZ_DCDC1> is set to 0		VDCDC1, nom-5%		V
R_{DIS}	Internal discharge resistor at L	DCDC1 disabled; the discharge function can be disabled as an EEPROM option	300	400		Ω
THERMAL PROTECTION FOR DCDC1 AND LDO1						
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		30		°C

(1) Output voltage specification does not include tolerance of external voltage programming resistors.

Electrical Characteristics (continued)

V_{SYS} = 3.6 V, V_{DCDC1} = 2.05 V, PFM mode, L = 3.3 µH, $C_{OUTDCDC1}$ = 4.7 µF, V_{INLDO1} = 2.05 V, V_{LDO1} = 1.85 V, T_A = –40°C to 85°C typical values apply in a temperature range of 10°C to 35°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VLDO1 LOW DROPOUT REGULATOR						
V_{INLDO}	Input voltage range for LDO1		1.8		5.6	V
V_{LDO1}	LDO1 output voltage range		0.8		3.3	V
V_{LDO1}	LDO1 output voltage	Default output voltage for TPS65720, TPS657201		1.85		V
V_{LDO1}	LDO1 output voltage	Default output voltage for TPS657202		2.85		V
V_{FB_LDO1}	Feedback voltage	Externally adjustable version only: TPS65721		0.8		V
I_{FB_LDO1}	FB pin input current				0.1	µA
I_O	Output current for LDO1				200	mA
I_{SC}	LDO1 short circuit current limit	VLDO1 = GND; V_{INLDO1} = 2.05 V		350	500	mA
	Dropout voltage at LDO1, YFF package	I_O = 200 mA, V_{INLDO} = 2.05 V			180	mV
	Dropout voltage at LDO1, RSN package	I_O = 200 mA, V_{INLDO} = 2.05 V		120		mV
	Output voltage accuracy for LDO1	I_O = 200 mA	–1.5%		2.5%	
	Line regulation for LDO1	V_{INLDO1} = V_{LDO1} + 0.5 V (min. 1.8 V) to 5.6 V (VSYS), I_O = 50 mA	–1%		1%	
	Load regulation for LDO1	I_O = 0 mA to 200 mA for LDO1	–1%		2%	
R_{DIS}	Internal discharge resistor at VLDO1	LDO disabled, discharge function per default disabled in register	250	400		Ω
BATTERY VOLTAGE AND BATTERY TEMPERATURE MONITOR WITH MULTIPLEXER; INTERNAL BATTERY VOLTAGE COMPARATOR						
V_{TS}	Input voltage range on TS pin for full scale output on pin TS_OUT (0 V to 1.4 V)	Equals –20°C to 60°C on a 10k NTC	0		1.4	V
V_{BAT}	Input voltage range on BAT pin for full scale output on pin TS_OUT (0 V to 1.4 V)		2.2		4.5	V
V_{TS_OUT}	Output voltage range on pin TS_OUT	I_{TS_OUT} = 0 mA	0		1.4	V
		0 < I_{TS_OUT} < 0.05 mA	0.06		1.4	
	Offset error on pin TS_OUT	In temperature-sense mode; V_O with V_{bat} = 2.2 V			±7.5	mV
SR	Slew rate	V_{TS_OUT}; 0 V to 1.4 V		1		V/ms
$I_{TS\_OUT\_SC}$	Short circuit current		0.1			mA
	Load capacitance	Maximum capacitance at TS_OUT			100	pF
	Battery voltage comparator threshold voltage	Depending on Bits <VBAT0>, <VBAT1>; falling voltage	–3%		3%	V
	Battery voltage comparator threshold voltage hysteresis	Rising voltage		200		mV
ACCURACY						
VBAT MODE						
	Offset	T_J = 10°C to 35°; for V(TS) ≥ 0.2 V	–22		22	mV
	Gain error	T_J = 10°C to 35°; for V(TS) ≥ 0.2 V	–11		11	mV
	Offset	T_J = –40°C to 85°C; for V(TS) ≥ 0.2 V	–30		30	mV
	Gain error	T_J = –40°C to 85°C; for V(TS) ≥ 0.2 V	–14		14	mV
TS MODE						
	Internal TS resistor (for 10k NTC, B=3380)	T_J = 25°C	–1.5%	29.23	1.5%	kΩ
	Internal TS resistor (for 100k NTC)	T_J = 25°C	–1.5%	292.3	1.5%	kΩ
	Internal TS resistor temperature drift	T_J = –40°C to 85°C		–4.5%		
	Internal V2V0 reference voltage	T_J = –40°C to 85°C	–1.2%	2	1.2%	V

Electrical Characteristics (continued)

V_{SYS} = 3.6 V, V_{DCDC1} = 2.05 V, PFM mode, L = 3.3 µH, $C_{OUTDCDC1}$ = 4.7 µF, V_{INLDO1} = 2.05 V, V_{LDO1} = 1.85 V, T_A = –40°C to 85°C typical values apply in a temperature range of 10°C to 35°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER PATH						
V_{UVLO}	Undervoltage lockout	V_{AC}: 0 V → 4 V	3.2	3.3	3.45	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	V_{AC}: 4 V → 0 V	200		300	mV
V_{IN-DT}	Input power detection threshold	(Input power detected if $V_{IN} > V_{BAT} + V_{IN-DT}$) V_{BAT} = 3.6 V, V_{IN}: 3.5 V → 4 V	40	80	140	mV
$V_{HYS-INDT}$	Hysteresis on VIN-DT	V_{BAT} = 3.6 V, V_{IN}: 4 V → 3.5 V	20			mV
V_{OVP}	Input overvoltage protection threshold	V_{AC}: 5 V → 7 V	6.4	6.6	6.8	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{AC}: 11 V → 5 V		105		mV
$V_{DO(AC-SYS)}$	AC pin to SYS pin dropout voltage $V_{AC} - V_{SYS}$	I_{SYS} = 0.3 A, V_{AC} = 4.35 V, V_{BAT} = 4.2 V; YFF package		170	285	mV
		I_{SYS} = 0.3 A, V_{AC} = 4.35 V, V_{BAT} = 4.2 V; RSN package		210	325	mV
$V_{DO(BAT-SYS)}$	Battery to SYS pin dropout voltage $V_{BAT} - V_{SYS}$	I_{SYS} = 0.2 A, V_{AC} = 0 V, V_{BAT} > 3 V; YFF package			80	mV
		I_{SYS} = 0.2 A, V_{AC} = 0 V, V_{BAT} > 3 V; RSN package			120	mV
$V_{SYS(REG)}$	SYS pin voltage regulation selectable register <CHGCONFIG0> Bits <VSYS1>; <VSYS0>	00: $V_{AC} > V_{SYS} + V_{DO(AC-SYS)}$, V_{BAT} < 3.3V	–5%	3.4	5%	V
		00: $V_{AC} > V_{SYS} + V_{DO(AC-SYS)}$, $V_{BAT} \geq$ 3.3 V	–5%	V_{BAT} + 200 mV	5%	
		01: $V_{AC} > V_{SYS} + V_{DO(AC-SYS)}$	–5%	4.4	5%	
		10: $V_{AC} > V_{SYS} + V_{DO(AC-SYS)}$	–5%	5.0	5%	
		11: $V_{AC} > V_{SYS} + V_{DO(AC-SYS)}$	–5%	5.5	5%	
I_{AC-MAX}	Maximum Input Current Register <CHCONFIG0>	Bit <AC input current1, AC input current0> = 00	90	95	100	mA
		Bit < AC input current1, AC input current0> = 01 or 10	450	475	500	
V_{AC-LOW}	Input voltage threshold when input current is reduced	Input current is reduced if voltage at AC falls below VAC-LOW to keep the AC voltage above 4.5 V	4.35	4.5	4.65	V
V_{DPM}	Output voltage threshold when charging current is reduced	Bit <V_DPPM> = 1		$V_{O(REG)}$ – 100 mV		V
	Register <CHCONFIG2>	Bit <V_DPPM> = 0		4.3		
V_{BSUP1}	Enter battery supplement mode			$V_{OUT} \leq V_{BAT}$ – 40 mV		V
V_{BSUP2}	Exit battery supplement mode			$V_{OUT} \geq V_{BAT}$ – 20 mV		V
$V_{O(SC1)}$	Output short-circuit detection threshold, power-on		0.8	0.9	1	V
$V_{O(SC2)}$	Output short-circuit detection threshold, supplement mode $V_{BAT} - V_{OUT} > V_{O(SC2)}$ indicates short-circuit		200	250	300	mV
BATTERY CHARGER						
QUIESCENT CURRENT						
$I_{IACSTDBY)}$	Standby current into AC pin	V_{IN} = 5 V; ACinputcurrent[1,0] = 11		60	80	µA
		V_{IN} = 28 V; ACinputcurrent[1,0] = 11			530	µA
I_{CC}	Active supply current, AC pin	V_{IN} = 5 V, no load on DCDC1, LDO1, SYS pin, VSYS[1,0] = 11; ACinputcurrent[1,0] = 10; CH_EN = 0			2	mA
IBAT(SC)	Source current for BAT pin short-circuit detection		4	7.5	11	mA
VBAT(SC)	BAT pin short-circuit detection threshold		1.6	1.8	2.0	V
$V_{o(BATREG)}$	Battery charger voltage	Depending on setting in CHGCONFIG3 And internal EEPROM Default = 4.2 V	–1%	4.15	1%	V
			–1%	4.175	1%	
			–1%	4.20	1%	
			–1%	4.225	1%	
			–1%	4.25	1%	
			–1%	4.275	1%	
			–1%	4.30	1%	
			–1%	4.325	1%	
V_{LOWV}	Precharge to fast-charge transition threshold		2.9	3.0	3.1	V

Electrical Characteristics (continued)

V_{SYS} = 3.6 V, V_{DCDC1} = 2.05 V, PFM mode, L = 3.3 µH, $C_{OUTDCDC1}$ = 4.7 µF, V_{INLDO1} = 2.05 V, V_{LDO1} = 1.85 V, T_A = –40°C to 85°C typical values apply in a temperature range of 10°C to 35°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT (continued)						
I_{CHG}	Maximum battery fast charge current	$V_{BAT(REG)} > V_{BAT} > V_{LOWV}$, $V_{IN} = V_{AC}$ or V_{USB} = 5 V	300			mA
	Minimum battery fast charge current				10	mA
	Battery fast charge current set factor	$V_{BAT} > V_{LOWV}$, V_{IN} = 5 V, $I_{IN-MAX} > I_{CHG}$, No load on SYS pin, thermal loop not active, DPPM loop not active		K_{ISET} / R_{ISET}		A
K_{ISET}	Fast charge current factor	at 300 mA for ICH_SCL[1,0] = 11 (charge current scaling is 100% of ISET value)	–15%	450	15%	AΩ
		at 40 mA for ICH_SCL[1,0] = 11 (charge current scaling is 100% of ISET value)	–20%	450	20%	
		at 225 mA range for ICH_SCL[1,0] = 10 (charge current scaling is 75% of ISET value)	–15%	338	15%	
		at 30 mA for ICH_SCL[1,0] = 10 (charge current scaling is 75% of ISET value)	–20%	338	20%	
		at 150 mA for ICH_SCL[1,0] = 01 (charge current scaling is 50% of ISET value)	–10%	225	10%	
		at 20 mA for ICH_SCL[1,0] = 01 (charge current scaling is 50% of ISET value)	–15%	225	15%	
		at 75 mA for ICH_SCL[1,0] = 00 (charge current scaling is 25% of ISET value)	–10%	112	10%	
		at 10 mA for ICH_SCL[1,0] = 00 (charge current scaling is 25% of ISET value)	–20%	112	20%	
I_{PRECHG}	Precharge current	for I_PRE[1,0] = 11 (pre-charge current scaling is 20% of charge current)	0.15 × I_{CHG}	0.2 × I_{CHG}	0.25 × I_{CHG}	
		for I_PRE[1,0] = 10 (pre-charge current scaling is 15% of charge current)	0.11 × I_{CHG}	0.15 × I_{CHG}	0.19 × I_{CHG}	
		for I_PRE[1,0] = 01 (pre-charge current scaling is 10% of charge current)	0.07 × I_{CHG}	0.1 × I_{CHG}	0.13 × I_{CHG}	
		for I_PRE[1,0] = 00 (pre-charge current scaling is 5% of charge current)	0.03 × I_{CHG}	0.05 × I_{CHG}	0.08 × I_{CHG}	
I_{TERM}	Charge current value for termination detection threshold (internally set)	for I_TERM[1,0] = 11 (termination current is 20% of charge current)	0.15 × I_{CHG}	0.2 × I_{CHG}	0.27 × I_{CHG}	
		for I_TERM[1,0] = 10 (termination current is 15% of charge current)	0.11 × I_{CHG}	0.15 × I_{CHG}	0.21 × I_{CHG}	
		for I_TERM[1,0] = 01 (termination current is 10% of charge current)	0.07 × I_{CHG}	0.1 × I_{CHG}	0.15 × I_{CHG}	
		for I_TERM[1,0] = 00 (termination current is 5% of charge current)	0.03 × I_{CHG}	0.05 × I_{CHG}	0.08 × I_{CHG}	
V_{RCH}	Recharge detection threshold	Voltage below nominal charger voltage	165	100	60	mV
$I_{BAT(DET)}$	Sink current for battery detection		5	7.5	10	mA
T_{CHG}	Charge safety timer	Safety timer range selectable by I^2C; default setting without DPPM or thermal loop active	–35%	5	35%	h
T_{PRECHG}	Pre-charge timer	Pre-charge timer range; default setting	–35%	30	35%	min

Electrical Characteristics (continued)

V_{SYS} = 3.6 V, V_{DCDC1} = 2.05 V, PFM mode, L = 3.3 µH, $C_{OUTDCDC1}$ = 4.7 µF, V_{INLDO1} = 2.05 V, V_{LDO1} = 1.85 V, T_A = –40°C to 85°C typical values apply in a temperature range of 10°C to 35°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY-PACK NTC MONITOR						
$RNTC_{HOT}$	Thermistor high temperature detection resistance (equals 45°C for 10-kΩ NTC; B = 3380)	Hot temperature detected and charging suspended when the resistance of the battery-NTC is lower than $RNTC_{HOT}$	4.3	5	5.7	kΩ
	Thermistor high temperature detection resistance (equals 50°C for 10-kΩ NTC; B = 3380)		3.5	4.1	4.8	kΩ
	Thermistor high temperature detection resistance (equals 55°C for 10-kΩ NTC; B = 3380)		2.9	3.5	4.2	kΩ
	Thermistor high temperature detection resistance (equals 60°C for 10-kΩ NTC; B = 3380)		2.4	3	3.5	kΩ
	Thermistor high temperature detection resistance (equals 45°C for 100-kΩ NTC)		43	50	57	kΩ
	Thermistor high temperature detection resistance (equals 50°C for 100-kΩ NTC)		35	41	48	kΩ
	Thermistor high temperature detection resistance (equals 55°C for 100-kΩ NTC)		29	35	42	kΩ
	Thermistor high temperature detection resistance (equals 60°C for 100-kΩ NTC)		24	30	35	kΩ
$RNTC_{COLD}$	Thermistor low temperature detection resistance (equals 0°C for 10-kΩ NTC; B = 3380)	Cold temperature detected and charging suspended when the resistance of the battery-NTC is higher than $RNTC_{COLD}$	25	27	30	kΩ
	Thermistor low temperature detection resistance (equals 5°C for 10-kΩ NTC; B = 3380)		20	22	24	kΩ
	Thermistor low temperature detection resistance (equals 10°C for 10-kΩ NTC; B = 3380)		16	18	20	kΩ
	Thermistor low temperature detection resistance (equals 15°C for 10-kΩ NTC; B = 3380)		13	15	16	kΩ
	Thermistor low temperature detection resistance (equals 0°C for 100-kΩ NTC)		250	270	300	kΩ
	Thermistor low temperature detection resistance (equals 5°C for 100-kΩ NTC)		200	220	240	kΩ
	Thermistor low temperature detection resistance (equals 10°C for 100-kΩ NTC)		160	180	200	kΩ
	Thermistor low temperature detection resistance (equals 15°C for 100-kΩ NTC)		130	150	160	kΩ
$V_{HYS(COLD)}$	Low temperature trip point hysteresis	For 10-kΩ NTC; B = 3380		5		°C
$R_{NOSENSOR}$	Thermistor not detected for 10k NTC	Hot temperature detected and charging suspended when the resistance of the battery-NTC is higher than $R_{NOSENSOR}$	260	340	620	kΩ
	Thermistor not detected for 100k NTC		2500	3400	6200	kΩ
THERMAL REGULATION						
$T_{J(REG)}$	Lower Temperature regulation limit			115		°C
$T_{J(REG)}$	Upper Temperature regulation limit			135		°C
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C

7.6 Dissipation Ratings

See (1)

PACKAGE	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
YFF	55 K/W	1.8 W	18 mW/K	1 W	0.7 W
RSN	38 K/W	2.6 W	26 mW/K	1.4 W	1 W

(1) The thermal resistance was measured on a high K board.

7.7 Timing Requirements

			MIN	NOM	MAX	UNIT
$\overline{\text{RESET}}$ and $\overline{\text{PB\_IN}}$						
T_{RESET}	Reset delay time on pin $\overline{\text{RESET}}$	Low to high transition of $\overline{\text{RESET}}$ pin, Bit RESET_DELAY = 0	9	11	13	ms
		Low to high transition of $\overline{\text{RESET}}$ pin, Bit RESET_DELAY = 1	70	90	110	ms
		HIGH to LOW transition of $\overline{\text{RESET}}$ pin $\overline{\text{RESET}}$ will go low by HOLD pin going LOW AND HOLD Bit set to 0 OR voltage at V_{reset} falling below the threshold		10		µs
$T_{debounce}$	Debounce time at $\overline{\text{PB\_IN}}$	Rising and falling voltage	39	50	60	ms
POWER OUTPUTS, DCDC1 and LDO1						
t_{Start}	DCDC1 Start-up time	Time from active EN to Start switching		170		µs
t_{Ramp}	DCDC1 V_{OUT} ramp time	Time to ramp from 5% to 95% of V_{OUT}		250		µs
	LDO1 PGOOD debounce time	Internal PGOOD comparator at VOUTLDO1 is debounced by		80		µs
t_{Ramp}	LDO1 V_{OUT} Ramp time	Internal soft-start when LDO is enabled; Time to ramp from 5% to 95% of V_{OUT}		250		µs
POWER PATH						
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	Time measured from V_{IN}: 0 V → 5 V 1 µs rise time to $\overline{\text{PGOOD}}$ = LO		2		ms
$t_{BLK(OVP)}$	Input overvoltage blanking time			50		µs
$t_{REC(OVP)}$	Input overvoltage recovery time	Time measured from V_{AC}: 11 V → 5 V 1 µs fall time to <CH_PGOOD> = 0		2		ms
$t_{DGL(SC2)}$	Output short-circuit detection deglitch time, supplement mode short circuit $V_{BAT} - V_{OUT} > V_{O(SC2)}$ indicates short-circuit			250		µs
$t_{REC(SC2)}$	Recovery time, supplement mode short circuit			60		ms
CHARGER						
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			25		ms
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			25		ms
$t_{DGL(TERM)}$	Deglitch time, termination detected			25		ms
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected			62.5		ms
$t_{DGL(NO-IN)}$	Delay time, input power loss to charger turn-off	VBAT = 3.6 V. Time measured from VIN: 5 V → 3.3 V 1 µs fall time		20		ms
t_{DET}	Battery detection timer			250		ms
BATTERY PACK MONITOR						
$t_{DGL(TS)}$	Deglitch time, pack temperature fault detection			50		ms
$t_{SW(VBAT-TS)}$	MUX switching time	Bit <OPAMP+MUX> toggles			1	ms

Timing Requirements (continued)

			MIN	NOM	MAX	UNIT
I²C COMMUNICATION						
f_{MAX}	Clock frequency				400	kHz
$t_{wH(HIGH)}$	Clock high time		600			ns
$t_{wL(LOW)}$	Clock low time		1300			ns
t_R	DATA and CLK rise time				300	ns
t_F	DATA and CLK fall time				300	ns
$t_{h(STA)}$	Hold time (repeated) START condition (after this period the first clock pulse is generated)		600			ns
$t_{h(DATA)}$	Setup time for repeated START condition		600			ns
$t_{h(DATA)}$	Data input hold time		0			ns
$t_{su(DATA)}$	Data input setup time		100			ns
$t_{su(STO)}$	STOP condition setup time		600			ns
$t_{(BUF)}$	Bus free time		1300			ns

7.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	DCDC1 Switching frequency		2.03	2.25	2.48	MHz

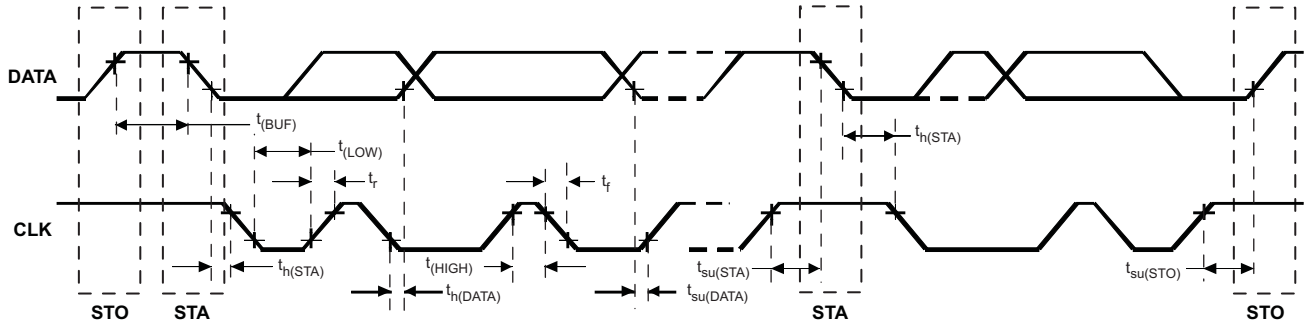


Figure 1. Serial I/f Timing Diagram

7.9 Typical Characteristics

The graphs have been generated on the TPS65720YFF EVM with the inductors as mentioned in the graphs. See the *TPS65720EVM User's Guide* (SLVU324) for details on the layout.

Table 1. Table Of Graphs

		FIGURE
Startup DCDC1 and LDO1	Scope plot using TPS65720 (battery powered) for PB_IN; Vo_DCDC1; Vo_LDO1	Figure 2
K_{ISET} vs R_{ISET}		Figure 3, Figure 4, Figure 5, Figure 6

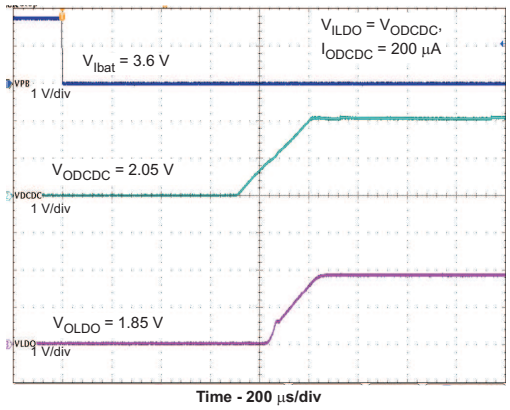


Figure 2. Start-Up DCDC1 and LDO1

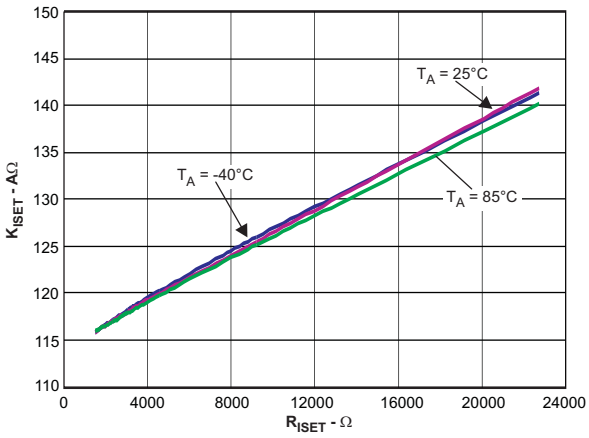


Figure 3. K_{ISET} vs R_{ISET}; ICH_SCL[1,0] = 00

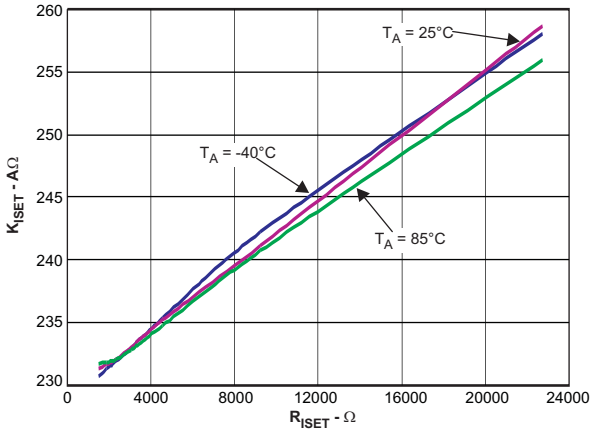


Figure 4. K_{ISET} vs R_{ISET}; ICH_SCL[1,0] = 01

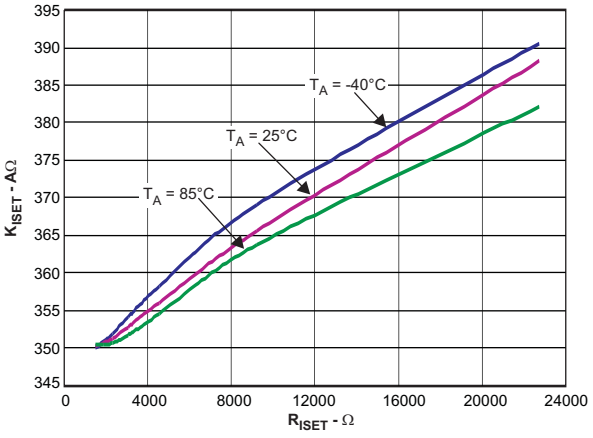


Figure 5. K_{ISET} vs R_{ISET}; ICH_SCL[1,0] = 10

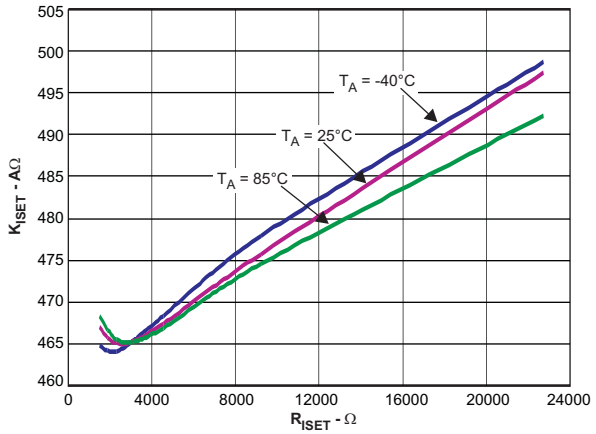


Figure 6. K_{ISET} vs R_{ISET}; ICH_SCL[1,0] = 11

8 Detailed Description

8.1 Overview

The TPS6572x device has a battery charger, DC-DC, and LDO that compliment most small low-power products such as wearables, accessories, and MCU systems. In addition to the power delivery the device has I^2C communication, push button, RESET control, and GPIOs/LED drivers for a complete power system. The DC-DC and LDO turn on automatically with push-button or valid AC input. The system holds them on by use of the HOLD_DCDC1 and HOLD_LDO1 pins.

8.2 Functional Block Diagrams

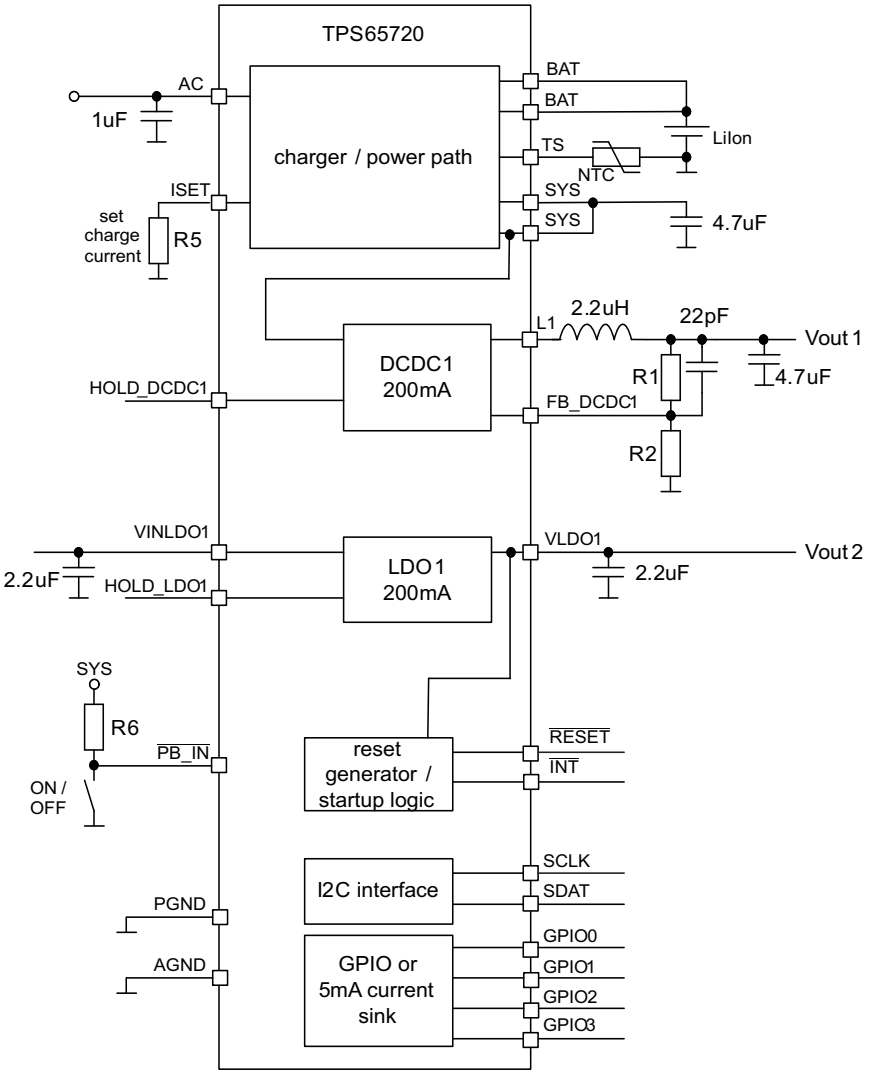


Figure 7. Functional Block Diagram for TPS65720

Functional Block Diagrams (continued)

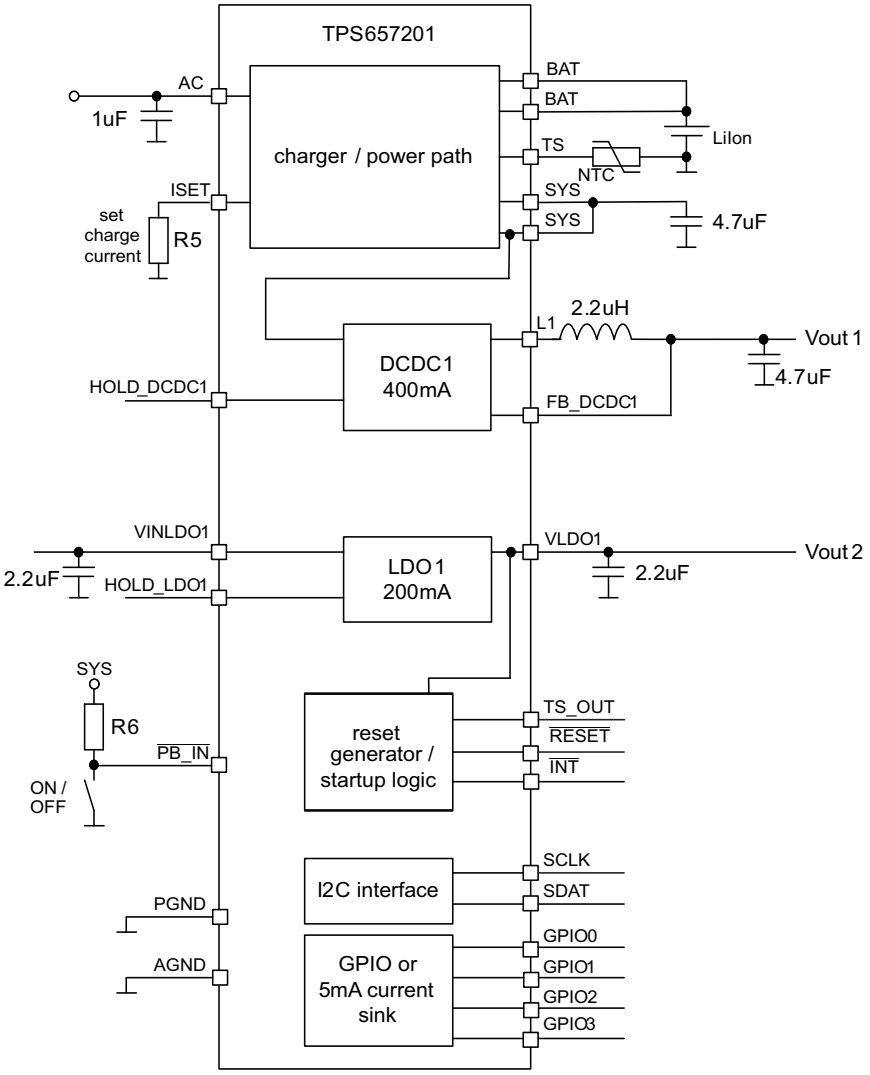


Figure 8. Functional Block Diagram for TPS657201, TPS657202

Functional Block Diagrams (continued)

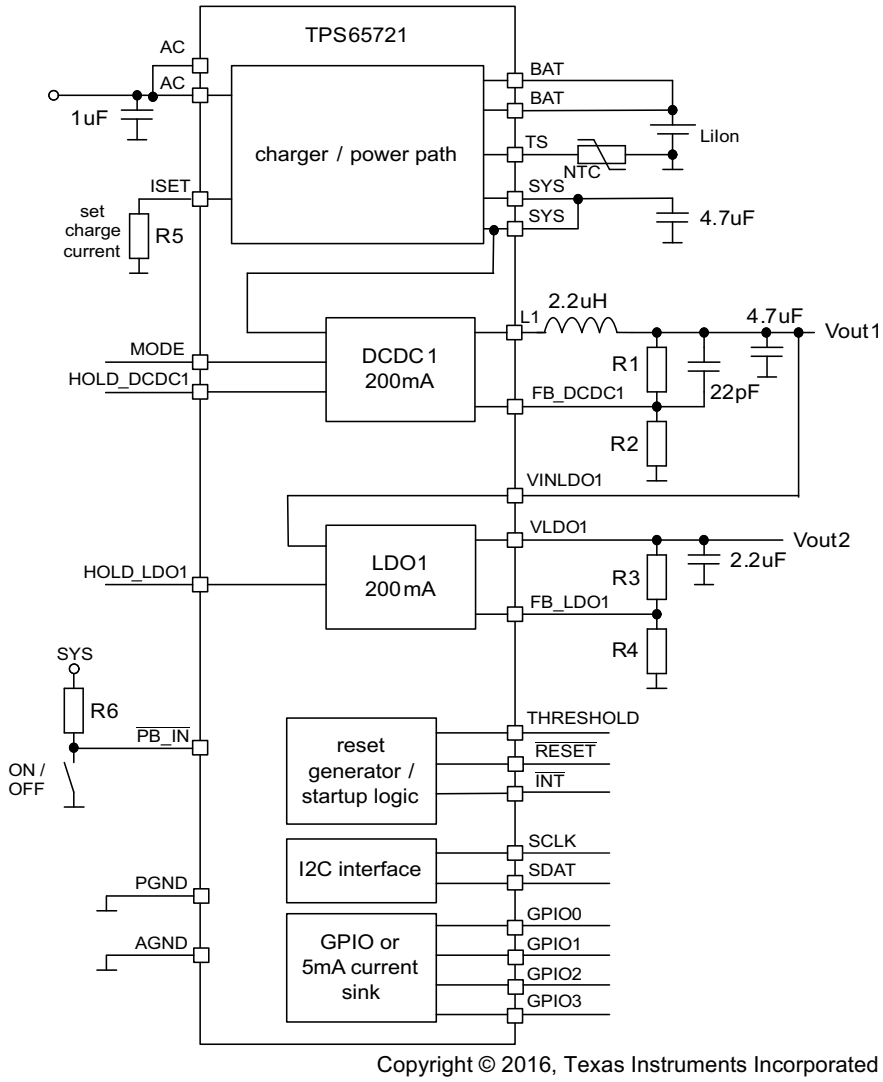


Figure 9. Functional Block Diagram for WQFN Version

8.3 Feature Description

8.3.1 Battery Charger and Power Path

The TPS6572x integrates a Li-Ion linear charger and system power-path management targeted at space-limited portable applications. The TPS6572x powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack. It also allows instant system turnon even with a totally discharged battery. The input power source for charging the battery and running the system can be an AC adapter or an USB port. The power-path management feature automatically reduces the charging current if the system load increases. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents.

Feature Description (continued)

8.3.2 Power-Path Management

The current at the input pin AC of the power path manager is shared between charging the battery and powering the system load on the SYS pin. Priority is given to the system load. The input current is monitored continuously. If the sum of the charging and system load currents exceeds the preset maximum input current (programmed internally by I^2C), the charging current is reduced automatically. The default value for the current limit is 500 mA for the AC pin.

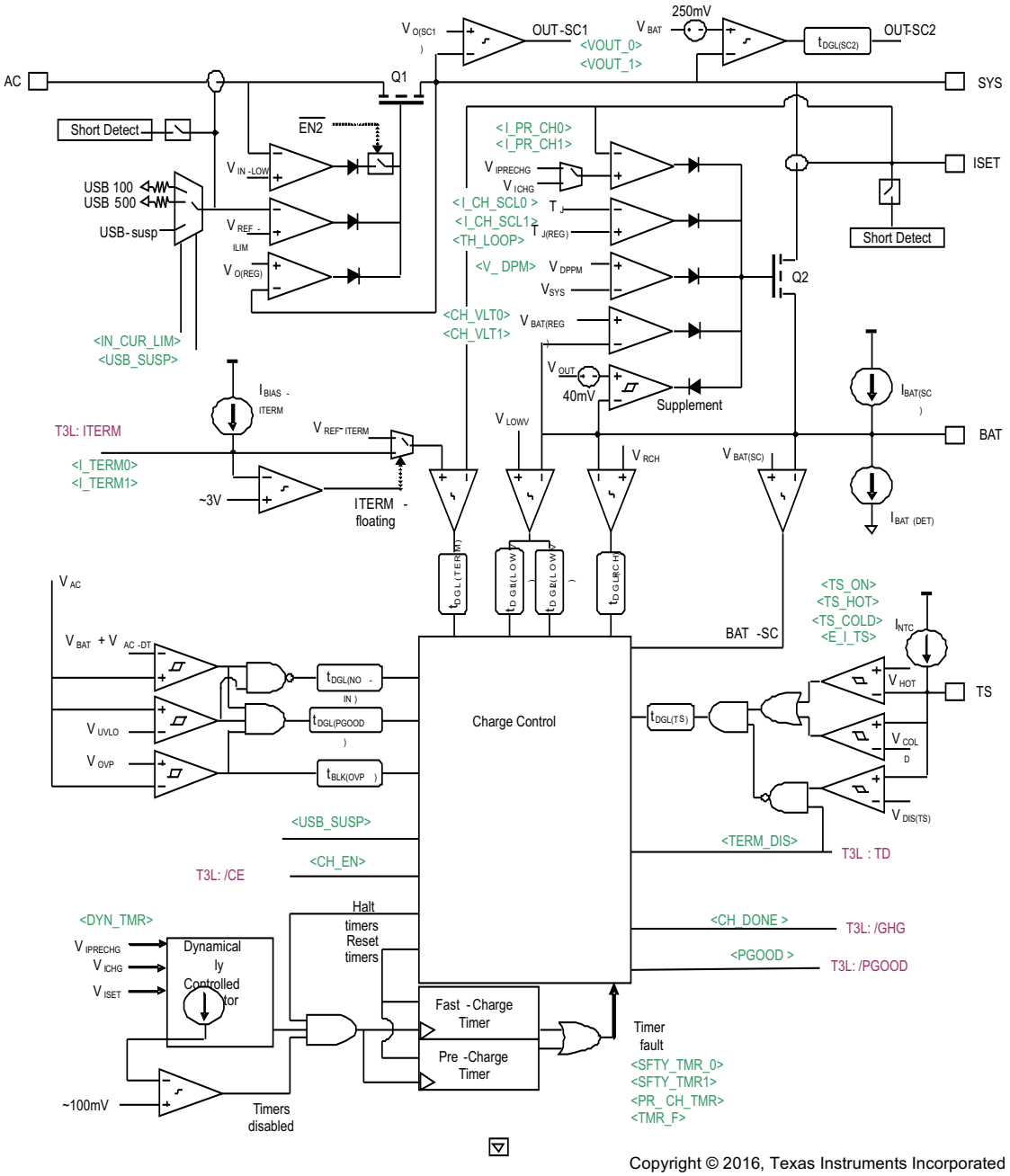


Figure 10. Charger Block Diagram

Feature Description (continued)

8.3.3 Battery Charging

When <CH_EN> = 1, battery charging begins. First, the device checks for a short circuit on the BAT pin by sourcing $I_{BAT(SC)}$ to the battery and monitoring the voltage. When the BAT voltage exceeds $V_{BAT(SC)}$, the battery charging continues. The battery is charged in three phases: conditioning pre-charge, constant-current fast charge (current regulation) and a constant-voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

Figure 11 shows what happens in each of the three phases:

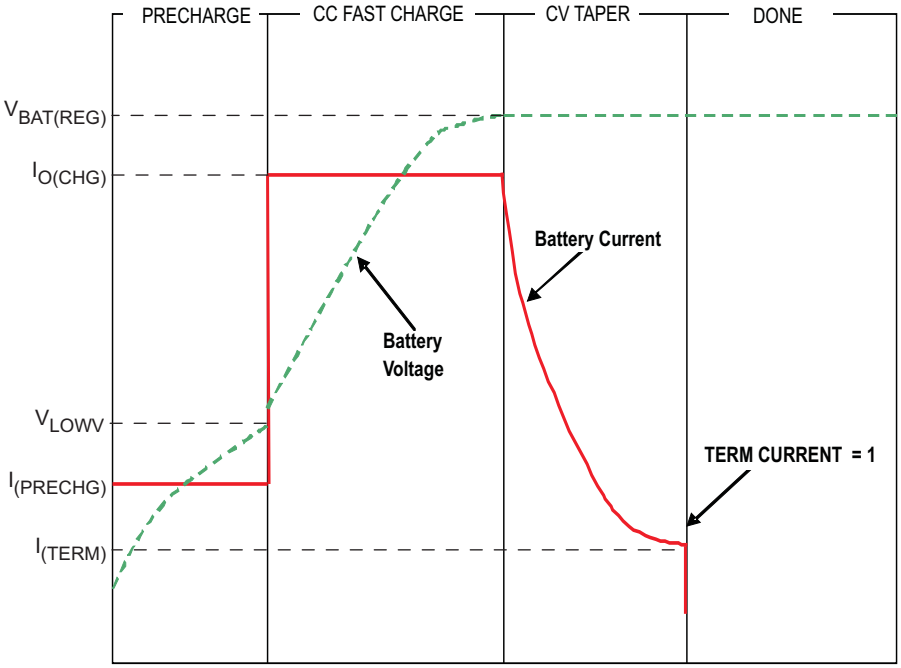


Figure 11. Battery Charge

In the pre-charge phase, the battery is charged with the pre-charge current (IPRECHG). Once the battery voltage crosses the VLOWV threshold, the battery is charged with the fast-charge current (ICHG). As the battery voltage reaches VBAT(REG), the battery is held at a constant voltage of VBAT(REG) and the charge current tapers off as the battery approaches full charge. Note that termination detection is disabled whenever the charge rate is reduced from the set point because of the actions of the thermal loop, the DPM loop, or the VIN(LOW) loop. The value of the fast-charge current is set by the resistor connected from the ISET pin to GND, and is given by Equation 1:

$$ICHG = K_{ISET} / R_{iset} \quad (1)$$

The charge current limit is adjustable up to 300 mA. The valid resistor range is 1500 Ω to 11.25 kΩ. Note that if ICHG is programmed as greater than the input current limit, the battery does not charge at the rate of ICHG, but at the slower rate of IACmax (minus the load current on the OUT pin, if any). In this case, the charger timers are proportionately slowed down.

8.3.3.1 I-PRECHARGE

The value for the pre-charge current is defined with Bits <I_PRE1, I_PRE0> based on the charge current defined with pin ISET and Bits <CH_SCL1, ICH_SCL0> in register CHCONFIG1. Pre-charge current is scaled to lower currents in DPPM mode or when the charger is in thermal regulation.

Feature Description (continued)

8.3.3.2 ITERM

The value for the termination current threshold can be set in register CHGCONFIG1 using Bits <I_TERM1, I_TERM0> based on the charge current defined with pin ISET and Bits <CH_SCL1, ICH_SCL0>. Termination current is not scaled in DPPM mode or when the charger is in thermal regulation.

8.3.3.3 Battery Detection and Recharge

The charger automatically detects if a battery is connected or removed. Once a charge cycle is complete, the battery voltage is monitored. When the battery voltage falls below VRCH, the device determines if the battery has been removed. A current, IBAT(DET), is pulled from the battery for a duration tDET. If the voltage on the BAT pin remains above V_{LOWV}, it indicates that the battery is still connected, but has discharged. If <CH_EN> = 1, the charger is turned on again to top off the battery. Recharge cycles are not indicated by the <CH_ACTIVE> Bit.

If the BAT voltage falls below VLOWV during the battery detection test, it indicates that the battery has been removed. The device then checks for battery insertion. The FET Q2 is turned on and sources I_{PRECHG} out of BAT for the duration of t_{DET}. If the battery voltage does not rise above V_{RCH}, it indicates that a battery has been inserted, and a new charge cycle begins. If the voltage rises above V_{RCH}, it is possible that a fully charged battery has been inserted. To check for this, $I_{BAT(DET)}$ is pulled from the battery for t_{DET}. If the voltage falls below V_{LOWV}, a battery is not present. The device continuously checks for the presence of a battery.

8.3.3.4 Charge Termination On/Off

Charge termination can be disabled by setting the Bit <TERM_EN> = 0. When termination is disabled, the device goes through the pre-charge, fast-charge, and CV phases, then remains in the CV phase. During the CV phase, the charger behaves like an LDO with an output voltage equal to $V_{BAT(REG)}$ and is able to source currents up to I_{CHG} or I_{INmax}, whichever is less. Battery detection is not performed. The Bit <CH_ACTIVE> = 0 once the current falls below ITERM and does not go t o1 until the input power is toggled. When termination is disabled, the pre-charge and fast-charge safety timers are also disabled. Battery pack temperature sensing (TS pin functionality) is also disabled if Bit <TERM_EN> = 0 and the TS pin is unconnected.

8.3.3.5 Timers

The charger in TPS6572x has internal safety timers for the pre-charge and fast-charge phases to prevent potential damage to either the battery or the system. The default values for the timers can be changed in register CHGCONFIG2.

The pre-charge timer and fast charge timer will run with their nominal speed defined in register CHCONFIG2 if ICH_SCL[1,0] = 01, which equals a charge current of 50% defined with the ISET resistor. If ICH_SCL[1,0] are set to higher or lower fast-charge current, the fast charge timers and precharge timers are scaled automatically. For instance, with ICH_SCL[1,0] = 11, which equals 100% of fast charge current, the safety timers will time out in half the time defined in register CHCONFIG2. Changing the pre-charge current with I_PRE[1,0] will not change the precharge or fast-charge timers.

8.3.3.6 Dynamic Timer Function

During the fast-charge phase, several events increase the timer durations.

- The system load current activates the DPM loop, which reduces the available charging current
- The input current is reduced because the input voltage has fallen to $V_{IN(LOW)}$
- The device has entered thermal regulation because the IC junction temperature has exceeded $T_{J(REG)}$

During each of these events, the internal timers are slowed down proportionately to the reduction in charging current. For example, if the charging current is reduced by half, the fast-charge timer is twice as long as programmed.

A modified charge cycle with the thermal loop active is shown in Figure 12.

Feature Description (continued)

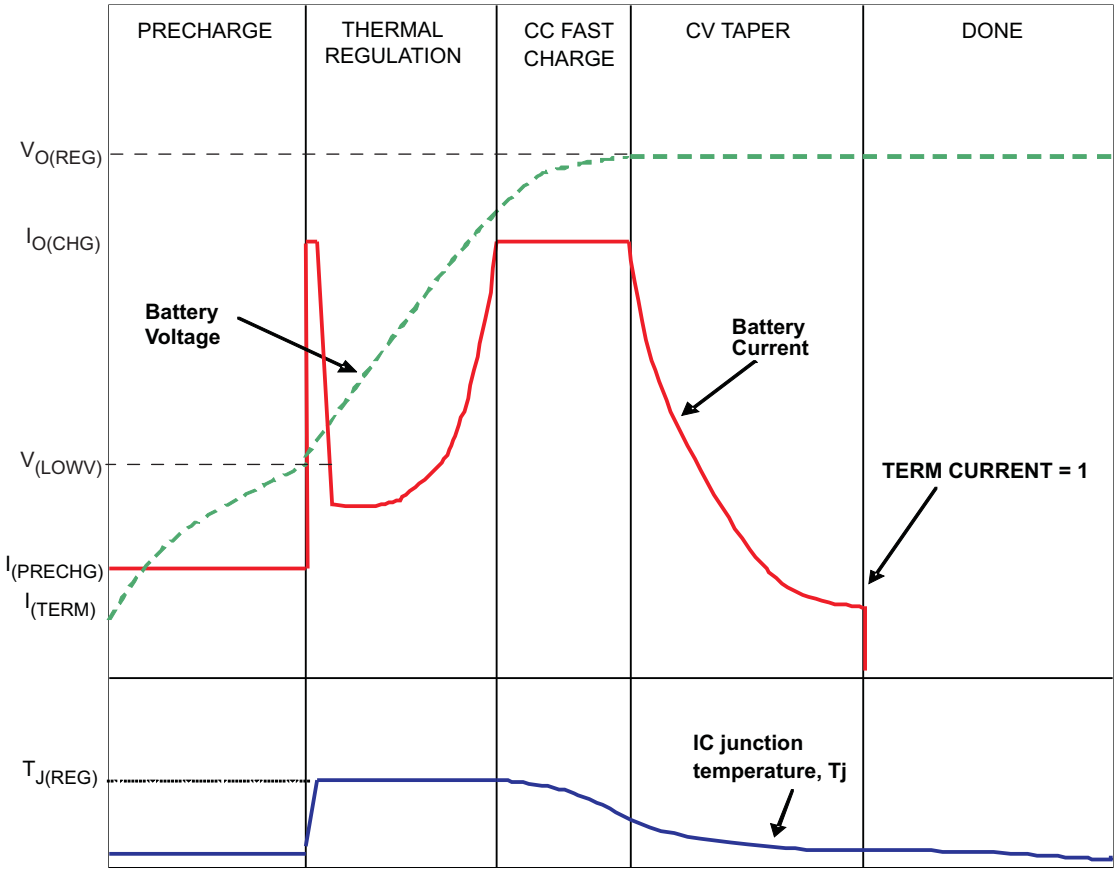


Figure 12. Thermal Loop

8.3.3.7 Charger Fault

If the precharge timer expires before the battery voltage reaches V_{LOWV}, the charger indicates a fault condition. Additionally, if the battery current does not fall to ITERM before the fast-charge timer expires, a fault is indicated by setting Bit <CH_FAULT> = 1.

8.3.4 Thermal Regulation and Thermal Shutdown

The charger contains a thermal regulation loop that monitors the die temperature. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high VAC and heavy system load conditions. Under these conditions, if the die temperature increases to $T_{J(OFF)}$, the input FET Q1 is turned OFF. FET Q2 is turned ON to ensure that the battery still powers the load on SYS. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the input FET Q1 is turned on and the device returns to thermal regulation. Continuous over-temperature conditions result in the pulsing of the Q1 FET. Note that this feature monitors the die temperature of the charger. This is not synonymous with ambient temperature. Self-heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm and the LDO mode for SYS.

8.3.5 Battery Pack Temperature Monitoring

The TPS6572x features an external battery pack temperature monitoring input. The TS input connects to the NTC resistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions. During charging, I_{NTC} is sourced to TS and the voltage at TS is continuously monitored. If, at any time, the voltage at TS is outside of the operating range (V_{COLD} to V_{HOT}), charging is suspended. The timers maintain their values but suspend counting. When the voltage measured at TS returns to within the operation

Feature Description (continued)

window, charging is resumed and the timers continue counting. When charging is suspended due to a battery pack temperature fault, the CH_ACTIVE Bit remains 1 and continues to indicate *charging*. Battery pack temperature sensing is disabled when termination is disabled (<TERM_EN = 0>) and the voltage at TS is greater than $V_{DIS(TS)}$. The battery pack temperature monitoring is disabled by connecting a 10-kΩ resistor from TS to GND.

TPS6572x contains a feature to shift the termination temperature to higher levels by setting Bits <TMP_SHIFT1, TMP_SHIFT0>.

8.3.6 DCDC1 Converter

The TPS6572x step-down converter operates with typically 2.25-MHz fixed-frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converter can automatically enter Power Save Mode and operates then in PFM mode.

During PWM operation, the converter use a unique fast response voltage mode control scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows now from the input capacitor through the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic will turn off the switch. The current-limit comparator will also turn off the switch in case the current limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot through current, the low-side MOSFET rectifier is turned on and the inductor current will ramp down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle will be initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the on the high-side MOSFET switch.

The DCDC1 converters output voltage is externally adjustable using a resistor-divider at FB_DCDC1.

8.3.7 Power Save Mode

The power save mode is enabled automatically with <F_PWM> = 0, which is the default setting. If the load current decreases, the converter will enter power save mode operation automatically. During power save mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter will position the output voltage typically +1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step. The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode. During the power save mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of VOUT nominal +1%, the device starts a PFM current pulse. The high-side MOSFET switch will turn on, and the inductor current ramps up. After the ON-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero. The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15-μA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold. With a fast single threshold comparator, the output voltage ripple during PFM mode operation can be kept small. The PFM pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values will minimize the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values. The PFM mode is left and PWM mode is entered in case the output current can not longer be supported in PFM mode. The power save mode can be disabled by setting <F_PWM> = 1. The converter will then operate in fixed-frequency PWM mode.

Feature Description (continued)

8.3.7.1 Dynamic Voltage Positioning

This feature reduces the voltage undershoots and overshoots at load steps from light to heavy load and vice versa. The feature is active in power-save mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off (see Figure 13).

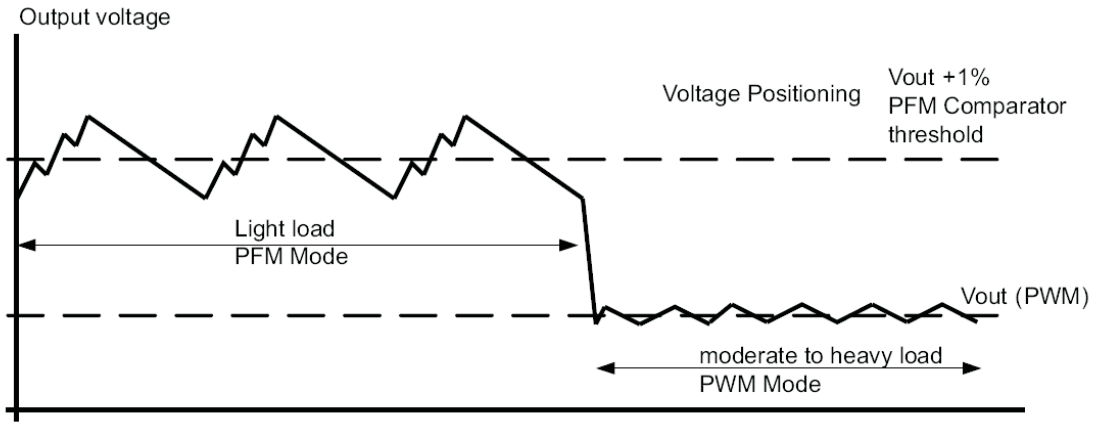


Figure 13. DVS Transition

8.3.7.2 Soft Start

The step-down converter in TPS6572x has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typical 250 µs. This limits the inrush current in the converter during ramp up and prevents possible input voltage drops when a battery or high impedance power source is used.

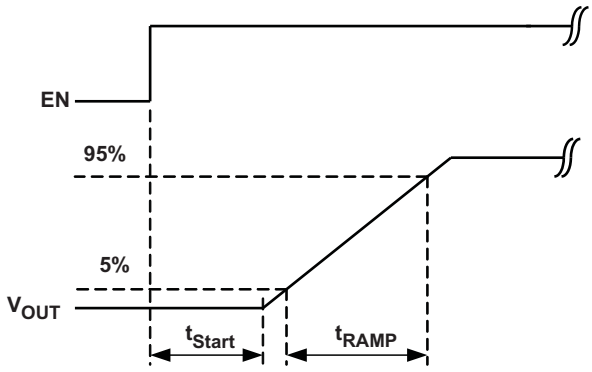


Figure 14. Soft Start

8.3.7.3 100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode once the input voltage comes close to the nominal output voltage. To maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles. With further decreasing VIN the high-side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated in Equation 2:

Feature Description (continued)

$V_{INmin} = V_{Omax} + I_{Omax} \times R_{DS(on)max} + R_L)$

where

- I_{Omax} = maximum output current plus inductor ripple current
- $R_{DS(on)max}$ = maximum high side switch RDSon
- R_L = DC resistance of the inductor
- V_{Omax} = nominal output voltage plus maximum output voltage tolerance (2)

8.3.7.4 Undervoltage Lockout

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the converters and LDOs. The under-voltage lockout threshold is typically 2.2 V.

8.3.8 Short-Circuit Protection

All outputs are short-circuit protected with a maximum output current as defined in *Electrical Characteristics*.

8.3.9 Thermal Shutdown

There are two thermal sensors in TPS6572x located at the main sources of power dissipation: the charger and the LDO. The maximum temperature of the charger is regulated by reducing its charge current. If the temperature increases further, the charger is disabled. See details in *Battery Charging*.

The second sensor is enabled as soon as the LDO is enabled. As soon as the junction temperature, T_J, exceeds typically 150°C, the device goes into thermal shutdown. In this mode, the low side and high side MOSFETs are turned off. A thermal shutdown for the LDO will disable both, LDO and the DC-DC converter simultaneously.

8.3.10 LDO1

The low dropout voltage regulator is designed to operate well with low value ceramic input and output capacitors. The regulator operates with input voltages down to 1.8 V. The LDOs offer a maximum dropout voltage of 160 mV at rated output current. LDO1 supports a current limit feature. Its output voltage is adjustable using a resistor-divider at FB_LDO1 for TPS65721. The LDO1 voltage is fixed to 1.85 V for TPS65720 and TPS657201. For TPS657202, the default LDO1 voltage is 2.85 V.

8.3.10.1 Default Voltage Setting for LDOs and DCDC1

Following are the output voltages of the different versions:

- TPS65720
  - DCDC1: externally adjustable
  - LDO1: 1.85 V
- TPS657201
  - DCDC1: 1.85 V
  - LDO1: 1.85 V
- TPS657202
  - DCDC1: 1.90 V
  - LDO1: 2.85 V
- TPS65721
  - DCDC1: externally adjustable
  - LDO1: externally adjustable

The I^2C registers allow changing the default voltage for LDO1 in a range of 0.8 V to 3.3 V. For DCDC1, the register also allows setting any voltage in the range from 0.8 V to 3.3 V, however for the adjustable versions, the change in the I^2C register has no effect on the output voltage. The registers will be set to the default value when the voltage at SYS drops below the undervoltage lockout threshold or by a reset event ($\overline{\text{RESET}}$ output is actively pulled low). See *Register Maps* for more details.

Feature Description (continued)

8.3.10.2 Internal Analog Multiplexer (BAT, TS, TS_OUT); TPS657201, TPS657202 Only

The internal Multiplexer switches the analog voltage on Pin BAT (battery voltage) or on pin TS (battery NTC) to pin TS_OUT. The input is selected by Bit <OPAMP_MUX> in register CONTROL1. The input voltage range of 2.5 V to 4.5 V on pin BAT is internally scaled to a voltage of 0 V to 1.4 V on pin TS_OUT. If the battery temperature is selected as the input by setting <OPAMP_MUX> = 1, a temperature range of –20°C to 60°C is scaled to a voltage of 0 V to 1.4 V on pin TS_OUT. If the charger is not active, the internal current source for the NTC inside the battery pack is enabled automatically if the multiplexer is enabled with <OPAMP_EN> = 1 AND temperature measurement is selected by <OPAMP_MUX> = 1. If the analog multiplexer is disabled with <OPAMP_EN> = 0, the output VBAT/TS_OUT is shorted internally to GND, allowing for offset correction at the ADC. See Figure 15 for more details.

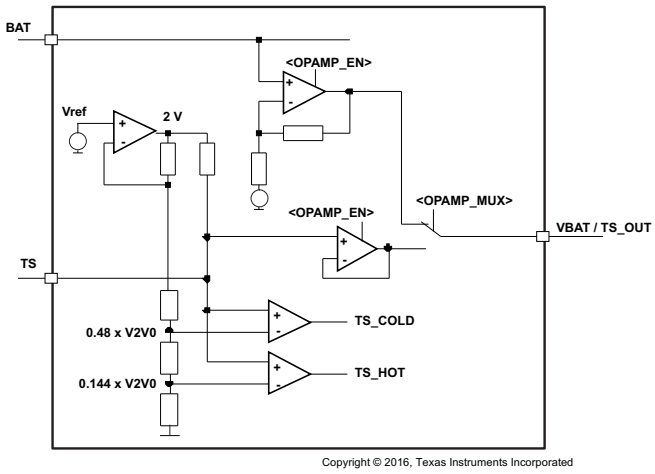


Figure 15. Multiplexer Block Diagram

The transfer function for the battery voltage is given in the Figure 16:

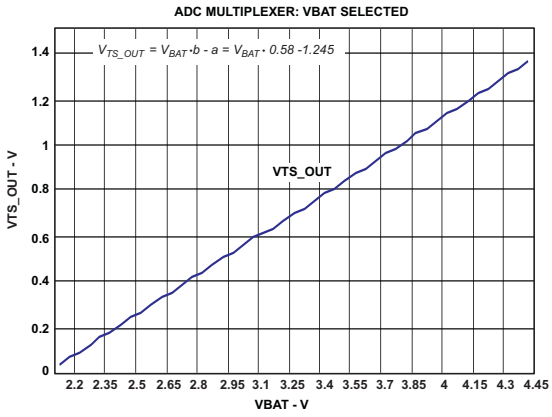


Figure 16. TS Multiplexer Output

8.3.10.3 Internal Battery Voltage Comparator

An internal comparator supervises the battery voltage at pin BAT when the device is configured for Li-primary battery (CH_EN = 0), compares it to a voltage defined with registers <VBAT1>, <VBAT0> and sets Bit <VBAT_COMP> in register CHCONFIG3 accordingly. An interrupt can be generated if the battery voltage falls below the threshold and the feature is unmasked in register IRMASK0. If the battery voltage comparator is disabled with VBAT_COMP_EN = 0 in register CHCONFIG2, the register containing the comparator output VBAT_COMP in CHCONFIG3 is read as a logic HIGH.

Feature Description (continued)

8.3.10.4 GPIOs, LED Drivers

TPS6572x contains 4 standard input/output pins (GPIOs) named GPIO0 to GPIO3. The output driver/input buffer is available in register GPIO_SSC while register GPIODIR selects the data direction and additional features. After RESET, GPIO0 and GPIO1 are pre-defined as general purpose inputs while GPIO2 and GPIO3 are configured as LED driver outputs which are high impedance. The LED driver outputs are designed to be constant current sinks to GND, sinking a constant current of 5 mA when enabled. The GPIOs do not have internal pull-up resistors. External pull-up resistors might be required if configured as inputs or outputs.

8.3.10.5 $\overline{\text{RESET}}$ Output

Actively low, open-drain reset output. Connect external pull-up resistor. The reset pin will go high impedance 100 ms after the reset condition is left. For TPS65720, TPS657201, TPS657202, reset is generated, depending on the power-good signal of LDO1, when the output voltage is below the threshold or LDO1 is disabled. For TPS65721, reset is generated depending on the voltage at pin THRESHOLD.

8.3.10.6 Threshold Input (TPS65721 Only)

This is an input to the comparator driving the $\overline{\text{RESET}}$ output. If the voltage applied at THRESHOLD is below the threshold, $\overline{\text{RESET}}$ is pulled actively LOW. If the voltage rises above the threshold + hysteresis, the $\overline{\text{RESET}}$ output is released after a delay time of 100 ms (typically).

8.3.10.6.1 ENABLE for DCDC1 and LDO1

The DCDC1 converter and LDO1 are enabled as soon as $\overline{\text{PB\_IN}}$ is pulled LOW OR input voltage at pin AC is detected (<CH_PGOOD> = 1).

There is a power-hold pin for DCDC1 (HOLD_DCDC1) and one for LDO1 (HOLD_LDO1). When HOLD_DCDC1 is pulled HIGH, DCDC1 is kept enabled after $\overline{\text{PB\_IN}}$ was released HIGH. HOLD_LDO1 serves the same function and keeps LDO1 enabled after $\overline{\text{PB\_IN}}$ was released HIGH. After first power-up by pulling $\overline{\text{PB\_IN}}$ = LOW or applying voltage at AC, the HOLD pins HOLD_DCDC1 and HOLD_LDO1 can also be used as enable pins, such that they turn on LDO1 or DCDC1, respectively when they are pulled HIGH. This function is available as long as there is a voltage at the battery. After the battery was removed or was discharged, first power-on needs to be done by pulling PB_IN = LOW.

Disabling the DC-DC converter or LDO, forces the device into shutdown, with a shutdown quiescent current as defined in *Electrical Characteristics*. In this mode, the low and high side MOSFETs are turned off and the entire internal control circuitry is switched-off. For proper operation the $\overline{\text{PB\_IN}}$, HOLD_DCDC1, EN_DLO1 pins must be terminated and must not be left floating.

8.3.10.6.2 $\overline{\text{PB\_IN}}$ Input

Enables DCDC1 and LDO1 if pulled to GND. Disables DCDC1 and LDO1 if pulled high. There is no internal pull-up resistor, so a resistor is needed externally to SYS. SYS is preferred over BAT because it is powered by either AC or BAT (whichever is higher). If BAT is used, the device may not get a valid HIGH signal if the battery is deeply discharged even when there is voltage at AC.

The input signal is debounced internally by 50 ms. When $\overline{\text{PB\_IN}}$ is pulled low, the DCDC1 converter and LDO1 will power up simultaneously. When PB_IN is deasserted, both converters are turned off. To leave the converters on, the HOLD_DCDC1 and HOLD_LDO1 pin need to be asserted high. The HOLD register Bit <CONTROL1:B5> will keep both, DCDC1 and LDO1 enabled if set to 1. For proper operation the $\overline{\text{PB\_IN}}$, HOLD_DCDC1 and HOLD_LDO1 pins must be terminated and must not be left floating.

Feature Description (continued)

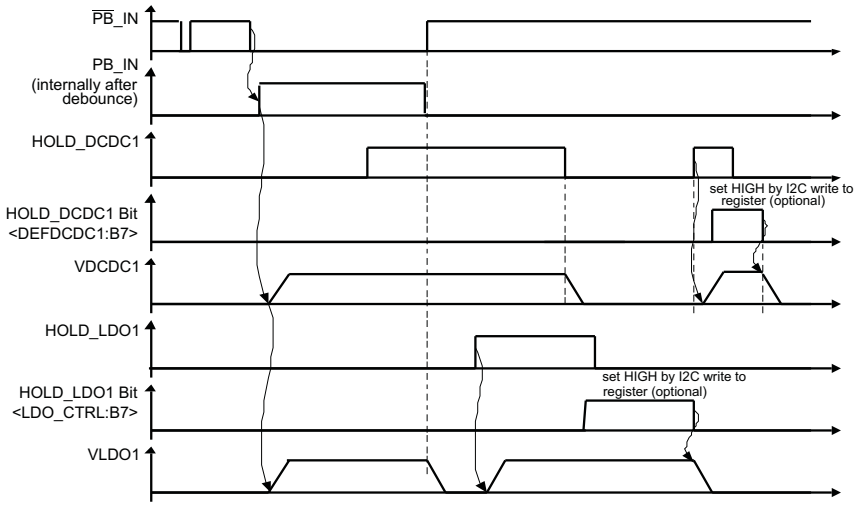


Figure 17. PB_IN Timing

8.3.10.6.3 HOLD_DCDC1 Input

Actively high hold input for DCDC1. Logically OR´d with the DCDC1 hold Bit <DEFDCDC1:B7>. If the input is driven HIGH after PB_IN was pulled LOW, the DCDC1 converter stays on after PB_IN was released.

8.3.10.6.4 HOLD_LDO1 Input

Actively high hold input for LDO1. Logically OR´d with the LDO1 hold Bit <LDO_CTRL:B7>. If the input is driven HIGH after PB_IN was pulled LOW, LDO1 stays on after PB_IN was released.

8.3.10.6.5 INT Output

Actively low, open-drain interrupt output. Connect external pull-up resistor. Interrupts are flagged in the registers IR0, IR1 and IR2 if the interrupt is not masked by registers IRMASK0, IRMASK1 and IRMASK2. Per default, all interrupts are masked. Interrupts which are unmasked will set the Bit in either on the rising edge or on both edges. Details can be found in the register description for IR0, IR1, and IR2 (see *Register Maps*). Any Bit in IR0, IR1 and IR2, set to 1 will drive the reset pin INT actively LOW.

The reset pin will go high impedance after the Bit generating the reset is read.

8.4 Device Functional Modes

8.4.1 Power Down

The charger remains in power-down mode when the input voltage at the AC pin is below the undervoltage lockout threshold (UVLO). During the power-down mode, the host commands through the I^2C interface are ignored. The Q1 FET connected between AC and SYS pins is off. The Q2 FET that connects BAT to SYS is ON.

(If <SYSOFF> = 1, Q2 is off). During power-down mode, the VOUT(SC2) circuitry is active and monitors for overload conditions on SYS.

8.4.2 Sleep Mode

The charger enters sleep mode when V_{AC} is greater than UVLO, but below V_{BAT} + $V_{IN(DT)}$. In sleep mode, the host commands are ignored. The Q1 FET connected between AC and SYS pins is off. The Q2 FET that connects BAT to SYS is ON. (If <SYSOFF> = 1, Q2 is off). During sleep mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on SYS.

Device Functional Modes (continued)

8.4.3 Standby Mode

When V_{AC} is greater than UVLO and VIN is greater than V_{BAT} + $V_{IN(DT)}$, the device is in standby mode. <CH_PGOOD> = 1 to indicate the valid power status and the host commands are read. The device enters standby mode whenever <AC input current1, AC input current0> = (1,1) or if an input overvoltage condition occurs. In standby mode, Q1 is OFF and Q2 is ON. (If <SYSOFF> = 1, Q2 is off). During standby mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on SYS.

8.4.4 Power-On Reset Mode

The charger enters power-on reset mode when the input voltage at AC is within the valid range: VAC > UVLO and VAC > VBAT + VIN(DT) and VAC < VOVP, and the Bits <AC input current1, AC input current0> indicate that the USB suspend mode is not enabled [<AC input current1, AC input current0>≠ (1,1)]. During power-on reset mode, all internal timers and other circuit blocks are activated. The device checks for short-circuits at the ISET pin. If no short conditions exists, the device switches on the input FET Q1 with a 100-mA current limit to check for a short circuit at SYS. If VOUT rises above VSC, the FET Q1 switches to the current-limit threshold set by <AC input current1, AC input current0>, and the device enters into the Idle mode.

8.4.5 Idle Mode

In the Idle mode, the system is powered by the input source (Q1 is on), and the device continuously monitors the status of the host commands. It also continuously monitors the input voltage conditions. Q2 is turned on whenever the input source cannot deliver the required load current (supplement mode). The device also enters Idle mode whenever <CH_EN> = 0 while the input voltage is in the valid range of operation.

8.5 Programming

8.5.1 Serial Interface

The serial interface is compatible with the standard and fast mode I^2C specifications, allowing transfers at up to 400 kHz. The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements and charger status to be monitored. Register contents remain intact as long as VCC remains above the UVLO threshold. The TPS6572x has a 7-bit address: 100 1000, other addresses are available upon contact with the factory. Attempting to read data from register addresses not listed in this section will result in 00h being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS6572x device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS6572x device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge–related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS6572x device must leave the data line high to enable the master to generate the stop condition.

For the WQFN version, the voltage the pull-up resistors for the I^2C interface at SCLK and SDAT are connected to, should be monitored by the reset circuitry. This is done by connecting THRESHOLD with a voltage divider to the voltage the SDAT and SCLK pins are pulled-up to. This is needed to ensure a falling supply voltage will cause a reset to the I^2C interface. Otherwise a START condition may be detected and the first access to the I^2C interface may return NO ACK (no acknowledge).

Programming (continued)

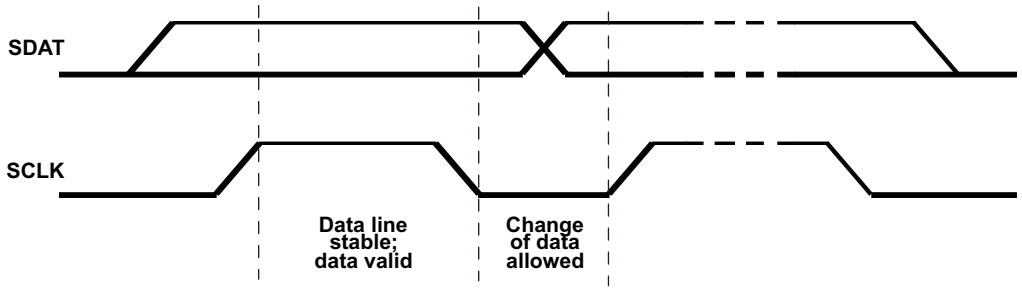


Figure 18. Bit Transfer on the Serial Interface

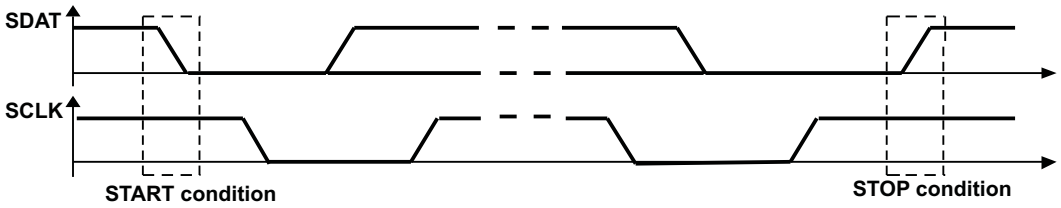
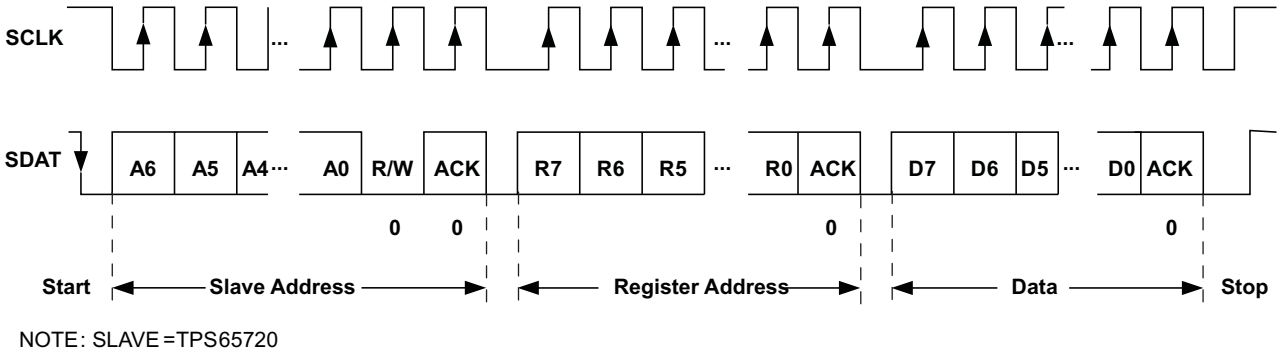
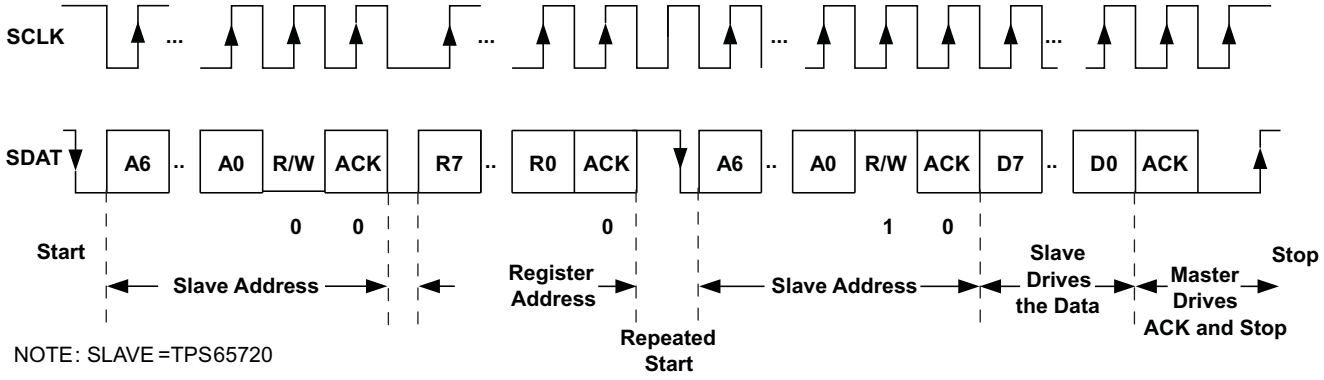


Figure 19. START and STOP Conditions



NOTE: SLAVE = TPS65720

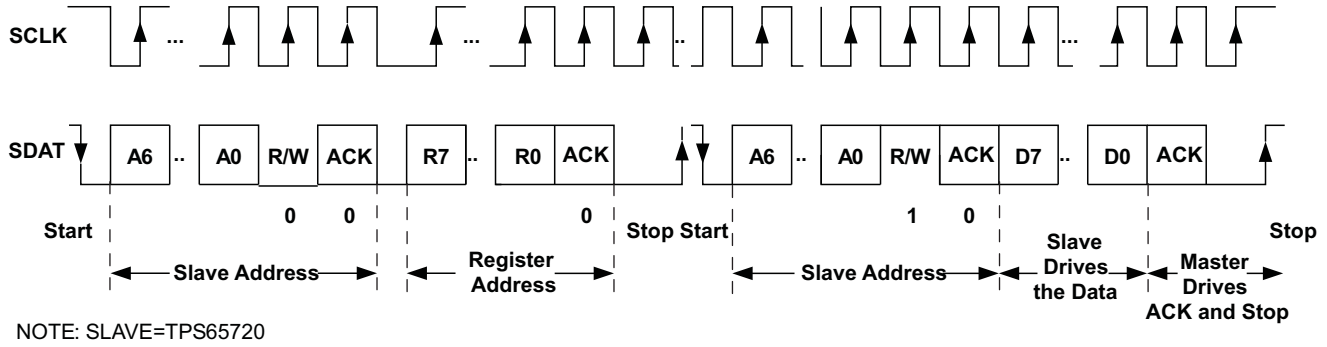
Figure 20. Serial I/f WRITE to TPS6572x Device



NOTE: SLAVE = TPS65720

Figure 21. Serial I/f READ From TPS6572x: Protocol A

Programming (continued)



NOTE: SLAVE=TPS65720

Figure 22. Serial I/f READ From TPS6572x: Protocol B

8.6 Register Maps

All registers are set to their default value by one of the following events:

- Voltage at the SYS pin is below the undervoltage lockout voltage (UVLO)
- RESET is active; $\overline{\text{RESET}}$ output is pulled LOW and goes high with a 100-ms delay

Table 2. Register Summary

ADDRESS	NAME	SHORT DESCRIPTION
0x01h	CHGSTATUS	Battery Charger Statuses
0x02h	CHGCONFIG0	Battery Charger Configuration and Control
0x03h	CHGCONFIG1	Battery Charger Configuration and Control
0x04h	CHGCONFIG2	Battery Charger Configuration and Control
0x05h	CHGCONFIG3	Battery Charger Configuration and Control
0x06h	CHGSTATE	Battery Charger Current State Notification
0x07h	DEFDCDC1	DCDC1 Output Voltage Setting and Control
0x08h	LDO_CTRL	LDO1 Output Voltage Setting and Control
0x09h	CONTROL0	Power Good Statuses and Force PWM Control
0x0Ah	CONTROL1	Miscellaneous Device Control and Push Button Status
0x0Bh	GPIO_SSC	Input Data for GPIOs If Set to Input Mode
0x0Ch	GPIO_DIR	GPIOs Configuration and Control
0x0Dh	IRMASK0	Interrupt Masking Control
0x0Eh	IRMASK1	Interrupt Masking Control
0x0Fh	IRMASK2	Interrupt Masking Control
0x10h	IR0	Interrupt Reporting
0x11h	IR1	Interrupt Reporting
0x12h	IR2	Interrupt Reporting

8.6.1 CHGSTATUS Register Address: 01h (read only)

CHGSTATUS	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	TS_HOT	TS_COLD	OVP		CH_ACTIVE	CH_PGOOD	CH_THLOOP	
Default	x	x	x	0	x	x	x	0
Default value loaded by:								
Read/write	R	R	R	R	R	R	R	R

Bit 7 TS_HOT:
0 = battery temperature is below high temperature threshold (45°C/50°C/55°C/60°C).
1 = battery temperature is above high temperature threshold (45°C/50°C/55°C/60°C).

Bit 6 TS_COLD:
0 = battery temperature is above low temperature threshold (0°C/5°C/10°C/15°C)
1 = battery temperature is below low temperature threshold (0°C/5°C/10°C/15°C)

Bit 5 OVP:
0 = Input overvoltage protection is not active (VAC<6.6 V)
1 = Input overvoltage protection is active (VAC>6.6 V)

Bit 3 CH_ACTIVE:
0 = charger is not active
1 = charger is charging the battery

Bit 2 CH_PGOOD:
0 = no input voltage at pin AC or voltage not inside the voltage range for changing
1 = power source is present and in the range valid for charging

Bit 1 CH_THLOOP:
0 = thermal loop or DPPM not active
1 = thermal loop or DPPM active, charge current is reduced due to thermal loop, low input voltage or system load.

8.6.2 CHGCONFIG0 Register Address: 02h (read/write)

CHGCONFIG0	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	VSYS1	VSYS0	AC input current1	AC input current0	TH_LOOP	DYN_TMR	TERM_EN	CH_EN
Default For TPS65720, TPS657201	0	1	1	0	1	1	1	1
Default for TPS657202	0	1	0	0	1	1	1	1
Default for TPS65721	1	0	1	0	1	1	1	1
Default value loaded by:	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7..6 VSYS1..VSYS0:

00 = the output voltage of the power path at pin SYS tracks the battery voltage;
VSYS = VBAT + 200 mV (Vbat > 3.3 V); VSYS = 3.4 V (VBAT ≤ 3.3 V); V_DPPM = 1 is forced in this case
01 = the output voltage of the power path at pin SYS is regulated to 4.4 V
10 = the output voltage of the power path at pin SYS is regulated to 5 V
11 = the output voltage of the power path at pin SYS is regulated to 5.5 V

Bit 5..4 AC input current1.. AC input current0:
00 = 100 mA, input voltage DPPM enabled
01 = 500 mA, input voltage DPPM enabled
10 = 500 mA, input voltage DPPM disabled
11 = USB suspend mode; standby

Bit 3 TH_LOOP:
0 = the thermal loop is disabled
1 = the thermal loop is enabled and the charge current is reduced if the temperature exceeds 125°C

Bit 2 DYN_TMR (dynamic timer function):
0 = safety timers run with their normal clock speed
1 = clock speed for the safety timers is reduced based on the actual charge current if DPPM or thermal loop is active

Bit 1 TERM_EN (charge termination enable):
0 = charge termination will not occur and the charger will always be on
1 = charge termination enabled based on timers and termination current

Bit 0 CH_EN:
0 = the charger is disabled
1 = the charger is enabled

8.6.3 CHGCONFIG1 Register Address: 03h (read/write)

CHGCONFIG1	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	I_PRE1	I_PRE0	ICH_SCL1	ICH_SCL0	I_TERM1	I_TERM0		
Default For TPS65720, TPS657201, TPS657202	0	1	0	1	0	1	0	0
Default for TPS65721	0	1	1	1	0	1	1	1
Default value loaded by:	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R		
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit 7..6 I_PRE1..I_PRE0 (Pre-charge current factor):
00 = 5% of value defined with ICH_SCL1, ICH_SCL0
01 = 10% of value defined with ICH_SCL1, ICH_SCL0
10 = 15% of value defined with ICH_SCL1, ICH_SCL0
11 = 20% of value defined with ICH_SCL1, ICH_SCL0

Bit 5..4 ICH_SCL1..ICH_SCL0 (charge current scaling factor):
00 = 25% of value defined with ISET resistor; safety timer will time out at 2x SFTY_TMR[0,1]
01 = 50% of value defined with ISET resistor; safety timer runs at its nominal time defined in SFTY_TMR[0,1]
10 = 75% of value defined with ISET resistor; safety timer will time out at 0.66x SFTY_TMR[0,1]
11 = 100% of value defined with ISET resistor; safety timer will time out at 0.5x SFTY_TMR[0,1]

Bit 3..2 I_TERM1..I_TERM0 (termination current scaling factor):
00 = 5% of value defined with ICH_SCL1, ICH_SCL0
01 = 10% of value defined with ICH_SCL1, ICH_SCL0
10 = 15% of value defined with ICH_SCL1, ICH_SCL0
11 = 20% of value defined with ICH_SCL1, ICH_SCL0

8.6.4 CHGCONFIG2 Register Address: 04h (read/write)

CHGCONFIG2	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	SFTY_TMR1 0	SFTY_TMR	PRE_TMR		NTC	V_DPPM	VBAT_COMP_EN	
Default	0	1	0	0	1	1	0	0
Default value loaded by:	UVLO/R	UVLO/R	UVLO/R		UVLO/R	UVLO/R	UVLO/R	
Read/write	R/W	R/W	R/W	R	R/W	R/W	R/W	R

Bit 7..6 SFTY_TMR1..SFTY_TMR0 (charge safety timer value):
00 = 4h
01 = 5h
10 = 6h
11 = 8h

Bit 5 PRE_TMR (pre-charge timer value):
0 = 30 min
1 = 60 min

Bit 3 NTC (sensor resistance):
0 = 100k NTC (I = 7.5 µA)
1 = 10k NTC (I = 75 µA)

Bit 2 V_DPPM (dynamic power path threshold):
0 = VBAT + 100 mV
1 = 4.3 V

Bit 1 VBAT_COMP_EN (battery voltage comparator enable):
0 = battery voltage comparator for Li-primary cells disabled; VBAT_COMP interrupt disabled
1 = battery voltage comparator for Li-primary cells enabled

8.6.5 CHGCONFIG3 Register Address: 05h (read/write)

CHGCONFIG3	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	CH_VLTG2	CH_VLTG1	CH_VLTG0	TMP_SHIFT1	TMP_SHIFT0	VBAT1	VBAT0	VBAT_COMP
Default	0	1	0	0	0	0	0	1
Default value loaded by:	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit 7..5 CH_VLTG2..CH_VLTG0 (charge voltage selection):
000 = 4.15 V
001 = 4.175 V
010 = 4.20 V
011 = 4.225 V
100 = 4.25 V
101 = 4.275 V
110 = 4.3 V
111 = 4.325 V

Bit 4..3 TMP_SHIFT1..TMP_SHIFT0 (battery temperature shift):
00 = the temperature for TS_COLD and TS_HOT is at 0°C/45°C
01 = the temperature window is shifted by 5°C to TS_COLD/TS_HOT = 5°C/50°C
10 = the temperature window is shifted by 10°C to TS_COLD/TS_HOT = 10°C/55°C
11 = the temperature window is shifted by 15°C to TS_COLD/TS_HOT = 15°C/60°C

Bit 2..1 VBAT1..VBAT0 (battery voltage comparator threshold; for Li primary cells):
00 = 2.2 V
01 = 2.3 V
10 = 2.4 V
11 = 2.5 V

Bit 0 VBAT_COMP (battery voltage comparator output):
0 = voltage above the threshold
1 = voltage below the threshold or comparator disabled

8.6.6 CHGSTATE Register Address: 06h (read only)

CHGSTATE	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	CH_SLEEP	CH_RESET	CH_IDLE	CH_PRECH	CH_CC_CV	CH_LDO	CH_FAULT	CH_SUSP
Default	X	X	X	X	X	X	X	X
Read/write	R	R	R	R	R	R	R	R

Bit 7 CH_SLEEP:
0 = charger is not in sleep state
1 = charger is in sleep state

Bit 6 CH_RESET:
0 = charger is not in reset state
1 = charger is in reset state

Bit 5 CH_IDLE:
0 = charger is not in idle state
1 = charger is in idle state

Bit 4 CH_PRECH:
0 = charger is not in precharge state
1 = charger is in precharge state

Bit 3 CH_CC_CV:
0 = charger is not in constant current mode or constant voltage mode
1 = charger is in constant current mode or constant voltage mode

Bit 2 CH_LDO:
0 = charger is not in LDO mode
1 = charger is in LDO mode

Bit 1 CH_FAULT:
0 = charger is not in fault state
1 = charger is in fault state

Bit 0 CH_SUSP:
0 = charger is not in suspend state
1 = charger is in suspend state

8.6.7 DEFDCDC1 Register Address: 07h (read/write)

DEFDCDC1	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	HOLD_ DCDC1	DCDC_DISCH	DCDC1[5]	DCDC1[4]	DCDC1[3]	DCDC1[2]	DCDC1[1]	DCDC1[0]
Default for TPS65720, TPS65721	0	0	1	0	1	0	0	1
Default for TPS657201	0	0	1	0	0	1	0	1
Default for TPS657202	0	0	1	0	0	1	1	0
Default value loaded by:	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 HOLD_DCDC1:
0 = DCDC1 is disabled when HOLD_DCDC1 pin is pulled LOW and $\overline{\text{PB\_IN}}$ is released HIGH
1 = DCDC1 stays enabled when HOLD_DCDC1 pin is pulled LOW and $\overline{\text{PB\_IN}}$ is released HIGH

Bit 6 DCDC_DISCH:
0 = DCDC1 output is not discharged when DCDC1 is disabled
1 = DCDC1 output is discharged when DCDC1 is disabled

Bit 5..0 Output voltage setting for DCDC1:
For reference only: A voltage change in the register will not have an effect on the output voltage for TPS65720 and TPS65721 as the voltage is set by an external resistor divider. Contact TI in case a fixed voltage version is needed.

A voltage change during operation must not exceed 8% of the value set in the register for each I^2C write access as this may trigger the internal power good comparator and will trigger the Reset of the device. This limitation is only for a voltage step to higher voltages. There is no limitation for programming lower voltages by I^2C.

	OUTPUT VOLTAGE [V]	B5	B4	B3	B2	B1	B0
0	0.800	0	0	0	0	0	0
1	0.825	0	0	0	0	0	1
2	0.850	0	0	0	0	1	0
3	0.875	0	0	0	0	1	1
4	0.900	0	0	0	1	0	0
5	0.925	0	0	0	1	0	1
6	0.950	0	0	0	1	1	0
7	0.975	0	0	0	1	1	1
8	1.000	0	0	1	0	0	0
9	1.025	0	0	1	0	0	1
10	1.050	0	0	1	0	1	0
11	1.075	0	0	1	0	1	1
12	1.100	0	0	1	1	0	0
13	1.125	0	0	1	1	0	1
14	1.150	0	0	1	1	1	0
15	1.175	0	0	1	1	1	1
16	1.200	0	1	0	0	0	0
17	1.225	0	1	0	0	0	1
18	1.250	0	1	0	0	1	0

	OUTPUT VOLTAGE [V]	B5	B4	B3	B2	B1	B0
19	1.275	0	1	0	0	1	1
20	1.300	0	1	0	1	0	0
21	1.325	0	1	0	1	0	1
22	1.350	0	1	0	1	1	0
23	1.375	0	1	0	1	1	1
24	1.400	0	1	1	0	0	0
25	1.425	0	1	1	0	0	1
26	1.450	0	1	1	0	1	0
27	1.475	0	1	1	0	1	1
28	1.500	0	1	1	1	0	0
29	1.525	0	1	1	1	0	1
30	1.550	0	1	1	1	1	0
31	1.575	0	1	1	1	1	1
32	1.600	1	0	0	0	0	0
33	1.650	1	0	0	0	0	1
34	1.700	1	0	0	0	1	0
35	1.750	1	0	0	0	1	1
36	1.800	1	0	0	1	0	0
37	1.850	1	0	0	1	0	1
38	1.900	1	0	0	1	1	0
39	1.950	1	0	0	1	1	1
40	2.000	1	0	1	0	0	0
41	2.050	1	0	1	0	0	1
42	2.100	1	0	1	0	1	0
43	2.150	1	0	1	0	1	1
44	2.200	1	0	1	1	0	0
45	2.250	1	0	1	1	0	1
46	2.300	1	0	1	1	1	0
47	2.350	1	0	1	1	1	1
48	2.400	1	1	0	0	0	0
49	2.450	1	1	0	0	0	1
50	2.500	1	1	0	0	1	0
51	2.550	1	1	0	0	1	1
52	2.600	1	1	0	1	0	0
53	2.650	1	1	0	1	0	1
54	2.700	1	1	0	1	1	0
55	2.750	1	1	0	1	1	1
56	2.800	1	1	1	0	0	0
57	2.850	1	1	1	0	0	1
58	2.900	1	1	1	0	1	0
59	2.950	1	1	1	0	1	1
60	3.000	1	1	1	1	0	0
61	3.100	1	1	1	1	0	1
62	3.200	1	1	1	1	1	0
63	3.300	1	1	1	1	1	1

8.6.8 LDO_CTRL Register Address: 08h (read/write)

LDO_CTRL	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	HOLD_LDO1	LDO1_DISCH	LDO1[5]	LDO1[4]	LDO1[3]	LDO1[2]	LDO1[1]	LDO1[0]
Default except TPS657202	0	1	1	0	0	1	0	1
Default for TPS657202	0	1	1	1	1	0	0	1
Default value loaded by:	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 HOLD_LDO1:
0 = LDO1 is disabled when HOLD_LDO1 pin is pulled LOW and $\overline{\text{PB\_IN}}$ is released HIGH
1 = LDO1 stays enabled when HOLD_LDO1 pin is pulled LOW and $\overline{\text{PB\_IN}}$ is released HIGH

Bit 6 LDO1_DISCH:
0 = LDO1 output is not discharged when LDO1 is disabled
1 = LDO1 output is discharged when LDO1 is disabled

Bit 5..0 LDO1 output voltage setting according to the table listed for DCDC1:
The voltage setting is only valid for TPS65720. For TPS65721, the LDO1 voltage is set by an external resistor-divider. The voltage setting is according to the same table given for DEFDCDC1.

8.6.9 CONTROL0 Register Address: 09h (read/write)

CONTROL0	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	F_PWM	PGOODZ_DCDC1	PGOODZ_LDO1					
Default	0	PGOODDCDC1	PGOODLDO1	0	0	0	0	0
Default value loaded by:	UVLO/R							
Read/write	R/W	R	R	R	R	R	R	R

Bit 7 F_PWM:
0 = DC-DC converter is in PWM/PFM mode
1 = DC-DC converter is in forced PWM mode

Bit 6 PGOODZ_DCDC1:
0 = indicates that the DC-DC converters output voltage is within its nominal range
1 = range indicates that the DC-DC converters output voltage is below the target regulation voltage or disabled

Bit 5 PGOODZ_LDO1:
0 = indicates that the LDO1 output voltage is within its nominal range
1 = indicates that the LDO1 output voltage is below the target regulation voltage or disabled

8.6.10 CONTROL1 Register Address: 0Ah (read/write)

CONTROL1	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function			HOLD	PB_STAT		OPAMP_MUX	OPAMP_EN	RESET_DELAY
Default	0	0	0		0	1	0	1
Default value loaded by:			UVLO/R	UVLO/R		UVLO/R	UVLO/R	UVLO/R
Read/write	R	R	R	R/W	R	R/W	R/W	R/W

Bit 5 HOLD (ORed with $\overline{PB\_IN}$):
0 = DCDC1 and LDO1 switched off
1 = DCDC1 and LDO1 enabled

Bit 4 PB_STAT (push-button status, after debounce):
0 = push-button not pressed
1 = push-button pressed

Bit 2 OPAMP_MUX (only for TPS657201):
0 = battery voltage measurement
1 = temperature measurement

Bit 1 OPAMP_EN (only for TPS657201):
0 = OPAMP and MUX disabled; enabled automatically if <CH_PGOOD> = 1
1 = OPAMP and MUX enabled

Bit 0 RESET_DELAY:
0 = 11 ms
1 = 90 ms

8.6.11 GPIO_SSC Register Address: 0Bh (read/write)

GPIO_SSC	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function					GPIO3	GPIO2	GPIO1	GPIO0
Default	0	0	0	0	1	1	1	1
Default value loaded by:					UVLO/R	UVLO/R	UVLO/R	UVLO/R
Read/write	R	R	R	R/W	R	R	R	R/W

Bit 3 GPIO3:
0 = data in input buffer / actively pulled low when configured as an output or LED driver enabled
1 = data in input buffer / high impedance when configured as an output or LED driver

Bit 2 GPIO2:
0 = data in input buffer / actively pulled low when configured as an output or LED driver enabled
1 = data in input buffer / high impedance when configured as an output or LED driver

Bit 1 GPIO1:
0 = data in input buffer / actively pulled low when configured as an output
1 = data in input buffer / high impedance when configured as an output

Bit 0 GPIO0:
0 = data in input buffer / actively pulled low when configured as an output
1 = data in input buffer / high impedance when configured as an output

8.6.12 GPIODIR Register Address: 0Ch (read/write)

GPIODIR	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	GPIO3_LED	GPIO2_LED			GPIO3_DIR	GPIO2_DIR	GPIO1_DIR	GPIO0_DIR
Default	1	1	1	1	0	0	1	1
Default value loaded by:	UVLO/R	UVLO/R			UVLO/R	UVLO/R	UVLO/R	UVLO/R
Read/write	R/W	R/W	R	R	R/W	R/W	R/W	R/W

Bit 7 GPIO3_LED:
0 = GPIO3 is configured as a standard GPIO
1 = GPIO3 is configured as 5-mA LED driver

Bit 6 GPIO2_LED:
0 = GPIO2 is configured as a standard GPIO
1 = GPIO2 is configured as 5-mA LED driver

Bit 3 GPIO3_DIR:
0 = GPIO3 is configured as an output / LED driver
1 = GPIO3 is configured as an input

Bit 2 GPIO2_DIR:
0 = GPIO2 is configured as an output / LED driver
1 = GPIO2 is configured as an input

Bit 1 GPIO1_DIR:
0 = GPIO1 is configured as an output
1 = GPIO1 is configured as an input

Bit 0 GPIO0_DIR:
0 = GPIO0 is configured as an output
1 = GPIO0 is configured as an input

8.6.13 IRMASK0 Register Address: 0Dh (read/write)

IRMASK0	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	M_TS_HOT	M_TS_COLD	M_OVP	Reserved	M_CH_ ACTIVE	M_CH_ PGOOD	M_VBAT_ COMP	M_THLOOP
Default	1	1	1	1	1	1	1	1
Default value loaded by:	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7..0 charger interrupt mask register:
0 = Interrupt not masked
1 = Interrupt masked (no interrupt based on the event)

8.6.14 IRMASK1 Register Address: 0Eh (read/write)

IRMASK1	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	M_CH_ SLEEP	M_CH_ RESET	M_CH_IDLE	M_CH_PRECH	M_CH_CC_ CV	M_CH_ LDO	M_CH_ FAULT	M_CH_ SUSP
Default	1	1	1	1	1	1	1	1
Default value loaded by:	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7..0 charger state interrupt mask register:
0 = Interrupt not masked
1 = Interrupt masked (no interrupt based on the event)

8.6.15 IRMASK2 Register Address: 0Fh (read/write)

IRMASK2	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	M_GPIO3	M_GPIO2	M_GPIO1	M_GPIO0	M_PGOODZ_ DCDC1	M_PGOODZ_ LDO1	M_PB_ STAT	
Default	1	1	1	1	1	1	1	1
Default value loaded by:	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit 7..0 charger state interrupt mask register:
0 = Interrupt not masked
1 = Interrupt masked (no interrupt based on the event)

8.6.16 IR0 Register Address: 10h (read only)

IR0	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	TS_HOT	TS_COLD	OVP	Reserved	CH_ACTIVE	CH_PGOOD	VBAT_COMP	TH_LOOP
Default	0	0	0	0	0	0	0	0
Default value loaded by:	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R
Set by:	Rising edge of TS_HOT	Rising edge of TS_COLD	Rising edge of OVP	Reserved	Rising edge and falling edge of CH_ACTIVE	Rising edge and falling edge of CH_PGOOD	Rising edge of VBAT_COMP*	Rising edge of TH_LOOP
Read/write	R	R	R	R	R	R	R	R

Bit 7..2 interrupt register:
0 = no interrupt
1 = Interrupt occurred (cleared when read); interrupt not masked in register IRMASK0

The VBAT_COMP interrupt is automatically disabled when the battery voltage comparator is disabled by clearing Bit 1 in register 04h (VBAT_COMP_EN)

8.6.17 IR1 Register Address: 11h (read)

IR1	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	CH_SLEEP	CH_RESET	CH_IDLE	CH_PRECH	CH_CC_CV	CH_LDO	CH_FAULT	CH_SUSP
Default	0	0	0	0	0	0	0	0
Default value loaded by:	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R
Set by:	Rising edge of CH_SLEEP	Rising edge of CH_RESET	Rising edge of CH_IDLE	Rising edge of CH_PRECH	Rising edge of CH_CC_CV	Rising edge of CH_LDO	Rising edge of VBAT_FAULT*	Rising edge of TH_SUSP
Read/write	R	R	R	R	R	R	R	R

Bit 7..0 interrupt register:
0 = no interrupt
1 = Interrupt occurred (cleared when read); interrupt not masked in register IRMASK1

8.6.18 IR2 Register Address: 12h (read)

IR2	B7	B6	B5	B4	B3	B2	B1	BO
Bit name and function	GPIO3	GPIO2	GPIO1	GPIO0	PGOODZ_ DCDC1	PGOODZ_ LDO1	PB_STAT	
Default	0	0	0	0	0	0	0	0
Default value loaded by:	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	UVLO/R	
Set by:	Rising and falling edge of GPIO3	Rising and falling edge of GPIO2	Rising and falling edge of GPIO1	Rising and falling edge of GPIO0	Rising edge of PGOODZ_ DCDC1	Rising edge of PGOODZ_ LDO1	Rising and falling edge of PB_ STAT	
Read/write	R	R	R	R	R	R	R	R

Bit 7..4 GPIO interrupt register:
0 = GPIO status did not change
1 = GPIO status changed; cleared when read; interrupt not masked in register IRMASK2

Bit 3..2 power good interrupt register:
0 = no interrupt (power good)
1 = interrupt occurred (output voltage of DCDC converter or LDO too low); cleared when read

Bit 1 PB_STAT interrupt register:
0 = no interrupt
1 = interrupt occurred; cleared when read; interrupt not masked in register IRMASK2

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The intended applications for the TPS6572x device are small handheld or wearable devices powered from a single cell Lithium-Ion battery. The input path current limit is great for charging from USB sources by allowing the selection between 100-mA or 500-mA input supply current.

9.2 Typical Application

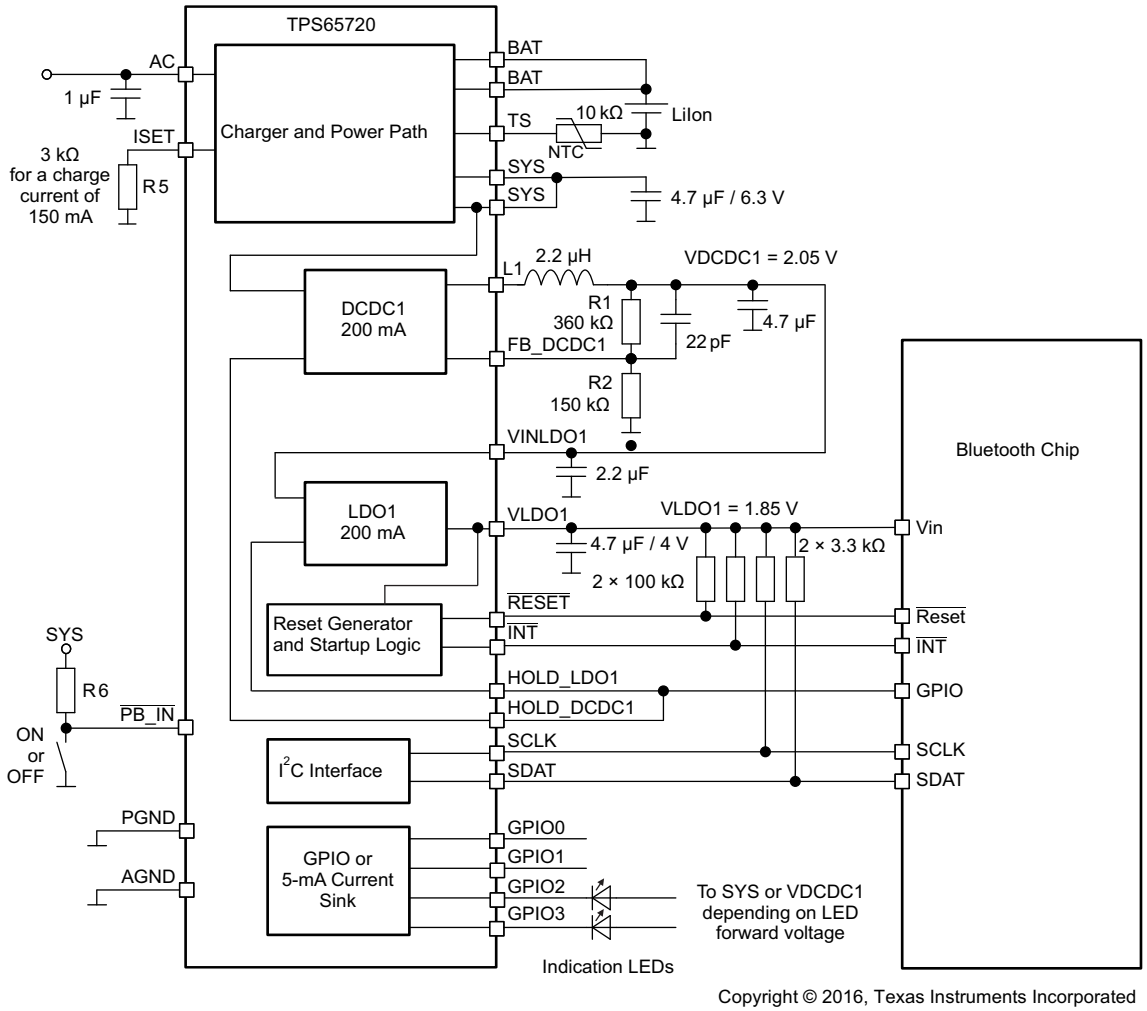


Figure 23. Typical Bluetooth Application

Typical Application (continued)

9.2.1 Design Requirements

With only a handful of required components to operate the TPS6572x, designing with the TPS6572x is easy. After setting the output voltage of both the LDO and DC-DC, it is required to select appropriate output filter in-order to ensure best operation of the DC-DC. The TPS6572x requires appropriate input and output capacitors for the DC-DC and LDO. The battery charger requires the charge current to be set by the use a resistor and may require an NTC thermistor at the battery.

For noise sensitive devices it is required to use a larger inductance value in-order to reduce the output ripple. Cascading the LDO from the DC-DC is great technique to reduce noise injected into the load and maintaining the high efficiency step-down from the DC-DC input to the LDO output.

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Setting

9.2.2.1.1 DCDC1

For TPS65720 and TPS65721, the output voltage of the DCDC converter can be set with external resistor network on Pin FB_DCDC1. The feedback voltage is 0.6 V.

TI recommends setting the total resistance of R1 + R2 to less than 1 MΩ. Route the FB_DCDC1 trace separate from noise sources, such as the inductor trace (L1).

$$V_{FB\text{-}DCDC1} = 0.6\ V$$

$$V_{OUT} = V_{FB\_DCDC1} \times \frac{R1 + R2}{R2} \qquad R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB\_DCDC1}} \right) - R2 \tag{3}$$

Table 3. Typical Resistor Values

OUTPUT VOLTAGE	R1	R2	NOMINAL VOLTAGE
3.3 V	680 kΩ	150 kΩ	3.32 V
3 V	510 kΩ	130 kΩ	2.95 V
2.85 V	560 kΩ	150 kΩ	2.84 V
2.5 V	510 kΩ	160 kΩ	2.51 V
2.05 V	360 kΩ	150 kΩ	2.04 V
2 V	470 kΩ	200 kΩ	2.01 V
1.8 V	300 kΩ	150 kΩ	1.8 V
1.6 V	200 kΩ	120 kΩ	1.6 V
1.5 V	300 kΩ	200 kΩ	1.5 V
1.2 V	330 kΩ	330 kΩ	1.2 V

A feedforward capacitor in parallel to the resistor from Vout to FB_DCDC1 is required. Its value should be based on transient performance and will be in the range from 4.7 pF to 22 pF.

For TPS657201, the output voltage of DCDC1 is fixed at 1.85 V per default and can be changed in register DEFDCDC1. For TPS657202, the default output voltage is 1.9 V. The feedback connection has to be made from pin FB_DCDC1 to the output capacitor directly. A voltage change to a higher voltage needs to be accomplished in steps of 8% maximum otherwise the power-good comparator will detect a too low voltage, will trigger and generate a reset. There is no limitation in programming output voltages to lower values.

9.2.2.1.2 LDO1

For TPS65720 and TPS657201, the default output voltage is 1.85 V while the default output voltage is 2.85 V for TPS657202, defined by register LDO_CTRL. The programmable voltage range is 0.8 V to 3.3 V. A voltage change to a higher voltage needs to be accomplished in steps of 8% maximum otherwise the power-good comparator will detect a too low voltage, will trigger and generate a reset. There is no limitation in programming output voltages to lower values.

For the TPS65721, the output voltage for LDO1 is externally adjustable using a resistor-divider at pin FB_LDO1. The feedback voltage is 0.8 V and the total resistance of the voltage divider should be kept in the 100-kΩ to 1-MΩ range. A feed-forward capacitor in parallel to the resistor from Vout to FB_LDO1 is required. It´s value should be based on transient performance and will be in the range from 4.7 pF to 22 pF.

The output voltage with an internal reference voltage $V_{FB\text{-}LDO1}$ = 0.8 V is calculated by Equation 4:

$$V_{OUT} = V_{FB\_LDOx} \times \frac{R3 + R4}{R4} \qquad R3 = R4 \times \left(\frac{V_{OUT}}{V_{FB\_LDO1}} \right) - R4 \tag{4}$$

Table 4. Typical Resistor Values

OUTPUT VOLTAGE	R3	R4	NOMINAL VOLTAGE
3.3 V	470 kΩ	150 kΩ	3.31 V
1.85 V	200 kΩ	150 kΩ	1.86 V
1.8 V	300 kΩ	240 kΩ	1.80 V

9.2.2.2 Output Filter Design (Inductor and Output Capacitor)

9.2.2.2.1 Inductor Selection

The converter operates typically with 3.3-µH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance will influence directly the efficiency of the converter. Therefore an inductor with lowest DC resistance should be selected for highest efficiency.

Equation 5 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 5. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \qquad I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \tag{5}$$

where

- f = Switching Frequency (2.25 MHz typical)
- L = Inductor Value
- ΔI_L = Peak-to-Peak inductor ripple current
- I_{Lmax} = Maximum Inductor current

The highest inductor current will occur at maximum Vin.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies.

Refer to Table 5 and the typical applications for possible inductors.

Table 5. Tested Inductors

INDUCTOR TYPE	INDUCTOR VALUE	SUPPLIER	COMMENTS
LQM21P	3.3 µH	Murata	For TPS65720
BRC1608T2R2M	2.2 µH	Taiyo Yuden	For TPS65720; Smallest solution size; up to 150 mA of output current
VLS201610ET-2R2M	2.2 µH	TDK	For TPS65720, TPS65721, TPS657201, TPS657202
GLFR1608T2R2M-LR	2.2 µH	TDK	For TPS65720; Smallest solution size; up to 150 mA of output current
MIPSA2520	2.2 µH	FDK	For TPS65721, TPS657201, TPS657202; highest efficiency

9.2.2.2.2 Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the step-down converter allows the use of small ceramic capacitors with a typical value of 10 µF, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple and are therefore recommended. For an inductor value of 3.3 µH, an output capacitor with 4.7 µF can be used. Refer to recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. Just for completeness the RMS ripple current is calculated by Equation 6:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (6)$$

At nominal load current the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor, as calculated by Equation 7:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (7)$$

Where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents the converter operates in power save mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

9.2.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes (see Table 6). The converters need a ceramic input capacitor of 4.7 µF. The input capacitor can be increased without any limit for better input voltage filtering.

Table 6. Tested Capacitors

TYPE	VALUE	VOLTAGE RATING	SIZE	SUPPLIER	MATERIAL
GRM155R60G475ME47D	4.7 µF	4 V	0402	Murata	Ceramic X5R
GRM155R60J225ME15D	2.2 µF	6.3 V	0402	Murata	Ceramic X5R
GRM188R60J475K	4.7 µF	6.3 V	0603	Murata	Ceramic X5R
GMK107BJ105K	1 µF	35 V	0603	Taiyo Yuden	Ceramic X5R

9.2.2.3 Charger/Power Path

9.2.2.3.1 Charger Stability

To ensure stable operation of the charger including the power path, a list of components and their recommended value is given in Table 7. These values represent the capacitance or inductance value in the application under the given operating conditions. For example, ceramic capacitors will typically show a drop in capacitance when a DC voltage is applied. Due to this dc bias effect, the capacitance in the applications when voltage is applied is much less than the nominal capacitor value. See the capacitor manufacturer data sheet for derating.

At pin AC, a series inductance of may be used with a values as stated in Table 7.

Pins AC, SYS and BAT have been tested to be stable with the values given in Table 7:

Table 7. Recommended Components for Charger

PIN NAME	Cmin (µF)	Cmax (µF)	Lmin (µH)	lmax (µH)
AC	0.1	1	0	2
SYS	1	10	—	—
BAT	0.1	4.7	—	—

9.2.2.3.2 Setting the Charge Current

The charge current is set with an external resistor connected form ISET to GND.

The resulting charge current is calculated by Equation 8:

$$I_{CHARGE} = \frac{K_{SET}}{R_{SET}} \qquad R_{SET} = \frac{K_{SET}}{I_{SET}} \tag{8}$$

Additionally, the charge current can be scaled to 100%, 75%, 50%, or 25% of the value set by Rset by software in register CHCONFIG1 using Bits ICH_SCL[1,0]. Precharge current and termination current is scaled accordingly.

9.2.2.3.3 Dynamic Power Path Management (DPPM)

The charger/power path in TPS6572x contains two different features to ensure there is sufficient power at the load and the input voltage supplying the charger/power path does not collapse.

First there is output voltage DPPM, which is a control loop to keep the voltage at the output of the power path above a certain limit. In TPS6572x, the voltage at the output of the power path (SYS) is regulated to what is defined with VSYS[1,0] in register CHCONFIG0. When the current needed for the load and for charging the battery exceeds the input current limit, the voltage at SYS will collapse. The DPPM loop will reduce the charge current, such that the total current for the load and the charge current equals the input current limit. This is done as soon as the voltage at SYS drops 100 mV below the target voltage.

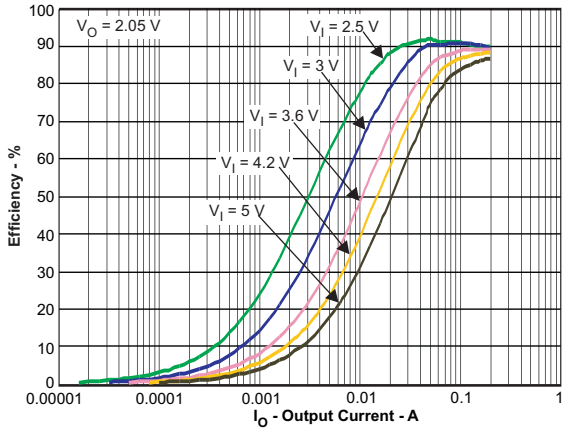
Second there is input voltage DPPM. For this, the input voltage to the charger/power path at pin AC is sensed to avoid the voltage from a USB port or dedicated charger to drop below a certain limit. This control loop will reduce the input current limit for pin AC as soon as the voltage at AC drops below 4.5 V (typically). With Bits ACinputcurrent[1,0] set to 00 or 01, input voltage DPPM is enabled, with ACinputcurrent=10, input voltage DPPM is disabled.

9.2.3 Application Curves

The graphs have been generated on the TPS65720YFF EVM with the inductors as mentioned in the graphs. See the *TPS65720EVM User's Guide* for details on the layout.

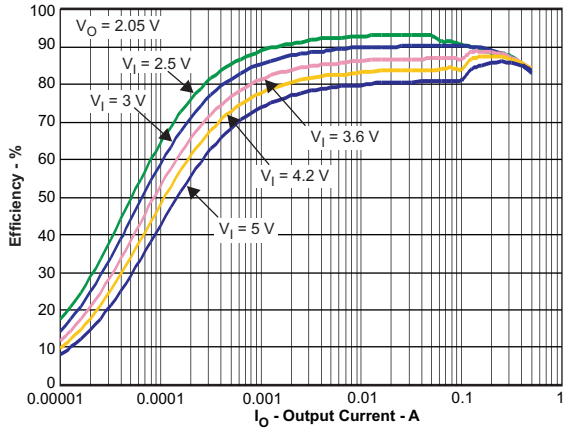
Table 8. Table Of Graphs

		FIGURE
TPS65720: Efficiency DCDC1 vs Load Current / PWM mode 200 mA; L = Murata LQM21P 3.3 µH	V_O = 2.05 V; V_I = 3 V, 3.6 V, 4.2 V, 5 V	Figure 24
TPS65720: Efficiency DCDC1 vs Load Current / PFM mode 200 mA; L = Murata LQM21P 3.3 µH	V_O = 2.05 V; V_I = 3 V, 3.6 V, 4.2 V, 5 V	Figure 25
TPS65720: Efficiency DCDC1 vs Load Current / PWM mode 200 mA; L = FDK MIPSA2520 2.2 µH	V_O = 2.05 V; V_I = 3 V, 3.6 V, 4.2 V, 5 V	Figure 26
TPS65720: Efficiency DCDC1 vs Load Current / PFM mode 200 mA; L = FDK MIPSA2520 2.2 µH	V_O = 2.05 V; V_I = 3 V, 3.6 V, 4.2 V, 5 V	Figure 27
TPS65721: Efficiency DCDC1 vs Load Current / PWM mode; L = FDK MIPSA2520 2.2 µH	V_O = 3.3 V; V_I = 3 V, 3.6 V, 4.2 V, 5 V	Figure 28
TPS65721: Efficiency DCDC1 vs Load Current / PFM mode 500 mA; L = FDK MIPSA2520 2.2 µH	V_O = 3.3 V; V_I = 3 V, 3.6 V, 4.2 V, 5 V	Figure 29
TPS65721: Efficiency DCDC1 vs Load Current / PWM mode; L = FDK MIPSA2520 2.2 µH	V_O = 1.8 V; V_I = 3 V, 3.6 V, 4.2 V, 5 V	Figure 30
TPS65721: Efficiency DCDC1 vs Load Current / PFM mode 500 mA; L = FDK MIPSA2520 2.2 µH	V_O = 1.8 V; V_I = 3 V, 3.6 V, 4.2 V, 5 V	Figure 31
Load Transient Response DCDC1; L = FDK MIPSA2520 2.2 µH, PFM mode	Scope plot I_O = 20 mA to 180 mA; V_O = 2.05 V; V_I = 3.6 V	Figure 32
Load Transient Response DCDC1; L = FDK MIPSA2520 2.2 µH, PWM mode	Scope plot I_O = 50 µA to 60 mA; V_O = 2.05 V; V_I = 3.6 V	Figure 33
Load Transient Response DCDC1; L = FDK MIPSA2520 2.2 µH, PWM mode	Scope plot I_O = 40 mA to 360 mA; V_O = 3.3 V; V_I = 3.6 V	Figure 34
Line Transient Response DCDC1; L = FDK MIPSA2520 2.2 µH, PWM mode	Scope plot; V_O = 2.05 V V_I = 3.6 V to 5 V to 3.6 V; I_O = 60 mA	Figure 35
Output Voltage Ripple in PFM Mode; DCDC1	Scope plot: V_I = 3.6 V V_O = 2.05 V; I_O = 50 µA (PFM); I_O = 60 mA (PWM)	Figure 36
Output Voltage Ripple in PWM Mode; DCDC1	Scope plot: V_I = 3.6 V V_O = 2.05 V; I_O = 60 mA (PWM)	Figure 37
Load Transient Response LDO1	Scope plot; V = 1.85 V; V_I = 2.05 V I = 50 µA to 60 mA to 50 µA	Figure 38
Line Transient Response LDO1	Scope plot; V_O = 1.85 V; V_I = 5 V to 3.6 V to 5 V	Figure 39
Efficiency vs Lout for DCDC1 = 2.05 V, LDO1 = 1.85 V, VinLDO = VDCDC1		Figure 40



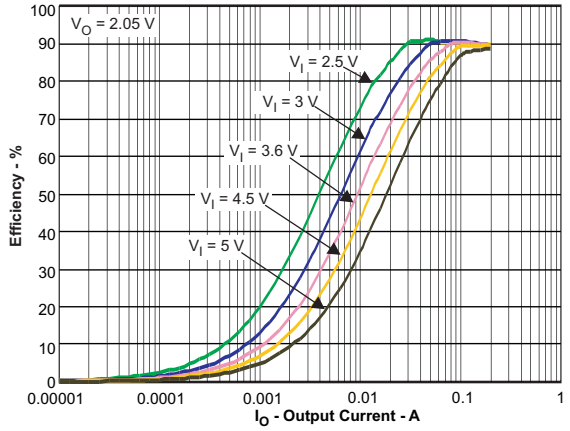
PWM Mode Inductor: LQM21P 3.3 µH

Figure 24. TPS65720 Efficiency of DCDC1 vs Load Current



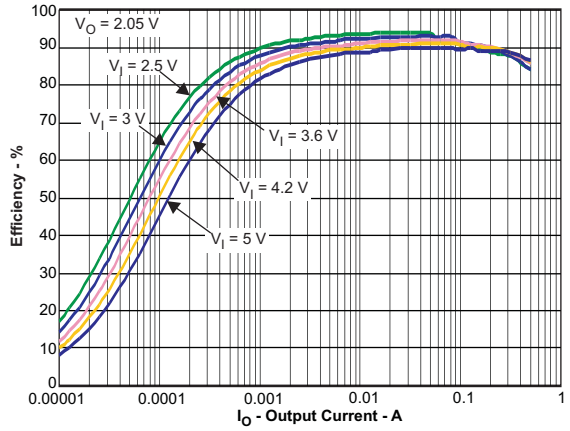
PFM Mode Inductor: LQM21P 3.3 µH

Figure 25. TPS65720 Efficiency of DCDC1 vs Load Current



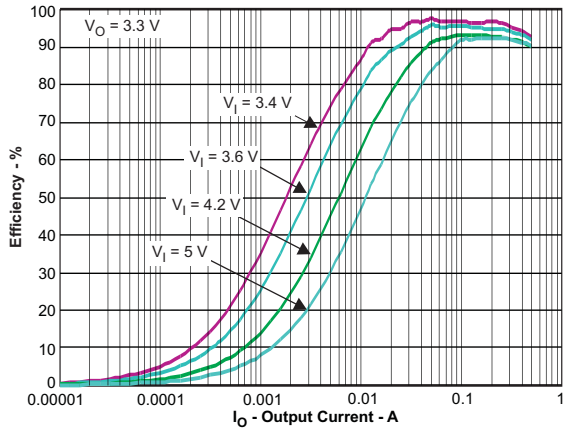
PWM Mode Inductor: MIPSA2520 2.2 µH

Figure 26. TPS65720 Efficiency of DCDC1 vs Load Current



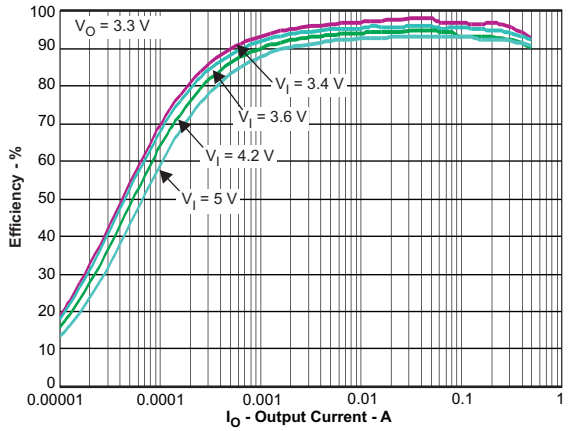
PFM Mode Inductor: MIPSA2520 2.2 µH

Figure 27. TPS65720 Efficiency of DCDC1 vs Load Current



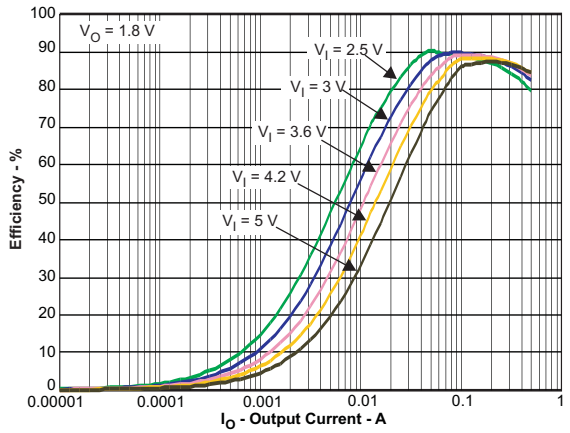
PWM Mode Inductor: MIPSA2520 2.2 µH

Figure 28. TPS65721 Efficiency of DCDC1 vs Load Current



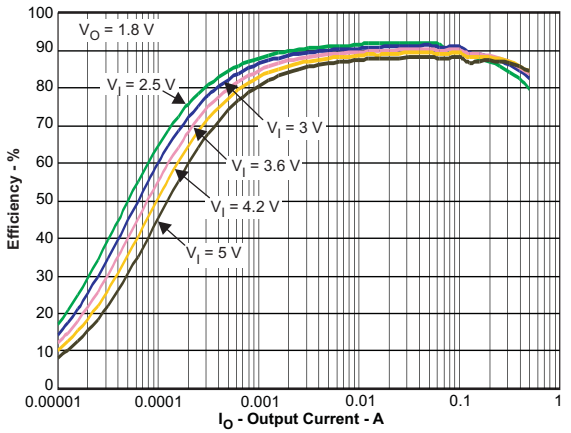
PFM Mode Inductor: MIPSA2520 2.2 µH

Figure 29. TPS65721 Efficiency of DCDC1 vs Load Current



PWM Mode Inductor: MIPSA2520 2.2 µH

Figure 30. TPS65721 Efficiency of DCDC1 vs Load Current



PFM Mode Inductor: MIPSA2520 2.2 µH

Figure 31. TPS65721 Efficiency of DCDC1 vs Load Current

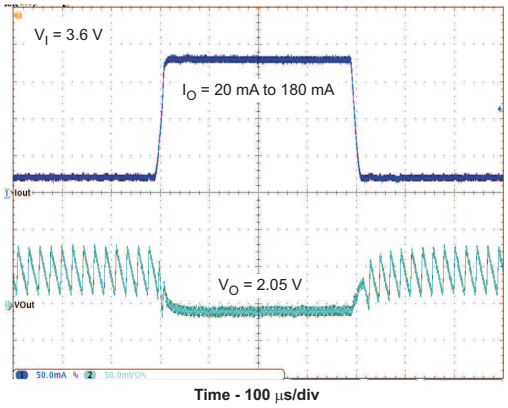


Figure 32. Load Transient Response PFM Mode

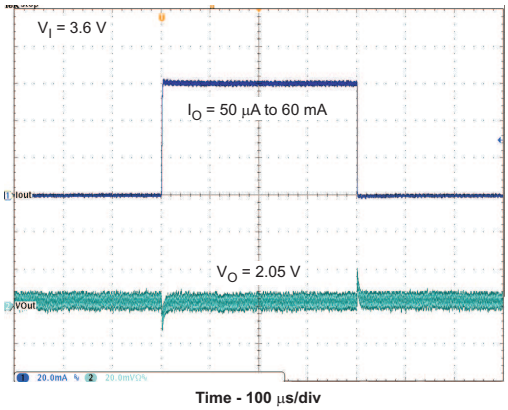


Figure 33. Load Transient Response PWM Mode

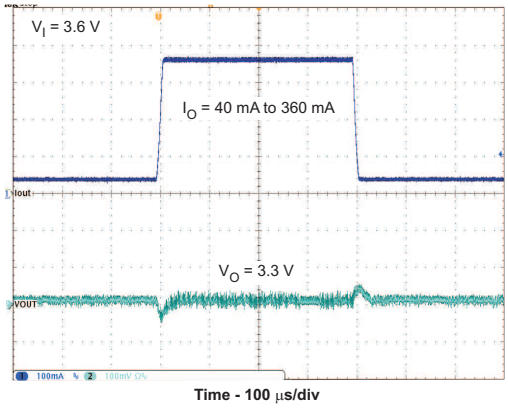


Figure 34. Load Transient Response PWM Mode

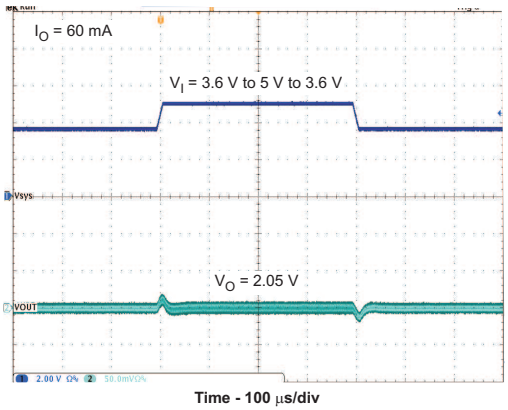


Figure 35. Line Transient Response PWM Mode

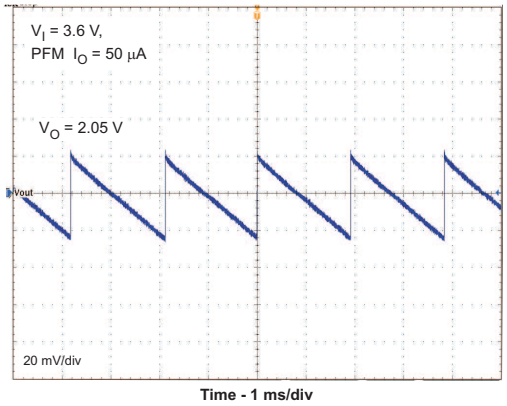


Figure 36. Output Voltage Ripple on DCDC1 PFM Mode

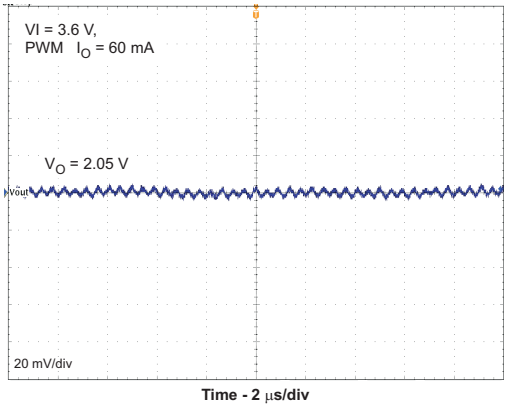


Figure 37. Output Voltage Ripple on DCDC1 PWM Mode

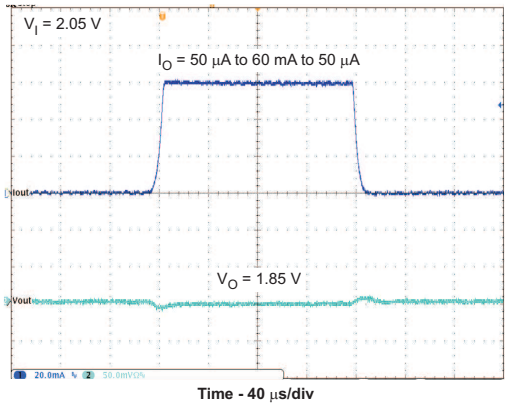


Figure 38. Load Transient Response LDO1

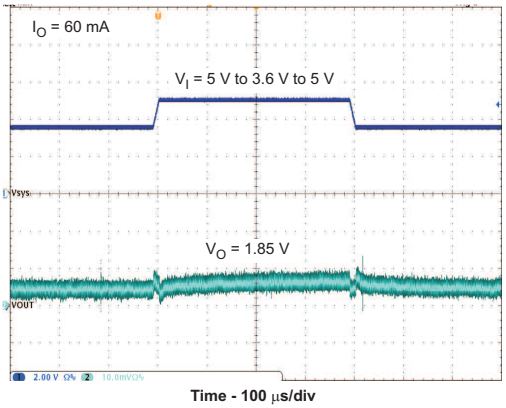
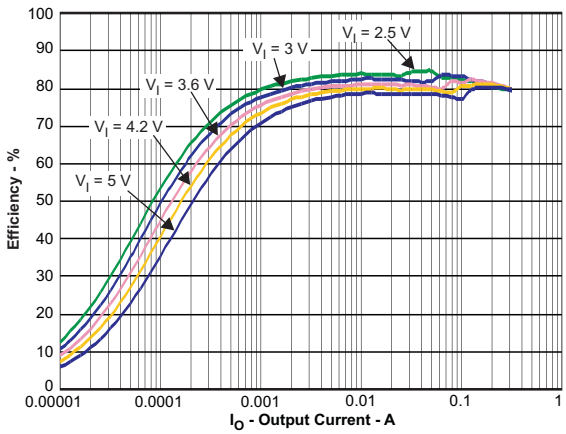


Figure 39. Line Transient Response LDO1



LDO1 powered by DCDC1 with VDCDC1 = 2.05 V

VLDO1 = 1.85 V

Figure 40. Efficiency vs Output Current for the Complete System

10 Power Supply Recommendations

The TPS6572x device has two paths for input supply, battery and AC adaptor or USB input. The AC pin the main input supply can be operated with a power supply from a USB or AC adaptor. The input voltage on the AC pin is recommended to be operated with a voltage between the V_{AC_LOW} and V_{OVP} of the device for most cases and charging capabilities. The battery can be supplied through the BAT pin and a Li-Ion signal cell battery is recommended for most applications.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulators may show poor line or load regulation, and additional stability issues as well as EMI problems. Providing a low impedance ground path is critical. Therefore, use wide and short traces for the main current paths. The input capacitors must be placed as close as possible to the IC pins as well as the inductor and output capacitor.

For TPS65721, connect the PGND pin of the device to the thermal pad land of the PCB and connect the analog ground connection (GND) to the PGND at the thermal pad. Keep the common path to the GND pin, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. The FB line should be connected right to the output capacitor and routed away from noisy components and traces (for example, the L1 line). See the *TPS65720EVM User's Guide* for details about the layout.

11.2 Layout Example

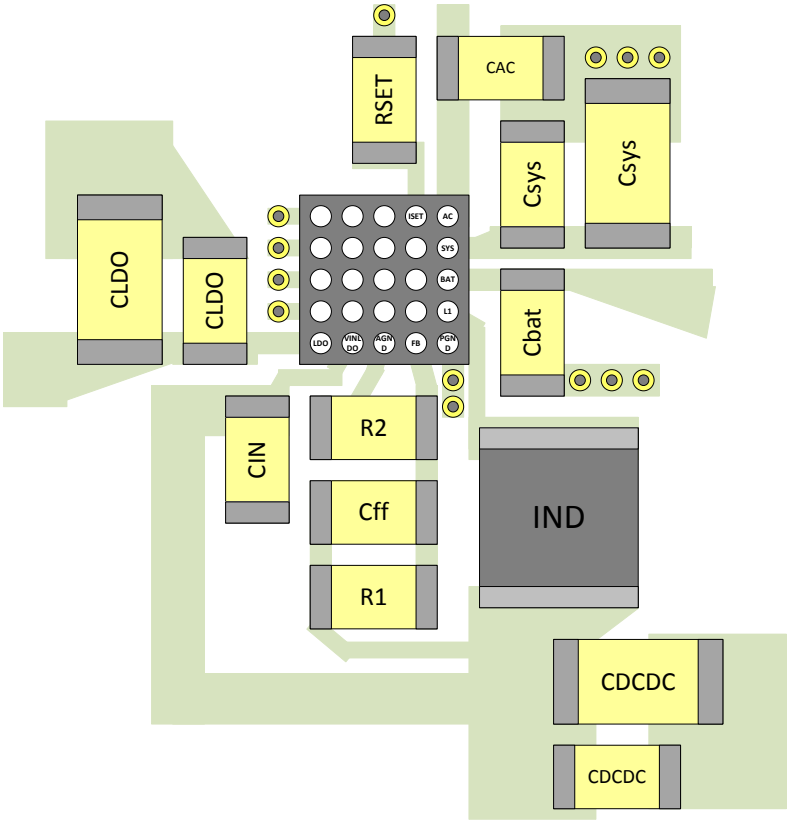


Figure 41. Layout Recommendation

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Basic Calculation of a Buck Converter's Power Stage* application report
- Texas Instruments, *Dynamic Power-Path Management and Dynamic Power Management* application report
- Texas Instruments, *Optimizing Resistor Dividers at a Comparator Input* application report
- Texas Instruments, *TPS65720EVM* user's guide
- Texas Instruments, *TPS65720 Power Management IC (PMIC) for Wearable and Fitness Devices*
- Texas Instruments, *TPS65721EVM* user's guide
- Texas Instruments, *Understanding the Absolute Maximum Ratings of the SW Node* application report

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS65720	Click here	Click here	Click here	Click here	Click here
TPS65721	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS657201YFFR	ACTIVE	DSBGA	YFF	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS657201	Samples
TPS657201YFFT	PREVIEW	DSBGA	YFF	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS657201	
TPS657202YFFR	PREVIEW	DSBGA	YFF	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS657202	
TPS657202YFFT	PREVIEW	DSBGA	YFF	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS657202	
TPS65720YFFR	ACTIVE	DSBGA	YFF	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS65720	Samples
TPS65720YFFT	ACTIVE	DSBGA	YFF	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS65720	Samples
TPS65721RSNR	ACTIVE	QFN	RSN	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65721	Samples
TPS65721RSNT	ACTIVE	QFN	RSN	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65721	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

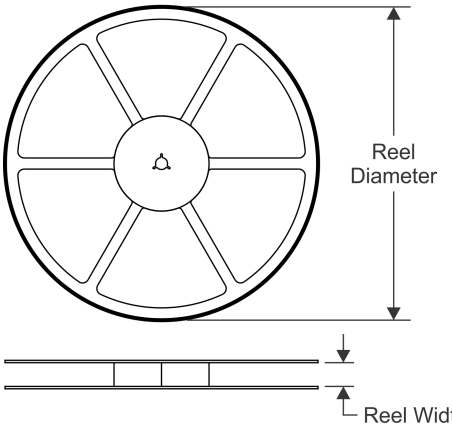
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

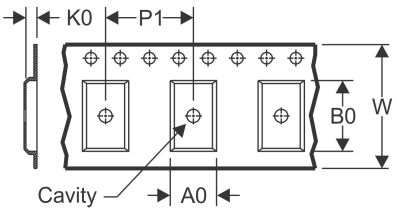
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

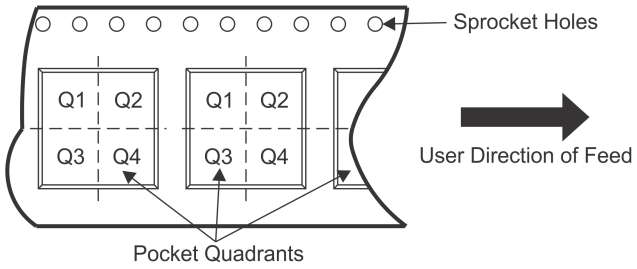


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

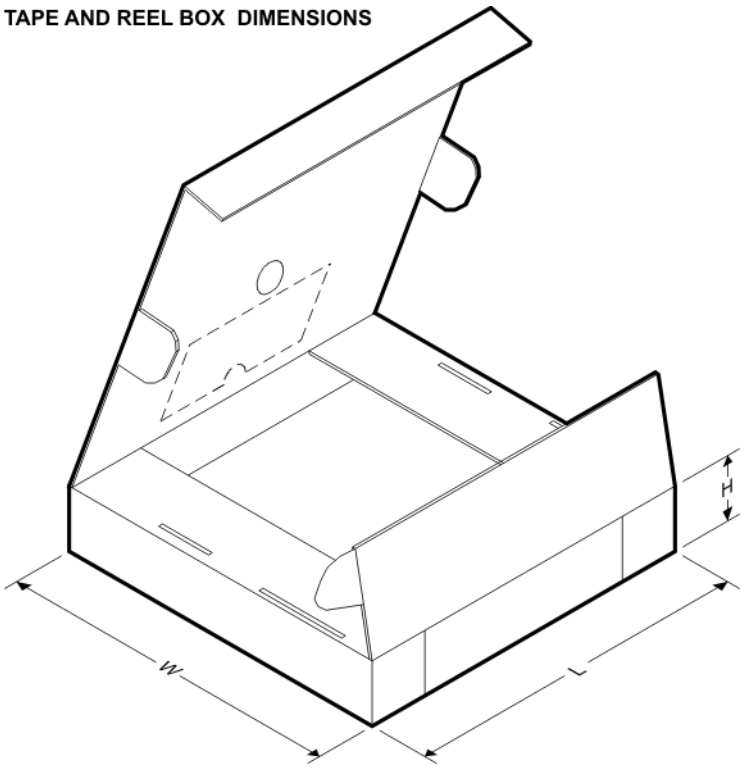
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

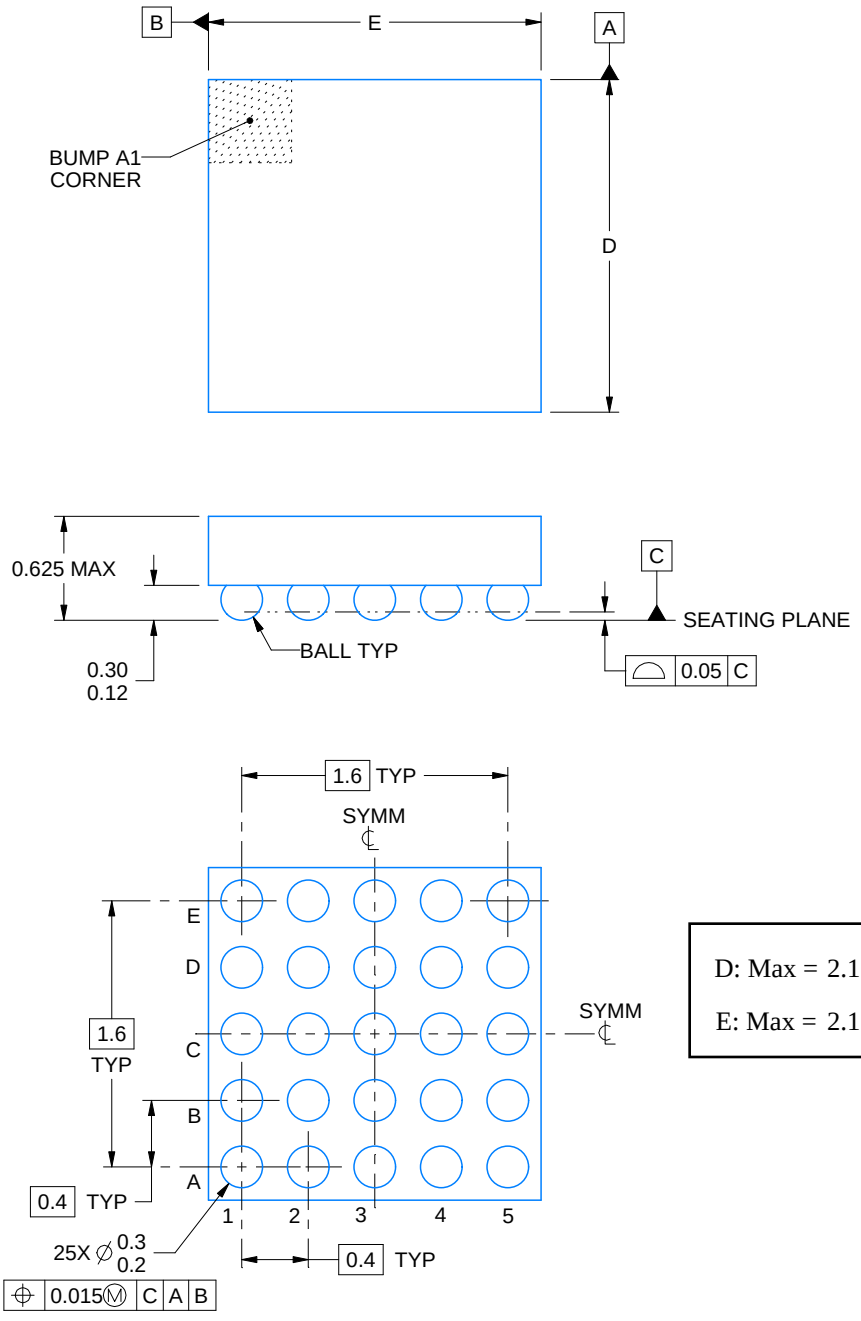
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS657201YFFR	DSBGA	YFF	25	3000	180.0	8.4	2.38	2.4	0.8	4.0	8.0	Q1
TPS65720YFFR	DSBGA	YFF	25	3000	180.0	8.4	2.38	2.4	0.8	4.0	8.0	Q1
TPS65720YFFT	DSBGA	YFF	25	250	180.0	8.4	2.38	2.4	0.8	4.0	8.0	Q1
TPS65721RSNR	QFN	RSN	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65721RSNT	QFN	RSN	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS657201YFFR	DSBGA	YFF	25	3000	182.0	182.0	20.0
TPS65720YFFR	DSBGA	YFF	25	3000	182.0	182.0	20.0
TPS65720YFFT	DSBGA	YFF	25	250	182.0	182.0	20.0
TPS65721RSNR	QFN	RSN	32	3000	367.0	367.0	35.0
TPS65721RSNT	QFN	RSN	32	250	210.0	185.0	35.0



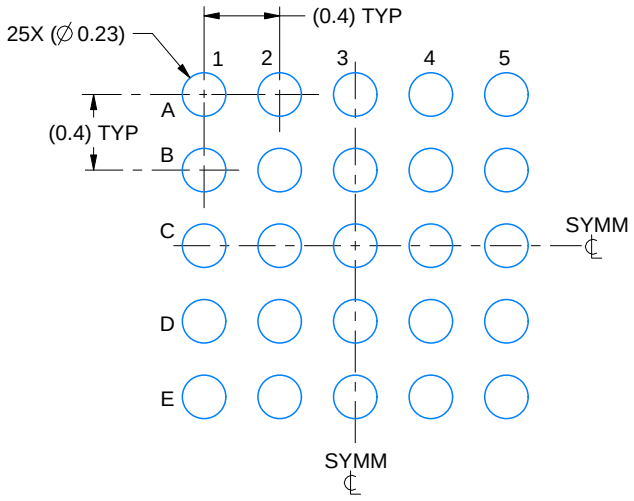
D: Max = 2.116 mm, Min =2.056 mm

E: Max = 2.116 mm, Min =2.056 mm

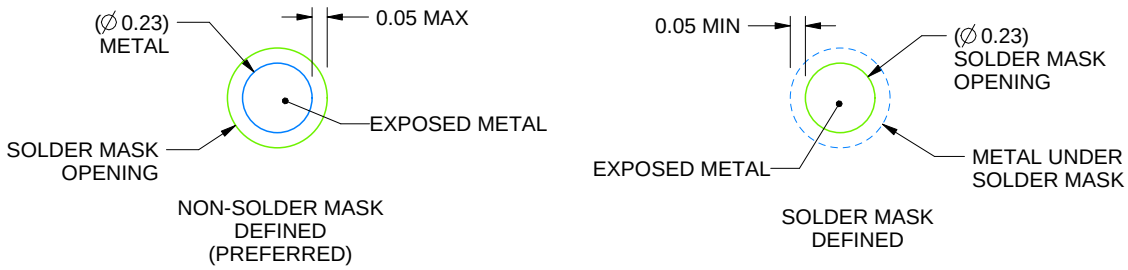
4223786/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

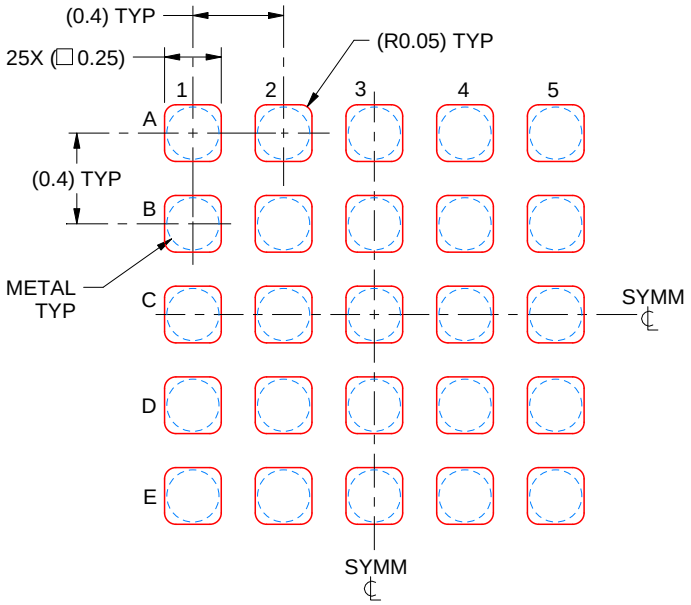


SOLDER MASK DETAILS
NOT TO SCALE

4223786/A 06/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



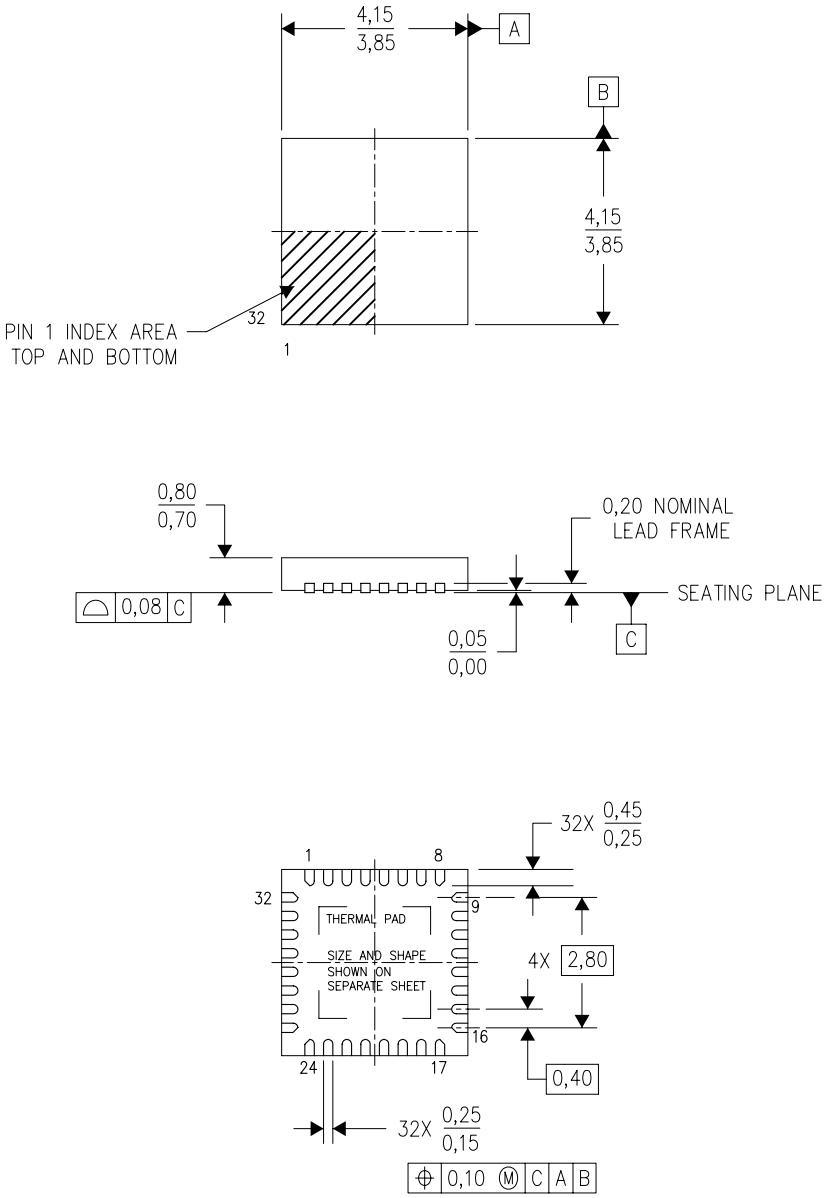
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223786/A 06/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

RSN (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4207561/C 08/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

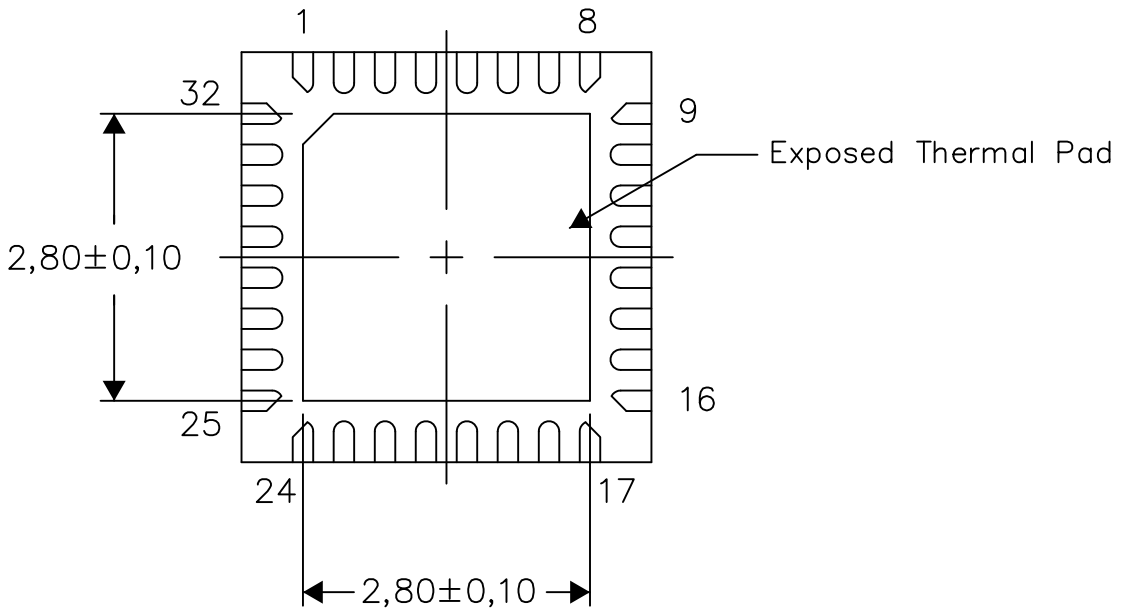
RSN (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



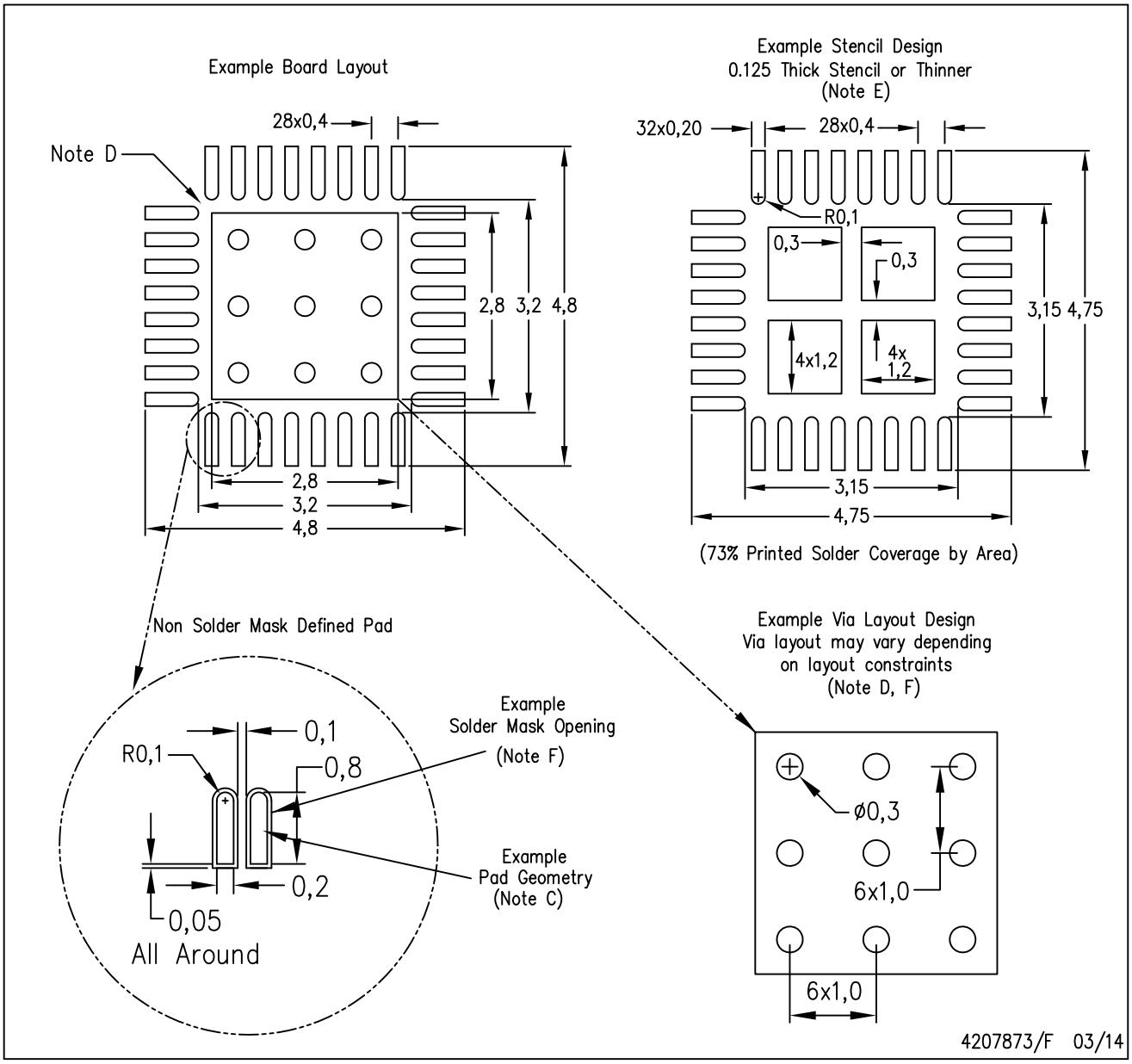
Bottom View

Exposed Thermal Pad Dimensions

4209775–2/F 03/14

NOTE: All linear dimensions are in millimeters

RSN (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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