THE DATASHEET OF

ADM823LYKSZ-R7

Supervisory Circuits with Watchdog and Manual Reset in 5-Lead SC70 and SOT-23

Data Sheet

ADM823/ADM824/ADM825

FEATURES

- Precision 2.5 V to 5 V power supply monitor
- 7 reset threshold options: 2.19 V to 4.63 V
- 140 ms (minimum) reset timeout
- Watchdog timer with 1.6 sec timeout (ADM823, ADM824)
- Manual reset input (ADM823, ADM825)
- Push-pull output stages
  - $\overline{\text{RESET}}$ (ADM823)
  - $\overline{\text{RESET}}$, RESET (ADM824/ADM825)
- Low power consumption: 5 µA
- Guaranteed reset output valid to V_{CC} = 1 V
- Power supply glitch immunity
- Specified over automotive temperature range
- 5-lead SC70 and SOT-23 packages

FUNCTIONAL BLOCK DIAGRAM

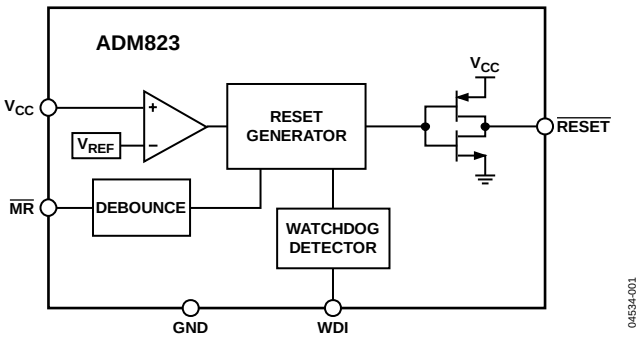

Figure 1.

APPLICATIONS

- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments
- Portable equipment

GENERAL DESCRIPTION

The ADM823/ADM824/ADM825 are supervisory circuits that monitor power supply voltage levels and code execution integrity in microprocessor-based systems. In addition to providing power-on reset signals, an on-chip watchdog timer can reset the microprocessor if it fails to strobe within a preset timeout period. A reset signal can also be asserted by an external push-button, through a manual reset input. The three parts feature different combinations of watchdog input, manual reset input, and output stage configuration, as shown in Table 1.

These parts are available in a choice of seven reset threshold options ranging from 2.19 V to 4.63 V. The reset and watchdog timeout periods are fixed at 140 ms (minimum) and 1.6 sec (typical), respectively.

The ADM823/ADM824/ADM825 are available in 5-lead SC70 and SOT-23 packages and typically consume only 5 µA, making them suitable for use in low power, portable applications.

Table 1. Selection Table

Part No.	Watchdog Timer	Manual Reset	Output Stage	
			$\overline{\text{RESET}}$	RESET
ADM823	Yes	Yes	Push-Pull	–
ADM824	Yes	–	Push-Pull	Push-Pull
ADM825	–	Yes	Push-Pull	Push-Pull

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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5/08—Rev. A to Rev. B

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2/07—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Ordering Guide ... 11

10/04—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 4.75 V to 5.5 V for ADM82xL, V_{CC} = 4.5 V to 5.5 V for ADM82xM, V_{CC} = 3.15 V to 3.6 V for ADM82xT, V_{CC} = 3 V to 3.6 V for ADM82xS, V_{CC} = 2.7 V to 3.6 V for ADM82xR, V_{CC} = 2.38 V to 2.75 V for ADM82xZ, V_{CC} = 2.25 V to 2.75 V for ADM82xY, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range	1		5.5	V	T_A = 0°C to 70°C
	1.2			V	$T_A = T_{MIN}$ to T_{MAX}
Supply Current		10	24	µA	WDI and $\overline{MR}$ unconnected ADM82xL/M
		5	12	µA	WDI and $\overline{MR}$ unconnected ADM82xT/S/R/Z/Y
RESET THRESHOLD VOLTAGE					
ADM82xL	4.56	4.63	4.70	V	T_A = 25°C
	4.50		4.75	V	$T_A = T_{MIN}$ to T_{MAX}
ADM82xM	4.31	4.38	4.45	V	T_A = 25°C
	4.25		4.50	V	$T_A = T_{MIN}$ to T_{MAX}
ADM82xT	3.04	3.08	3.11	V	T_A = 25°C
	3.00		3.15	V	$T_A = T_{MIN}$ to T_{MAX}
ADM82xS	2.89	2.93	2.96	V	T_A = 25°C
	2.85		3.00	V	$T_A = T_{MIN}$ to T_{MAX}
ADM82xR	2.59	2.63	2.66	V	T_A = 25°C
	2.55		2.70	V	$T_A = T_{MIN}$ to T_{MAX}
ADM82xZ (SC70 Only)	2.28	2.32	2.35	V	T_A = 25°C
	2.25		2.38	V	$T_A = T_{MIN}$ to T_{MAX}
ADM82xY (SC70 Only)	2.16	2.19	2.22	V	T_A = 25°C
	2.13		2.25	V	$T_A = T_{MIN}$ to T_{MAX}
RESET THRESHOLD TEMPERATURE COEFFICIENT		40		ppm/°C	
RESET THRESHOLD HYSTERESIS		10		mV	ADM82xL/M
		5		mV	ADM82xT/S/R/Z/Y
RESET TIMEOUT PERIOD	140	200	280	ms	
V_{CC} TO RESET DELAY		40		µs	$V_{TH} - V_{CC}$ = 100 mV
$\overline{RESET}$/RESET					
$\overline{RESET}$ Output Voltage			0.4	V	$V_{CC} = V_{TH}$ min, I_{SINK} = 3.2 mA, ADM82xL/M
			0.3	V	$V_{CC} = V_{TH}$ min, I_{SINK} = 1.2 mA, ADM82xT/S/R/Z/Y
			0.3	V	T_A = 0°C to 70°C, V_{CC} = 1 V, V_{CC} falling, I_{SINK} = 50 µA
	V_{CC} − 1.5			V	$V_{CC} = V_{TH}$ max, I_{SOURCE} = 120 µA, ADM82xL/M
	0.8 × V_{CC}			V	$V_{CC} = V_{TH}$ max, I_{SOURCE} = 30 µA, ADM82xT/S/R/Z/Y
RESET Output Voltage (ADM824, ADM825)			0.4	V	$V_{CC} = V_{TH}$ max, I_{SINK} = 3.2 mA, ADM82xL/M
			0.3	V	$V_{CC} = V_{TH}$ max, I_{SINK} = 1.2 mA, ADM82xT/S/R/Z/Y
	0.8 × V_{CC}			V	$V_{CC} \geq$ 1.8 V, I_{SOURCE} = 150 µA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
WATCHDOG INPUT (ADM823, ADM824)					
Watchdog Timeout Period	1.12	1.6	2.40	sec	
WDI Pulse Width	50			ns	V_{IL} = 0.4 V, V_{IH} = 0.8 × V_{CC}
WDI Input Threshold, V_{IL}	0.7 × V_{CC}		0.3 × V_{CC}	V	
WDI Input Current		120	160	µA	V_{WDI} = V_{CC}, time average
	−20	−15		µA	V_{WDI} = 0 V, time average
MANUAL RESET INPUT (ADM823, ADM825)					
$\overline{MR}$ Input Threshold	0.7 × V_{CC}		0.3 × V_{CC}	V	
$\overline{MR}$ Input Pulse Width	1			µs	
$\overline{MR}$ Glitch Rejection		100		ns	
$\overline{MR}$ Pull-Up Resistance	35	52	75	kΩ	
$\overline{MR}$ to Reset Delay		500		ns	

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
Output Current (RESET, $\overline{RESET}$)	20 mA
All Other Pins	−0.3 V to (V_{CC} + 0.3 V)
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
θ_{JA} Thermal Impedance	
SC70	146°C/W
SOT-23	270°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

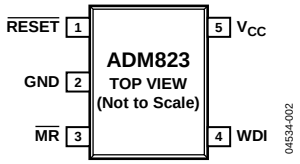


Figure 2. ADM823 Pin Configuration

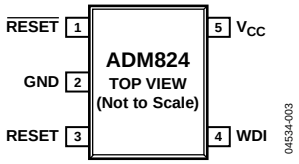


Figure 3. ADM824 Pin Configuration

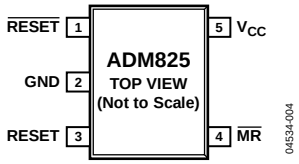


Figure 4. ADM825 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Active Low, Push-Pull Reset Output. Asserted whenever V_{CC} is below the reset threshold, V_{TH}.
2	GND	Ground.
3	$\overline{\text{MR}}$ (ADM823)	Manual Reset Input. This is an active low input which, when forced low for at least 1 µs, generates a reset. It features a 52 kΩ internal pull-up.
	RESET (ADM824/ADM825)	Active High, Push-Pull Reset Output.
4	WDI (ADM823/ADM824)	Watchdog Input. Generates a reset if the voltage on the pin remains low or high for the duration of the watchdog timeout. The timer is cleared if a logic transition occurs on this pin or if a reset is generated.
	$\overline{\text{MR}}$ (ADM825)	Manual Reset Input. This is an active low input which, when forced low for at least 1 µs, generates a reset. It features a 52 kΩ internal pull-up.
5	V_{CC}	Power Supply Voltage Being Monitored.

TYPICAL PERFORMANCE CHARACTERISTICS

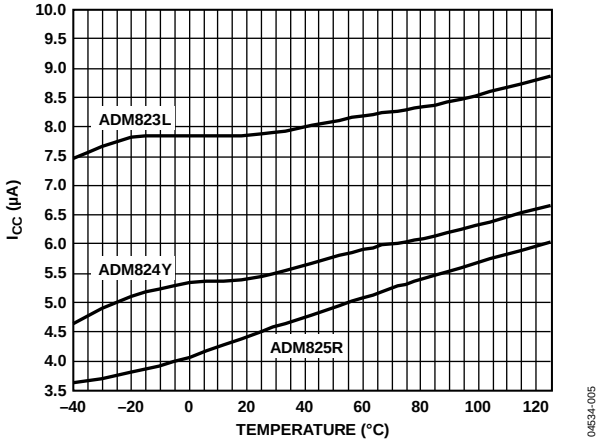


Figure 5. Supply Current vs. Temperature

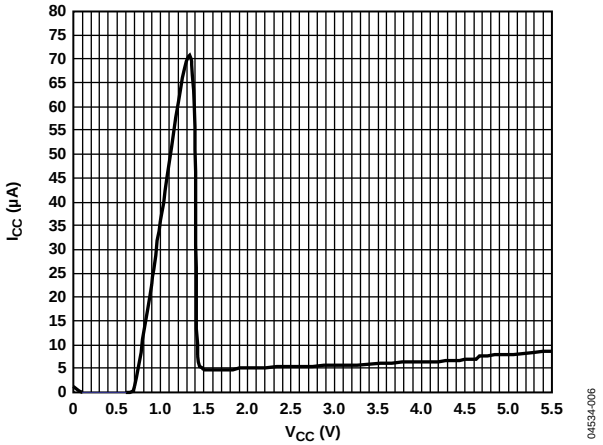


Figure 6. Supply Current vs. Supply Voltage

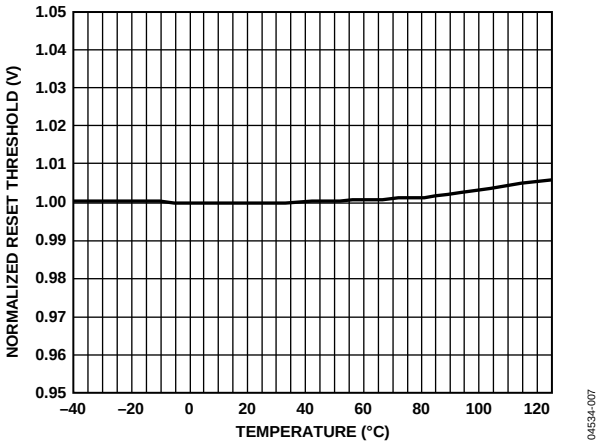


Figure 7. Normalized Reset Threshold vs. Temperature

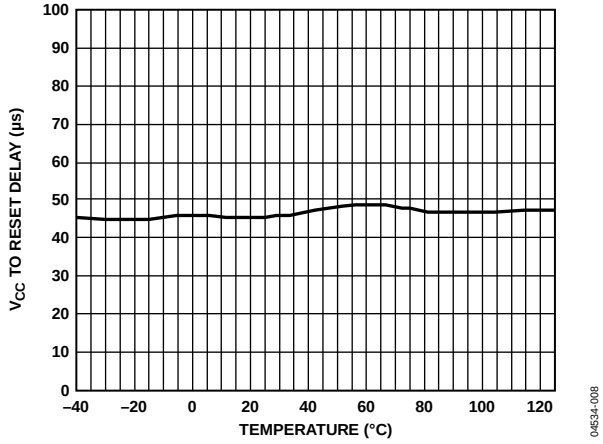


Figure 8. Reset Comparator Propagation Delay vs. Temperature (V_{CC} Falling)

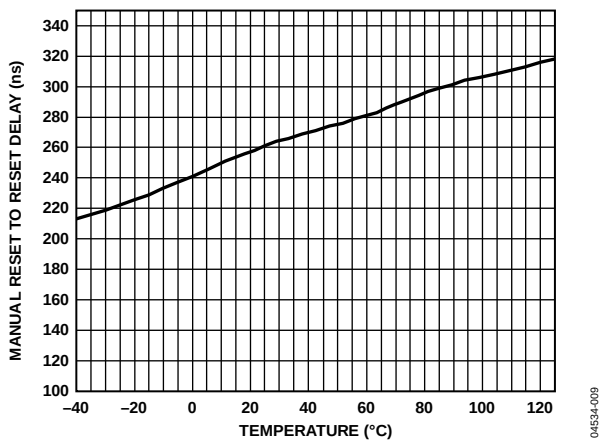


Figure 9. Manual Reset to Reset Propagation Delay vs. Temperature (ADM823/ADM825)

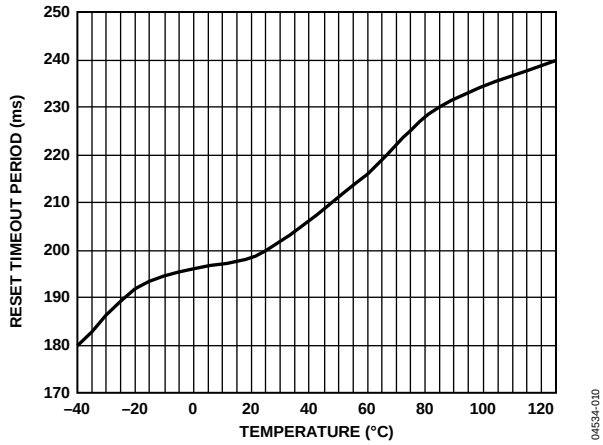


Figure 10. Reset Timeout Period vs. Temperature

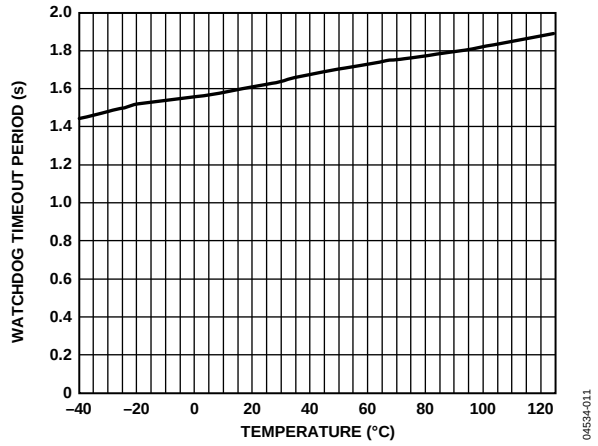


Figure 11. Watchdog Timeout Period vs. Temperature (ADM823/ADM824)

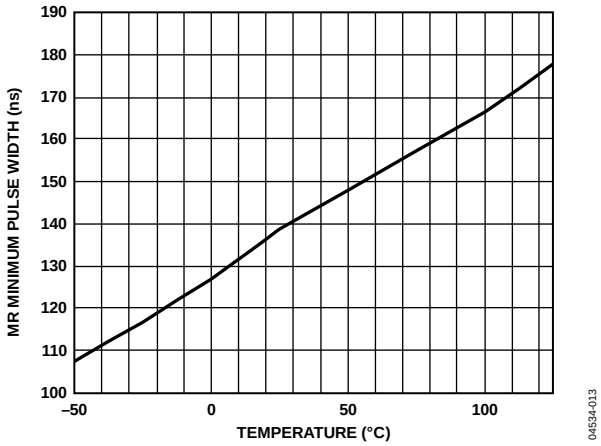


Figure 13. Manual Reset Minimum Pulse Width vs. Temperature (ADM823/ADM825)

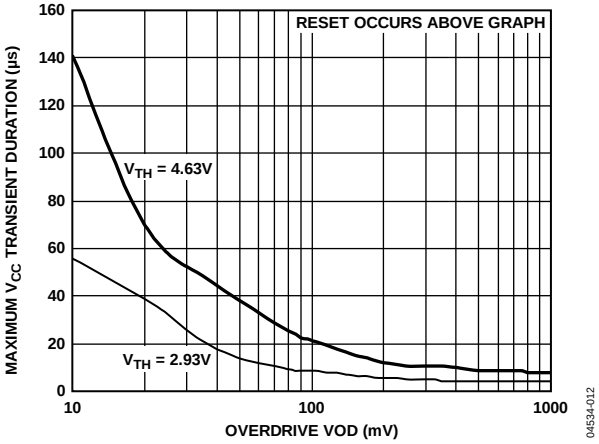


Figure 12. Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive

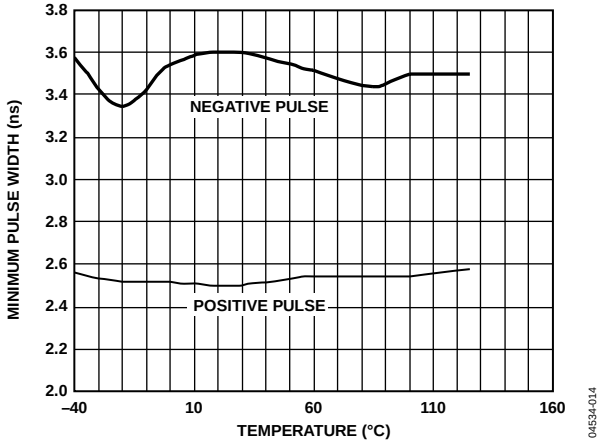


Figure 14. Watchdog Input Minimum Pulse Width vs. Temperature (ADM823/ADM824)

CIRCUIT DESCRIPTION

The ADM823/ADM824/ADM825 provide microprocessor supply voltage supervision by controlling the reset input of the microprocessor. Code execution errors are avoided during power-up, power-down, and brownout conditions by asserting a reset signal when the supply voltage is below a preset threshold. Errors are also avoided by allowing supply voltage stabilization with a fixed timeout reset pulse after the supply voltage rises above the threshold. In addition, problems with microprocessor code execution can be monitored and corrected with a watchdog timer (ADM823/ADM824). By including watchdog strobe instructions in microprocessor code, a watchdog timer can detect whether the microprocessor code breaks down or becomes stuck in an infinite loop. If this happens, the watchdog timer asserts a reset pulse that restarts the microprocessor in a known state. If the user detects a problem with the system's operation, a manual reset input is available (ADM823/ADM825) to reset the microprocessor with an external push-button, for example.

RESET OUTPUT

The ADM823 features an active low, push-pull reset output, and the ADM824/ADM825 feature dual active low and active high push-pull reset outputs. For active low and active high outputs, the reset signal is guaranteed to be logic low and logic high, respectively, for $V_{CC} \geq 1$ V.

The reset output is asserted when V_{CC} is below the reset threshold (V_{TH}), when $\overline{MR}$ is driven low, or when WDI is not serviced within the watchdog timeout period (t_{WD}). Reset remains asserted for the duration of the reset active timeout period (t_{RP}) after V_{CC} rises above the reset threshold, after $\overline{MR}$ transitions from low to high, or after the watchdog timer times out. Figure 15 illustrates the behavior of the reset outputs.

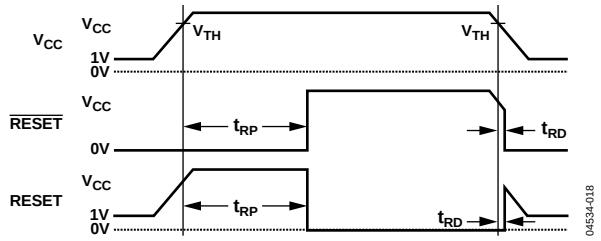


Figure 15. Reset Timing Diagram

MANUAL RESET INPUT

The ADM823/ADM825 feature a manual reset input ($\overline{MR}$) which, when driven low, asserts the reset output. When $\overline{MR}$ transitions from low to high, reset remains asserted for the duration of the reset active timeout period before deasserting. The $\overline{MR}$ input has a 52 kΩ internal pull-up so that the input is always high when unconnected. An external push-button switch can be connected between $\overline{MR}$ and ground so that the user can generate a reset. Debounce circuitry for this purpose is integrated on chip. Noise immunity is provided on the $\overline{MR}$ input and fast, negative-going transients of up to 100 ns (typical) are ignored. A 0.1 µF capacitor between $\overline{MR}$ and ground provides additional noise immunity.

WATCHDOG INPUT

The ADM823/ADM824 feature a watchdog timer that monitors microprocessor activity. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI), which detects pulses as short as 50 ns. If the timer counts through the preset watchdog timeout period (t_{WD}), reset is asserted. The microprocessor is required to toggle the WDI pin to avoid being reset. Failure of the microprocessor to toggle WDI within the timeout period, therefore, indicates a code execution error, and the reset pulse generated restarts the microprocessor in a known state.

In addition to logic transitions on WDI, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on V_{CC} or by $\overline{MR}$ being pulled low. When reset is asserted, the watchdog timer is cleared and does not begin counting again until reset is deasserted. The watchdog timer can be disabled by leaving WDI floating or by three-stating the WDI driver.

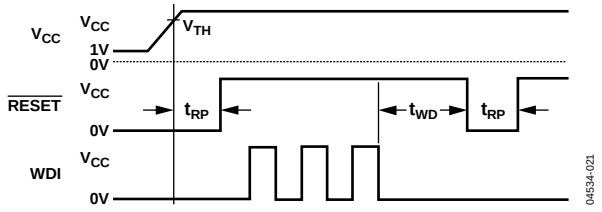


Figure 16. Watchdog Timing Diagram

APPLICATIONS INFORMATION

WATCHDOG INPUT CURRENT

To minimize the watchdog input current (and minimize overall power consumption), leave WDI low for the majority of the watchdog timeout period. When driven high, WDI can draw as much as 160 µA. Pulsing WDI low-high-low at a low duty cycle reduces the effect of the large input current. When WDI is unconnected, a window comparator disconnects the watchdog timer from the reset output circuitry so that reset is not asserted when the watchdog timer times out.

NEGATIVE-GOING V_{CC} TRANSIENTS

To avoid unnecessary resets caused by fast power supply transients, the ADM823/ADM824/ADM825 are equipped with glitch rejection circuitry. The typical performance characteristic in Figure 12 plots V_{CC} transient duration vs. the transient magnitude. The curves show combinations of transient magnitude and duration for which a reset is not generated for 4.63 V and 2.93 V reset threshold parts. For example, with the 2.93 V threshold, a transient that goes 100 mV below the threshold and lasts 8 µs typically does not cause a reset, but if the transient is any larger in magnitude or duration, a reset is generated. An optional 0.1 µF bypass capacitor mounted close to V_{CC} provides additional glitch rejection.

ENSURING RESET VALID TO V_{CC} = 0 V

Both active low and active high reset outputs are guaranteed to be valid for V_{CC} as low as 1 V. However, by using an external resistor with push-pull configured reset outputs, valid outputs for V_{CC} as low as 0 V are possible. For an active low reset output, a resistor connected between $\overline{\text{RESET}}$ and ground pulls the output low when it is unable to sink current. For an active high reset output, a resistor connected between RESET and V_{CC} pulls the output high when it is unable to source current. A large resistance such as 100 kΩ should be used so that the reset output is not overloaded when V_{CC} is above 1 V.

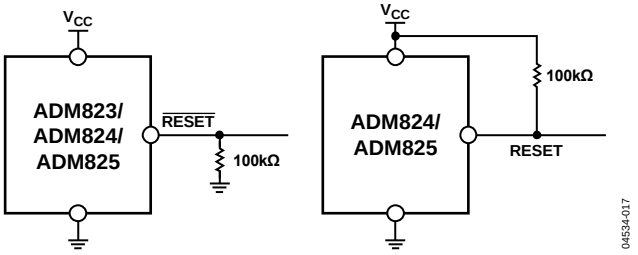


Figure 17. Ensuring Reset Valid to V_{CC} = 0 V

WATCHDOG SOFTWARE CONSIDERATIONS

In implementing the microprocessor watchdog strobe code, quickly switching WDI low-to-high and then high-to-low (minimizing WDI high time) is desirable for current consumption reasons. However, a more effective way of using the watchdog function can be considered.

A low-high-low WDI pulse within a given subroutine prevents the watchdog timing out. However, if the subroutine becomes stuck in an infinite loop, the watchdog cannot detect this condition because the subroutine continues to toggle WDI. A more effective coding scheme for detecting this error involves using a slightly longer watchdog timeout. In the program that calls the subroutine, WDI is set high (see Figure 18). The subroutine sets WDI low when it is called. If the program executes without error, WDI is toggled high and low with every loop of the program. If the subroutine enters an infinite loop, WDI is kept low, the watchdog times out, and the microprocessor is reset.

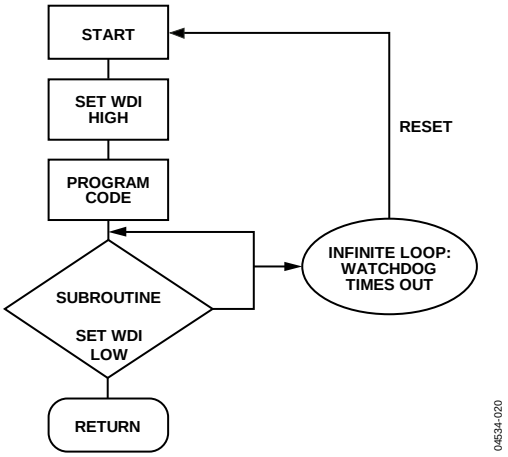


Figure 18. Watchdog Flow Diagram

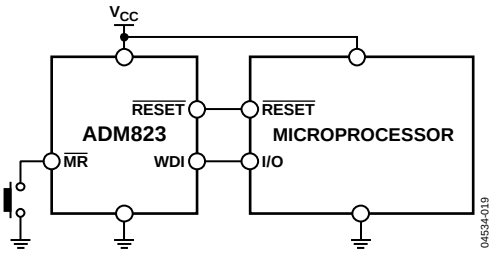
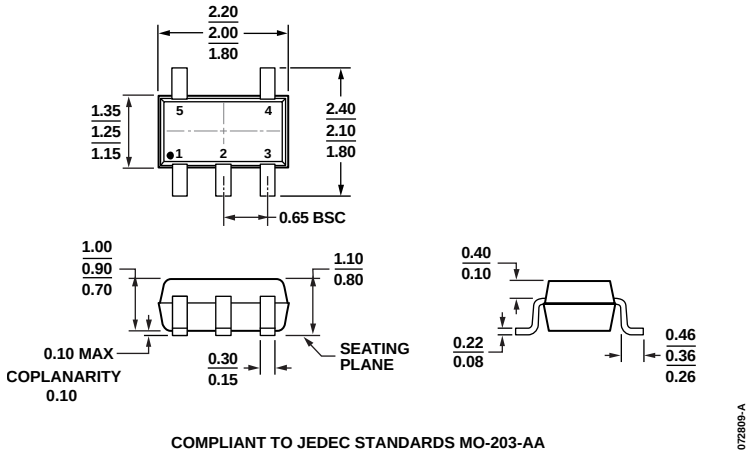


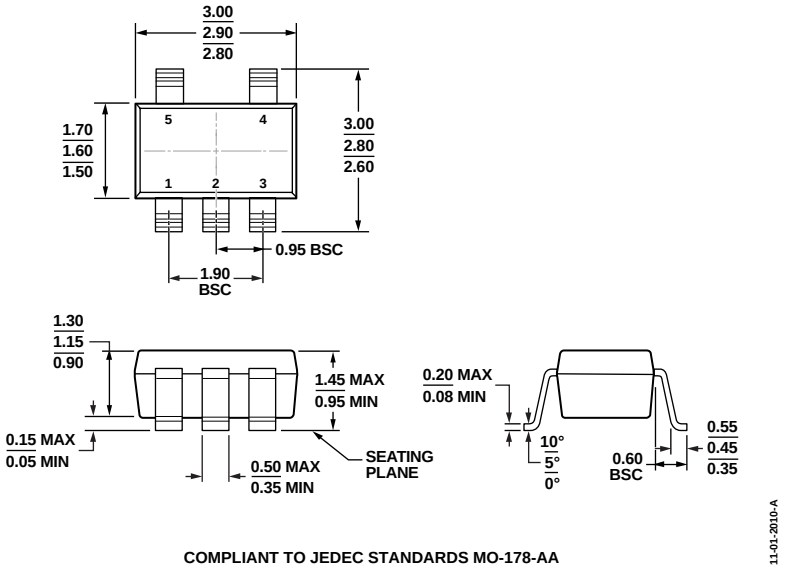
Figure 19. Typical Application Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 20. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 21. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model [1]	Reset Threshold (V)	Temperature Range	Quantity	Package Description	Package Option	Branding
ADM823LYKSZ-R7	4.63	−40°C to +125°C	3k	5-Lead SC70	KS-5	M4L
ADM823LYRJ-R7	4.63	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N07
ADM823LYRJZ-R7	4.63	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	M4L
ADM823MYKSZ-R7	4.38	−40°C to +125°C	3k	5-Lead SC70	KS-5	M4L
ADM823MYRJZ-R7	4.38	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	M4L
ADM823TYKSZ-R7	3.08	−40°C to +125°C	3k	5-Lead SC70	KS-5	M4L
ADM823TYRJ-R7	3.08	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N07
ADM823TYRJZ-R7	3.08	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	M4L
ADM823SYKSZ-R7	2.93	−40°C to +125°C	3k	5-Lead SC70	KS-5	M4L
ADM823SYRJ-R7	2.93	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N07
ADM823SYRJZ-R7	2.93	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	M4L

Model [1]	Reset Threshold (V)	Temperature Range	Quantity	Package Description	Package Option	Branding
ADM823RYRJZ-R7	2.63	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	M4L
ADM823ZYKSZ-R7	2.32	−40°C to +125°C	3k	5-Lead SC70	KS-5	M4L
ADM823YYKSZ-R7	2.19	−40°C to +125°C	3k	5-Lead SC70	KS-5	M4L
ADM824LYRJZ-REEL7	4.63	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	L9M
ADM824SYKSZ-REEL7	2.93	−40°C to +125°C	3k	5-Lead SC70	KS-5	M8G
ADM824RYKSZ-REEL7	2.63	−40°C to +125°C	3k	5-Lead SC70	KS-5	M8G
ADM824SYRJZ-REEL7	2.93	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	M8G
ADM825LYRJ-R7	4.63	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N09
ADM825LYRJZ-R7	4.63	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	M8H
ADM825MYRJ-R7	4.38	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N09
ADM825TYKSZ-R7	3.08	−40°C to +125°C	3k	5-Lead SC70	KS-5	M8H
ADM825TYRJ-R7	3.08	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N09
ADM825TYRJZ-R7	3.08	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	M8H
ADM825SYKSZ-R7	2.93	−40°C to +125°C	3k	5-Lead SC70	KS-5	M8H
ADM825SYRJ-R7	2.93	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N09
ADM825SYRJZ-R7	2.93	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	M8H
ADM825RYRJ-R7	2.63	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N09
ADM825RYRJZ-R7	2.63	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	M8H
ADM825ZYKSZ-R7	2.32	−40°C to +125°C	3k	5-Lead SC70	KS-5	M8H

[1] Z = RoHS Compliant Part.

Looking for pricing, stock, or lifecycle information?

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- View ADM823LYKSZ-R7 on WIN SOURCE
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