THE DATASHEET OF

ADSP-2183KCA-210

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ANALOG DEVICES

DSP Microcomputer

ADSP-2183

FEATURES

PERFORMANCE

- 19 ns Instruction Cycle Time from 26.32 MHz Crystal @ 3.3 Volts
- 52 MIPS Sustained Performance
- Single-Cycle Instruction Execution
- Single-Cycle Context Switch
- 3-Bus Architecture Allows Dual Operand Fetches in Every Instruction Cycle
- Multifunction Instructions
- Power-Down Mode Featuring Low CMOS Standby Power Dissipation with 300 Cycle Recovery from Power-Down Condition
- Low Power Dissipation in Idle Mode

INTEGRATION

- ADSP-2100 Family Code Compatible, with Instruction Set Extensions
- 80K Bytes of On-Chip RAM, Configured as
  16K Words On-Chip Program Memory RAM
  16K Words On-Chip Data Memory RAM
- Dual Purpose Program Memory for Both Instruction and Data Storage
- Independent ALU, Multiplier/Accumulator, and Barrel Shifter Computational Units
- Two Independent Data Address Generators
- Powerful Program Sequencer Provides
  Zero Overhead Looping
  Conditional Instruction Execution
- Programmable 16-Bit Interval Timer with Prescaler
- 128-Lead LQFP, 144-Ball Mini-BGA

SYSTEM INTERFACE

- 16-Bit Internal DMA Port for High Speed Access to On-Chip Memory
- 4 MByte Memory Interface for Storage of Data Tables and Program Overlays
- 8-Bit DMA to Byte Memory for Transparent Program and Data Memory Transfers
- I/O Memory Interface with 2048 Locations Supports Parallel Peripherals
- Programmable Memory Strobe and Separate I/O Memory Space Permits "Glueless" System Design
- Programmable Wait State Generation
- Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
- Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Internal DMA Port
- Six External Interrupts
- 13 Programmable Flag Pins Provide Flexible System Signaling
- ICE-Port™ Emulator Interface Supports Debugging in Final Systems

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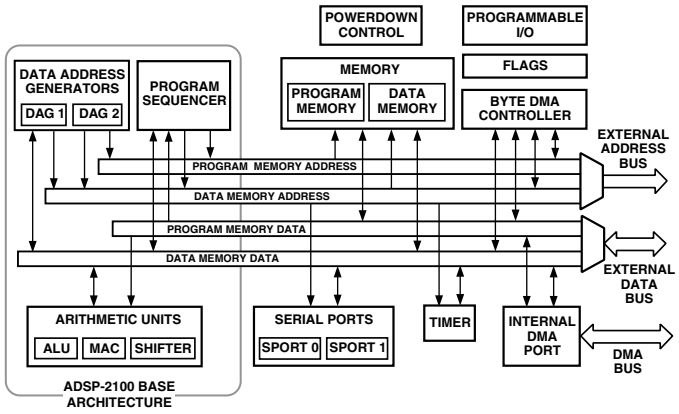
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSP-2183 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high speed numeric processing applications.

The ADSP-2183 combines the ADSP-2100 family base architecture (three computational units, data address generators and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

The ADSP-2183 integrates 80K bytes of on-chip memory configured as 16K words (24-bit) of program RAM, and 16K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-2183 is available in 128-lead LQFP, and 144-Ball Mini-BGA packages.

In addition, the ADSP-2183 supports new instructions, which include bit manipulations—bit set, bit clear, bit toggle, bit test—new ALU constants, new multiplication instruction (x squared), biased rounding, result free ALU operations, I/O memory transfers and global interrupt masking, for increased flexibility.

Fabricated in a high speed, double metal, low power, CMOS process, the ADSP-2183 operates with a 19 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-2183's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle the ADSP-2183 can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

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This takes place while the processor continues to:
- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

Development System

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-2183. The assembler has an algebraic syntax that is easy to program and debug. The linker combines object files into an executable file. The simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment.

The EZ-KIT Lite is a hardware/software kit offering a complete development environment for the ADSP-21xx family: an ADSP-2189M evaluation board with PC monitor software plus Assembler, Linker, Simulator and PROM Splitter software. The ADSP-2189M evaluation board is a low-cost, easy to use hardware platform on which you can quickly get started with your DSP software design. The EZ-KIT Lite include the following features:

- 35.7 MHz ADSP-2189M
- Full 16-bit Stereo Audio I/O with AD73322 CODEC
- RS-232 Interface
- EZ-ICE Connector for Emulator Control
- DSP Demo Programs
- Evaluation Suite of VisualDSP

The ADSP-218x EZ-ICE® Emulator aids in the hardware debugging of ADSP-218x systems. The ADSP-218x integrates on-chip emulation support with a 14-pin ICE-Port interface. This interface provides a simpler target board connection requiring fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICEs. The ADSP-218x device need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.

The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

(See Designing An EZ-ICE-Compatible Target System section of this data sheet for exact specifications of the EZ-ICE target board connector.)

Additional Information

This data sheet provides a general overview of ADSP-2183 functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual,* Third Edition. For more information about the development tools, refer to the *ADSP-2100 Family Development Tools Data Sheet*.

ARCHITECTURE OVERVIEW

The ADSP-2183 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2183 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Figure 1 is an overall block diagram of the ADSP-2183. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

The ADSP-21xx family DSPs contain a shadow register that is useful for single cycle context switching of the processor.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2183 executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-2183 to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2183 can fetch an operand from program memory and the next instruction in the same cycle.

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In addition to the address and data bus for external memory connection, the ADSP-2183 has a 16-bit Internal DMA port (IDMA port) for connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSPs on-chip program and data RAM.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$ and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-2183 to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSP-2183 can respond to thirteen possible interrupts, eleven of which are accessible at any given time. There can be up to six external interrupts (one edge-sensitive, two level-sensitive and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port and the power-down circuitry. There is also a master $\overline{RESET}$ signal.

The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each port can generate an internal programmable serial clock or accept an external serial clock.

The ADSP-2183 provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* processor cycle, where *n* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-2183 incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-2183 SPORTs. Refer to the *ADSP-2100 Family User's Manual,* Third Edition, for further details.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals, internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.

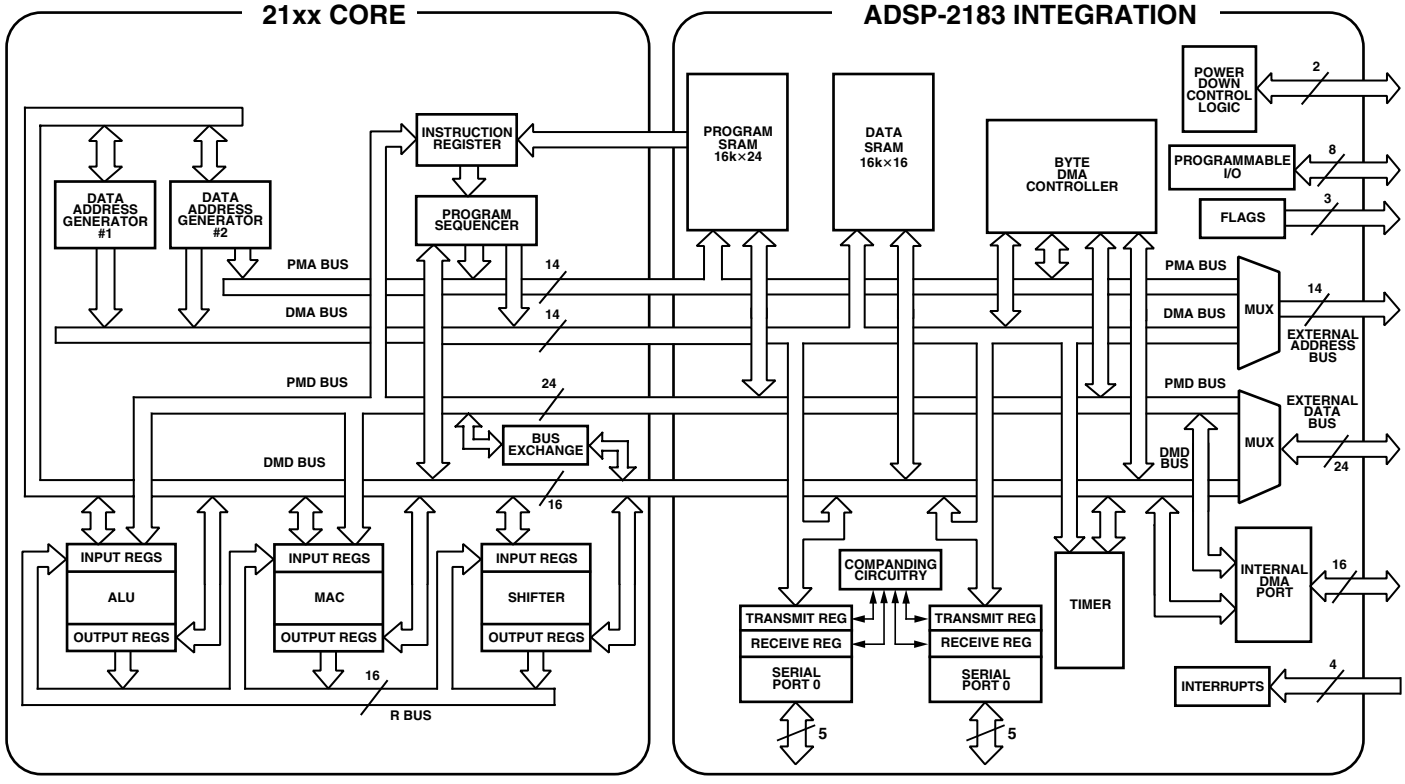


Figure 1. Block Diagram

- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 or 32 word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

Pin Descriptions

The ADSP-2183 is available in a 128-lead LQFP package, and Mini-BGA.

PIN FUNCTION DESCRIPTIONS

Pin Name(s)	# of Pins	Input/ Output	Function
Address	14	O	Address Output Pins for Program, Data, Byte, & I/O Spaces
Data	24	I/O	Data I/O Pins for Program and Data Memory Spaces (8 MSBs Are Also Used as Byte Space Addresses)
$\overline{RESET}$	1	I	Processor Reset Input
$\overline{IRQ2}$	1	I	Edge- or Level-Sensitive Interrupt Request
$\overline{IRQL0}$, $\overline{IRQL1}$	2	I	Level-Sensitive Interrupt Requests
$\overline{IRQE}$	1	I	Edge-Sensitive Interrupt Request
$\overline{BR}$	1	I	Bus Request Input
$\overline{BG}$	1	O	Bus Grant Output
$\overline{BGH}$	1	O	Bus Grant Hung Output
$\overline{PMS}$	1	O	Program Memory Select Output
$\overline{DMS}$	1	O	Data Memory Select Output
$\overline{BMS}$	1	O	Byte Memory Select Output
$\overline{IOMS}$	1	O	I/O Space Memory Select Output
$\overline{CMS}$	1	O	Combined Memory Select Output
$\overline{RD}$	1	O	Memory Read Enable Output
$\overline{WR}$	1	O	Memory Write Enable Output
MMAP	1	I	Memory Map Select Input
BMODE	1	I	Boot Option Control Input
CLKIN, XTAL	2	I	Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output.
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1	5	I/O	Serial Port 1 *or* Two External $\overline{IRQ}$s, Flag In and Flag Out
$\overline{IRD}$, $\overline{IWR}$	2	I	IDMA Port Read/Write Inputs
$\overline{IS}$	1	I	IDMA Port Select
IAL	1	I	IDMA Port Address Latch Enable
IAD	16	I/O	IDMA Port Address/Data Bus
$\overline{IACK}$	1	O	IDMA Port Access Ready Acknowledge
$\overline{PWD}$	1	I	Power-Down Control
PWDACK	1	O	Power-Down Control
FL0, FL1, FL2	3	O	Output Flags
PF7:0	8	I/O	Programmable I/O Pins
EE	1	*	(Emulator Only*)
$\overline{EBR}$	1	*	(Emulator Only*)
$\overline{EBG}$	1	*	(Emulator Only*)
$\overline{ERESET}$	1	*	(Emulator Only*)
$\overline{EMS}$	1	*	(Emulator Only*)
$\overline{EINT}$	1	*	(Emulator Only*)
ECLK	1	*	(Emulator Only*)
ELIN	1	*	(Emulator Only*)
ELOUT	1	*	(Emulator Only*)
GND	11		Ground Pins (LQFP)
VDD	6		Power Supply Pins (LQFP)
GND	22		Ground Pins (Mini-BGA)
VDD	11		Power Supply Pins (Mini-BGA)

*These ADSP-2183 pins must be connected *only* to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors.

Interrupts

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. The ADSP-2183 provides four dedicated external interrupt input pins, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$ and $\overline{IRQE}$. In addition, SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, FLAG_IN and FLAG_OUT, for a total of six external interrupts. The ADSP-2183 also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power-down and reset). The $\overline{IRQ2}$, $\overline{IRQ0}$ and $\overline{IRQ1}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{IRQL0}$ and $\overline{IRQL1}$ are level-sensitive and $\overline{IRQE}$ is edge sensitive. The priorities and vector addresses of all interrupts are shown in Table I.

Table I. Interrupt Priority and Interrupt Vector Addresses

Source of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0000 (*Highest Priority*)
Power-Down (Nonmaskable)	002C
$\overline{\text{IRQ2}}$	0004
$\overline{\text{IRQL1}}$	0008
$\overline{\text{IRQL0}}$	000C
SPORT0 Transmit	0010
SPORT0 Receive	0014
$\overline{\text{IRQE}}$	0018
BDMA Interrupt	001C
SPORT1 Transmit or $\overline{\text{IRQ1}}$	0020
SPORT1 Receive or $\overline{\text{IRQ0}}$	0024
Timer	0028 (*Lowest Priority*)

Interrupt routines can either be nested, with higher priority interrupts taking precedence, or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

The ADSP-2183 masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ pins are external level-sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts.

On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are twelve levels deep to allow interrupt, loop and subroutine nesting.

The following instructions allow global enable or disable servicing of the interrupts (including power down), regardless of the state of IMASK. Disabling the interrupts does not affect serial port autobuffering or DMA.

ENA INTS;
DIS INTS;

When the processor is reset, interrupt servicing is enabled.

LOW POWER OPERATION

The ADSP-2183 has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

The ADSP-2183 processor has a low power feature that lets the processor enter a very low power dormant state through hardware or software control. Here is a brief list of power-down features. Refer to the *ADSP-2100 Family User's Manual*, Third Edition, "System Interface" chapter for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 300 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 300 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits 4096 CLKIN cycles for the crystal oscillator to start and stabilize), and letting the oscillator run to allow 300 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit.
- Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin indicates when the processor has entered power-down.

Idle

When the ADSP-2183 is in the Idle Mode, the processor waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the *IDLE* instruction.

Slow Idle

The *IDLE* instruction is enhanced on the ADSP-2183 to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the *IDLE* instruction. The format of the instruction is

IDLE (n);

where n = 16, 32, 64 or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard *IDLE* instruction.

When the *IDLE (n)* instruction is used, it effectively slows down the processor's internal clock, and thus its response time, to incoming interrupts. The one-cycle response time of the standard idle state is increased by *n*, the clock divisor. When an enabled interrupt is received, the ADSP-2183 will remain in the idle state for up to a maximum of *n* processor cycles (*n* = 16, 32, 64 or 128) before resuming normal operation.

When the *IDLE (n)* instruction is used in systems with an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of *n* processor cycles).

SYSTEM INTERFACE

Figure 2 shows a typical basic system configuration with the ADSP-2183, two serial devices, a byte-wide EPROM and optional external program and data overlay memories. Programmable wait state generation allows the processor to connect easily to slow peripheral devices. The ADSP-2183 also provides four external interrupts and two serial ports or six external interrupts and one serial port.

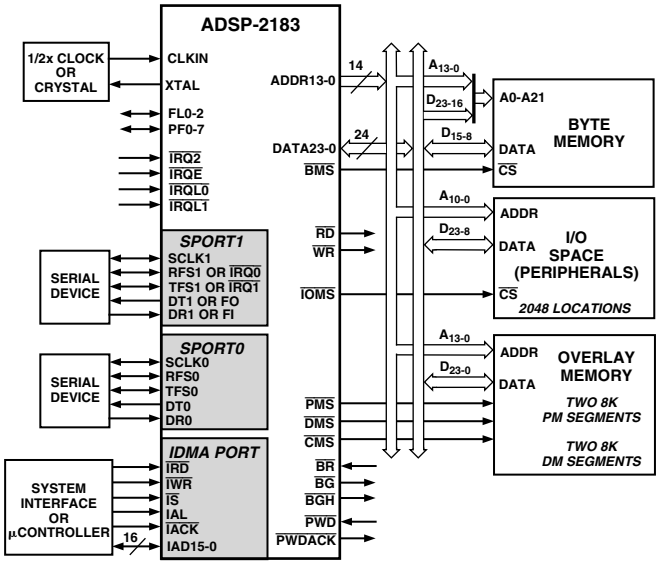


Figure 2. ADSP-2183 Basic System Configuration

Clock Signals

The ADSP-2183 can be clocked by either a crystal or a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation or operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual,* Third Edition, for detailed information on this power-down feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input *must* be left unconnected.

The ADSP-2183 uses an input clock with a frequency equal to half the instruction rate; a 16.67 MHz input clock yields a 30 ns processor cycle (which is equivalent to 33 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the ADSP-2183 includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.

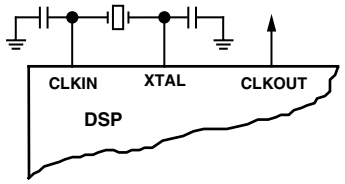


Figure 3. External Crystal Connections

Reset

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-2183. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked, but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulsewidth specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if you use an RC circuit to generate your $\overline{\text{RESET}}$ signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting (MMAP = 0), the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

Memory Architecture
The ADSP-2183 provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory and I/O.

Program Memory is a 24-bit-wide space for storing both instruction opcodes and data. The ADSP-2183 has 16K words of Program Memory RAM on chip and the capability of accessing up to two 8K external memory overlay spaces using the external data bus. Both an instruction opcode and a data value can be read from on-chip program memory in a single cycle.

Data Memory is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-2183 has 16K words on Data Memory RAM on chip, consisting of 16,352 user-accessible locations and 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus.

Byte Memory provides access to an 8-bit-wide memory space through the Byte DMA (BDMA) port. The Byte Memory interface provides access to 4 MBytes of memory by utilizing eight data lines as additional address lines. This gives the BDMA Port an effective 22-bit address range. On power-up, the DSP can automatically load bootstrap code from byte memory.

I/O Space allows access to 2048 locations of 16-bit-wide data. It is intended to be used to communicate with parallel peripheral devices such as data converters and external registers or latches.

Program Memory
The ADSP-2183 contains a 16K × 24 on-chip program RAM. The on-chip program memory is designed to allow up to two accesses each cycle so that all operations can complete in a single cycle. In addition, the ADSP-2183 allows the use of 8K external memory overlays.

The program memory space organization is controlled by the MMAP pin and the PMOVLAY register. Normally, the ADSP-2183 is configured with MMAP = 0 and program memory organized as shown in Figure 4.

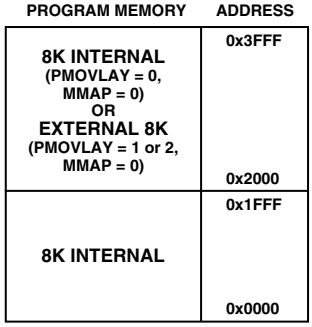


Figure 4. Program Memory (MMAP = 0)

There are 16K words of memory accessible internally when the PMOVLAY register is set to 0. When PMOVLAY is set to something other than 0, external accesses occur at addresses 0x2000 through 0x3FFF. The external address is generated as shown in Table II.

Table II.

PMOVLAY	Memory	A13	A12:0
0	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

This organization provides for two external 8K overlay segments using only the normal 14 address bits. This allows for simple program overlays using one of the two external segments in place of the on-chip memory. Care must be taken in using this overlay space because the processor core (i.e., the sequencer) does not take the PMOVLAY register value into account. For example, if a loop operation were occurring on one of the external overlays, and the program changes to another external overlay or internal memory, an incorrect loop operation could occur. In addition, care must be taken in interrupt service routines as the overlay registers are not automatically saved and restored on the processor mode stack.

For ADSP-2100 Family compatibility, MMAP = 1 is allowed. In this mode, booting is disabled and overlay memory is disabled (*PMOVLAY* must be 0). Figure 5 shows the memory map in this configuration.

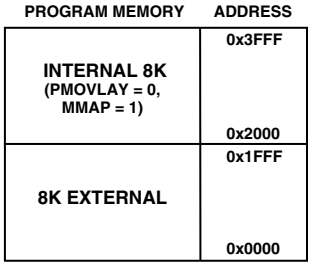


Figure 5. Program Memory (MMAP = 1)

Data Memory
The ADSP-2183 has 16,352 16-bit words of internal data memory. In addition, the ADSP-2183 allows the use of 8K external memory overlays. Figure 6 shows the organization of the data memory.

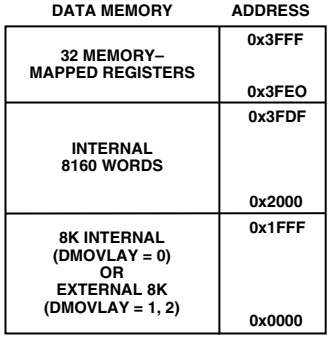


Figure 6. Data Memory

There are 16,352 words of memory accessible internally when the DMOVLAY register is set to 0. When DMOVLAY is set to something other than 0, external accesses occur at addresses 0x0000 through 0x1FFF. The external address is generated as shown in Table III.

Table III.

DMOVLAY	Memory	A13	A12:0
0	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x0000 and 0x1FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x0000 and 0x1FFF

This organization allows for two external 8K overlays using only the normal 14 address bits.

All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register.

I/O Space

The ADSP-2183 supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals or to bus interface ASIC data registers. I/O space supports 2048 locations. The lower eleven bits of the external address bus are used; the upper 3 bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated 3-bit wait state registers, IOWAIT0-3, which specify up to seven wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table IV.

Table IV.

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0
0x200–0x3FF	IOWAIT1
0x400–0x5FF	IOWAIT2
0x600–0x7FF	IOWAIT3

Composite Memory Select ($\overline{\text{CMS}}$)

The ADSP-2183 has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality.

When set, each bit in the CMSSEL register causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the PMS and DMS bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory; use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals, with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits, except the $\overline{\text{BMS}}$ bit, default to 1 at reset.

Byte Memory

The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8.

The byte memory space on the ADSP-2183 supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses data bits 23:16 and address bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register.

Byte Memory DMA (BDMA)

The Byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space, while the processor is operating normally and steals only one DSP cycle per 8-, 16- or 24-bit word transferred.

The BDMA circuit supports four different data formats which are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table V shows the data formats supported by the BDMA circuit.

Table V.

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register. The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory, regardless of the values of MMAP, PMOVLAY or DMOVLAY.

When the BWCOUNT register is written with a nonzero value the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor and start execution at address 0 when the BDMA accesses have completed.

Internal Memory DMA Port (IDMA Port)
The IDMA Port provides an efficient means of communication between a host system and the ADSP-2183. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP's memory-mapped control registers.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written to while the ADSP-2183 is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location; the destination type specifies whether it is a DM or PM access. The falling edge of the address latch signal latches this value into the IDMAA register.

Once the address is stored, data can either be read from or written to the ADSP-2183's on-chip memory. Asserting the select line ($\overline{IS}$) and the appropriate read or write line ($\overline{IRD}$ and $\overline{IWR}$ respectively) signals the ADSP-2183 that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation.

Bootstrap Loading (Booting)
The ADSP-2183 has two mechanisms to allow automatic loading of the on-chip program memory after reset. The method for booting after reset is controlled by the MMAP and BMODE pins as shown in Table VI.

Table VI. Boot Summary Table

MMAP	BMODE	Booting Method
0	0	BDMA feature is used in default mode to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded.
0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to.
1	X	Bootstrap features disabled. Program execution immediately starts from location 0.

BDMA Booting
When the BMODE and MMAP pins specify BDMA booting (MMAP = 0, BMODE = 0), the ADSP-2183 initiates a BDMA boot sequence when reset is released. The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24 bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

The ADSP-2100 Family Development Software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte memory space compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface.

IDMA Booting
The ADSP-2183 can also boot programs through its Internal DMA port. If BMODE = 1 and MMAP = 0, the ADSP-2183 boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until on-chip program memory location 0 is written to.

The ADSP-2100 Family Development Software (Revision 5.02 and later) can generate IDMA compatible boot code.

Bus Request and Bus Grant
The ADSP-2183 can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{BR}$) signal. If the ADSP-2183 is not performing an external memory access, then it responds to the active $\overline{BR}$ input in the following processor cycle by:

- three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- asserting the bus grant ($\overline{BG}$) signal, and
- halting program execution.

If Go Mode is enabled, the ADSP-2183 will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-2183 is performing an external memory access when the external device asserts the $\overline{BR}$ signal, then it will not three-state the memory interfaces or assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, reenables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when the ADSP-2183 is ready to execute an instruction, but is stopped because the external bus is already granted to another device. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-2183 deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

Flag I/O Pins

The ADSP-2183 has eight general purpose programmable input/output flag pins. They are controlled by two memory mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-2183's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, the ADSP-2183 has five fixed-mode flags, FLAG_IN, FLAG_OUT, FL0, FL1 and FL2. FL0-FL2 are dedicated output flags. FLAG_IN and FLAG_OUT are available as an alternate configuration of SPORT1.

INSTRUCTION SET DESCRIPTION

The ADSP-2183 assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-2183's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

DESIGNING AN EZ-ICE-COMPATIBLE SYSTEM

The ADSP-2183 has on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug.

The ICE-Port interface consists of the following ADSP-2183 pins:

$\overline{EBR}$	$\overline{EBG}$	$\overline{ERESET}$
$\overline{EMS}$	$\overline{EINT}$	ECLK
ELIN	ELOUT	EE

These ADSP-2183 pins must be connected *only* to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-2183 and the connector must be kept as short as possible, no longer than three inches.

The following pins are also used by the EZ-ICE:

$\overline{BR}$	$\overline{BG}$
$\overline{RESET}$	GND

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-2183 in the target system. This causes the processor to use its $\overline{ERESET}$, $\overline{EBR}$ and $\overline{EBG}$ pins instead of the $\overline{RESET}$, $\overline{BR}$ and $\overline{BG}$ pins. The $\overline{BG}$ output is three-stated. These signals do not need to be jumper-isolated in your system.

The EZ-ICE connects to your target system via a ribbon cable and a 14-pin female plug. The ribbon cable is 10 inches in length with one end fixed to the EZ-ICE. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Target Board Connector for EZ-ICE Probe
The EZ-ICE connector (a standard pin strip header) is shown in Figure 7. You must add this connector to your target board design if you intend to use the EZ-ICE. Be sure to allow enough room in your system to fit the EZ-ICE probe onto the 14-pin connector.

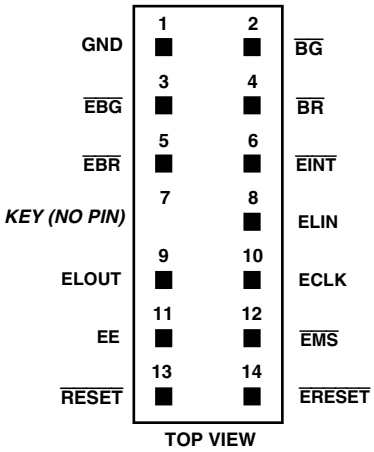


Figure 7. Target Board Connector for EZ-ICE

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—you must remove Pin 7 from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ-ICE probe plug. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

Target Memory Interface
For your target system to be compatible with the EZ-ICE emulator, it must comply with the memory interface guidelines listed below.

PM, DM, BM, IOM and CM
Design your Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM), and Composite Memory (CM) external interfaces to comply with worst case device timing requirements and switching characteristics as specified in the DSP's data sheet. The performance of the EZ-ICE may approach published worst case specification for some memory access timing requirements and switching characteristics.

Note: If your target does not meet the worst case chip specification for memory access parameters, you may not be able to emulate your circuitry at the desired CLKIN frequency. Depending on the severity of the specification violation, you may have trouble manufacturing your system as DSP components statistically vary in switching characteristic and timing requirements within published limits.

Restriction: All memory strobe signals on the ADSP-2183 ($\overline{RD}$, $\overline{WR}$, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$ and $\overline{IOMS}$) used in your target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed at your option when the EZ-ICE is not being used.

Target System Interface Signals
When the EZ-ICE board is installed, the performance on some system signals changes. Design your system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{RESET}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{BR}$ signal.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{BR}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus *only* if bus grant ($\overline{BG}$) is asserted by the EZ-ICE board's DSP.

Target Architecture File
The EZ-ICE software lets you load your program in its linked (executable) form. The EZ-ICE PC program can not load sections of your executable located in boot pages (by the linker). With the exception of boot page 0 (loaded into PM RAM), all sections of your executable mapped into boot pages are not loaded.

Write your target architecture file to indicate that only PM RAM is available for *program storage*, when using the EZ-ICE software's loading feature. Data can be loaded to PM RAM or DM RAM.

ADSP-2183–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	3.0	3.6	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DD} = max	2.0			V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min			0.4	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DD} = min				
		I_{OH} = –0.5 mA	2.4			V
		@ V_{DD} = min				
		I_{OH} = –100 µA[6]	V_{DD} – 0.3			V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DD} = min				
		I_{OL} = 2 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DD} = max				
		V_{IN} = V_{DD} max			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DD} = max				
		V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DD} = max				
		V_{IN} = V_{DD} max[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DD} = max				
		V_{IN} = 0 V[8]			8	µA
I_{DD}	Supply Current (Idle)[9, 10]	@ V_{DD} = 3.3				
		T_{AMB} = +25°C				
		t_{CK} = 19 ns[11]		10		mA
		t_{CK} = 25 ns[11]		9		mA
		t_{CK} = 30 ns[11]		8		mA
		t_{CK} = 34.7 ns[11]		6		mA
I_{DD}	Supply Current (Dynamic)[10, 12]	@ V_{DD} = 3.3				
		T_{AMB} = +25°C				
		t_{CK} = 19 ns[11]		44		mA
		t_{CK} = 25 ns[11]		35		mA
		t_{CK} = 30 ns[11]		30		mA
		t_{CK} = 34.7 ns[11]		26		mA
C_I	Input Pin Capacitance[3, 6, 13]	@ V_{IN} = 2.5 V				
		f_{IN} = 1.0 MHz				
		T_{AMB} = +25°C			8	pF
C_O	Output Pin Capacitance[6, 7, 13, 14]	@ V_{IN} = 2.5 V				
		f_{IN} = 1.0 MHz				
		T_{AMB} = +25°C			8	pF

NOTES

[1]Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, IAD0–IAD15, PF0–PF7.

[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR0, DR1, $\overline{\text{PWD}}$, $\overline{\text{IRQL0}}$, $\overline{\text{IRQL1}}$, $\overline{\text{IRQE}}$, $\overline{\text{IS}}$, $\overline{\text{IRD}}$, $\overline{\text{IWR}}$, IAL.

[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR0, DR1, $\overline{\text{IS}}$, IAL, $\overline{\text{IRD}}$, $\overline{\text{IWR}}$, $\overline{\text{IRQL0}}$, $\overline{\text{IRQL1}}$, $\overline{\text{IRQE}}$, $\overline{\text{PWD}}$.

[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IACK}}$, PWDACK, A0–A13, DT0, DT1, CLKOUT, FL2-0.

[5]Although specified for TTL outputs, all ADSP-2183 outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.

[6]Guaranteed but not tested.

[7]Three-statable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, IAD0–IAD15, PF0–PF7.

[8]0 V on $\overline{\text{BR}}$, CLKIN Active (to force three-state condition).

[9]Idle refers to ADSP-2183 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

[10]Current reflects device operating with no output loads.

[11]V_{IN} = 0.4 V and 2.4 V. For typical figures for supply currents, refer to Power Dissipation section.

[12]I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (types 1, 4, 5, 12, 13, 14), 30% are type 2 and type 6, and 20% are idle instructions.

[13]Applies to LQFP package type and Mini-BGA.

[14]Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.6 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Operating Temperature Range (Ambient) . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) LQFP . . . . . +280°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-2183 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY TIMING SPECIFICATIONS

The table below shows common memory device specifications and the corresponding ADSP-2183 timing parameters, for your convenience.

Memory Device Specification	ADSP-2183 Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted
Data Setup Time	t_{DW}	Data Setup before $\overline{WR}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{WR}$ High
$\overline{OE}$ to Data Valid	t_{RDD}	$\overline{RD}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid

$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$.

FREQUENCY DEPENDENCY FOR TIMING SPECIFICATIONS

t_{CK} is defined as $0.5t_{CKI}$. The ADSP-2183 uses an input clock with a frequency equal to half the instruction rate: a 16.67 MHz input clock (which is equivalent to 60 ns) yields a 30 ns processor cycle (equivalent to 33 MHz). t_{CK} values within the range of $0.5t_{CKI}$ period should be substituted for all relevant timing parameters to obtain the specification value.

Example: $t_{CKH} = 0.5t_{CK} – 7$ ns = 0.5 (34.7 ns) – 7 ns = 10.35 ns

Parameter		Min	Max	Unit
Clock Signals and Reset				
Timing Requirements:				
t_{CKI}	CLKIN Period	38	100	ns
t_{CKIL}	CLKIN Width Low	15		ns
t_{CKIH}	CLKIN Width High	15		ns
Switching Characteristics:				
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} - 7$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} - 7$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirement:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	$5t_{CK}$[1]		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator start-up time).

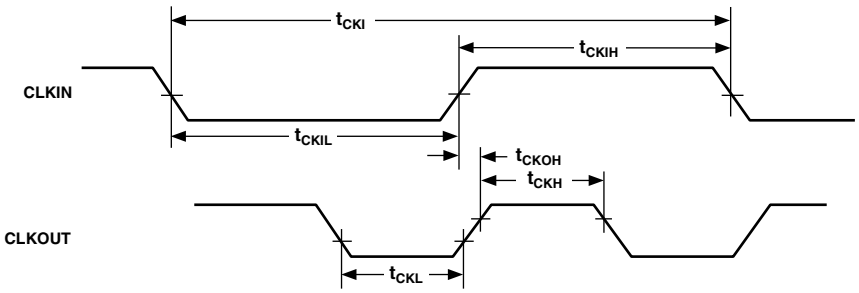


Figure 8. Clock Signals

Parameter		Min	Max	Unit
Interrupts and Flag				
Timing Requirements:				
t_{IFS}	$\overline{\text{IRQx}}$, FI, or PFx Setup before CLKOUT Low [1, 2, 3, 4]	$0.25t_{CK} + 15$		ns
t_{IFH}	$\overline{\text{IRQx}}$, FI, or PFx Hold after CLKOUT High [1, 2, 3, 4]	$0.25t_{CK}$		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	$0.5t_{CK} - 7$		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]		$0.5t_{CK} + 6$	ns

NOTES
[1]If $\overline{\text{IRQx}}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to Interrupt Controller Operation in the Program Control chapter of the User's Manual for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulsewidths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{\text{IRQx}}$ = $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$, $\overline{\text{IRQL0}}$, $\overline{\text{IRQL1}}$, $\overline{\text{IRQE}}$.
[4]PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.
[5]Flag outputs = PFx, FL0, FL1, FL2, Flag_out4.

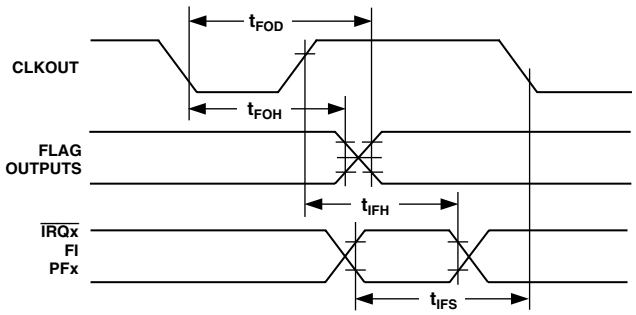


Figure 9. Interrupts and Flags

Parameter		Min	Max	Unit
Bus Request–Bus Grant				
Timing Requirements:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK}$ + 2		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK}$ + 17		ns
Switching Characteristics:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable		$0.25t_{CK}$ + 10	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK}$ – 4		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[2]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[2]	0		ns

NOTES
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.
[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual,* Third Edition, for $\overline{BR}$/$\overline{BG}$ cycle relationships.
[2]$\overline{BGH}$ is asserted when the bus is granted and the processor requires control of the bus to continue.

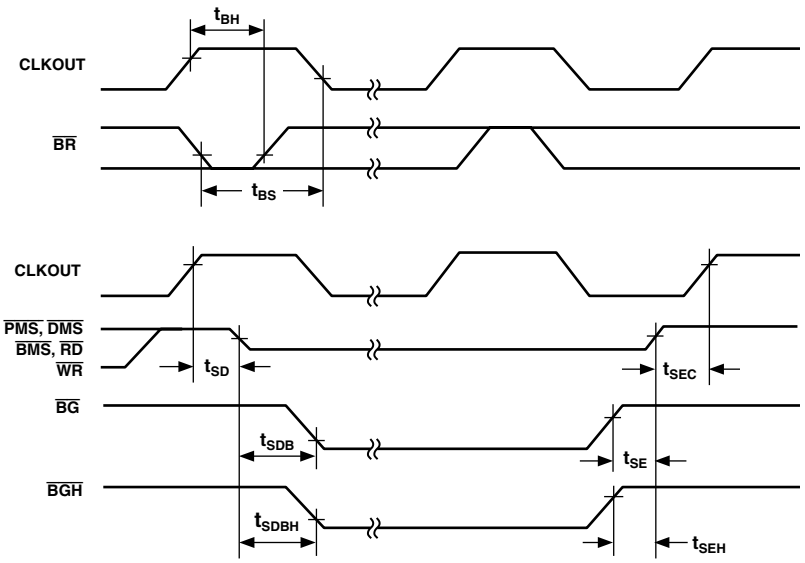


Figure 10. Bus Request–Bus Grant

Parameter		Min	Max	Unit
Memory Read				
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 8 + w$	ns
t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid		$0.75t_{CK} - 10.5 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulsewidth	$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 7$	ns
t_{ASR}	A0–A13, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 4$		ns
t_{RDA}	A0–A13, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

w = wait states × t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

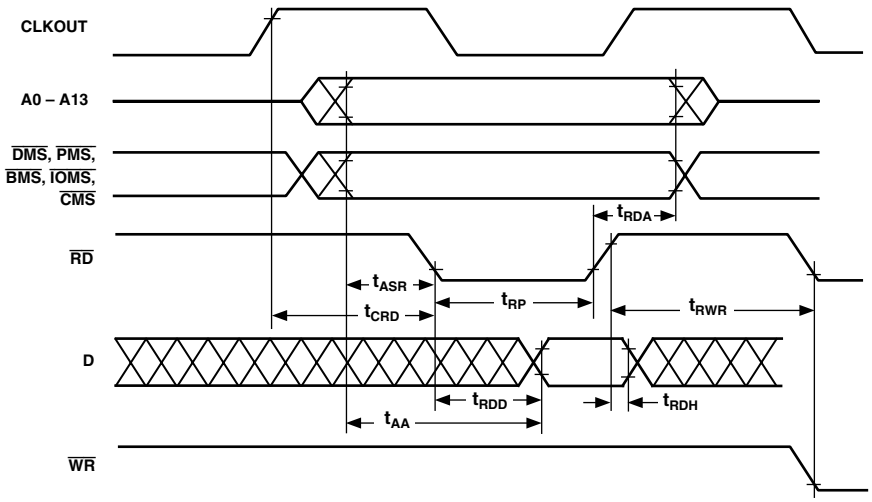


Figure 11. Memory Read

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 7 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 2$		ns
t_{WP}	$\overline{WR}$ Pulsewidth	$0.5t_{CK} - 5 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 4$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 4$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 2$	$0.25\ t_{CK} + 7$	ns
t_{AW}	A0–A13, $\overline{xMS}$, Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 9 + w$		ns
t_{WRA}	A0–A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

w = wait states × t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

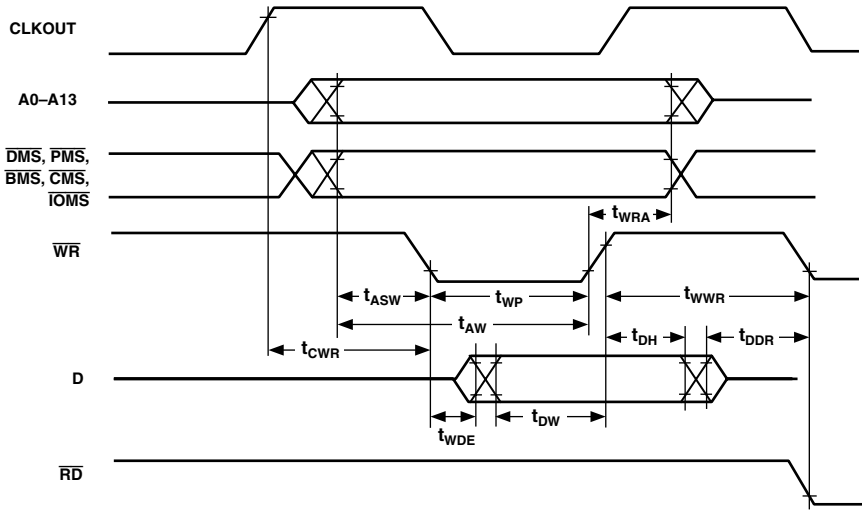


Figure 12. Memory Write

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirements:				
t_{SCK}	SCLK Period	38		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	7		ns
t_{SCP}	$SCLK_{IN}$ Width	15		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to $SCLK_{OUT}$	$0.25t_{CK}$	$0.25t_{CK}$ + 10	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		15	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		15	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		14	ns
t_{SCDD}	SCLK High to DT Disable		15	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		15	ns

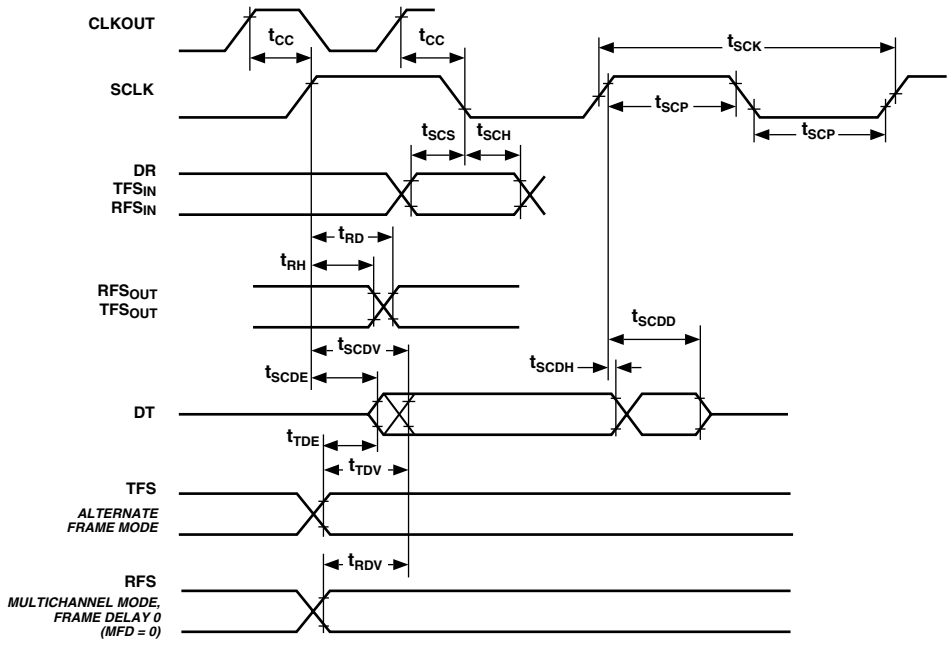


Figure 13. Serial Ports

Parameter		Min	Max	Unit
IDMA Address Latch				
Timing Requirements:				
t_{IALP}	Duration of Address Latch[1, 2]	10		ns
t_{IASU}	IAD15–0 Address Setup before Address Latch End[2]	5		ns
t_{IAH}	IAD15–0 Address Hold after Address Latch End[2]	2		ns
t_{IKA}	$\overline{IACK}$ Low before Start of Address Latch[1]	0		ns
t_{IALS}	Start of Write or Read after Address Latch End[2, 3]	3		ns

NOTES
[1]Start of Address Latch = $\overline{IS}$ Low and IAL High.
[2]End of Address Latch = $\overline{IS}$ High or IAL Low.
[3]Start of Write or Read = $\overline{IS}$ Low and $\overline{IWR}$ Low or $\overline{IRD}$ Low.

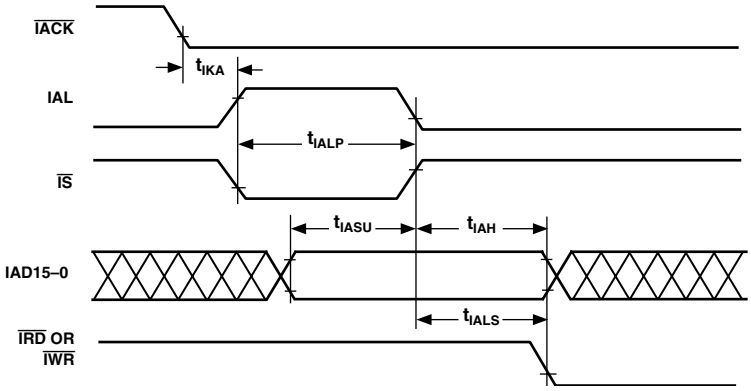


Figure 14. IDMA Address Latch

Parameter		Min	Max	Unit
IDMA Write, Short Write Cycle				
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	15		ns
t_{IDSU}	IAD15–0 Data Setup before End of Write[2, 3, 4]	5		ns
t_{IDH}	IAD15–0 Data Hold after End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High		15	ns

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

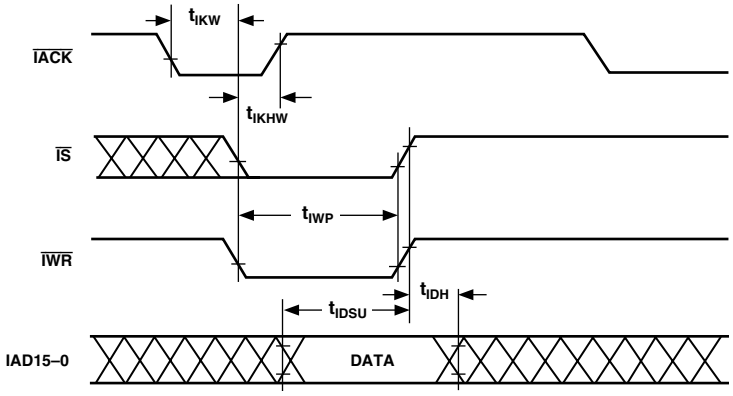


Figure 15. IDMA Write, Short Write Cycle

Parameter		Min	Max	Unit
IDMA Write, Long Write Cycle				
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	0		ns
t_{IKSU}	IAD15–0 Data Setup before $\overline{IACK}$ Low[2, 3]	$0.5t_{CK}$ + 10		ns
t_{IKH}	IAD15–0 Data Hold after $\overline{IACK}$ Low[2, 3]	2		ns
Switching Characteristics:				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low[4]	$1.5t_{CK}$		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High		15	ns

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[3]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[4]This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write Cycle relationships, please refer to the *ADSP-21xx Family User's Manual*, Third Edition.

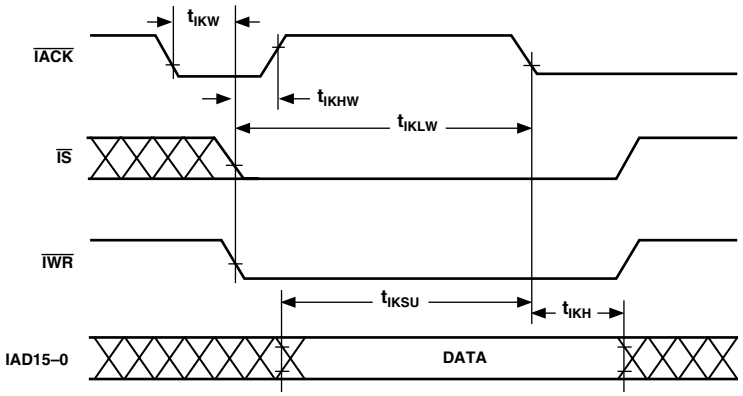


Figure 16. IDMA Write, Long Write Cycle

Parameter		Min	Max	Unit
IDMA Read, Long Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRP}	Duration of Read	15		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]		15	ns
t_{IKDS}	IAD15–0 Data Setup before IACK Low	$0.5t_{CK} - 7$		ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		15	ns
t_{IRDH1}	IAD15–0 Previous Data Hold after Start of Read (DM/PM1)[3]	$2t_{CK} - 5$		ns
t_{IRDH2}	IAD15–0 Previous Data Hold after Start of Read (PM2)[4]	$t_{CK} - 5$		ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.
[3]DM read or first half of PM read.
[4]Second half of PM read.

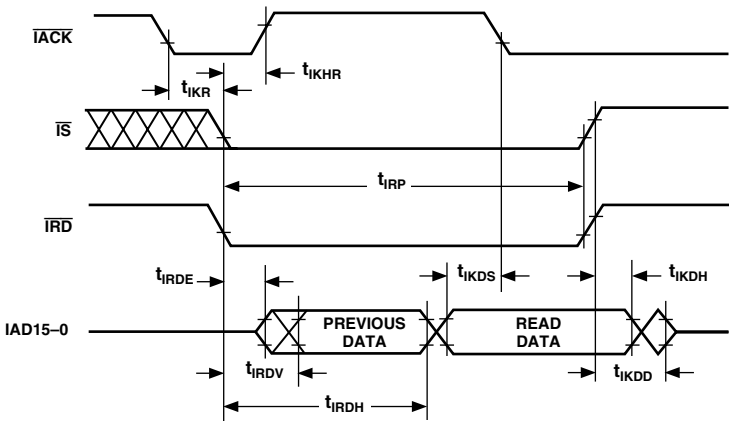


Figure 17. IDMA Read, Long Read Cycle

Parameter		Min	Max	Unit
IDMA Read, Short Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRP}	Duration of Read	15		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]		15	ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		15	ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

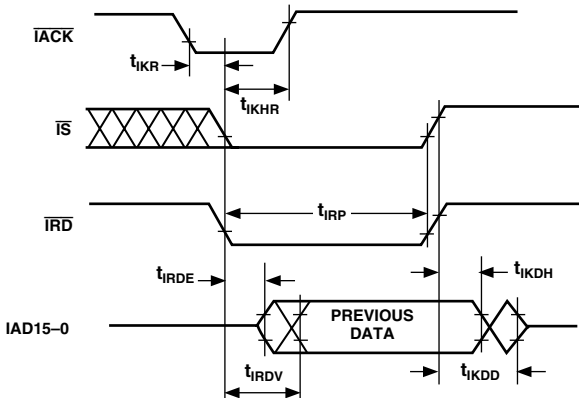


Figure 18. IDMA Read, Short Read Cycle

OUTPUT DRIVE CURRENTS

Figure 19 shows typical I-V characteristics for the output drivers of the ADSP-2183. The curves represent the current drive capability of the output drivers as a function of output voltage.

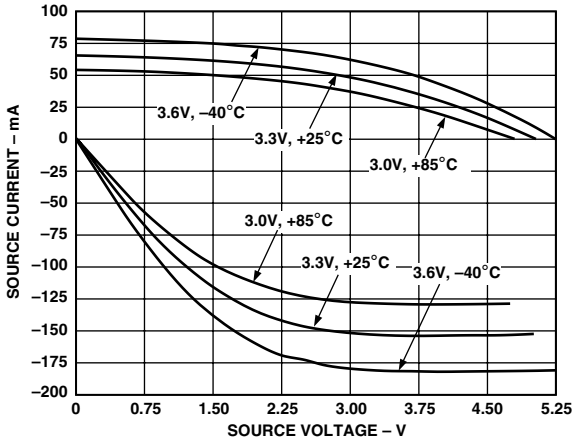
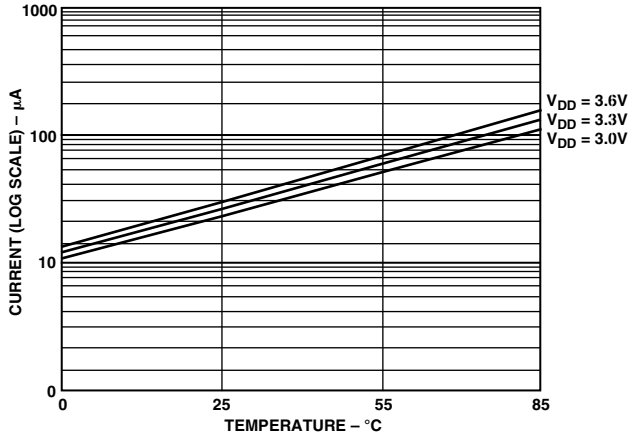


Figure 19. Typical Drive Currents



NOTES:
1. REFLECTS ADSP-2183 OPERATION IN LOWEST POWER MODE. (SEE "SYSTEM INTERFACE" CHAPTER OF THE *ADSP-2100 FAMILY USER'S MANUAL* FOR DETAILS.)
2. CURRENT REFLECTS DEVICE OPERATING WITH NO INPUT LOADS.

Figure 20. Power-Down Supply Current (Typical)

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:
In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 3.3 V and t_{CK} = 30.0 ns.

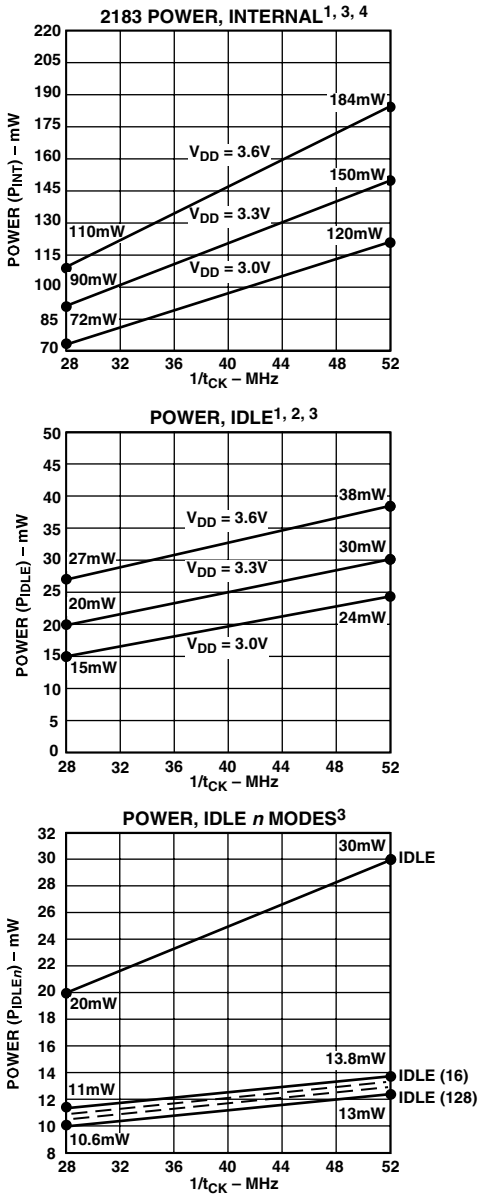
Total Power Dissipation = P_{INT} + $(C \times V_{DD}^2 \times f)$

P_{INT} = internal power dissipation from Power vs. Frequency graph (Figure 20).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

	# of Pins	× C	× V_{DD}^2	× f		
Address, $\overline{DMS}$	8	× 10 pF	× 3.3^2 V	× 33.3 MHz	=	29.0 mW
Data Output, $\overline{WR}$	9	× 10 pF	× 3.3^2 V	× 16.67 MHz	=	16.3 mW
$\overline{RD}$	1	× 10 pF	× 3.3^2 V	× 16.67 MHz	=	1.8 mW
CLKOUT	1	× 10 pF	× 3.3^2 V	× 33.3 MHz	=	3.6 mW
						50.7 mW

Total power dissipation for this example is P_{INT} + 50.7 mW.



VALID FOR ALL TEMPERATURE GRADES.
1POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2IDLE REFERS TO ADSP-2183 STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.
3TYPICAL POWER DISSIPATION AT 3.3V V_{DD} AND 25°C EXCEPT WHERE SPECIFIED.
4I_{DD} MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% OF THE INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1,4,5,12,13,14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.

Figure 21. Power vs. Frequency

CAPACITIVE LOADING

Figures 22 and 23 show the capacitive loading characteristics of the ADSP-2183.

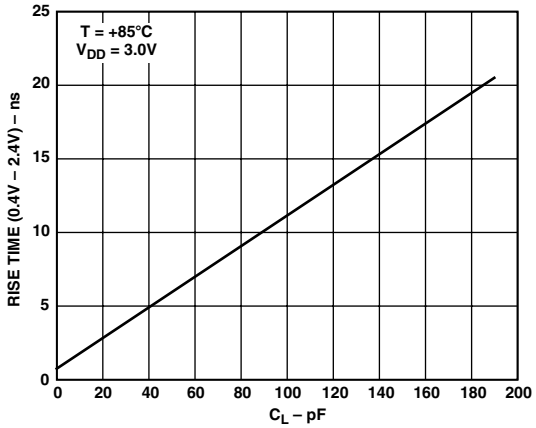


Figure 22. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

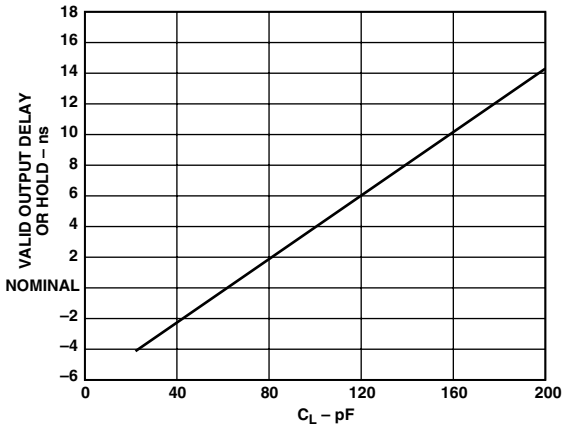


Figure 23. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \bullet 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Figure 24. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

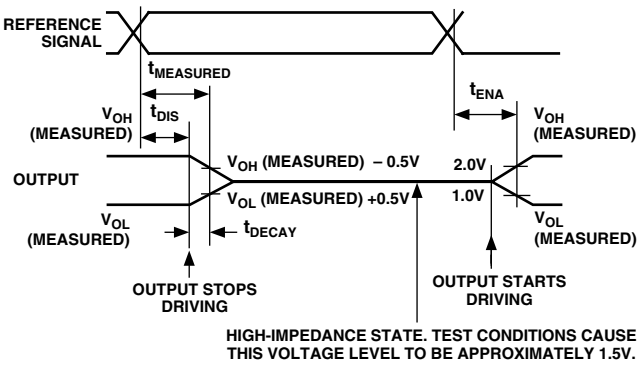


Figure 25. Output Enable/Disable

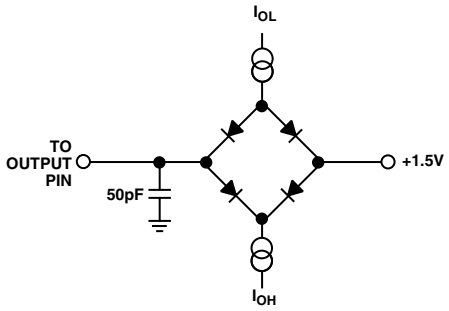


Figure 26. Equivalent Device Loading for AC Measurements (Including All Fixtures)

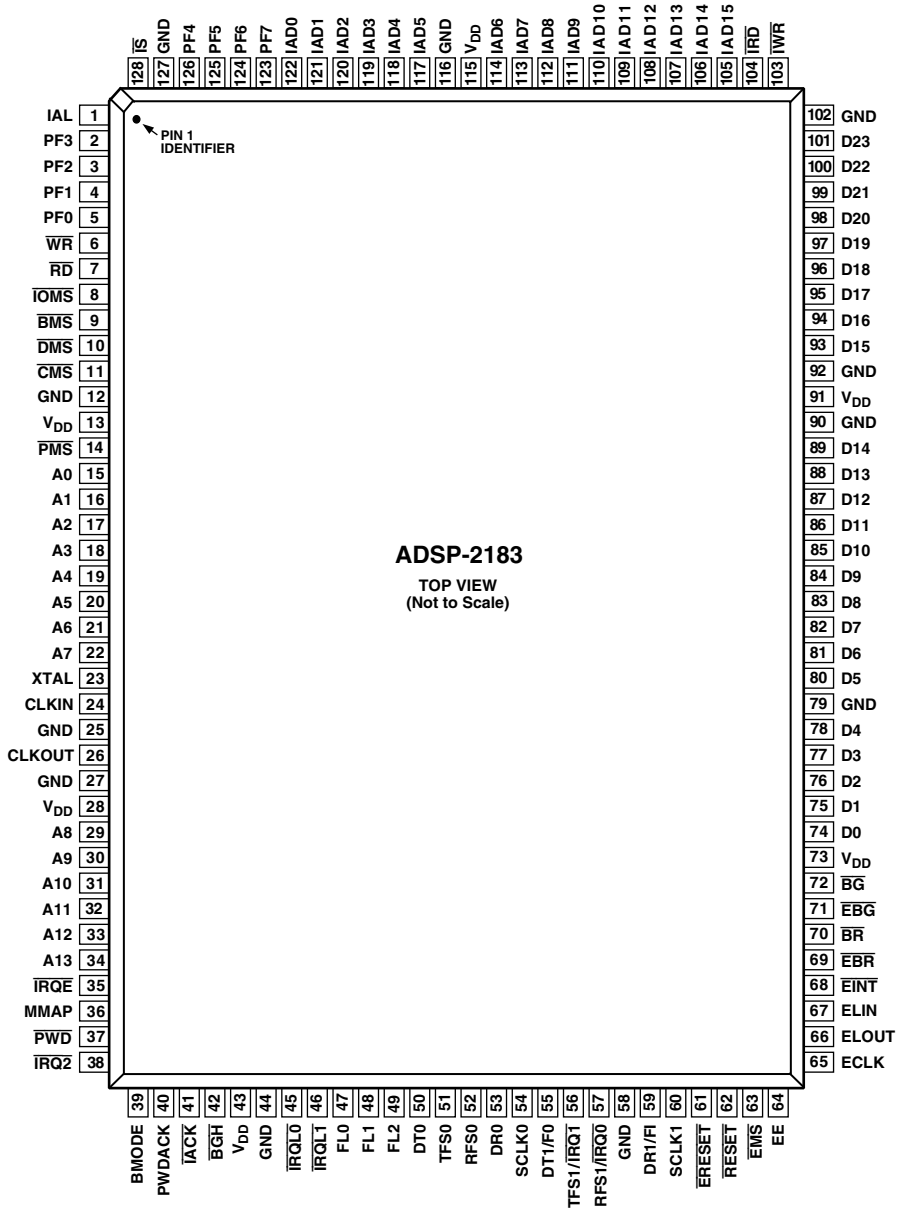
ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
LQFP	50°C/W	2°C/W	48°C/W
Mini-BGA	70.7°C/W	7.4°C/W	63.3°C/W

128-Lead LQFP Package Pinout



LQFP Pin Configurations

LQFP Number	Pin Name	LQFP Number	Pin Name	LQFP Number	Pin Name	LQFP Number	Pin Name
1	IAL	33	A12	65	ECLK	97	D19
2	PF3	34	A13	66	ELOUT	98	D20
3	PF2	35	$\overline{\text{IRQE}}$	67	ELIN	99	D21
4	PF1	36	MMAP	68	$\overline{\text{EINT}}$	100	D22
5	PF0	37	$\overline{\text{PWD}}$	69	$\overline{\text{EBR}}$	101	D23
6	$\overline{\text{WR}}$	38	$\overline{\text{IRQ2}}$	70	$\overline{\text{BR}}$	102	GND
7	$\overline{\text{RD}}$	39	BMODE	71	$\overline{\text{EBG}}$	103	$\overline{\text{IWR}}$
8	$\overline{\text{IOMS}}$	40	PWDACK	72	$\overline{\text{BG}}$	104	$\overline{\text{IRD}}$
9	$\overline{\text{BMS}}$	41	$\overline{\text{IACK}}$	73	VDD	105	IAD15
10	$\overline{\text{DMS}}$	42	$\overline{\text{BGH}}$	74	D0	106	IAD14
11	$\overline{\text{CMS}}$	43	VDD	75	D1	107	IAD13
12	GND	44	GND	76	D2	108	IAD12
13	VDD	45	$\overline{\text{IRQL0}}$	77	D3	109	IAD11
14	$\overline{\text{PMS}}$	46	$\overline{\text{IRQL1}}$	78	D4	110	IAD10
15	A0	47	FL0	79	GND	111	IAD9
16	A1	48	FL1	80	D5	112	IAD8
17	A2	49	FL2	81	D6	113	IAD7
18	A3	50	DT0	82	D7	114	IAD6
19	A4	51	TFS0	83	D8	115	VDD
20	A5	52	RFS0	84	D9	116	GND
21	A6	53	DR0	85	D10	117	IAD5
22	A7	54	SCLK0	86	D11	118	IAD4
23	XTAL	55	DT1/F0	87	D12	119	IAD3
24	CLKIN	56	TFS1/$\overline{\text{IRQ1}}$	88	D13	120	IAD2
25	GND	57	RFS1/$\overline{\text{IRQ0}}$	89	D14	121	IAD1
26	CLKOUT	58	GND	90	GND	122	IAD0
27	GND	59	DR1/FI	91	VDD	123	PF7
28	VDD	60	SCLK1	92	GND	124	PF6
29	A8	61	$\overline{\text{ERESET}}$	93	D15	125	PF5
30	A9	62	$\overline{\text{RESET}}$	94	D16	126	PF4
31	A10	63	$\overline{\text{EMS}}$	95	D17	127	GND
32	A11	64	EE	96	D18	128	$\overline{\text{IS}}$

144-Lead Mini-BGA Package Pinout
(Bottom View)

12	11	10	9	8	7	6	5	4	3	2	1	
GND	GND	$\overline{\text{IWR}}$	IAD14	IAD10	IAD6	GND	IAD2	PF6	GND	$\overline{\text{IS}}$	IAL	A
D21	D23	$\overline{\text{IRD}}$	IAD15	IAD11	VDD	GND	IAD1	PF5	GND	PF3	PF1	B
D17	D20	D22	IAD13	IAD8	VDD	IAD0	PF4	PF2	$\overline{\text{WR}}$	PF0	$\overline{\text{RD}}$	C
GND	D15	D18	D19	D16	IAD9	IAD5	PF7	$\overline{\text{IOMS}}$	GND	$\overline{\text{DMS}}$	GND	D
D14	GND	VDD	GND	GND	IAD7	$\overline{\text{CMS}}$	IAD3	$\overline{\text{BMS}}$	A0	VDD	VDD	E
D10	D11	D13	D12	IAD12	D8	IAD4	$\overline{\text{PMS}}$	A3	A4	A1	A2	F
D6	D5	D9	D4	D7	DT0	A7	A8	A6	GND	A5	XTAL	G
GND	D2	GND	D0	D3	DT1	$\overline{\text{IRQL0}}$	VDD	GND	GND	GND	CLKIN	H
VDD	VDD	D1	BG	RFS1	SCLK0	$\overline{\text{IRQL1}}$	VDD	VDD	A10	VDD	CLKOUT	J
$\overline{\text{EBG}}$	$\overline{\text{BR}}$	$\overline{\text{EBR}}$	$\overline{\text{ERESET}}$	SCLK1	TFS1	TFS0	FL2	PWDACK	A11	A12	A9	K
$\overline{\text{EINT}}$	ELOUT	ELIN	$\overline{\text{RESET}}$	GND	DR0	FL0	GND	$\overline{\text{IACK}}$	$\overline{\text{IRQE}}$	MMAP	A13	L
ECLK	EE	$\overline{\text{EMS}}$	DR1	GND	RFS0	FL1	GND	$\overline{\text{BGH}}$	BMODE	$\overline{\text{IRQ2}}$	$\overline{\text{PWD}}$	M

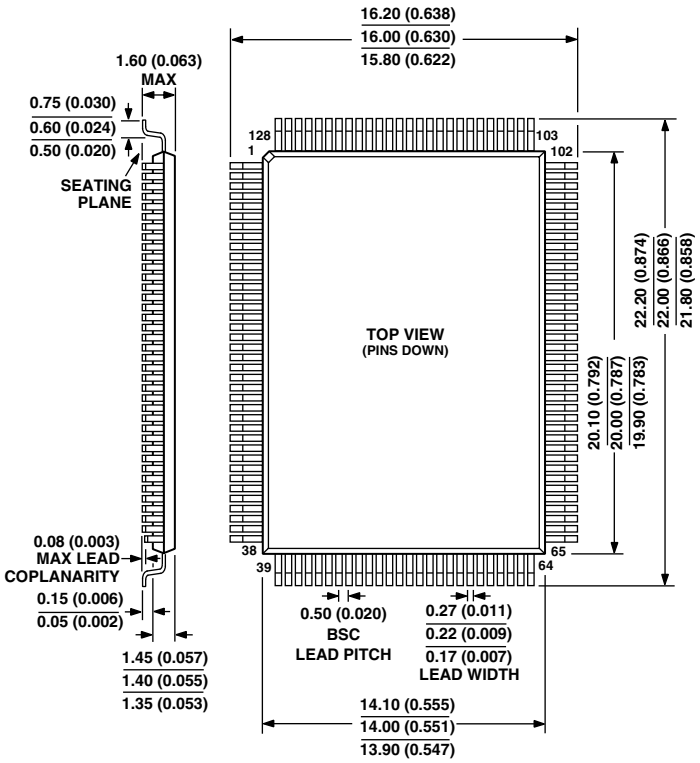
Mini-BGA Pin Configurations

Ball #	Name	Ball #	Name	Ball #	Name	Ball #	Name
A01	IAL	D01	GND	G01	XTAL	K01	A9
A02	$\overline{IS}$	D02	$\overline{DMS}$	G02	A5	K02	A12
A03	GND	D03	GND	G03	GND	K03	A11
A04	PF6	D04	$\overline{IOMS}$	G04	A6	K04	PWDACK
A05	IAD2	D05	PF7	G05	A8	K05	FL2
A06	GND	D06	IAD5	G06	A7	K06	TFS0
A07	IAD6	D07	IAD9	G07	DT0	K07	TFS1
A08	IAD10	D08	D16	G08	D7	K08	SCLK1
A09	IAD14	D09	D19	G09	D4	K09	$\overline{ERESET}$
A10	$\overline{IWR}$	D10	D18	G10	D9	K10	EBR
A11	GND	D11	D15	G11	D5	K11	BR
A12	GND	D12	GND	G12	D6	K12	EBG
B01	PF1	E01	VDD	H01	CLKIN	L01	A13
B02	PF3	E02	VDD	H02	GND	L02	MMAP
B03	GND	E03	A0	H03	GND	L03	$\overline{IRQE}$
B04	PF5	E04	$\overline{BMS}$	H04	GND	L04	$\overline{IACK}$
B05	IAD1	E05	IAD3	H05	VDD	L05	GND
B06	GND	E06	$\overline{CMS}$	H06	$\overline{IRQL0}$	L06	FL0
B07	VDD	E07	IAD7	H07	DT1	L07	DR0
B08	IAD11	E08	GND	H08	D3	L08	GND
B09	IAD15	E09	GND	H09	D0	L09	$\overline{RESET}$
B10	$\overline{IRD}$	E10	VDD	H10	GND	L10	ELIN
B11	D23	E11	GND	H11	D2	L11	ELOUT
B12	D21	E12	D14	H12	GND	L12	EINT
C01	$\overline{RD}$	F01	A2	J01	CLKOUT	M01	$\overline{PWD}$
C02	PF0	F02	A1	J02	VDD	M02	$\overline{IRQ2}$
C03	$\overline{WR}$	F03	A4	J03	A10	M03	BMODE
C04	PF2	F04	A3	J04	VDD	M04	$\overline{BGH}$
C05	PF4	F05	$\overline{PMS}$	J05	VDD	M05	GND
C06	IAD0	F06	IAD4	J06	$\overline{IRQL1}$	M06	FL1
C07	VDD	F07	D8	J07	SCLK0	M07	RFS0
C08	IAD8	F08	IAD12	J08	RFS1	M08	GND
C09	IAD13	F09	D12	J09	BG	M09	DR1
C10	D22	F10	D13	J10	D1	M10	$\overline{EMS}$
C11	D20	F11	D11	J11	VDD	M11	EE
C12	D17	F12	D10	J12	VDD	M12	ECLK

OUTLINE DIMENSIONS

Dimensions given in mm and (inches).

128-Lead Metric Plastic Thin Quad Flatpack (LQFP) (ST-128)

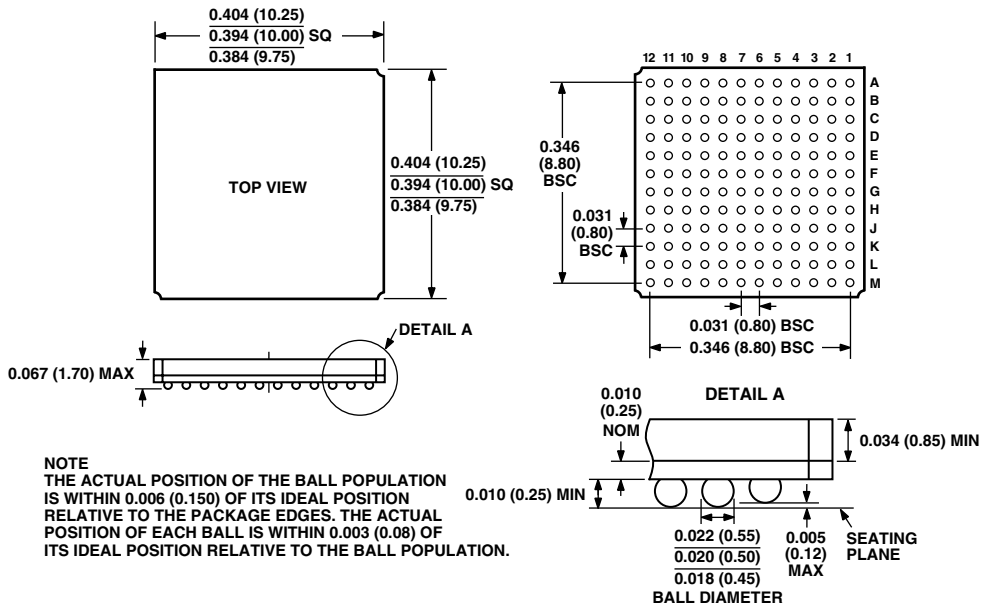


NOTES:
THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 (0.0032) FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.
CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED

OUTLINE DIMENSIONS

Dimensions given in mm and (inches).

144-Lead Mini-BGA Package Pinout
(CA-144)



NOTE
THE ACTUAL POSITION OF THE BALL POPULATION IS WITHIN 0.006 (0.150) OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.003 (0.08) OF ITS IDEAL POSITION RELATIVE TO THE BALL POPULATION.

ORDERING GUIDE

Part Number	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2183KST-115	0°C to +70°C	28.8	128-Lead LQFP	ST-128
ADSP-2183BST-115	–40°C to +85°C	28.8	128-Lead LQFP	ST-128
ADSP-2183KST-133	0°C to +70°C	33.3	128-Lead LQFP	ST-128
ADSP-2183BST-133	–40°C to +85°C	33.3	128-Lead LQFP	ST-128
ADSP-2183KST-160	0°C to +70°C	40	128-Lead LQFP	ST-128
ADSP-2183BST-160	–40°C to +85°C	40	128-Lead LQFP	ST-128
ADSP-2183KST-210	0°C to +70°C	52	128-Lead LQFP	ST-128
ADSP-2183KCA-210	0°C to +70°C	52	144-Lead Mini-BGA	CA-144

C00184b–0–7/00 (rev. C)

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