



# THE DATASHEET OF STP8N80K5



## N-channel 800 V, 0.8 $\Omega$ typ., 6 A Zener-protected SuperMESH™ 5 Power MOSFET in TO-220 and IPAK packages

Datasheet – production data

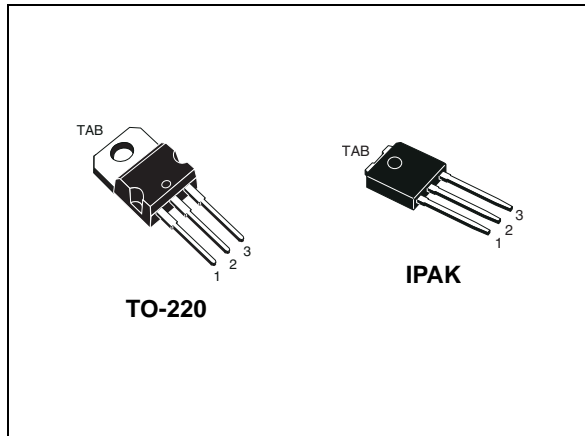
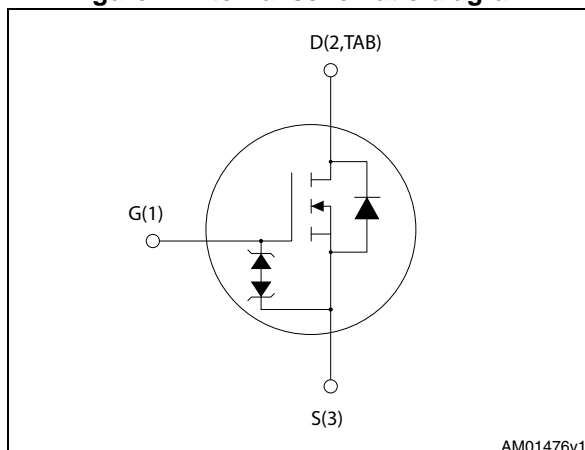


Figure 1. Internal schematic diagram



### Features

Order codes	$V_{DS}$	$R_{DS(on)max.}$	$I_D$	$P_{TOT}$
STP8N80K5	800 V	0.95 $\Omega$	6 A	110 W
STU8N80K5				

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

These N-channel Zener-protected Power MOSFETs are designed using ST's revolutionary avalanche-rugged very high voltage SuperMESH™ 5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STP8N80K5	8N80K5	TO-220	Tube
STU8N80K5		IPAK	

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## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current $T_C = 25\text{ }^\circ\text{C}$	6	A
$I_D$	Drain current $T_C = 100\text{ }^\circ\text{C}$	4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	24	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	110	W
$I_{AR}^{(2)}$	Max current during repetitive or single pulse avalanche	2	A
$E_{AS}^{(3)}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	114	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(5)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	- 55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2. Pulse width limited by  $T_{Jmax}$ .
3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AS}$ ,  $V_{DD} = 50\text{ V}$
4.  $I_{SD} \leq 6\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} \leq V_{(BR)DSS}$
5.  $V_{DS} \leq 640\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		TO-220	IPAK	
$R_{thj-case}$	Thermal resistance junction-case max.	1.14		$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max.	62.5	100	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	800			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 800 V,			1	μA
		V <sub>DS</sub> = 800 V, T <sub>c</sub> =125 °C			50	μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			±10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3 A		0.8	0.95	Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0	-	450	-	pF
C <sub>oss</sub>	Output capacitance		-	50	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	1	-	pF
C <sub>o(tr)</sub> <sup>(1)</sup>	Equivalent capacitance time related	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0 to 640 V	-	57	-	pF
C <sub>o(er)</sub> <sup>(2)</sup>	Equivalent capacitance energy related		-	24	-	pF
R <sub>G</sub>	Intrinsic gate resistance	f = 1 MHz open drain	-	6	-	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 640 V, I <sub>D</sub> = 6 A V <sub>GS</sub> = 10 V (see <a href="#">Figure 18</a> )	-	16.5	-	nC
Q <sub>gs</sub>	Gate-source charge		-	3.2	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	11	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 3\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 20</a> )	-	12	-	ns
$t_r$	Rise time		-	14	-	ns
$t_{d(off)}$	Turn-off delay time		-	32	-	ns
$t_f$	Fall time		-	20	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		6	A
$I_{SDM}$	Source-drain current (pulsed)				24	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 6\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , (see <a href="#">Figure 19</a> )	-	300		ns
$Q_{rr}$	Reverse recovery charge		-	3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	20		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 19</a> )	-	415		ns
$Q_{rr}$	Reverse recovery charge		-	3.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	18		A

1. Pulsed: pulse duration =  $300\ \mu\text{s}$ , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

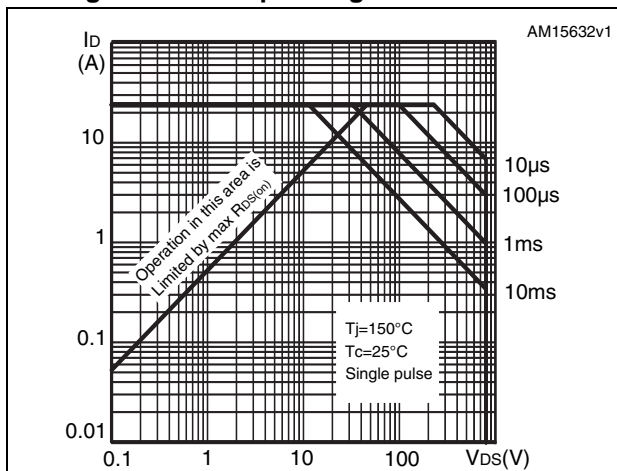


Figure 3. Thermal impedance for TO-220

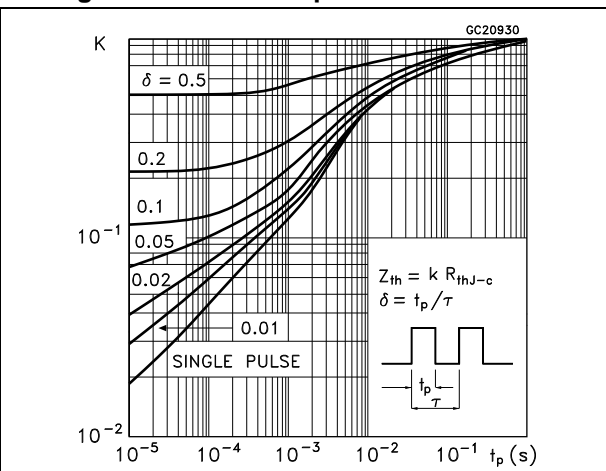


Figure 4. Safe operating area for IPAK

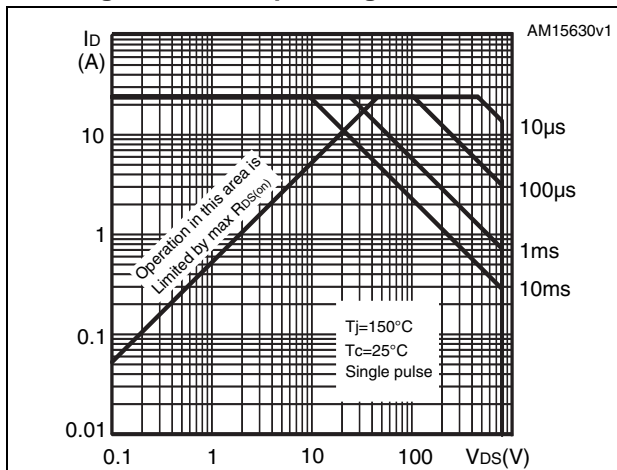


Figure 5. Thermal impedance for IPAK

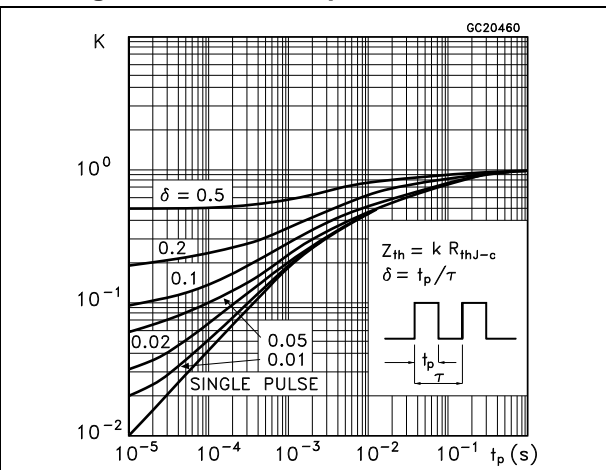


Figure 6. Output characteristics

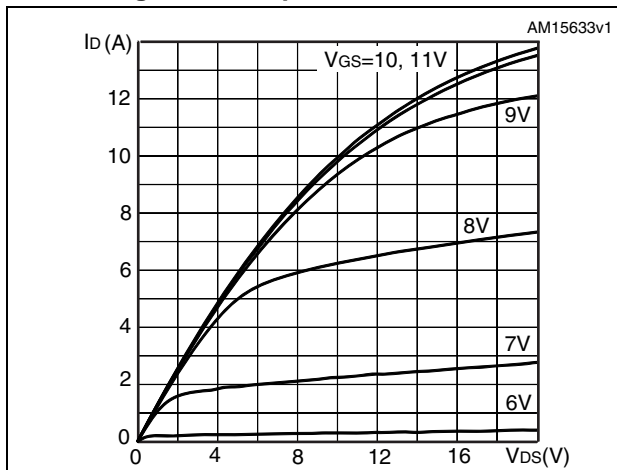


Figure 7. Transfer characteristics

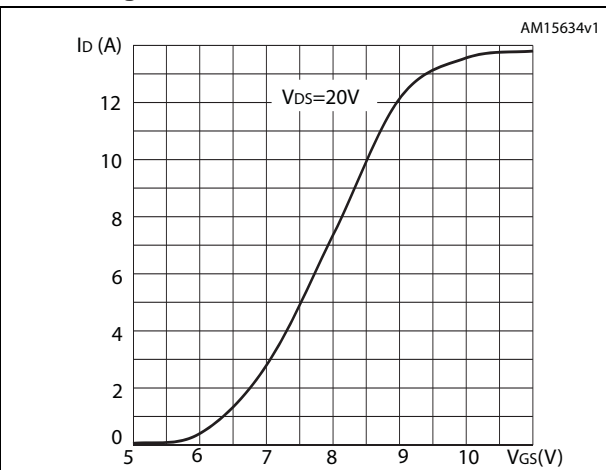


Figure 8. Gate charge vs gate-source voltage

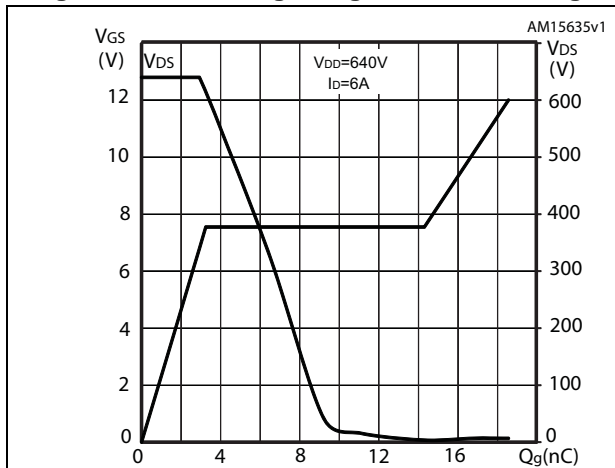


Figure 9. Static drain-source on-resistance

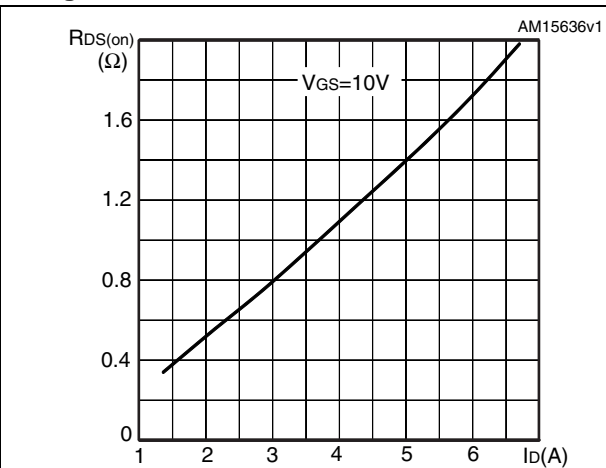


Figure 10. Capacitance variations

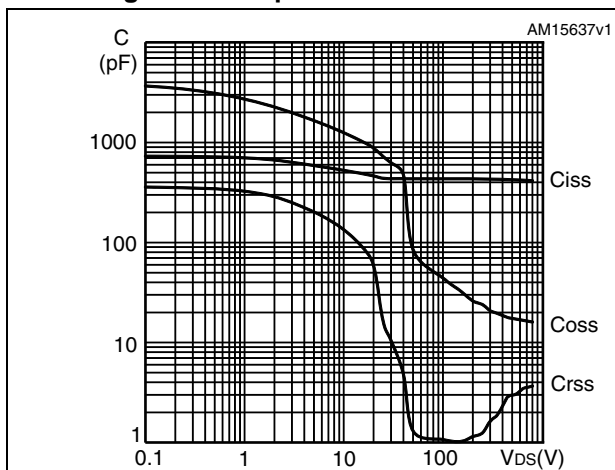


Figure 11. Output capacitance stored energy

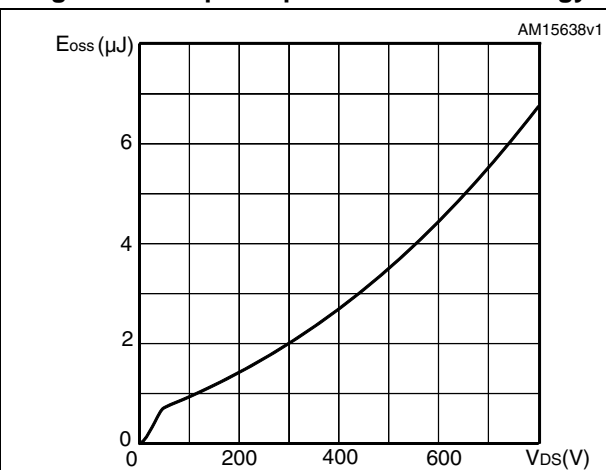


Figure 12. Normalized gate threshold voltage vs. temperature

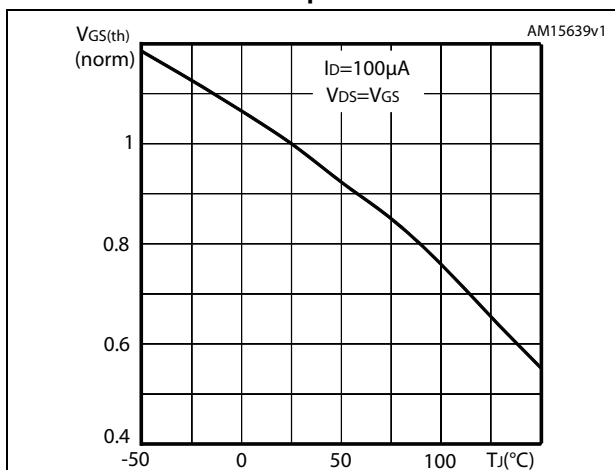


Figure 13. Normalized on-resistance vs. temperature

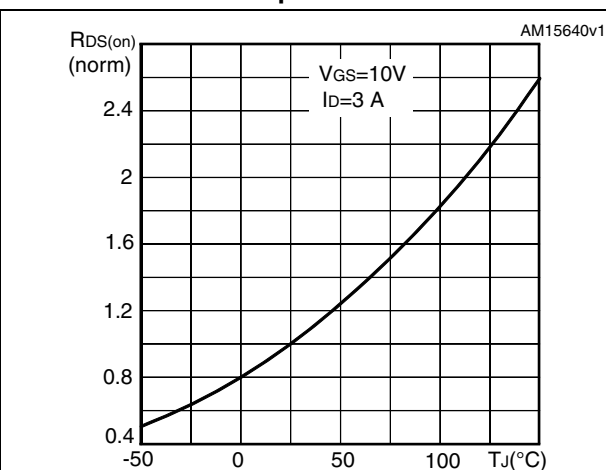


Figure 14. Drain-source diode forward characteristics

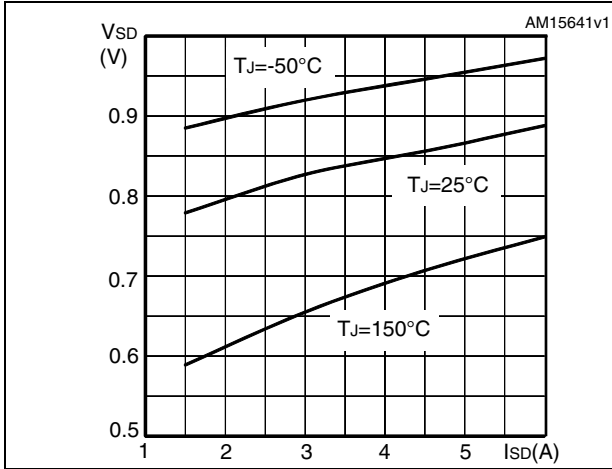


Figure 15. Normalized V<sub>DS</sub> vs. temperature

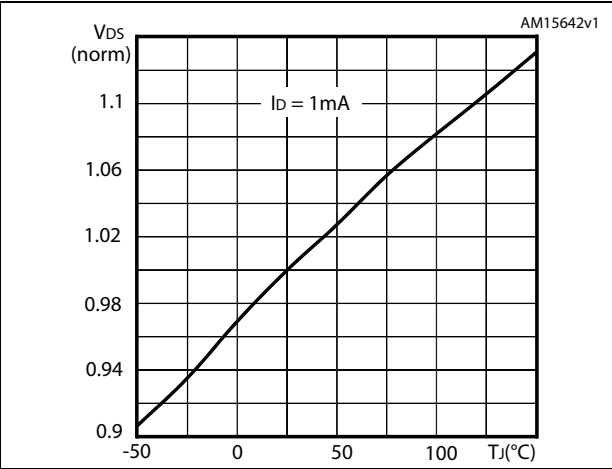
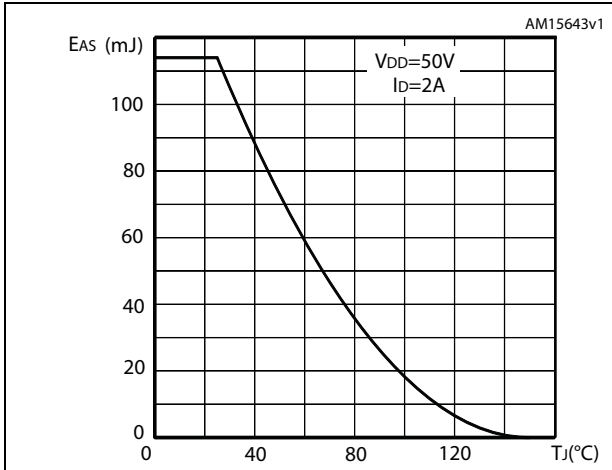


Figure 16. Maximum avalanche energy vs. starting TJ



### 3 Test circuits

Figure 17. Switching times test circuit for resistive load

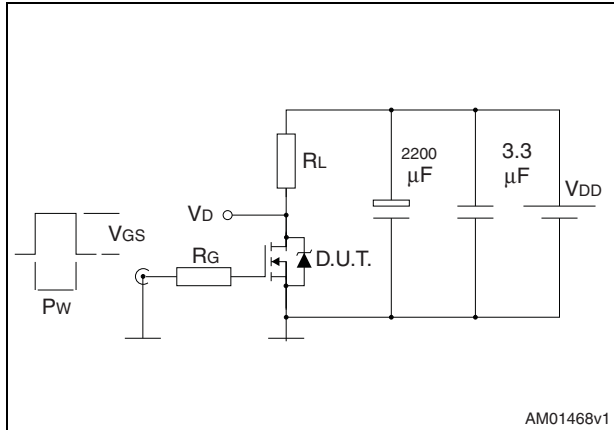


Figure 18. Gate charge test circuit

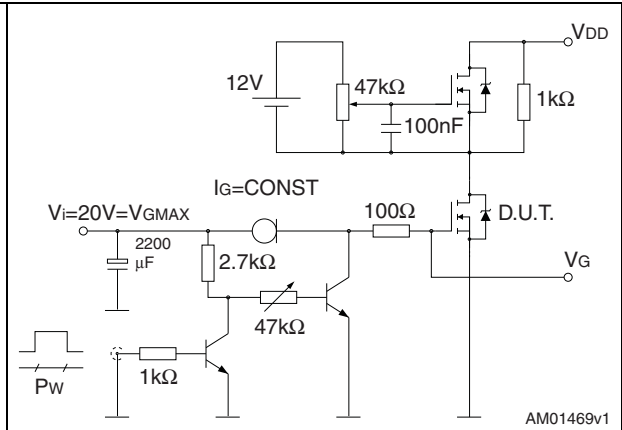


Figure 19. Test circuit for inductive load switching and diode recovery times

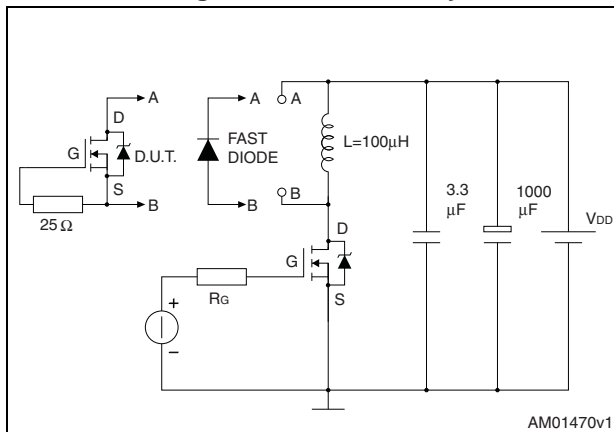


Figure 20. Unclamped inductive load test circuit

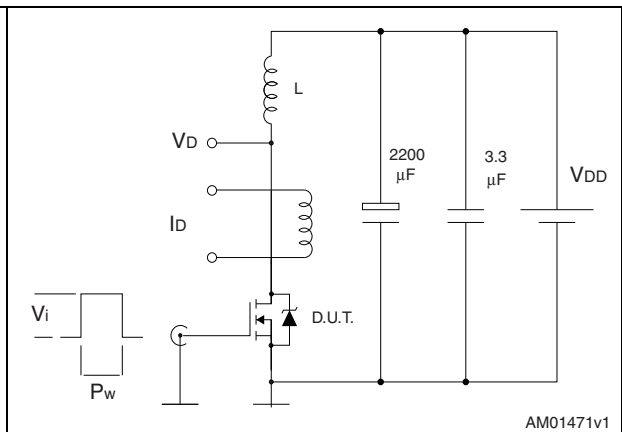


Figure 21. Unclamped inductive waveform

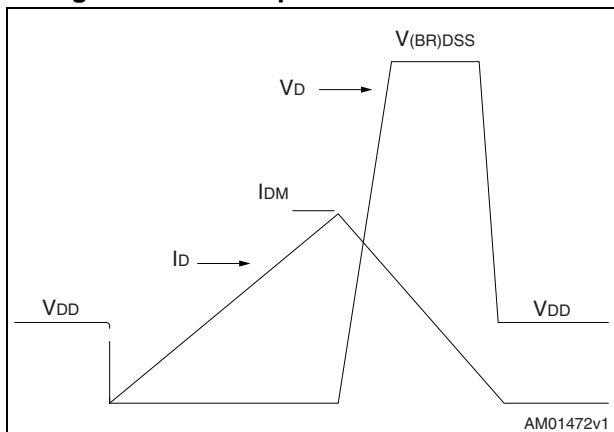
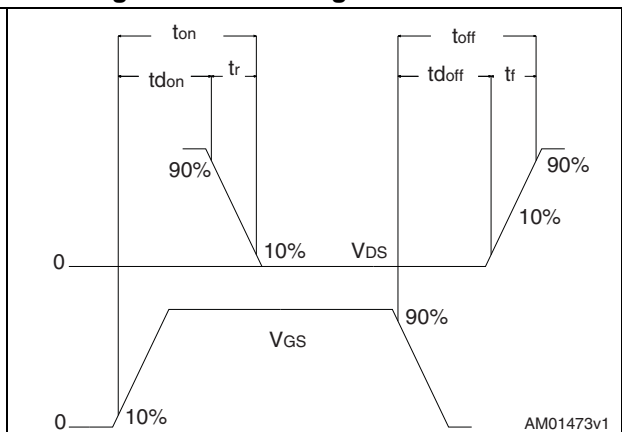


Figure 22. Switching time waveform



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 23. TO-220 type A drawing

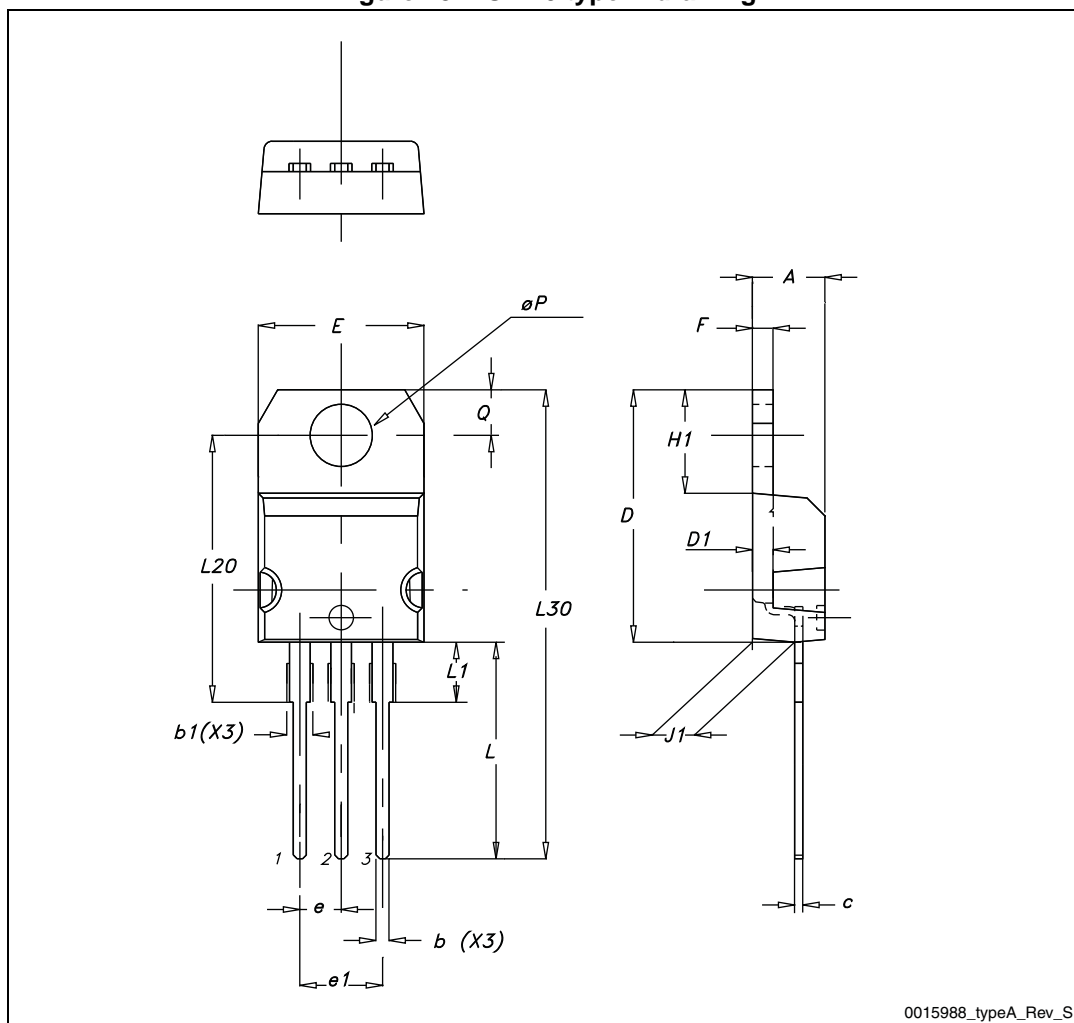
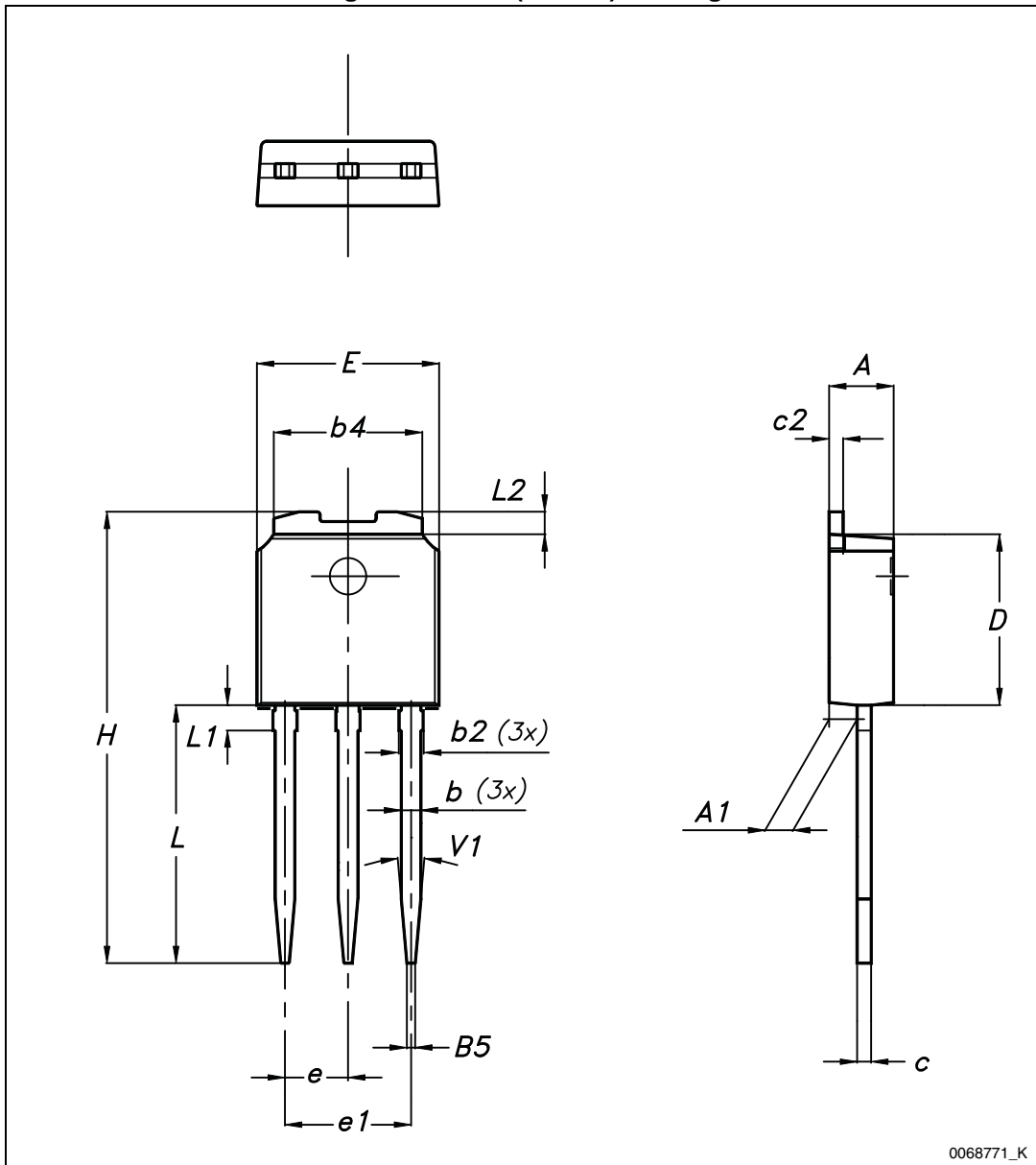


Table 10. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 24. IPAK (TO-251) drawing



## 5 Revision history

**Table 11. Document revision history**

Date	Revision	Changes
06-Aug-2012	1	First release.
16-Oct-2012	2	<ul style="list-style-type: none"> <li>– Minor text changes in cover page</li> <li>– Updated: <math>P_{TOT}</math> value for DPAK, TO-220 and IPAK in <a href="#">Table 2</a>, <math>R_{thj-case}</math> value for DPAK in <a href="#">Table 3</a>, <math>V_{SD}</math> value in <a href="#">Table 7</a></li> <li>– Deleted <math>T_I</math> in <a href="#">Table 3</a></li> <li>– Updated <a href="#">Section 4: Package mechanical data</a> for DPAK and IPAK</li> </ul>
21-Mar-2013	3	<ul style="list-style-type: none"> <li>– Minor text changes</li> <li>– Added: <a href="#">Section 2.1: Electrical characteristics (curves)</a></li> <li>– Modified: <a href="#">Figure 1</a>, <math>I_{AR}</math>, <math>I_{AS}</math>, <a href="#">note 4</a> on <a href="#">Table 2</a>, <math>R_{DS(on)}</math> typical value on <a href="#">Table 4</a>, typical values on <a href="#">Table 5</a>, <a href="#">6</a> and <a href="#">7</a></li> <li>– Updated: <a href="#">Section 4: Package mechanical data</a></li> <li>– The part numbers STF8N80K5, STFI8N80K5 and STD8N80K5 have been moved to the separate datasheets</li> </ul>
27-Mar-2013	4	Added: MOSFET dv/dt ruggedness on <a href="#">Table 2</a>

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