



# THE DATASHEET OF ADS804E





# 12-Bit, 10MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- HIGH SFDR: 80dB at NYQUIST
- HIGH SNR: 69dB
- LOW POWER: 180mW
- LOW DLE:  $\pm 0.3$ LSB
- FLEXIBLE INPUT RANGE
- OVERRANGE INDICATOR

## APPLICATIONS

- IF AND BASEBAND DIGITIZATION
- CCD IMAGING
- SCANNERS
- TEST INSTRUMENTATION

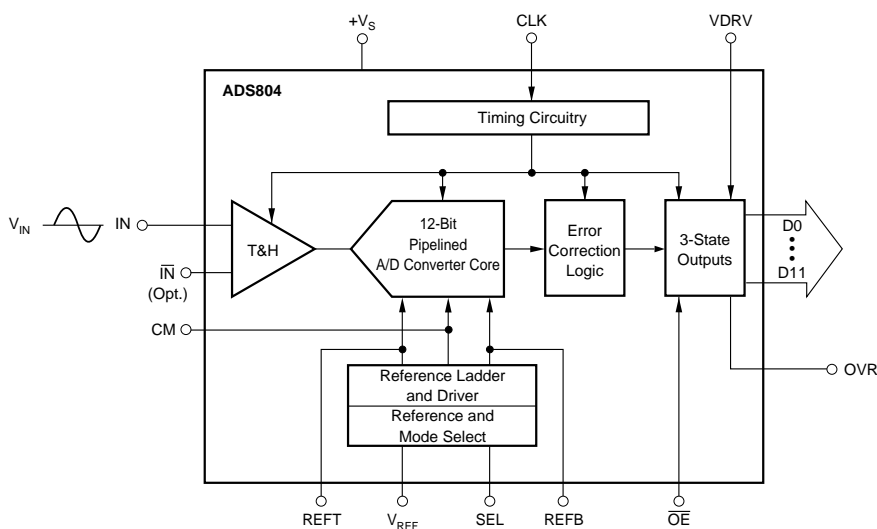
## DESCRIPTION

The ADS804 is a high-speed, high dynamic range, 12-bit, pipelined Analog-to-Digital (A/D) converter. This converter includes a high-bandwidth track-and-hold that gives excellent spurious performance up to and beyond the Nyquist rate. This high-bandwidth, linear track-and-hold minimizes harmonics and has low jitter, leading to excellent SNR performance. The ADS804 is also pin-compatible with the 5MHz ADS803 and the 20MHz ADS805.

The ADS804 provides an internal reference and can be programmed for a 2Vp-p input range for the best spurious performance and ease of driving. Alternatively, the 5Vp-p input range can be used for the lowest input referred noise

of 0.09LSBs rms giving superior imaging performance. There is also a capability to set the input range in between the 2Vp-p and 5Vp-p input ranges or to use external reference. The ADS804 also provides an over-range indicator flag to indicate an input range that exceeds the full-scale input range of the converter. This flag can be used to reduce the gain of the front end gain-ranging circuitry.

The ADS804 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for communications, medical imaging, video, and test instrumentation applications. The ADS804 is available in a SSOP-28 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

+V <sub>S</sub> , VDRV .....	+6V
Analog Input .....	(-0.3V) to (+V <sub>S</sub> + 0.3V)
Logic Input .....	(-0.3V) to (+V <sub>S</sub> + 0.3V)
Case Temperature .....	+100°C
Junction Temperature .....	+150°C
Storage Temperature .....	+150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR <sup>(1)</sup>	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS804	SSOP-28	DB	-40°C to +85°C	ADS804E	ADS804E	Rails, 48
"	"	"	"	"	ADS804E/1K	Tape and Reel, 1000

NOTE: (1) For the most current specifications and package information, refer to our web site at [www.ti.com](http://www.ti.com).

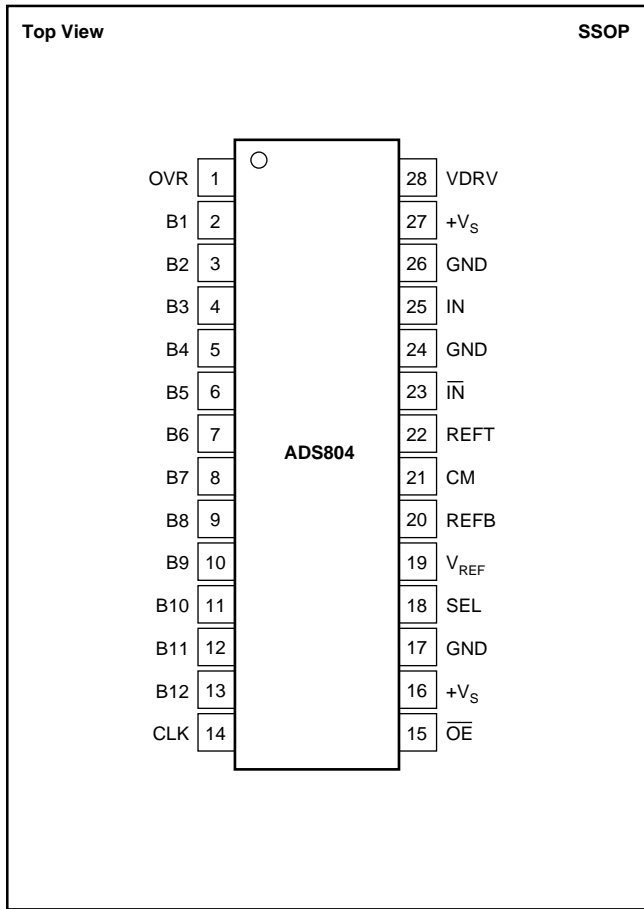
## ELECTRICAL CHARACTERISTICS

At T<sub>A</sub> = full specified temperature range, V<sub>S</sub> = +5V, specified input range = 1.5V to 3.5V, single-ended input, and sampling rate = 5MHz, unless otherwise specified.

PARAMETER	CONDITIONS	ADS804E			UNITS
		MIN	TYP	MAX	
RESOLUTION			12		Bits
SPECIFIED TEMPERATURE RANGE			-40 to +85		°C
<b>CONVERSION CHARACTERISTICS</b>					
Sample Rate		10k		10M	Samples/s
Data Latency			6		Clk Cycles
<b>ANALOG INPUT</b>					
Single-Ended Input Range		1.5		3.5	V
Single-Ended Input Range (Optional)		0		5	V
Common-Mode Voltage			+2.5		V
Input Impedance			1.25    16		MΩ    pF
Track-Mode Input Bandwidth	-3dBFS Input		270		MHz
<b>DYNAMIC CHARACTERISTICS</b>					
Differential Linearity Error (Largest Code Error)			±0.3	±0.75	LSB
f = 500kHz			Tested		
No Missing Codes					
Spurious-Free Dynamic Range <sup>(1)</sup>		73	80		dBFS
f = 4.8MHz					
2-Tone Intermodulation Distortion <sup>(3)</sup>			76		dBc
f = 3.5MHz and 4.0MHz (-7dBFS each tone)					
Signal-to-Noise Ratio (SNR)		66.5	69		dBFS
f = 4.8MHz					
Signal-to-(Noise + Distortion) (SINAD)		65	68		dBFS
f = 4.8MHz					
Effective Number of Bits at 4.8MHz <sup>(4)</sup>			11		Bits
Input Referred Noise	0V to 5V Input		0.09		LSBs rms
	1.5V to 3.5V Input		0.23		LSBs rms
Integral Nonlinearity Error			±1	±2	LSB
f = 500kHz					
Aperture Delay Time			1		ns
Aperture Jitter			4		ps rms
Over-Voltage Recovery Time	1.5 • FS Input		2		ns
Full-Scale Step Acquisition Time			30		ns



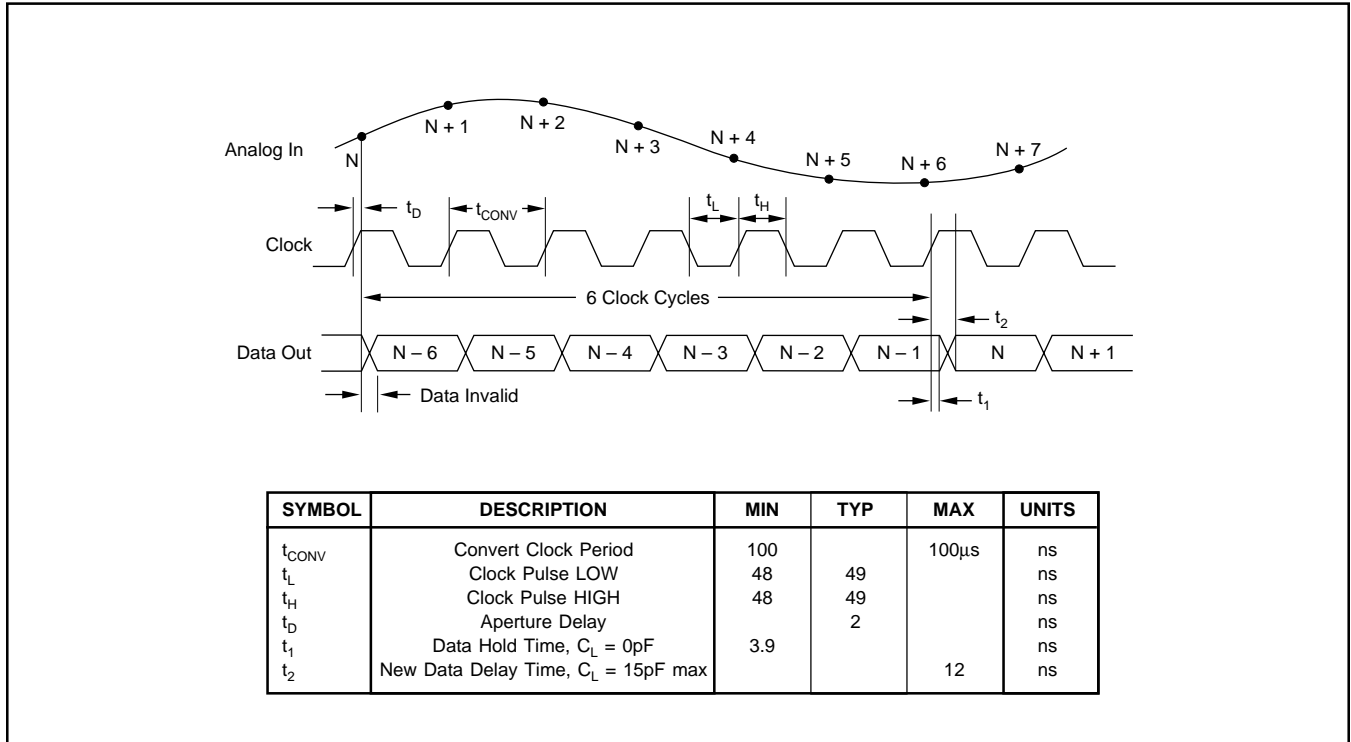
## PIN CONFIGURATION



## PIN DESCRIPTIONS

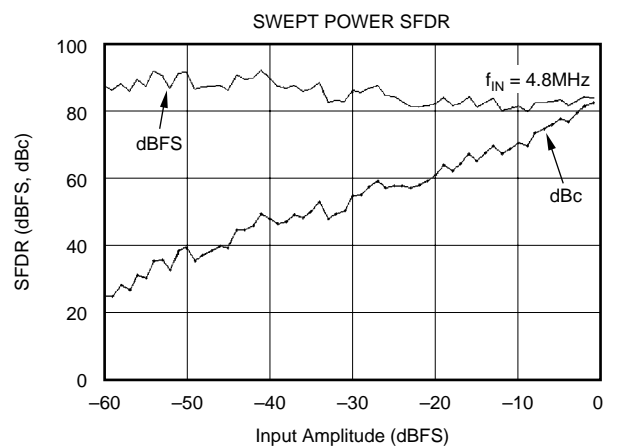
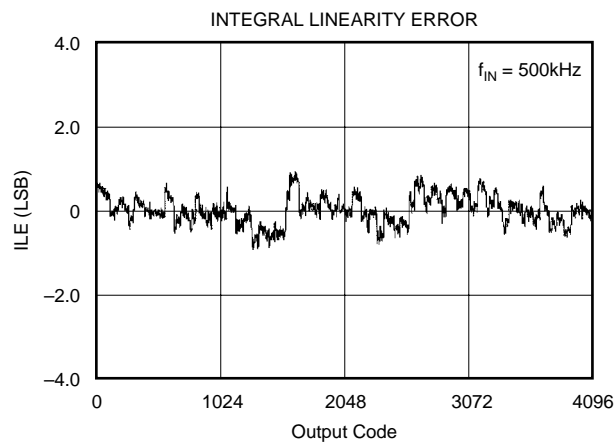
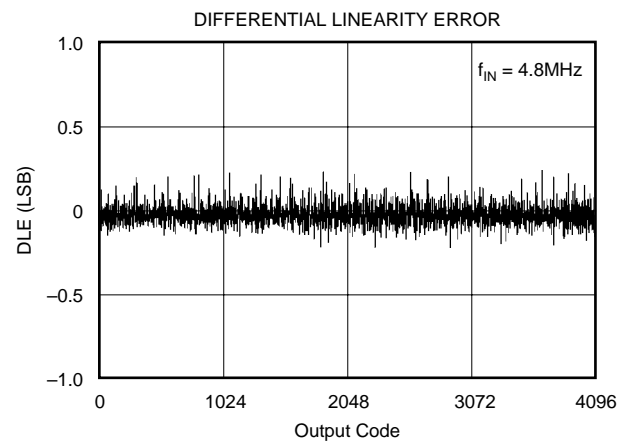
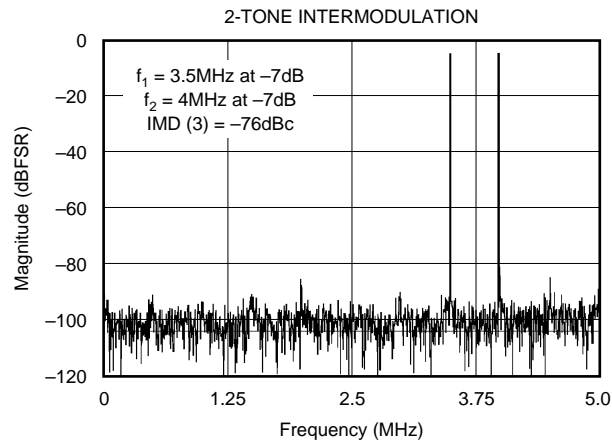
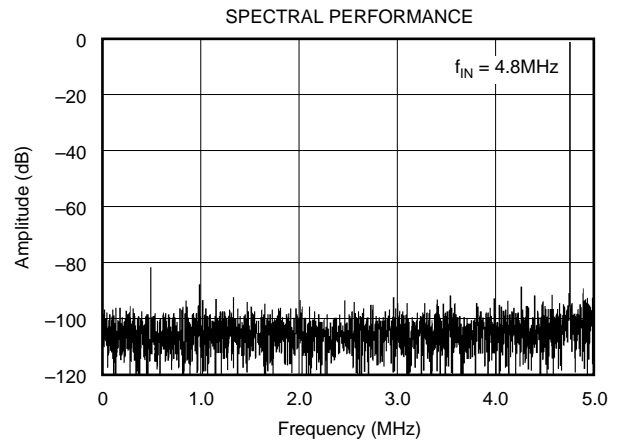
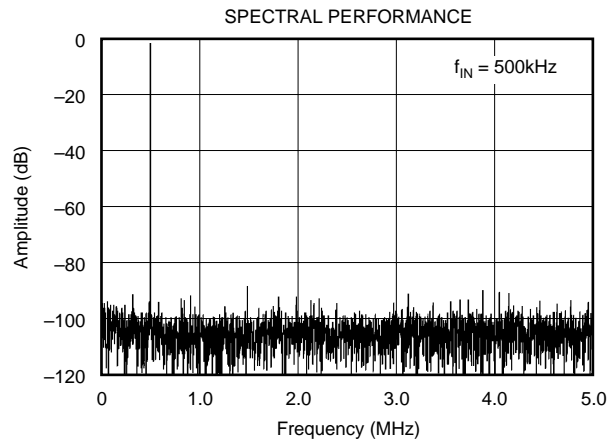
PIN	DESIGNATOR	DESCRIPTION
1	OVR	Over-Range Indicator (See Application Section)
2	B1	Data Bit 1 (D11) (MSB)
3	B2	Data Bit 2 (D10)
4	B3	Data Bit 3 (D9)
5	B4	Data Bit 4 (D8)
6	B5	Data Bit 5 (D7)
7	B6	Data Bit 6 (D6)
8	B7	Data Bit 7 (D5)
9	B8	Data Bit 8 (D4)
10	B9	Data Bit 9 (D3)
11	B10	Data Bit 10 (D2)
12	B11	Data Bit 11 (D1)
13	B12	Data Bit 12 (D0) (LSB)
14	CLK	Convert Clock Input
15	$\overline{OE}$	Output Enable. H = High Impedance State. L = Low or floating, normal operation (Internal pull-down resistor).
16	+V <sub>S</sub>	+5V Supply
17	GND	Ground
18	SEL	Input Range Select (See Application Section)
19	V <sub>REF</sub>	Reference Voltage Select (I/O)
20	REFB	Bottom Reference
21	CM	Common-Mode Voltage
22	REFT	Top Reference
23	$\overline{IN}$	Analog Input (-)
24	GND	Ground
25	IN	Analog Input (+)
26	GND	Ground
27	+V <sub>S</sub>	+5V Supply
28	VDRV	Output Driver Voltage (See Application Section)

## TIMING DIAGRAM



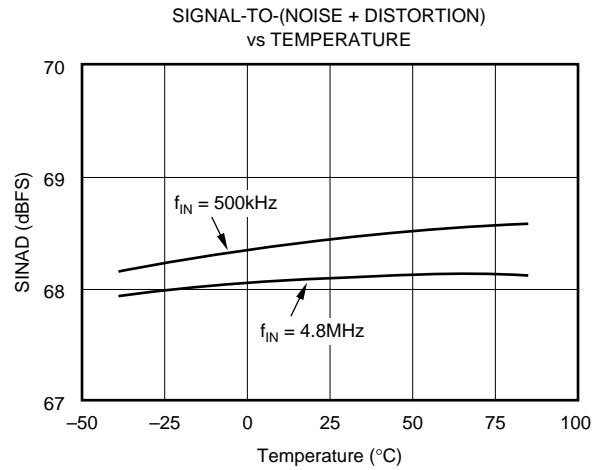
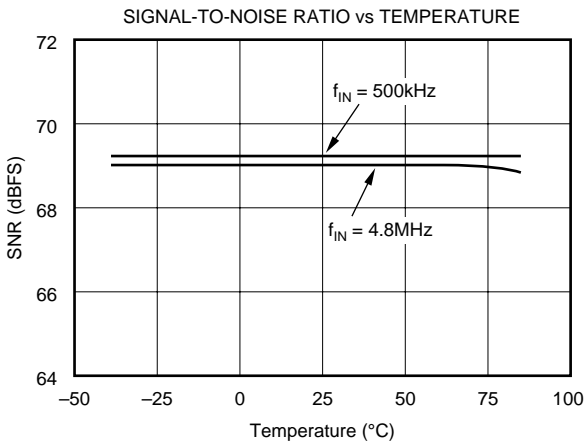
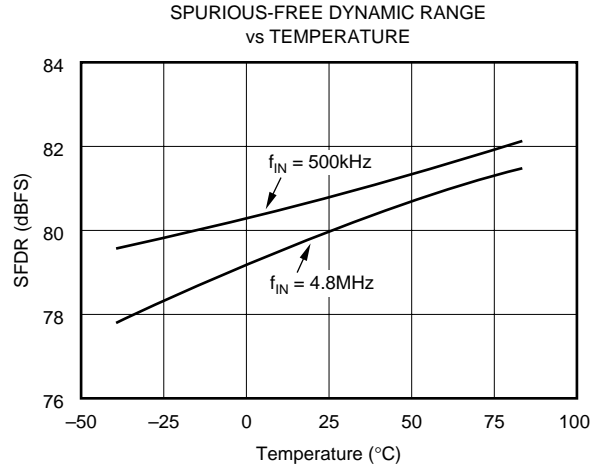
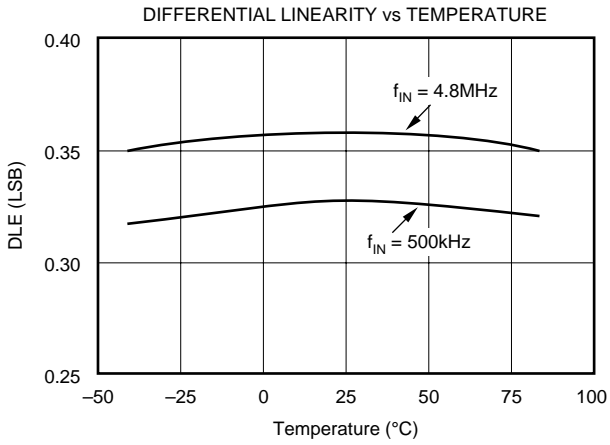
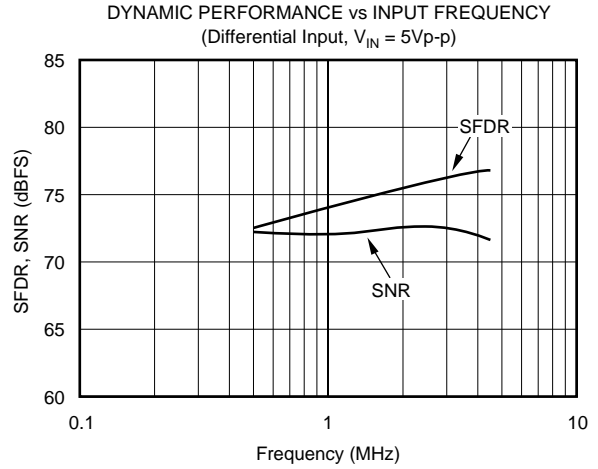
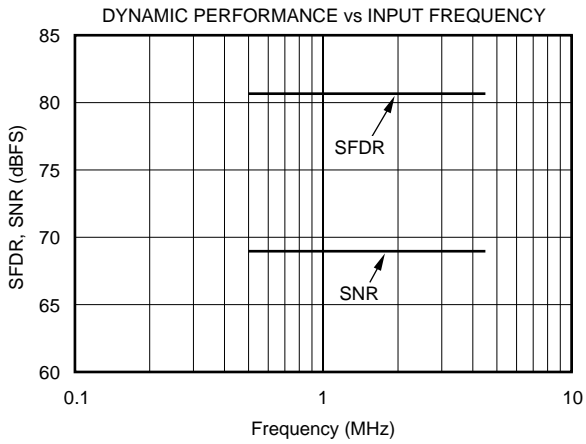
# TYPICAL CHARACTERISTICS

At  $T_A$  = full specified temperature range,  $V_S$  = +5V, specified single-ended input range = 1.5V to 3.5V, and sampling rate = 10MHz, unless otherwise specified.



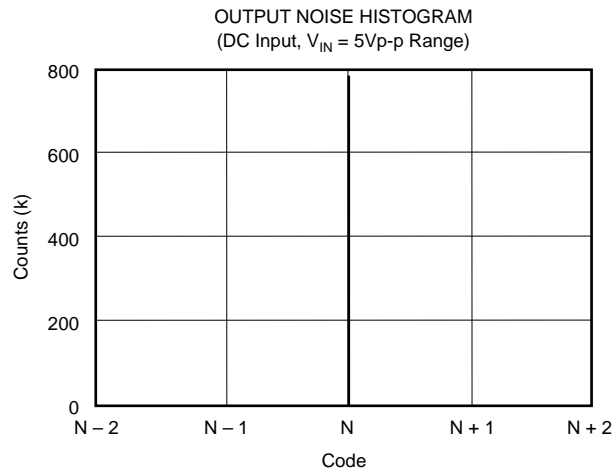
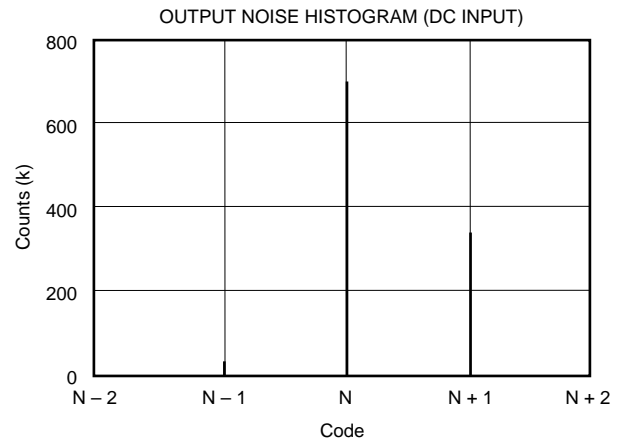
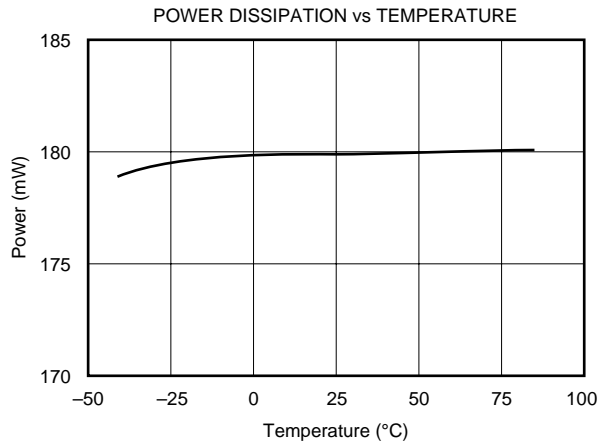
# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A$  = full specified temperature range,  $V_S$  = +5V, specified single-ended input range = 1.5V to 3.5V, and sampling rate = 10MHz, unless otherwise specified.



# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A$  = full specified temperature range,  $V_S = +5V$ , specified single-ended input range = 1.5V to 3.5V, and sampling rate = 10MHz, unless otherwise specified.





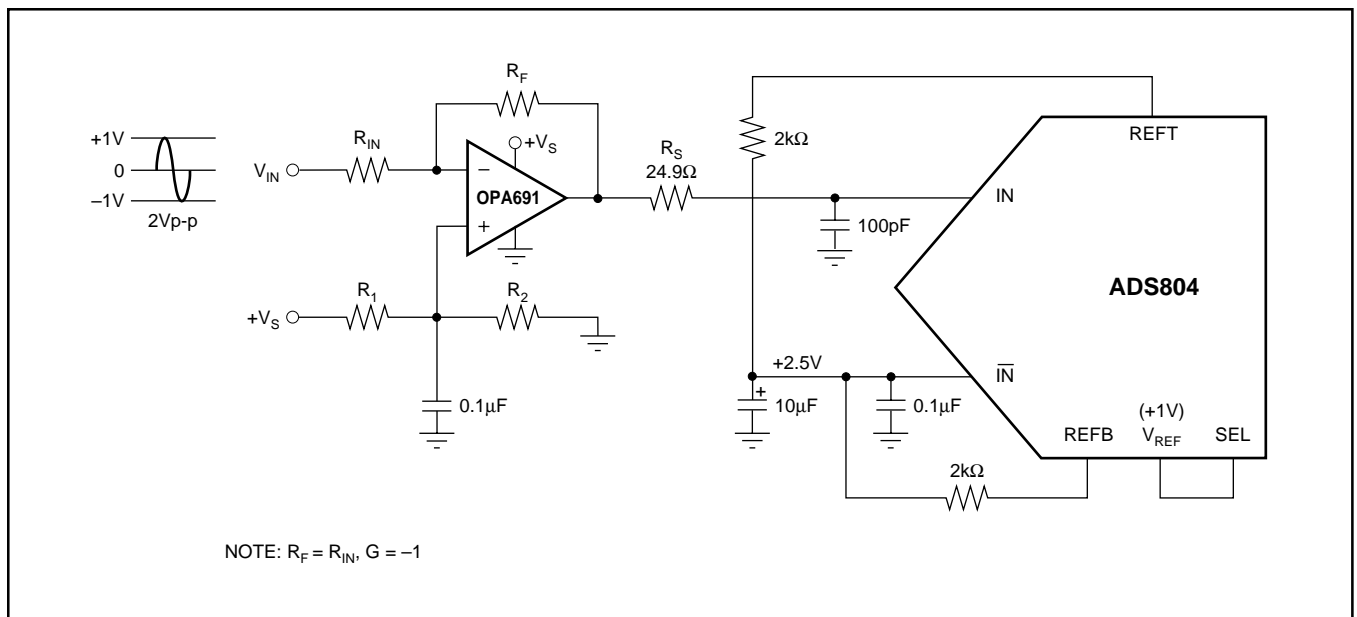


FIGURE 2. DC-Coupled, Single-Ended Input Configuration with DC-Level Shift.

DC voltage differences between the IN and  $\overline{\text{IN}}$  inputs of the ADS804 effectively will produce an offset, which can be corrected for by adjusting the values of resistors  $R_1$  and  $R_2$ . The bias current of the op amp may also result in an undesired offset. The selection criteria of the appropriate op amp should include the input bias current, output voltage swing, distortion, and noise specification. Note that in this example the overall signal phase is inverted. To re-establish the original signal polarity it is always possible to interchange the IN and  $\overline{\text{IN}}$  connections.

### SINGLE-ENDED-TO-DIFFERENTIAL CONFIGURATION (TRANSFORMER COUPLED)

In order to select the best suited interface circuit for the ADS804, the performance requirements must be known. If an ac-coupled input is needed for a particular application, the next step is to determine the method of applying the signal; either single-ended or differentially. The differential input configuration may provide a noticeable advantage of achieving good SFDR performance based on the fact that in the differential mode, the signal swing can be reduced to half of the swing required for single-ended drive. Secondly, by driving the ADS804 differentially, the even-order harmonics will be reduced. Figure 3 shows the schematic for the suggested transformer-coupled interface circuit. The resistor across the secondary side ( $R_T$ ) should be set to get an input impedance match (e.g.,  $R_T = n^2 \cdot R_G$ ).

### REFERENCE OPERATION

Integrated into the ADS804 is a bandgap reference circuit including logic that provides either a +1V or +2.5V reference output, by simply selecting the corresponding pin-strap configuration. Different reference voltages can be generated by the use of two external resistors, which will set a different

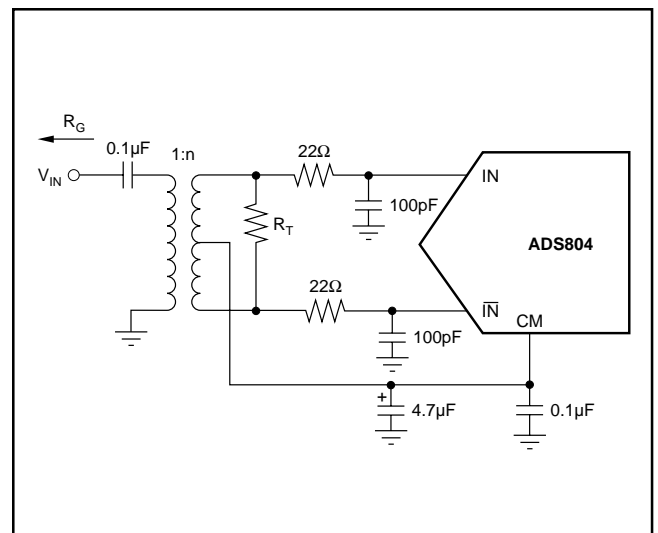


FIGURE 3. Transformer-Coupled Input.

gain for the internal reference buffer. For more design flexibility, the internal reference can be shut off and an external reference voltage used. Table I provides an overview of the possible reference options and pin configurations.

MODE	INPUT FULL-SCALE RANGE	REQUIRED $V_{REF}$	CONNECT	TO
Internal	2Vp-p	+1V	SEL	$V_{REF}$
Internal	5Vp-p	+2.5V	SEL	GND
Internal	$2V \leq \text{FSR} < 5V$ $\text{FSR} = 2 \cdot V_{REF}$	$1V < V_{REF} < 2.5V$ $V_{REF} = 1 + (R_1/R_2)$	$R_1$ $R_2$	$V_{REF}$ and SEL SEL and Gnd
External	$1V < \text{FSR} < 5V$	$0.5V < V_{REF} < 2.5V$	SEL $V_{REF}$	$+V_S$ Ext. $V_{REF}$

TABLE I. Selected Reference Configuration Examples.

A simple model of the internal reference circuit is shown in Figure 4. The internal blocks are a 1V-bandgap voltage reference, buffer, the resistive reference ladder, and the drivers for the top and bottom reference which supply the necessary current to the internal nodes. As shown, the output of the buffer appears at the  $V_{REF}$  pin. The full-scale input span of the ADS804 is determined by the voltage at  $V_{REF}$ , according to equation (1):

$$\text{Full-Scale Input Span} = 2 \cdot V_{REF} \quad (1)$$

Note that the current drive capability of this amplifier is limited to about 1mA and should not be used to drive low loads. The programmable reference circuit is controlled by the voltage applied to the select pin (SEL). Refer to Table I for an overview.

The top reference (REFT) and the bottom reference (REFB) are brought out mainly for external bypassing. For proper operation with all reference configurations, it is necessary to provide solid bypassing to the reference pins in order to keep the clock feedthrough to a minimum. Figure 5 shows the recommended decoupling network.

In addition, the common-mode voltage (CMV) may be used as a reference level to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this node, which is not buffered and has a high impedance. An alternate method of generating a common-mode voltage is given in Figure 6. Here, two external precision resistors (tolerance 1% or better) are located between the top and bottom reference pins. The common-mode level will appear at the midpoint. The output buffers of the top and bottom reference are designed to supply approximately 2mA of output current.

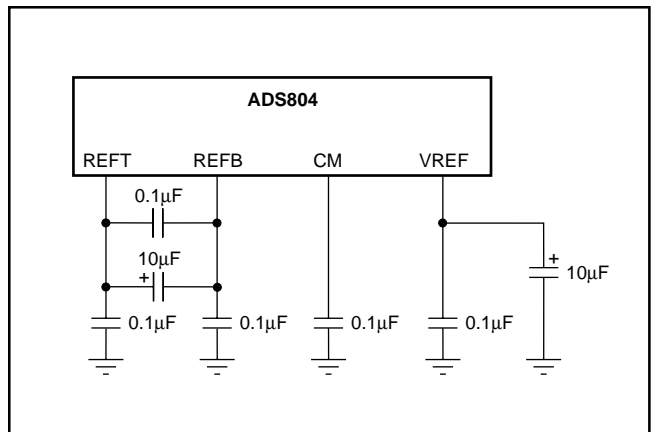


FIGURE 5. Recommended Reference Bypassing Scheme.

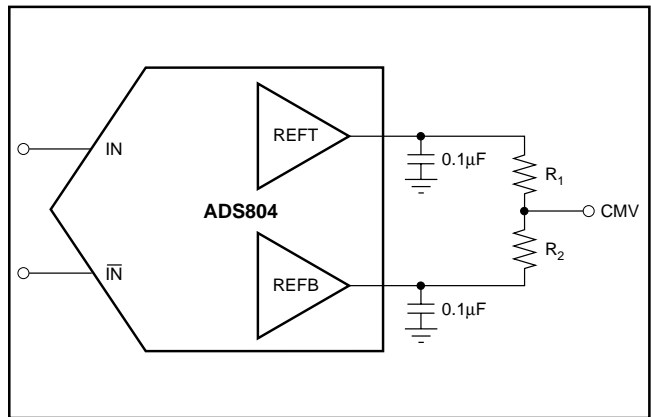


FIGURE 6. Alternative Circuit to Generate Common-Mode Voltage.

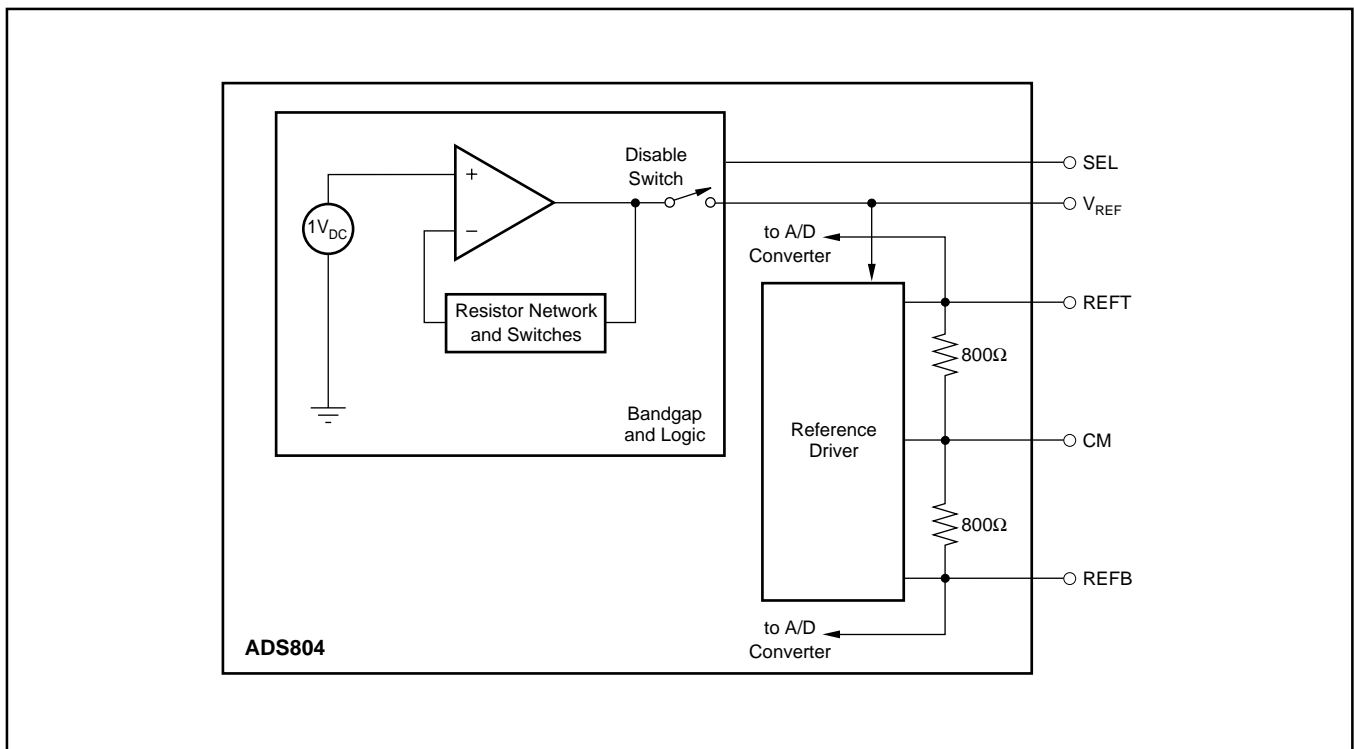


FIGURE 4. Equivalent Reference Circuit.

## SELECTING THE INPUT RANGE AND REFERENCE

Figures 7 through 9 show a selection of circuits for the most common input ranges when using the internal reference of the ADS804. All examples are for single-ended input and operate with a nominal common-mode voltage of +2.5V.

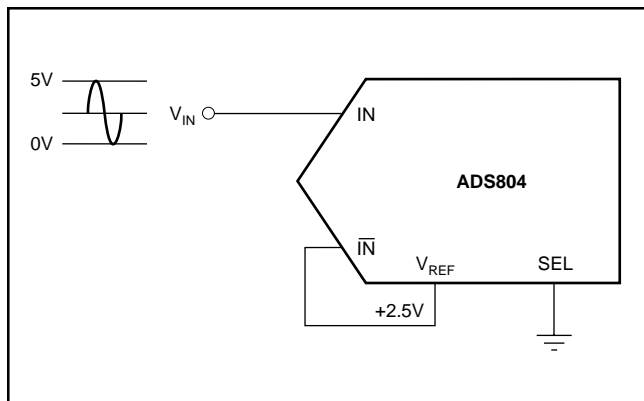


FIGURE 7. Internal Reference with 0V to 5V Input Range.

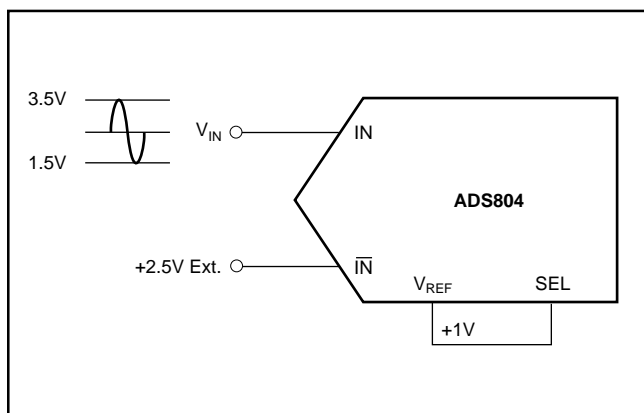


FIGURE 8. Internal Reference with 1.5V to 3.5V Input Range.

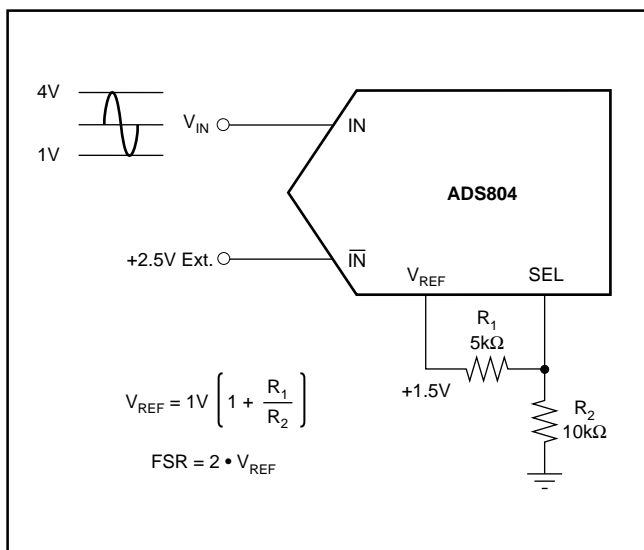


FIGURE 9. Internal Reference with 1V to 4V Input Range.

## EXTERNAL REFERENCE OPERATION

Depending on the application requirements, it might be advantageous to operate the ADS804 with an external reference. This may improve the DC accuracy if the external reference circuitry is superior in its drift and accuracy. To use the ADS804 with an external reference, the user must disable the internal reference (as shown in Figure 10). By connecting the SEL pin to +V<sub>S</sub>, the internal logic will shut down the internal reference. At the same time, the output of the internal reference buffer is disconnected from the V<sub>REF</sub> pin, which now must be driven with the external reference. Note that a similar bypassing scheme should be maintained as described for the internal reference operation.

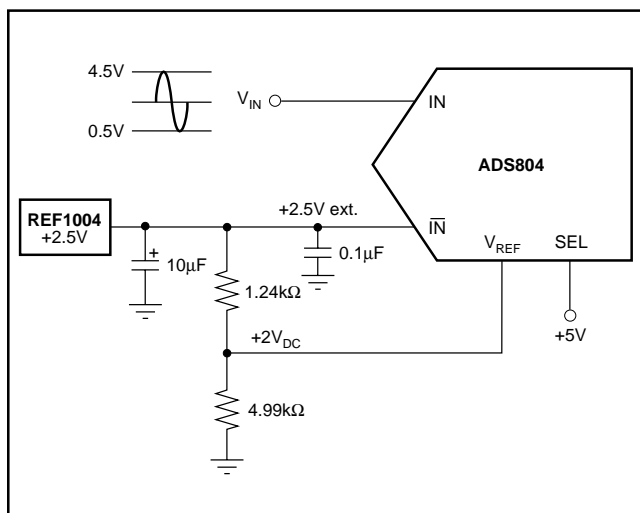


FIGURE 10. External Reference, Input Range 0.5V to 4.5V (4Vp-p), with +2.5V Common-Mode Voltage.

## DIGITAL INPUTS AND OUTPUTS

### Over-Range (OVR)

One feature of the ADS804 is its 'Over-Range' digital output (OVR). This pin can be used to monitor any out-of-range condition, which occurs every time the applied analog input voltage exceeds the input range (set by V<sub>REF</sub>). The OVR output is LO when the input voltage is within the defined input range. It becomes HI when the input voltage is beyond the input range. This is the case when the input voltage is either below the bottom reference voltage or above the top reference voltage. OVR will remain active until the analog input returns to its normal signal range and another conversion is completed. Using the MSB and its complement in conjunction with OVR a simple clue logic can be built that detects the over-range and under-range conditions, (see Figure 11). It should be noted that OVR is a digital output which is updated along with the bit information corresponding to the particular sampling incidence of the analog signal. Therefore, the OVR data is subject to the same pipeline delay (latency) as the digital data.

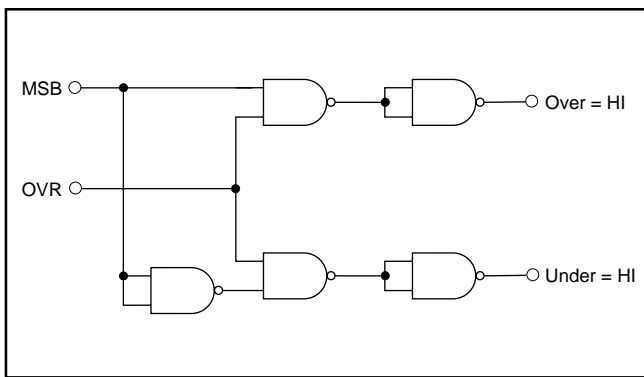


FIGURE 11. External Logic for Decoding Under- and Over-range Conditions.

## CLOCK INPUT REQUIREMENTS

Clock jitter is critical to the SNR performance of high speed, high resolution A/D converters. It leads to aperture jitter ( $t_A$ ) which adds noise to the signal being converted. The ADS804 samples the input signal on the rising edge of the CLK input. Therefore, this edge should have the lowest possible jitter. The jitter noise contribution to total SNR is given by the following equation. If this value is near your system requirements, input clock jitter must be reduced.

$$\text{JitterSNR} = 20 \log \frac{1}{2\pi f_{IN} t_A} \text{ rms signal to rms noise}$$

Where:  $f_{IN}$  is Input Signal Frequency

$t_A$  is rms Clock Jitter

Particularly in undersampling applications, special consideration should be given to clock jitter. The clock input should be treated as an analog input in order to achieve the highest level of performance. Any overshoot or undershoot of the clock signal may cause degradation of the performance. When digitizing at high sampling rates, the clock should have a 50% duty cycle ( $t_H = t_L$ ), along with fast rise and fall times of 2ns or less.

## DIGITAL OUTPUTS

The digital outputs of the ADS804 are designed to be compatible with both high-speed TTL and CMOS logic families. The driver stage for the digital outputs is supplied through a separate supply pin, VDRV, which is not connected to the analog supply pins. By adjusting the voltage on VDRV, the digital output levels will vary respectively. Therefore, it is possible to operate the ADS804 on a +5V analog supply while interfacing the digital outputs to 3V logic.

It is recommended to keep the capacitive loading on the data lines as low as possible ( $\leq 15\text{pF}$ ). Larger capacitive loads demand higher charging currents as the outputs are changing. Those high current surges can feed back to the analog portion of the ADS804 and influence the performance. If necessary, external buffers or latches may be used which

provide the added benefit of isolating the ADS804 from any digital noise activities on the bus coupling back high frequency noise. In addition, resistors in series with each data line may help maintain the ac performance of the ADS804. Their use depends on the capacitive loading seen by the converter. Values in the range of 100Ω to 200Ω will limit the instantaneous current the output stage has to provide for recharging the parasitic capacitances, as the output levels change from LO-to-HI or HI-to-LO.

## GROUNDING AND DECOUPLING

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Multi-layer PC boards are recommended for best performance since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. It is recommended that the analog and digital ground pins of the ADS804 be joined together at the IC and be connected only to the analog ground of the system.

The ADS804 has analog and digital supply pins, however, the converter should be treated as an analog component and all supply pins should be powered by the analog supply. This will ensure the most consistent results, since digital supply lines often carry high levels of noise that would otherwise be coupled into the converter and degrade the achievable performance.

Because of the pipeline architecture, the converter also generates high-frequency current transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently bypassed. Figure 12 shows the recommended decoupling scheme for the analog supplies. In most cases, 0.1μF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible. In addition, a larger size bipolar capacitor (1μF to 22μF) should be placed on the PC board in close proximity to the converter circuit.

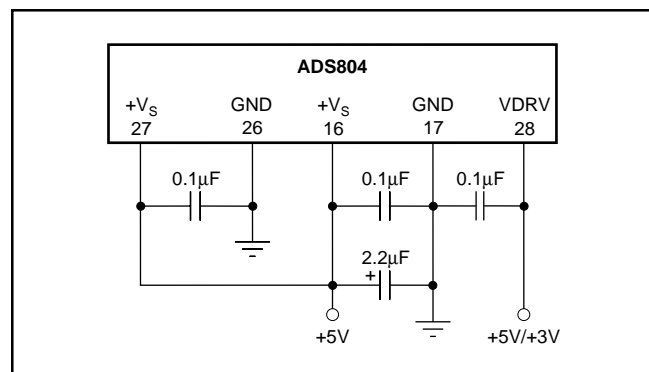


FIGURE 12. Recommended Bypassing for Analog Supply Pins.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS804E	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS804E	<a href="#">Samples</a>
ADS804E/1K	ACTIVE	SSOP	DB	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS804E	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS804E/1K	SSOP	DB	28	1000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS804E/1K	SSOP	DB	28	1000	350.0	350.0	43.0

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