



**THE DATASHEET OF
MC10LVEP16DTR2G**



MC10LVEP16, MC100LVEP16

2.5 V / 3.3 V ECL Differential Receiver/Driver

Description

The MC10/100LVEP16 is a world class differential receiver/driver. The device is functionally equivalent to the EL16, EP16 and LVEL16 devices. With output transition times significantly faster than the EL16 and LVEL16, the LVEP16 is ideally suited for interfacing with high frequency and low voltage (2.5 V) sources. Single-Ended CLK input operation is limited to a $V_{CC} \geq 3.0$ V in PECL mode, or $V_{EE} \leq -3.0$ V in NECL mode.

The V_{BB} pin, an internally generated Voltage supply, is available to this device only. For Single-Ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

Features

- 240 ps Propagation Delay
- Maximum Frequency = > 4 GHz Typical
- PECL Mode Operating Range:
 $V_{CC} = 2.375$ V to 3.8 V with $V_{EE} = 0$ V
- NECL Mode Operating Range:
 $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.8 V
- V_{BB} Output
- Open Input Default State
- LVDS Input Compatible
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



ON Semiconductor®

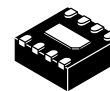
www.onsemi.com



SOIC-8 NB
D SUFFIX
CASE 751-07

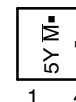
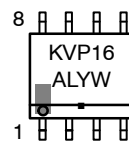
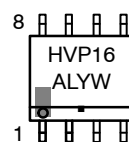


TSSOP-8
DT SUFFIX
CASE 948R-02



DFN8
MN SUFFIX
CASE 506AA

MARKING DIAGRAMS*



SOIC-8 NB

TSSOP-8

DFN8

H = MC10 A = Assembly Location
K = MC100 L = Wafer Lot
5Y = MC10 Y = Year
4L = MC100 W = Work Week
M = Date Code ■ = Pb-Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

MC10LVEP16, MC100LVEP16

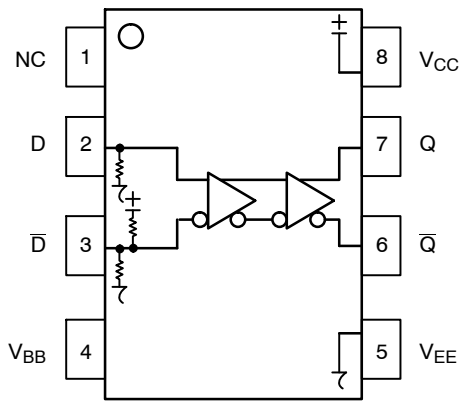


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

| Pin | Function |
|--------------------|--|
| D*, \bar{D}^{**} | ECL Data Inputs |
| Q, \bar{Q} | ECL Data Outputs |
| V _{BB} | Ref. Voltage Output |
| V _{CC} | Positive Supply |
| V _{EE} | Negative Supply |
| NC | No Connect |
| EP | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

* Pins will default LOW when left open.

**Pins will default to $V_{CC}/2$ when left open.

Table 2. ATTRIBUTES

| Characteristics | Value |
|---|-------------------------------|
| Internal Input Pulldown Resistor | 75 k Ω |
| Internal Input Pullup Resistor | 37.5 k Ω |
| ESD Protection Human Body Model Machine Model Charged Device Model | > 4 kV > 200 V > 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb-Free Pkg |
| SOIC-8 NB NB TSSOP-8 DFN8 | Level 1 Level 3 Level 1 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 167 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note [AND8003/D](#).

MC10LVEP16, MC100LVEP16

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|--|--|-------------|------|
| V _{CC} | PECL Mode Power Supply | V _{EE} = 0 V | | 6 | V |
| V _{EE} | NECL Mode Power Supply | V _{CC} = 0 V | | -6 | V |
| V _I | PECL Mode Input Voltage NECL Mode Input Voltage | V _{EE} = 0 V V _{CC} = 0 V | V _I ≤ V _{CC} V _I ≥ V _{EE} | 6 -6 | V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA |
| I _{BB} | V _{BB} Sink/Source | | | ±0.5 | mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | SOIC-8 NB SOIC-8 NB | 190 130 | °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC-8 NB | 41 to 44 | °C/W |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | TSSOP-8 TSSOP-8 | 185 140 | °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | TSSOP-8 | 41 to 44 | °C/W |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | DFN8 DFN8 | 129 84 | °C/W |
| T _{sol} | Wave Solder (Pb-Free) | < 2 to 3 sec @ 260°C | | 265 | °C |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | (Note 1) | DFN8 | 35 to 40 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

MC10LVEP16, MC100LVEP16

Table 4. 10EP DC CHARACTERISTICS, PECL ($V_{CC} = 2.5\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------------|------|------|-------------|------|------|-------------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 17 | 22 | 27 | 17 | 22 | 27 | 17 | 22 | 28 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | 1365 | 1490 | 1615 | 1430 | 1555 | 1680 | 1490 | 1615 | 1740 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | 565 | 740 | 865 | 630 | 805 | 930 | 690 | 865 | 990 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Notes 3, 4) | 1.2 | | 2.5 | 1.2 | | 2.5 | 1.2 | | 2.5 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current D \bar{D} | 0.5 -150 | | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.125 V to -1.3 V.
2. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.
3. Do not use V_{BB} at $V_{CC} < 3.0\text{ V}$. Single ended input CLK pin operation is limited to $V_{CC} \geq 3.0\text{ V}$ in PECL mode.
4. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 5. 10EP DC CHARACTERISTICS, PECL ($V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------------|------|------|-------------|------|------|-------------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 17 | 22 | 27 | 17 | 22 | 27 | 17 | 22 | 28 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | 2165 | 2290 | 2415 | 2230 | 2355 | 2480 | 2290 | 2415 | 2540 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | 1365 | 1540 | 1665 | 1430 | 1605 | 1730 | 1490 | 1665 | 1790 | mV |
| V_{IH} | Input HIGH Voltage (Single Ended) | 2090 | | 2415 | 2155 | | 2480 | 2215 | | 2540 | mV |
| V_{IL} | Input LOW Voltage (Single Ended) | 1365 | | 1690 | 1430 | | 1755 | 1490 | | 1815 | mV |
| V_{BB} | Output Voltage Reference (Note 3) | 1790 | 1890 | 1990 | 1855 | 1955 | 2055 | 1915 | 2015 | 2115 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current D \bar{D} | 0.5 -150 | | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925 V to -0.5 V.
2. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.
3. Single ended input CLK pin operation is limited to $V_{CC} \geq 3.0\text{ V}$ in PECL mode.
4. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC10LVEP16, MC100LVEP16

Table 6. 10EP DC CHARACTERISTICS, NECL ($V_{CC} = 0\text{ V}$, $V_{EE} = -3.8\text{ V}$ to -2.375 V (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|--------------|-------|-------|--------------|-------|-------|--------------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 17 | 22 | 27 | 17 | 22 | 27 | 17 | 22 | 28 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | -1135 | -1010 | -885 | -1070 | -945 | -820 | -1010 | -885 | -760 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | -1935 | -1760 | -1635 | -1870 | -1695 | -1570 | -1810 | -1635 | -1510 | mV |
| V_{IH} | Input HIGH Voltage (Single Ended) | -1210 | | -885 | -1145 | | -820 | -1085 | | -760 | mV |
| V_{IL} | Input LOW Voltage (Single Ended) | -1935 | | -1610 | -1870 | | -1545 | -1810 | | -1485 | mV |
| V_{BB} | Output Voltage Reference (Note 3) | -1510 | -1410 | -1310 | -1445 | -1345 | -1245 | -1385 | -1285 | -1185 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | $V_{EE}+1.2$ | | 0.0 | $V_{EE}+1.2$ | | 0.0 | $V_{EE}+1.2$ | | 0.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current D \bar{D} | 0.5 -150 | | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} .
2. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.
3. Single ended input CLK pin operation is limited to $V_{EE} \leq -3.0\text{ V}$ in NECL mode.
4. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. 100EP DC CHARACTERISTICS, PECL ($V_{CC} = 2.5\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------------|------|------|-------------|------|------|-------------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 19 | 24 | 29 | 22 | 28 | 34 | 24 | 30 | 36 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | 555 | 730 | 900 | 555 | 730 | 900 | 555 | 730 | 900 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Notes 3, 4) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current D \bar{D} | 0.5 -150 | | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $+0.125\text{ V}$ to -1.3 V .
2. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.
3. Do not use V_{BB} at $V_{CC} < 3.0\text{ V}$. Single ended input CLK pin operation is limited to $V_{CC} \geq 3.0\text{ V}$ in PECL mode.
4. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC10LVEP16, MC100LVEP16

Table 8. 100EP DC CHARACTERISTICS, PECL ($V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------------|------|------|-------------|------|------|-------------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 19 | 24 | 29 | 22 | 28 | 34 | 24 | 30 | 36 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | 1355 | 1530 | 1700 | 1355 | 1530 | 1700 | 1355 | 1530 | 1700 | mV |
| V_{IH} | Input HIGH Voltage (Single Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| V_{IL} | Input LOW Voltage (Single Ended) | 1355 | | 1700 | 1355 | | 1700 | 1355 | | 1700 | mV |
| V_{BB} | Output Voltage Reference (Note 3) | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current D \bar{D} | 0.5 -150 | | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925 V to -0.5 V.
2. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.
3. Single ended input CLK pin operation is limited to $V_{CC} \geq 3.0\text{ V}$ in PECL mode.
4. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 9. 100EP DC CHARACTERISTICS, NECL ($V_{CC} = 0\text{ V}$, $V_{EE} = -3.8\text{ V}$ to -2.375 V (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|--------------|-------|-------|--------------|-------|-------|--------------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 19 | 24 | 29 | 22 | 28 | 34 | 24 | 30 | 36 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | -1145 | -1020 | -895 | -1145 | -1020 | -895 | -1145 | -1020 | -895 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | -1945 | -1770 | -1600 | -1945 | -1770 | -1600 | -1945 | -1770 | -1600 | mV |
| V_{IH} | Input HIGH Voltage (Single Ended) | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single Ended) | -1945 | | -1600 | -1945 | | -1600 | -1945 | | -1600 | mV |
| V_{BB} | Output Voltage Reference (Note 3) | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | $V_{EE}+1.2$ | | 0.0 | $V_{EE}+1.2$ | | 0.0 | $V_{EE}+1.2$ | | 0.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current D \bar{D} | 0.5 -150 | | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} .
2. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.
3. Single ended input CLK pin operation is limited to $V_{EE} \leq -3.0\text{ V}$ in NECL mode.
4. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC10LVEP16, MC100LVEP16

Table 10. AC CHARACTERISTICS ($V_{CC} = 0\text{ V}$; $V_{EE} = -3.8\text{ V}$ to -2.375 V or $V_{CC} = 2.375\text{ V}$ to 3.8 V ; $V_{EE} = 0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------|---|-------|--|--|------|--|--|------|--|--|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Frequency (See Figure 2. $F_{max}/JITTER$) | | > 4 | | | > 4 | | | > 4 | | GHz |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential | 150 | 220 | 300 | 170 | 240 | 320 | 190 | 260 | 330 | ps |
| t_{SKEW} | Duty Cycle Skew (Note 2) | | 5.0 | 20 | | 5.0 | 20 | | 5.0 | 20 | ps |
| t_{JITTER} | CLOCK Random Jitter (RMS) @ $\leq 1.0\text{ GHz}$ @ $\leq 1.5\text{ GHz}$ @ $\leq 2.0\text{ GHz}$ @ $\leq 2.5\text{ GHz}$ @ $\leq 3.0\text{ GHz}$ @ $\leq 3.5\text{ GHz}$ | | 0.134 0.077 0.115 0.117 0.122 0.123 | 0.2 0.2 0.2 0.2 0.2 0.2 | | 0.147 0.104 0.141 0.132 0.143 0.145 | 0.3 0.3 0.3 0.3 0.3 0.3 | | 0.166 0.145 0.153 0.156 0.177 0.202 | 0.3 0.3 0.3 0.3 0.3 0.3 | ps |
| V_{PP} | Input Voltage Swing (Differential Configuration) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| t_r t_f | Output Rise/Fall Times (20% – 80%) Q, \bar{Q} | 70 | 120 | 170 | 80 | 130 | 180 | 100 | 150 | 200 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10LVEP16, MC100LVEP16

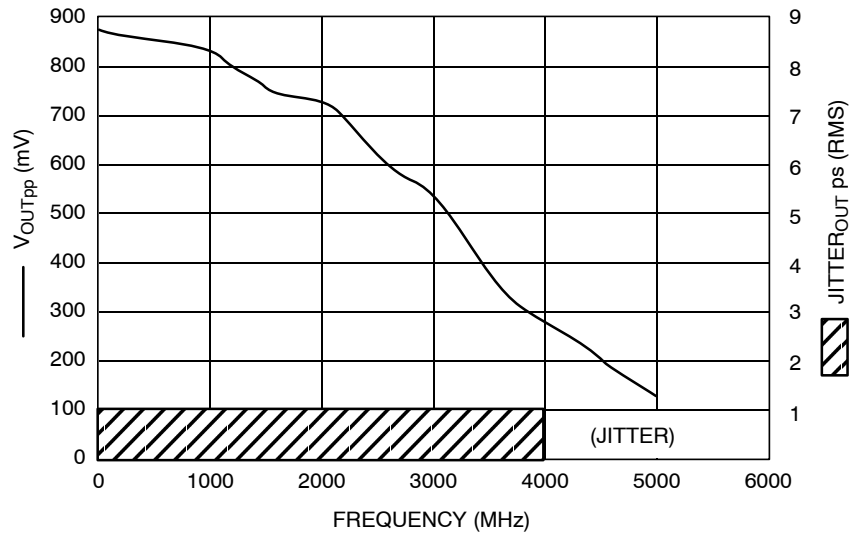


Figure 2. F_{max}/Jitter

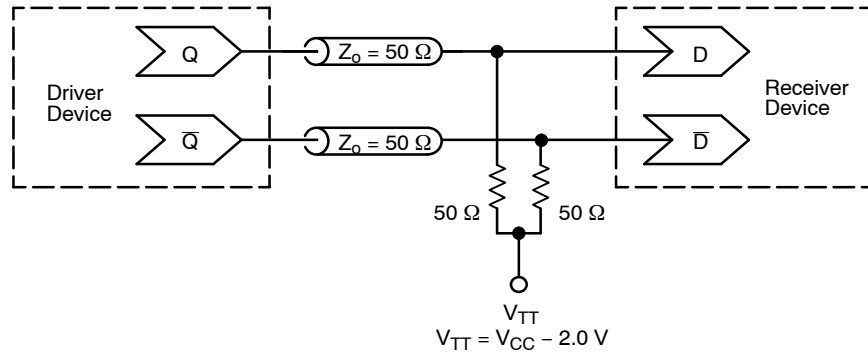


Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

MC10LVEP16, MC100LVEP16

ORDERING INFORMATION

| Device | Package | Shipping† |
|------------------|------------------------|--------------------|
| MC10LVEP16DG | SOIC-8 NB (Pb-Free) | 98 Units / Tube |
| MC10LVEP16DR2G | SOIC-8 NB (Pb-Free) | 2500 / Tape & Reel |
| MC10LVEP16DTG | TSSOP-8 (Pb-Free) | 100 Units / Tube |
| MC10LVEP16DTR2G | TSSOP-8 (Pb-Free) | 2500 / Tape & Reel |
| MC100LVEP16DG | SOIC-8 NB (Pb-Free) | 98 Units / Tube |
| MC100LVEP16DR2G | SOIC-8 NB (Pb-Free) | 2500 / Tape & Reel |
| MC100LVEP16DTG | TSSOP-8 (Pb-Free) | 100 Units / Tube |
| MC100LVEP16DTR2G | TSSOP-8 (Pb-Free) | 2500 / Tape & Reel |
| MC100LVEP16MNR4G | DFN8 (Pb-Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

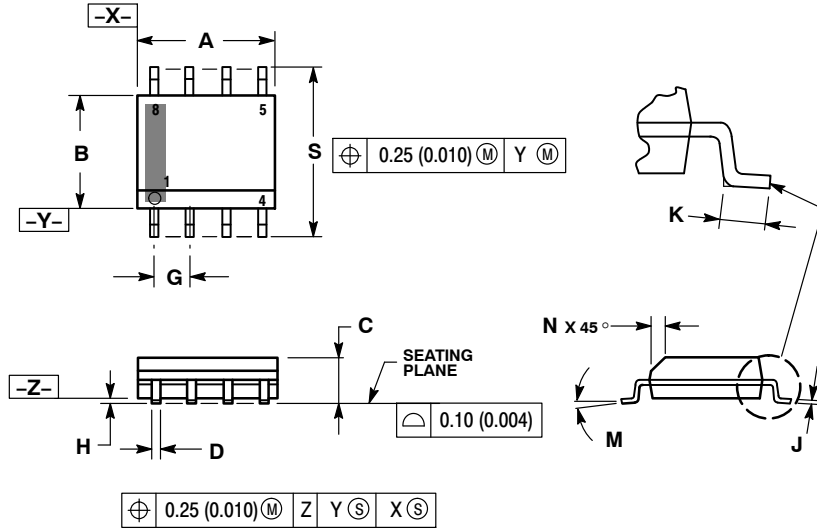
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MC10LVEP16, MC100LVEP16

PACKAGE DIMENSIONS

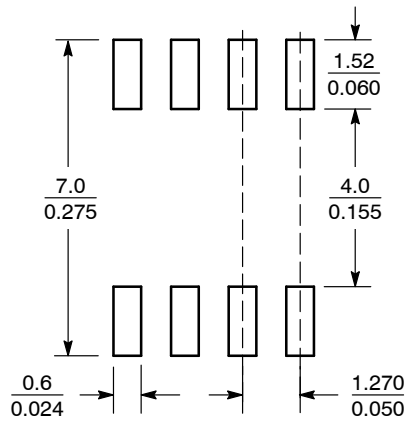
SOIC-8 NB
D SUFFIX
CASE 751-07
ISSUE AK



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



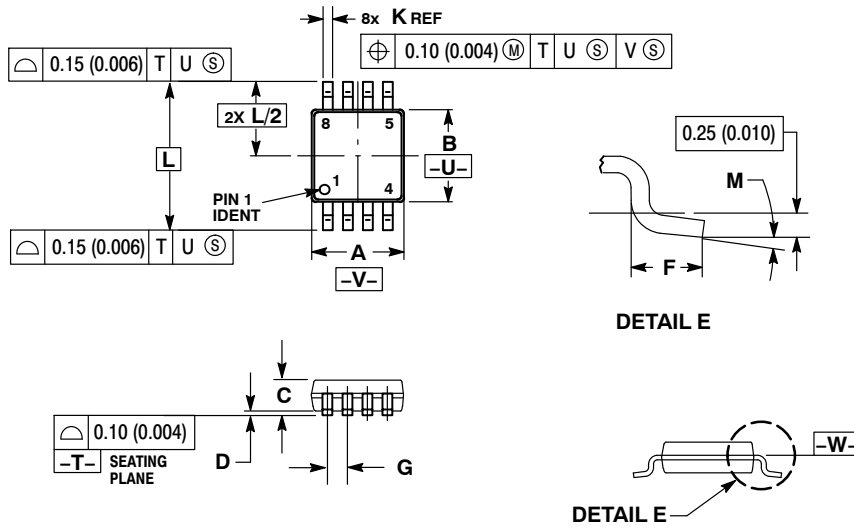
SCALE 6:1 ($\frac{\text{mm}}{\text{inches}}$)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC10LVEP16, MC100LVEP16

PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
CASE 948R-02
ISSUE A



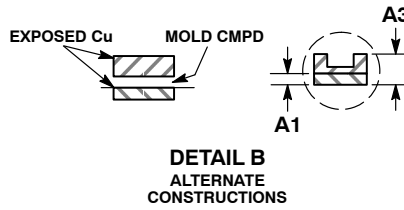
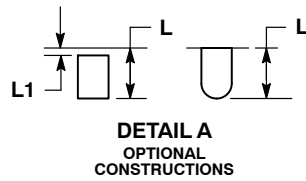
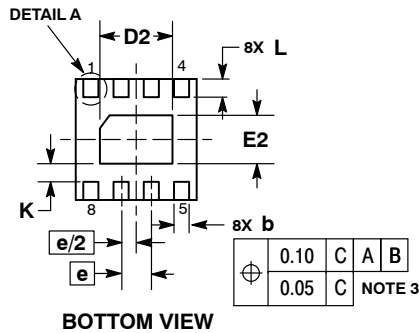
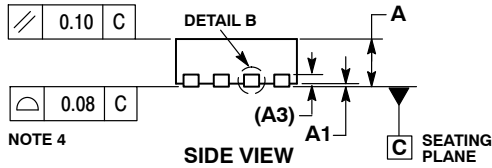
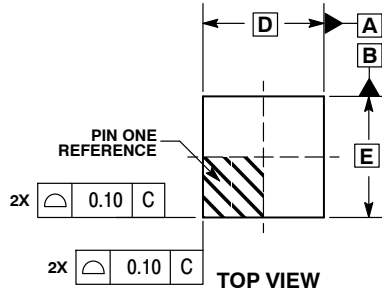
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | 0.80 | 1.10 | 0.031 | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.40 | 0.70 | 0.016 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| K | 0.25 | 0.40 | 0.010 | 0.016 |
| L | 4.90 BSC | | 0.193 BSC | |
| M | 0° | 6° | 0° | 6° |

MC10LVEP16, MC100LVEP16

PACKAGE DIMENSIONS

DFN8 2x2, 0.5 P
MN SUFFIX
CASE 506AA
ISSUE F

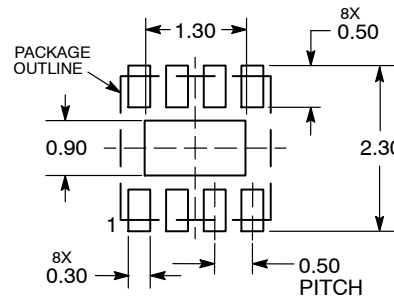


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.20 | 0.30 |
| D | 2.00 | BSC |
| D2 | 1.10 | 1.30 |
| E | 2.00 | BSC |
| E2 | 0.70 | 0.90 |
| e | 0.50 | BSC |
| K | 0.30 | REF |
| L | 0.25 | 0.35 |
| L1 | --- | 0.10 |

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View MC10LVEP16DTR2G on WIN SOURCE](#)

 [ON Semiconductor](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management