THE DATASHEET OF

ADS7843E

ADS7843

SBAS090B – SEPTEMBER 2000 – REVISED MAY 2002

TOUCH SCREEN CONTROLLER

FEATURES

- 4-WIRE TOUCH SCREEN INTERFACE
- RATIOMETRIC CONVERSION
- SINGLE SUPPLY: 2.7V to 5V
- UP TO 125kHz CONVERSION RATE
- SERIAL INTERFACE
- PROGRAMMABLE 8- OR 12-BIT RESOLUTION
- 2 AUXILIARY ANALOG INPUTS
- FULL POWER-DOWN CONTROL

APPLICATIONS

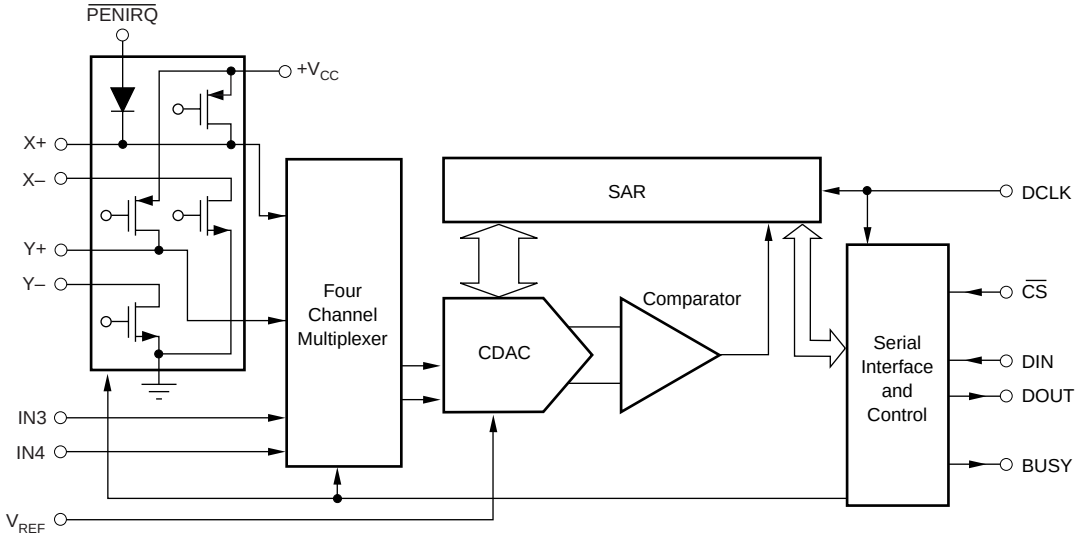
- PERSONAL DIGITAL ASSISTANTS
- PORTABLE INSTRUMENTS
- POINT-OF-SALES TERMINALS
- PAGERS
- TOUCH SCREEN MONITORS

DESCRIPTION

The ADS7843 is a 12-bit sampling Analog-to-Digital Converter (ADC) with a synchronous serial interface and low on-resistance switches for driving touch screens. Typical power dissipation is 750µW at a 125kHz throughput rate and a +2.7V supply. The reference voltage (V_{REF}) can be varied between 1V and $+V_{CC}$, providing a corresponding input voltage range of 0V to V_{REF}. The device includes a shutdown mode which reduces typical power dissipation to under 0.5µW. The ADS7843 is specified down to 2.7V operation.

Low power, high speed, and onboard switches make the ADS7843 ideal for battery-operated systems such as personal digital assistants with resistive touch screens and other portable equipment. The ADS7843 is available in an SSOP-16 package and is specified over the –40°C to +85°C temperature range.

US Patent No. 6246394



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ABSOLUTE MAXIMUM RATINGS[1]

$+V_{CC}$ to GND	–0.3V to +6V
Analog Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Digital Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

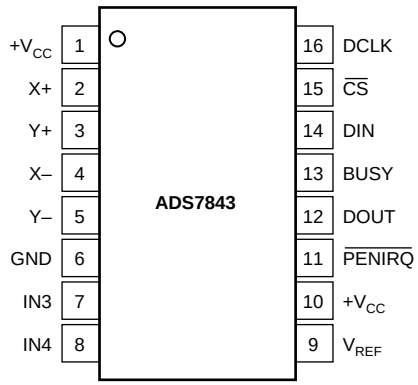
PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7843E	±2	SSOP-16	DBQ	–40°C to +85°C	ADS7843E	ADS7843E	Rails, 100
"	"	"	"	"	ADS7843E	ADS7843E/2K5	Tape and Reel, 2500

NOTES: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATION

Top View **SSOP**



PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	$+V_{CC}$	Power Supply, 2.7V to 5V.
2	X+	X+ Position Input. ADC input Channel 1.
3	Y+	Y+ Position Input. ADC input Channel 2.
4	X–	X– Position Input
5	Y–	Y– Position Input
6	GND	Ground
7	IN3	Auxiliary Input 1. ADC input Channel 3.
8	IN4	Auxiliary Input 2. ADC input Channel 4.
9	V_{REF}	Voltage Reference Input
10	$+V_{CC}$	Power Supply, 2.7V to 5V.
11	$\overline{PENIRQ}$	Pen Interrupt. Open anode output (requires 10kΩ to 100kΩ pull-up resistor externally).
12	DOUT	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{CS}$ is HIGH.
13	BUSY	Busy Output. This output is high impedance when $\overline{CS}$ is HIGH.
14	DIN	Serial Data Input. If $\overline{CS}$ is LOW, data is latched on rising edge of DCLK.
15	$\overline{CS}$	Chip Select Input. Controls conversion timing and enables the serial input/output register.
16	DCLK	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, f_{CLK} = 16 • f_{SAMPLE} = 2MHz, 12-bit mode, and digital inputs = GND or $+V_{CC}$, unless otherwise noted.

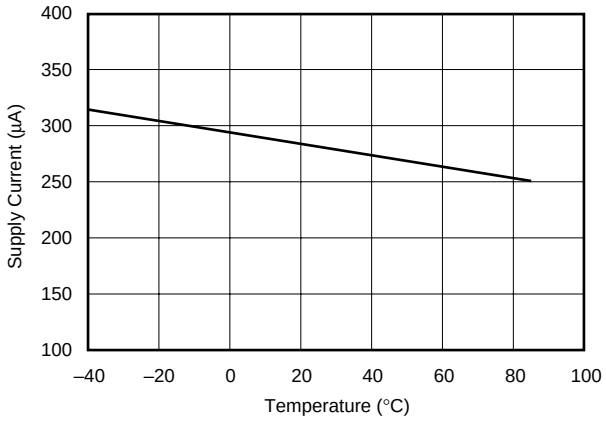
PARAMETER	CONDITIONS	ADS7843E MIN	ADS7843E TYP	ADS7843E MAX	UNITS
ANALOG INPUT					
Full-Scale Input Span	Positive Input – Negative Input	0		V_{REF}	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ +0.2	V
	Negative Input	–0.2		+0.2	V
Capacitance			25		pF
Leakage Current			0.1		µA
SYSTEM PERFORMANCE					
Resolution			12		Bits
No Missing Codes		11			Bits
Integral Linearity Error				±2	LSB[1]
Offset Error				±6	LSB
Offset Error Match			0.1	1.0	LSB
Gain Error				±4	LSB
Gain Error Match			0.1	1.0	LSB
Noise			30		µVrms
Power-Supply Rejection			70		dB
SAMPLING DYNAMICS					
Conversion Time				12	Clk Cycles
Acquisition Time		3			Clk Cycles
Throughput Rate				125	kHz
Multiplexer Settling Time			500		ns
Aperture Delay			30		ns
Aperture Jitter			100		ps
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100		dB
SWITCH DRIVERS					
On-Resistance					
Y+, X+			5		Ω
Y–, X–			6		Ω
REFERENCE INPUT					
Range		1.0		$+V_{CC}$	V
Resistance	$\overline{CS}$ = GND or $+V_{CC}$		5		GΩ
Input Current			13	40	µA
	f_{SAMPLE} = 12.5kHz		2.5		µA
	$\overline{CS}$ = $+V_{CC}$		0.001	3	µA
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Levels, Except $\overline{PENIRQ}$					
V_{IH}	| I_{IH} | ≤ +5µA	$+V_{CC}$ • 0.7		$+V_{CC}$ +0.3	
V_{IL}	| I_{IL} | ≤ +5µA	–0.3		+0.8	V
V_{OH}	I_{OH} = –250µA	$+V_{CC}$ • 0.8			V
V_{OL}	I_{OL} = 250µA			0.4	V
$\overline{PENIRQ}$					
V_{OL}	T_A = 0°C to +85°C, 100kΩ Pull-Up			0.8	V
Data Format			Straight Binary		
POWER-SUPPLY REQUIREMENTS					
$+V_{CC}$	Specified Performance	2.7		3.6	V
Quiescent Current			280	650	µA
	f_{SAMPLE} = 12.5kHz		220		µA
	Shutdown Mode with DCLK = DIN = $+V_{CC}$			3	µA
Power Dissipation	$+V_{CC}$ = +2.7V			1.8	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C

NOTE: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, 1LSB is 610µV.

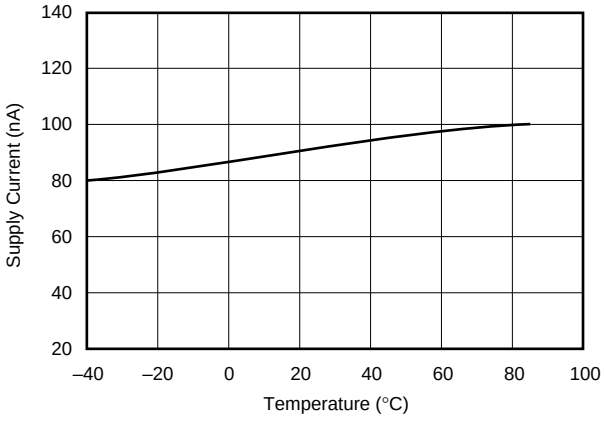
TYPICAL CHARACTERISTICS

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

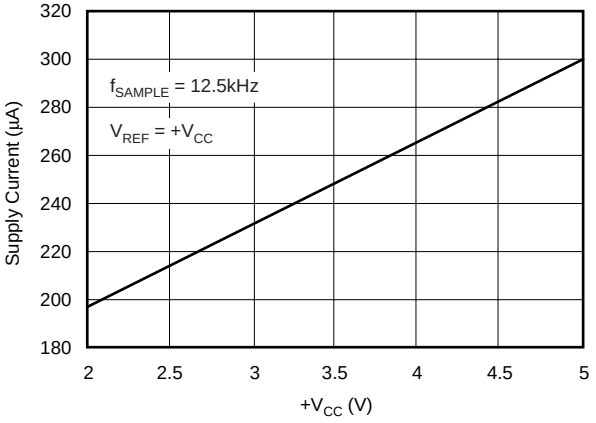
SUPPLY CURRENT vs TEMPERATURE



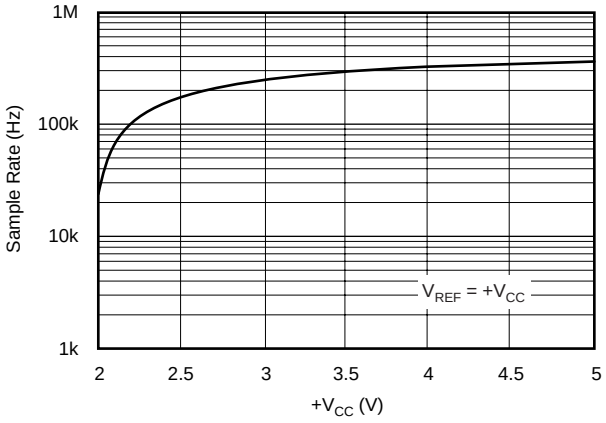
POWER-DOWN SUPPLY CURRENT vs TEMPERATURE



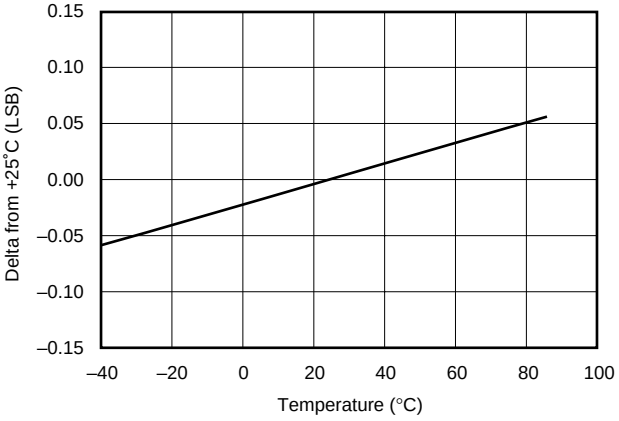
SUPPLY CURRENT vs $+V_{CC}$



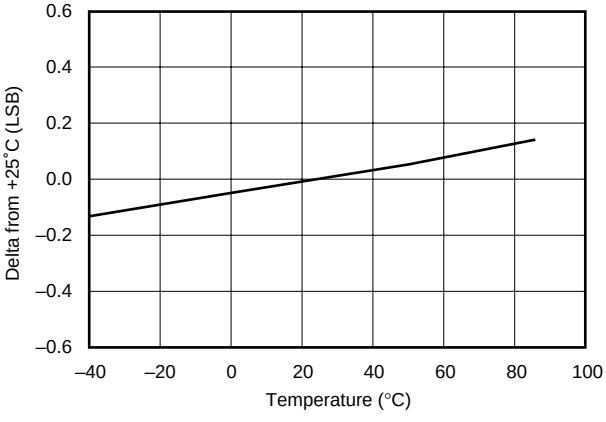
MAXIMUM SAMPLE RATE vs $+V_{CC}$



CHANGE IN GAIN vs TEMPERATURE



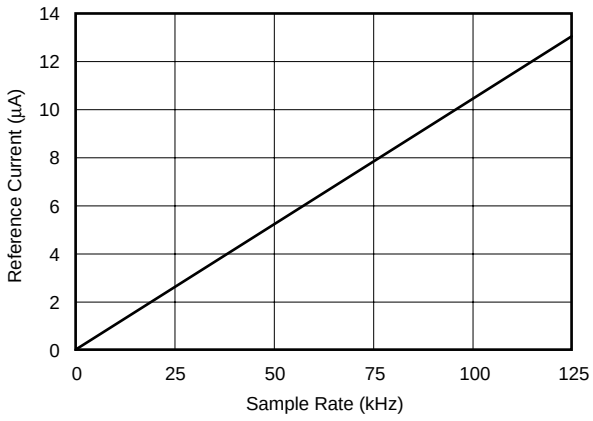
CHANGE IN OFFSET vs TEMPERATURE



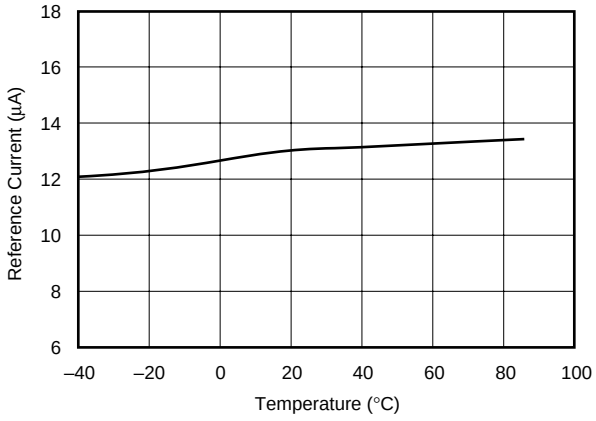
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

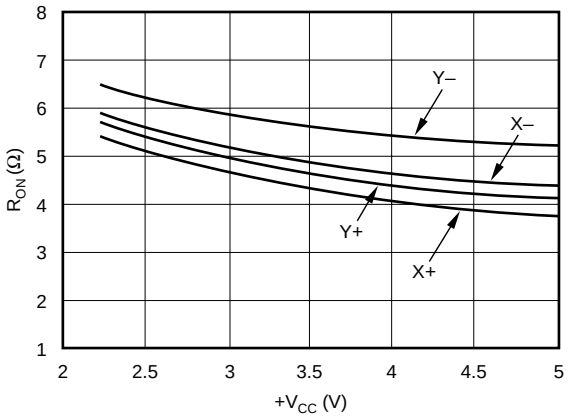
REFERENCE CURRENT vs SAMPLE RATE



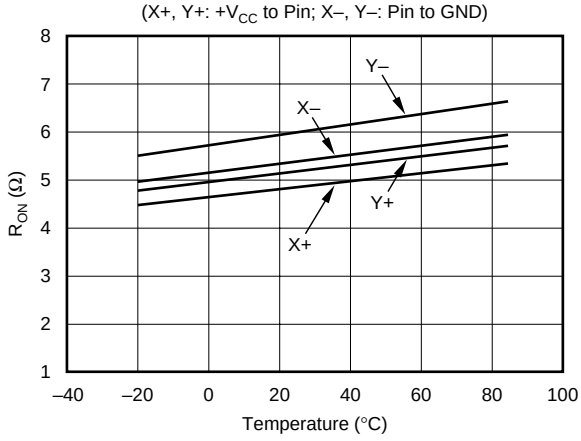
REFERENCE CURRENT vs TEMPERATURE



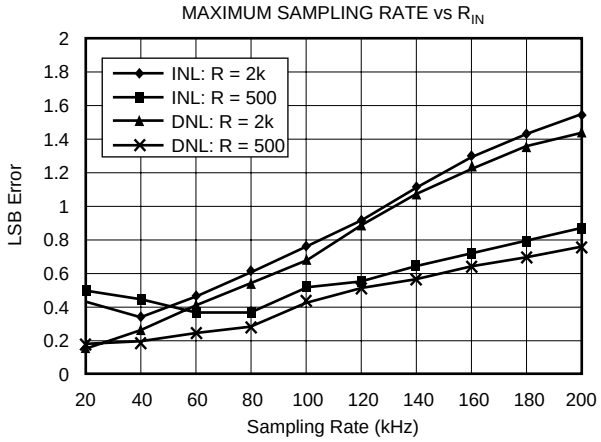
SWITCH-ON RESISTANCE vs $+V_{CC}$
(X+, Y+: $+V_{CC}$ to Pin; X–, Y–: Pin to GND)



SWITCH-ON RESISTANCE vs TEMPERATURE
(X+, Y+: $+V_{CC}$ to Pin; X–, Y–: Pin to GND)



MAXIMUM SAMPLING RATE vs R_{IN}



THEORY OF OPERATION

The ADS7843 is a classic Successive Approximation Register (SAR) ADC. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µs CMOS process.

The basic operation of the ADS7843 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 1V and $+V_{CC}$. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS7843.

The analog input to the converter is provided via a four-channel multiplexer. A unique configuration of low on-resistance switches allows an unselected ADC input channel to provide power and an accompanying pin to provide ground for an external device. By maintaining a differential input to the converter and a differential reference architecture, it is possible to negate the switch's on-resistance error (should this be a source of error for the particular measurement).

ANALOG INPUT

See Figure 2 for a block diagram of the input multiplexer on the ADS7843, the differential input of the ADC, and the converter's differential reference. Table I and Table II show the relationship between the A2, A1, A0, and SER/$\overline{\text{DFR}}$ control bits and the configuration of the ADS7843. The control bits are provided serially via the DIN pin—see the Digital Interface section of this data sheet for more details.

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs (see Figure 2) is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

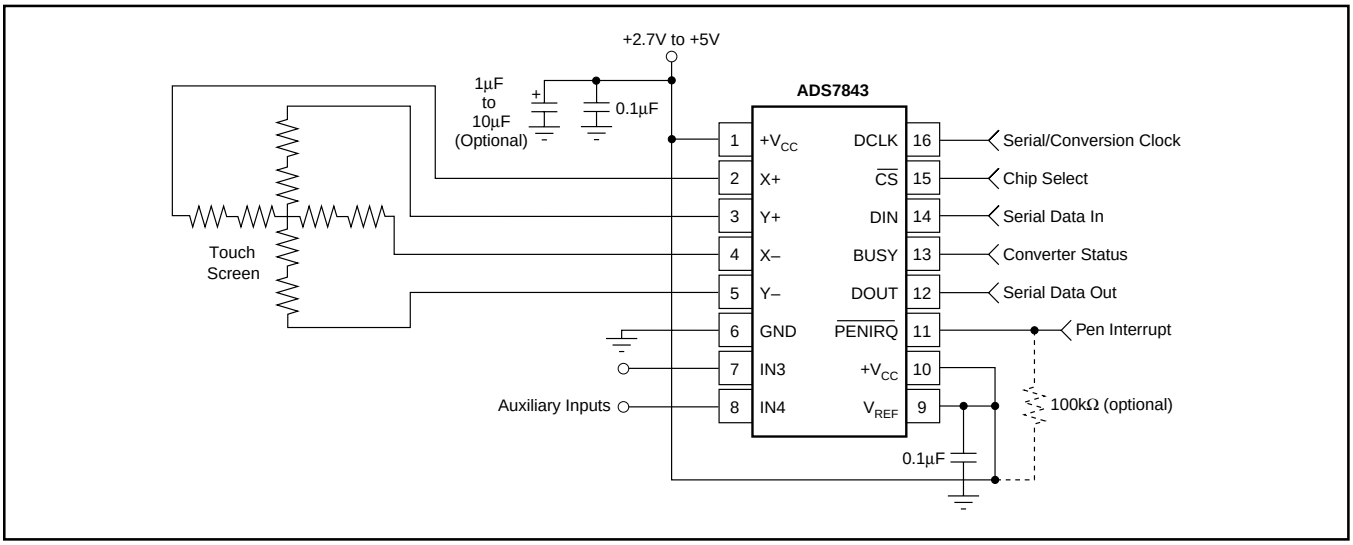


FIGURE 1. Basic Operation of the ADS7843.

A2	A1	A0	X+	Y+	IN3	IN4	–IN(1)	X SWITCHES	Y SWITCHES	+REF(1)	–REF(1)
0	0	1	+IN				GND	OFF	ON	$+V_{REF}$	GND
1	0	1		+IN			GND	ON	OFF	$+V_{REF}$	GND
0	1	0			+IN		GND	OFF	OFF	$+V_{REF}$	GND
1	1	0				+IN	GND	OFF	OFF	$+V_{REF}$	GND

NOTE: (1) Internal node, for clarification only—not directly accessible by the user.

TABLE I. Input Configuration, Single-Ended Reference Mode (SER/$\overline{\text{DFR}}$ HIGH).

A2	A1	A0	X+	Y+	IN3	IN4	–IN(1)	X SWITCHES	Y SWITCHES	+REF(1)	–REF(1)
0	0	1	+IN				–Y	OFF	ON	+Y	–Y
1	0	1		+IN			–X	ON	OFF	+X	–X
0	1	0			+IN		GND	OFF	OFF	$+V_{REF}$	GND
1	1	0				+IN	GND	OFF	OFF	$+V_{REF}$	GND

NOTE: (1) Internal node, for clarification only—not directly accessible by the user.

TABLE II. Input Configuration, Differential Reference Mode (SER/$\overline{\text{DFR}}$ LOW).

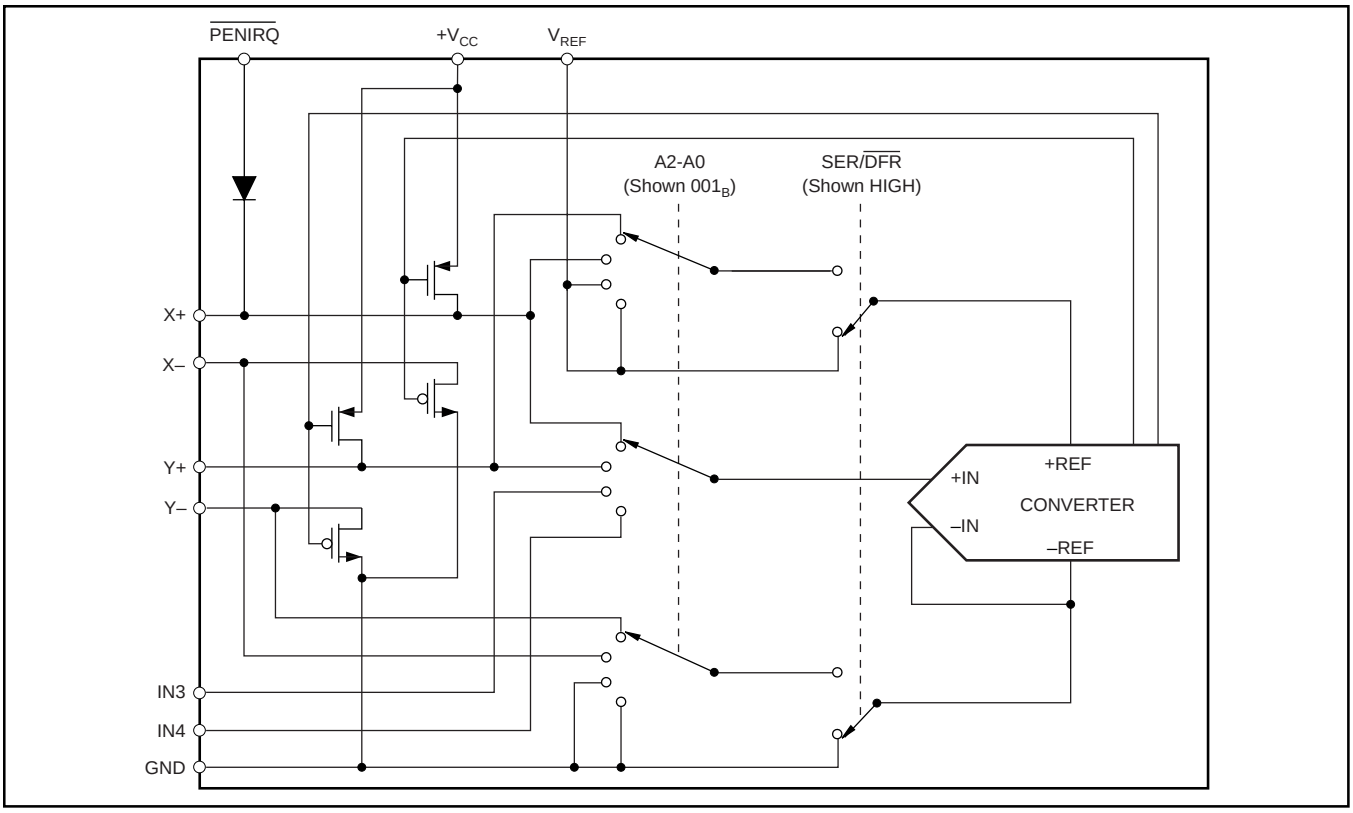


FIGURE 2. Simplified Diagram of Analog Input.

REFERENCE INPUT

The voltage difference between +REF and –REF (shown in Figure 2) sets the analog input range. The ADS7843 will operate with a reference in the range of 1V to $+V_{CC}$. There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the ADC will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2LSBs with a 2.5V reference, it will typically be 5LSBs with a 1V reference. In each case, the actual offset of the device is the same, 1.22mV. With a lower reference voltage, more care must be taken to provide a clean layout including adequate bypassing, a clean (low noise, low ripple) power supply, a low-noise reference, and a low-noise input signal.

The voltage into the V_{REF} input is not buffered and directly drives the Capacitor Digital-to-Analog Converter (CDAC) portion of the ADS7843. Typically, the input current is 13µA with V_{REF} = 2.7V and f_{SAMPLE} = 125kHz. This value will vary by a few microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

There is also a critical item regarding the reference when making measurements where the switch drivers are on. For this discussion, it's useful to consider the basic operation of the ADS7843 as shown in Figure 1. This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y position of the pointing device is made by connecting the X+ input to the ADC, turning on the Y+ and Y– drivers, and digitizing the voltage on X+ (shown in Figure 3). For this measurement, the resistance in the X+ lead does not affect the conversion (it does affect the settling time, but the resistance is usually small enough that this is not a concern).

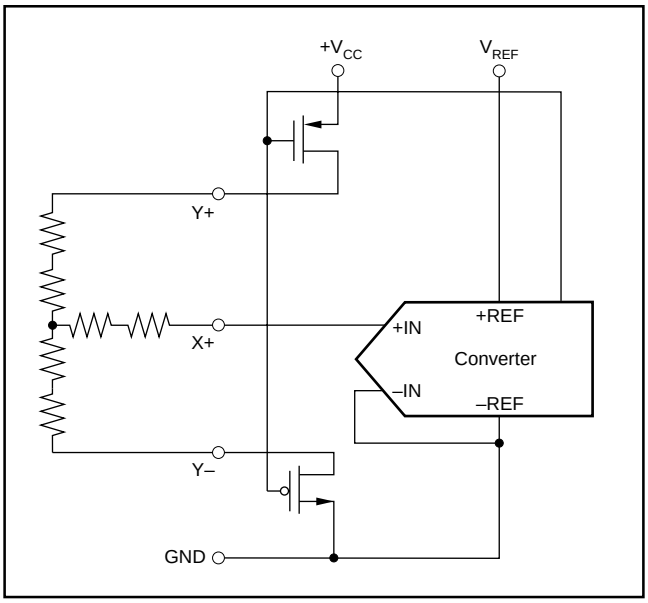


FIGURE 3. Simplified Diagram of Single-Ended Reference (SER/DFR HIGH, Y Switches Enabled, X+ is Analog Input).

However, since the resistance between Y+ and Y– is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it would not be possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error.

This situation can be remedied as shown in Figure 4. By setting the SER/$\overline{\text{DFR}}$ bit LOW, the +REF and –REF inputs are connected directly to Y+ and Y–. This makes the A/D conversion ratiometric. The result of the conversion is always a percentage of the external resistance, regardless of how it changes in relation to the on-resistance of the internal switches. Note that there is an important consideration regarding power dissipation when using the ratiometric mode of operation, see the Power Dissipation section for more details.

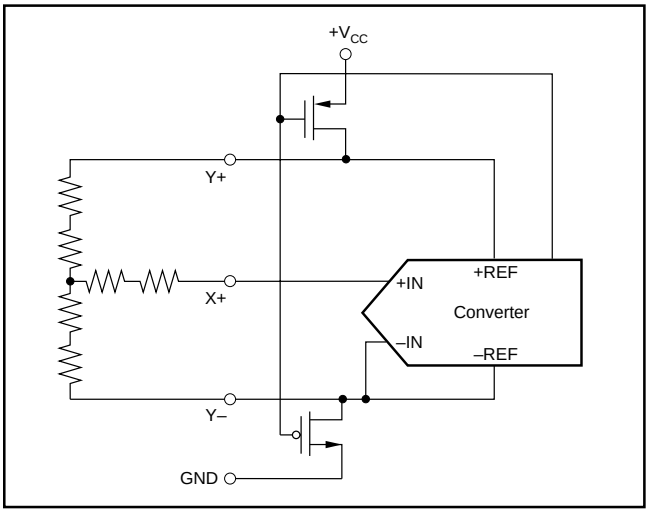


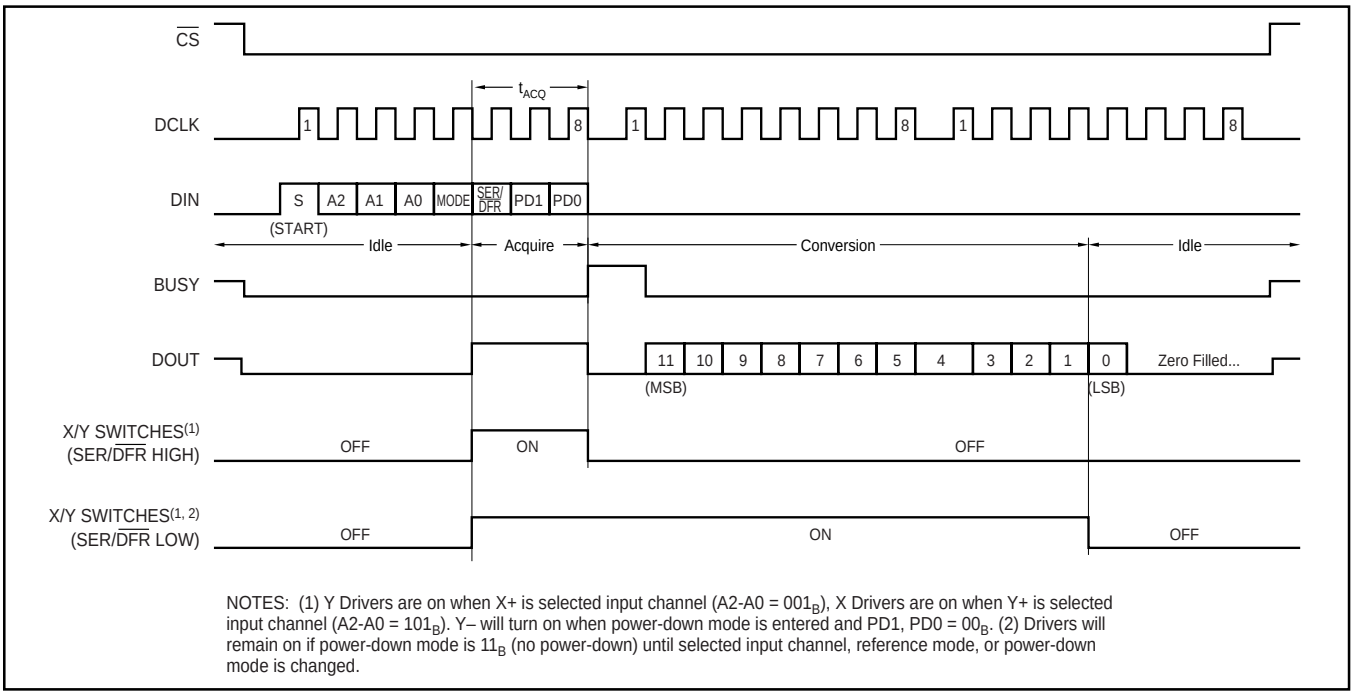
FIGURE 4. Simplified Diagram of Differential Reference (SER/$\overline{\text{DFR}}$ LOW, Y Switches Enabled, X+ is Analog Input).

As a final note about the differential reference mode, it must be used with +V_{CC} as the source of the +REF voltage and cannot be used with V_{REF}. It is possible to use a high precision reference on V_{REF} and single-ended reference mode for measurements which do not need to be ratiometric. Or, in some cases, it could be possible to power the converter directly from a precision reference. Most references can provide enough power for the ADS7843, but they might not be able to supply enough current for the external load (such as a resistive touch screen).

DIGITAL INTERFACE

Figure 5 shows the typical operation of the ADS7843's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface. Each communication between the processor and the converter consists of eight clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer, switches, and reference inputs appropriately, the converter enters the acquisition (sample) mode and, if needed, the internal switches are turned on. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the hold mode and the internal switches may turn off. The



NOTES: (1) Y Drivers are on when X+ is selected input channel (A2-A0 = 001_B), X Drivers are on when Y+ is selected input channel (A2-A0 = 101_B). Y– will turn on when power-down mode is entered and PD1, PD0 = 00_B. (2) Drivers will remain on if power-down mode is 11_B (no power-down) until selected input channel, reference mode, or power-down mode is changed.

FIGURE 5. Conversion Timing, 24 Clocks per Conversion, 8-bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.

next 12th clock cycles accomplish the actual A/D conversion. If the conversion is ratiometric (SER/$\overline{DFR}$ LOW), the internal switches are on during the conversion. A 13th clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be LOW). These will be ignored by the converter.

Control Byte

See Figure 5 for the placement and order of the control bits within the control byte. Tables III and IV give detailed information about these bits. The first bit, the 'S' bit, must always be HIGH and indicates the start of the control byte. The ADS7843 will ignore inputs on the DIN pin until the start bit is detected. The next three bits (A2-A0) select the active input channel or channels of the input multiplexer (see Tables I and II and Figure 2). The MODE bit determines the number of bits for each conversion, either 12 bits (LOW) or 8 bits (HIGH).

The SER/$\overline{DFR}$ bit controls the reference mode: either single-ended (HIGH) or differential (LOW). (The differential mode is also referred to as the ratiometric conversion mode.) In single-ended mode, the converter's reference voltage is always the difference between the V_{REF} and GND pins. In differential mode, the reference voltage is the difference between the currently enabled switches. See Tables I and II and Figures 2 through 4 for more information. The last two bits (PD1-PD0) select the power-down mode as shown in Table V. If both inputs are HIGH, the device is always powered up. If both inputs are LOW, the device enters a power-down mode between conversions. When a new conversion is initiated, the device will resume normal operation instantly—no delay is needed to allow the device to power up and the very first conversion will be valid. There are two power-down modes: one where $\overline{PENIRQ}$ is disabled and one where it is enabled.

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	MODE	SER/$\overline{DFR}$	PD1	PD0

TABLE III. Order of the Control Bits in the Control Byte.

16-Clocks per Conversion

The control bits for conversion n + 1 can be overlapped with conversion 'n' to allow for a conversion every 16 clock cycles, as shown in Figure 6. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer between the processor and the converter.

BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first HIGH bit on DIN. A new control byte can start every 16th clock cycle in 12-bit conversion mode or every 12th clock cycle in 8-bit conversion mode.
6-4	A2-A0	Channel Select Bits. Along with the SER/$\overline{DFR}$ bit, these bits control the setting of the multiplexer input, switches, and reference inputs, see Tables I and II.
3	MODE	12-Bit/8-Bit Conversion Select Bit. This bit controls the number of bits for the following conversion: 12 bits (LOW) or 8 bits (HIGH).
2	SER/$\overline{DFR}$	Single-Ended/Differential Reference Select Bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input, switches, and reference inputs, see Tables I and II.
1-0	PD1-PD0	Power-Down Mode Select Bits. See Table V for details.

TABLE IV. Descriptions of the Control Bits within the Control Byte.

PD1	PD0	PENIRQ	DESCRIPTION
0	0	Enabled	Power-down between conversions. When each conversion is finished, the converter enters a low power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid. The Y– switch is on while in power-down.
0	1	Disabled	Same as mode 00, except $\overline{PENIRQ}$ is disabled. The Y– switch is off while in power-down mode.
1	0	Disabled	Reserved for future use.
1	1	Disabled	No power-down between conversions, device is always powered.

TABLE V. Power-Down Selection.

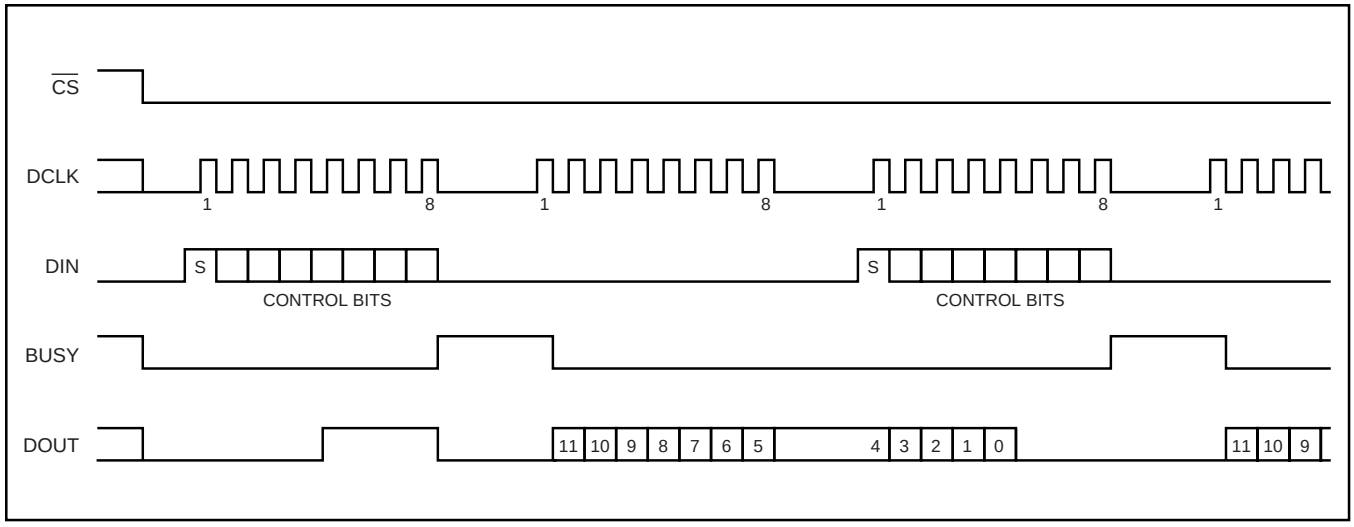


FIGURE 6. Conversion Timing, 16 Clocks per Conversion, 8-bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.

This is possible provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that has been captured on the input sample-and-hold may droop enough to affect the conversion result. Note that the ADS7843 is fully powered while other serial communications are taking place during a conversion.

Digital Timing

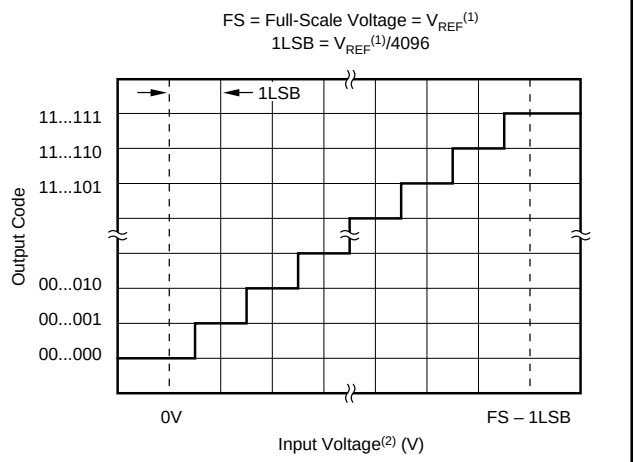
Figure 7 and Table VI provide detailed timing for the digital interface of the ADS7843.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	1.5			µs
t_{DS}	DIN Valid Prior to DCLK Rising	100			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			200	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			200	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			200	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	100			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	200			ns
t_{CL}	DCLK LOW	200			ns
t_{BD}	DCLK Falling to BUSY Rising			200	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			200	ns

TABLE VI. Timing Specifications ($+V_{CC}$ = +2.7V and Above, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

Data Format

The ADS7843 output data is in Straight Binary format, as shown in Figure 8. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



NOTES: (1) Reference voltage at converter: +REF – (–REF). See Figure 2.
(2) Input voltage at converter, after multiplexer: +IN – (–IN). See Figure 2

FIGURE 8. Ideal Input Voltages and Output Codes.

8-Bit Conversion

The ADS7843 provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. This could be used in conjunction with serial interfaces that provide 12-bit transfers or two conversions could be accomplished with three 8-bit transfers. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This is because the internal settling time of the ADS7843 is not as critical—settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.

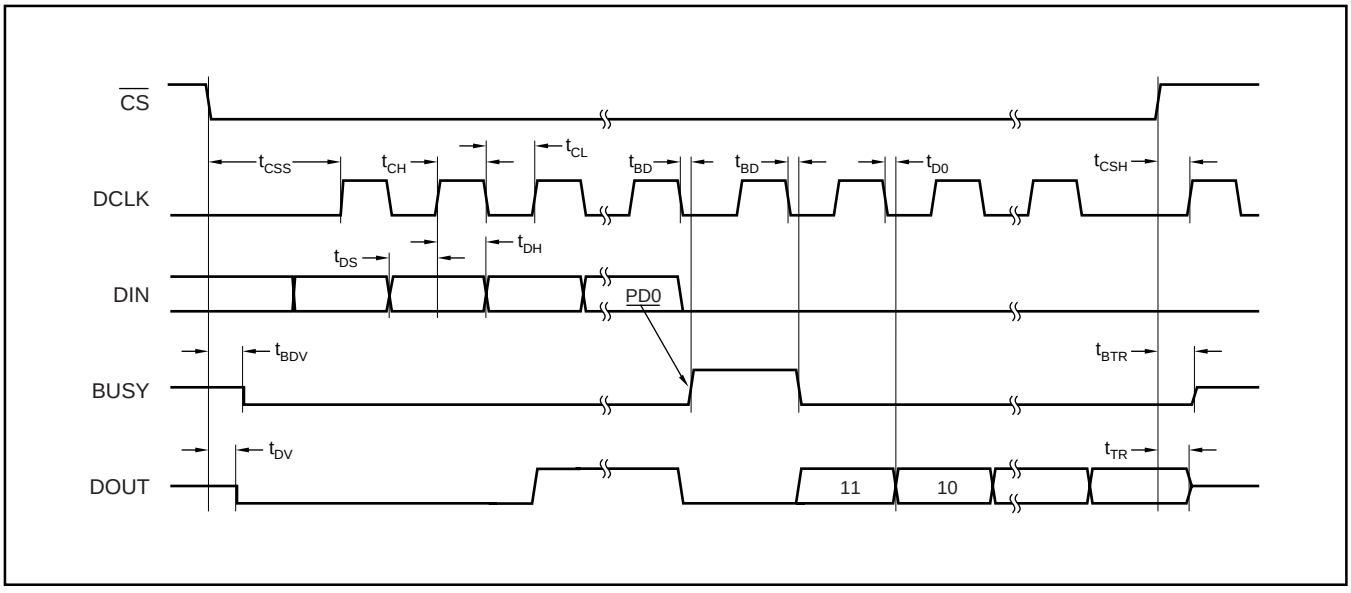


FIGURE 7. Detailed Timing Diagram.

POWER DISSIPATION

There are two major power modes for the ADS7843: full power (PD1-PD0 = 11_B) and auto power-down (PD1-PD0 = 00_B). When operating at full speed and 16 clocks per conversion (see Figure 6), the ADS7843 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Therefore, the difference between full power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion but conversions are simply done less often, the difference between the two modes is dramatic.

Figure 9 shows the difference between reducing the DCLK frequency ("scaling" DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversions per second. In the later case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).

Another important consideration for power dissipation is the reference mode of the converter. In the single-ended reference mode, the converter's internal switches are on only when the analog input voltage is being acquired (see Figure 5). Thus, the external device, such as a resistive touch screen, is only powered during the acquisition period. In the differential reference mode, the external device must be powered throughout the acquisition and conversion periods (see Figure 5). If the conversion rate is high, this could substantially increase power dissipation.

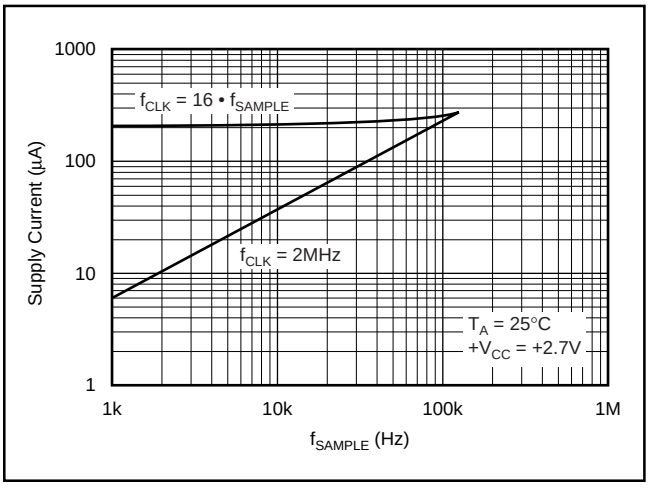


FIGURE 9. Supply Current versus Directly Scaling the Frequency of DCLK with Sample Rate or Keeping DCLK at the Maximum Possible Frequency.

LAYOUT

The following layout suggestions should provide the most optimum performance from the ADS7843. However, many portable applications have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly "clean" power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter's power and less concern regarding grounding. Still, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the ADS7843 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an 'n-bit' SAR converter, there are n 'windows' in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS7843 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. A 1µF to 10µF capacitor may also be needed if the impedance of the connection between +V_{CC} and the power supply is high.

The reference should be similarly bypassed with a 0.1µF capacitor. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation. The ADS7843 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

The ADS7843 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery connection point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Since resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Longer connections will be a source of error, much like the on-resistance of the internal switches. Likewise, loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS7843E	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7843E	Samples
ADS7843E/2K5	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7843E	Samples
ADS7843E/2K5G4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7843E	Samples
ADS7843EG4	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7843E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF ADS7843 :

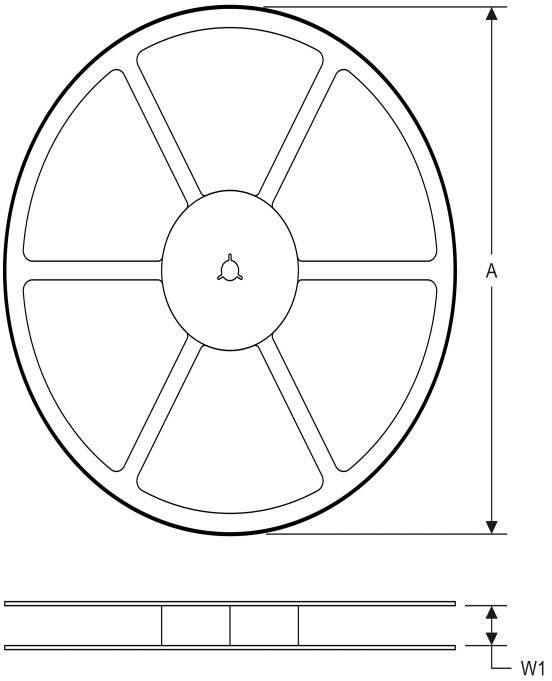
- Automotive: ADS7843-Q1

NOTE: Qualified Version Definitions:

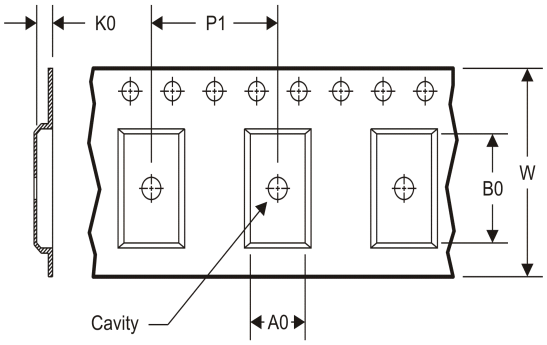
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



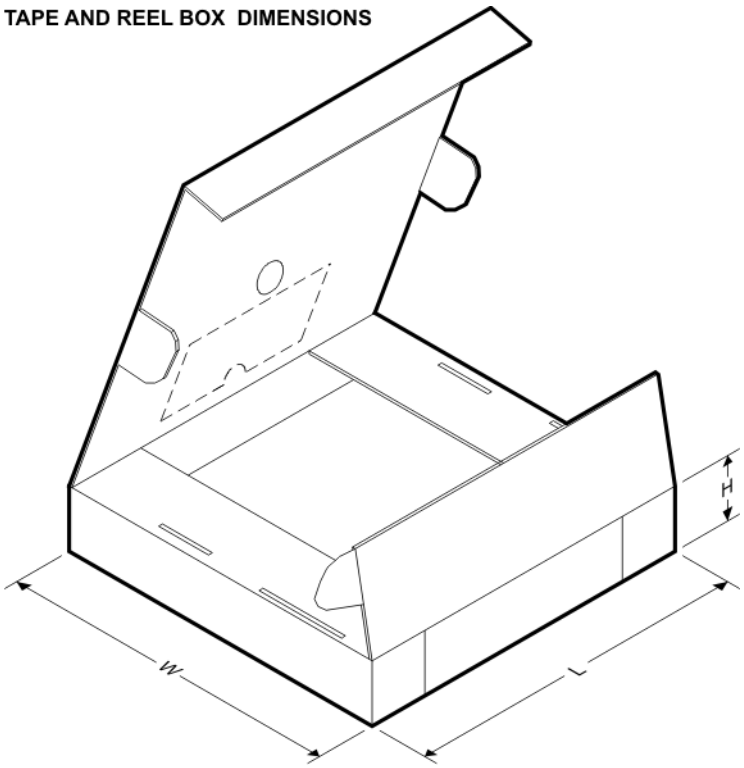
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7843E/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



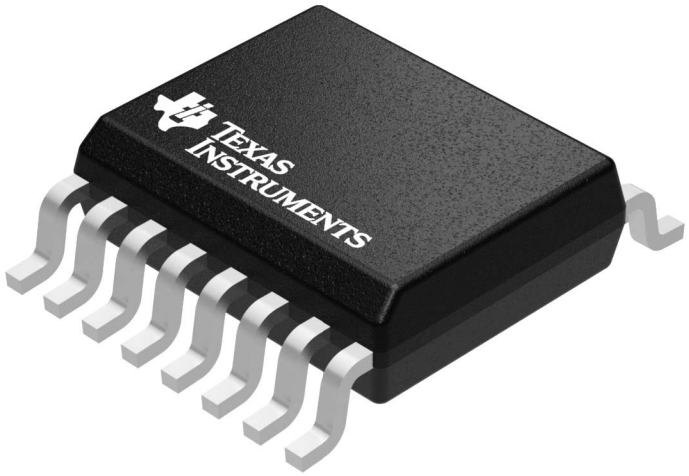
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7843E/2K5	SSOP	DBQ	16	2500	367.0	367.0	35.0

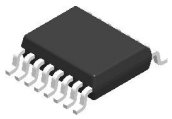
GENERIC PACKAGE VIEW

DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

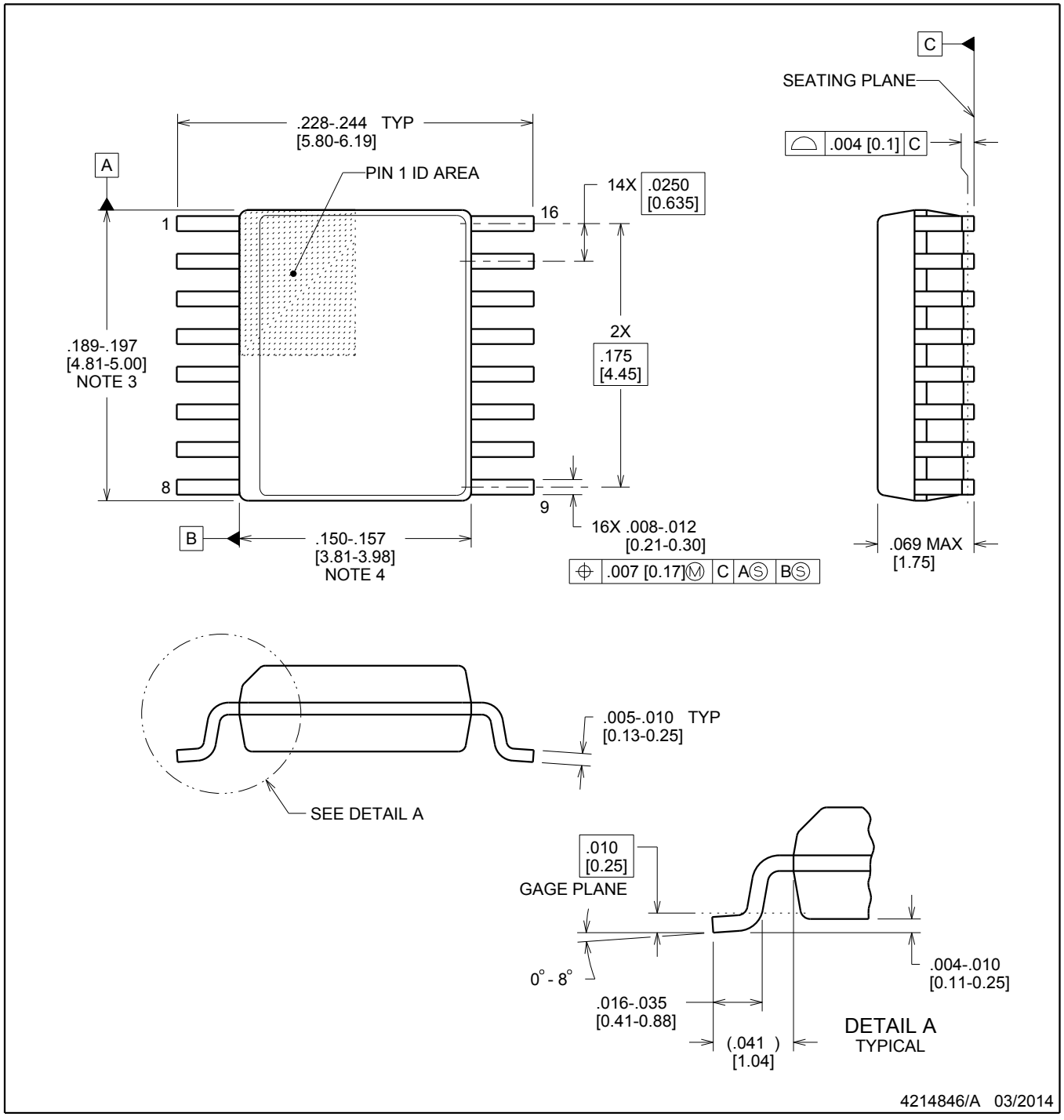


PACKAGE OUTLINE

DBQ0016A

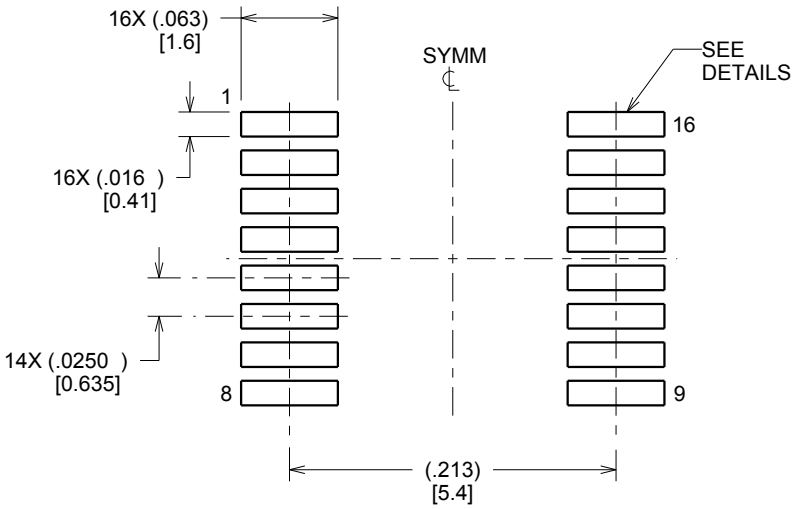
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

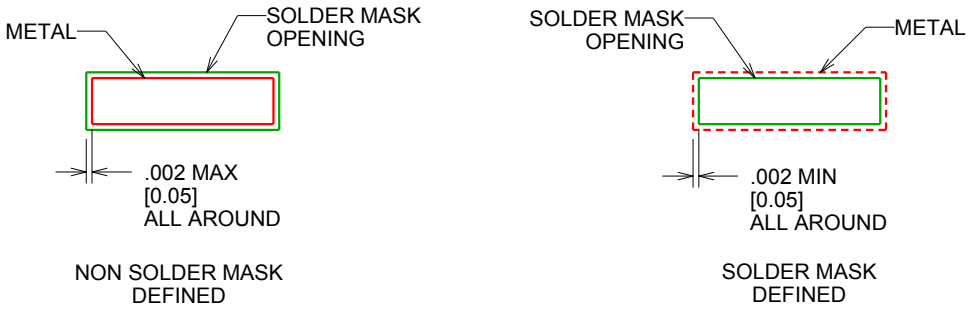


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

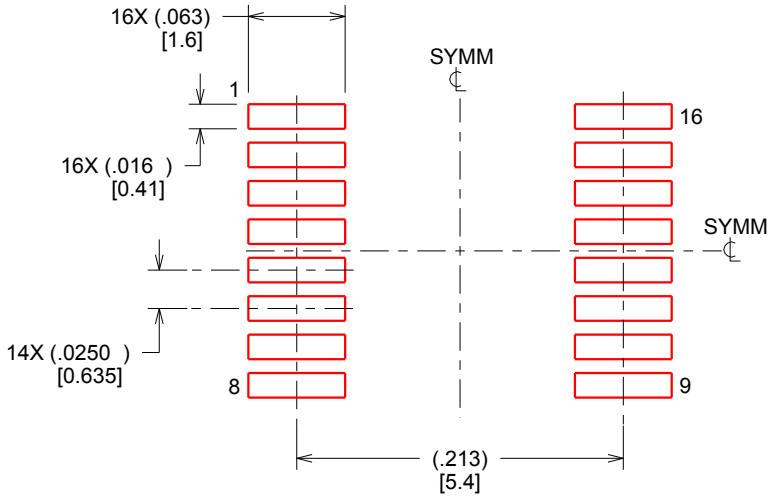
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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