



**THE DATASHEET OF  
SUM110P04-04L-E3**





# P-Channel 40 V (D-S) 175 °C MOSFET

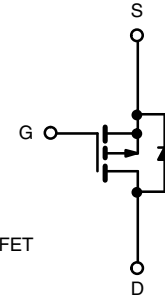
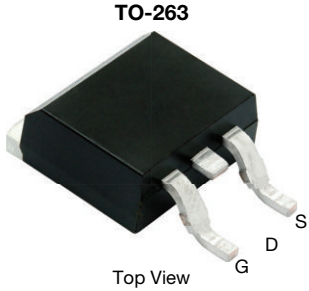
PRODUCT SUMMARY		
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>d</sup>
-40	0.0042 at $V_{GS} = -10$ V	-110
	0.0062 at $V_{GS} = -4.5$ V	-110

## FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- Low thermal resistance
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS COMPLIANT



## Ordering Information:

SUM110P04-04L-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175$ °C) <sup>d</sup>	$I_D$	$T_C = 25$ °C	-110
		$T_C = 125$ °C	-110
Pulsed Drain Current	$I_{DM}$	-240	A
Avalanche Current	$I_{AS}$	-75	
Single Pulse Avalanche Energy <sup>a</sup>	$E_{AS}$	281	mJ
Power Dissipation	$P_D$	$T_C = 25$ °C	375 <sup>c</sup>
		$T_A = 25$ °C <sup>b</sup>	3.75
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient PCB Mount <sup>b</sup>	$R_{thJA}$	40	°C/W
Junction-to-Case	$R_{thJC}$	0.4	

## Notes

- Duty cycle  $\leq 1$  %.
- When mounted on 1" square PCB (FR-4 material).
- See SOA curve for voltage derating.
- Limited by package.



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-40			V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1		-3	V	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V			-1	μA	
		V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			-50		
		V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			-250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -10 V	-120			A	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -30 A		0.0034	0.0042	Ω	
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -30 A, T <sub>J</sub> = 125 °C			0.0063		
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -30 A, T <sub>J</sub> = 175 °C			0.0076		
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -20 A		0.005	0.0062		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -30 A	20			S	
<b>Dynamic <sup>b</sup></b>							
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -25 V, f = 1 MHz		11 200		pF	
Output Capacitance	C <sub>OSS</sub>			1650			
Reverse Transfer Capacitance	C <sub>RSS</sub>			1200			
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -110 A		235	350	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			45			
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			65			
Gate Resistance	R <sub>g</sub>			3		Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -20 V, R <sub>L</sub> = 0.18 Ω I <sub>D</sub> ≅ -110 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 2.5 Ω		25	40	ns	
Rise Time <sup>c</sup>	t <sub>r</sub>			30	45		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			190	300		
Fall Time <sup>c</sup>	t <sub>f</sub>			110	165		
<b>Source-Drain Diode Ratings and Characteristics (T<sub>C</sub> = 25 °C) <sup>b</sup></b>							
Continuous Current	I <sub>S</sub>				-110	A	
Pulsed Current	I <sub>SM</sub>				-240		
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = -85 A, V <sub>GS</sub> = 0 V		-1	-1.5	V	
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -85 A, di/dt = 100 A/μs		65	100	ns	
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>				-3.7	-5.6	A
Reverse Recovery Charge	Q <sub>rr</sub>				0.12	0.28	μC

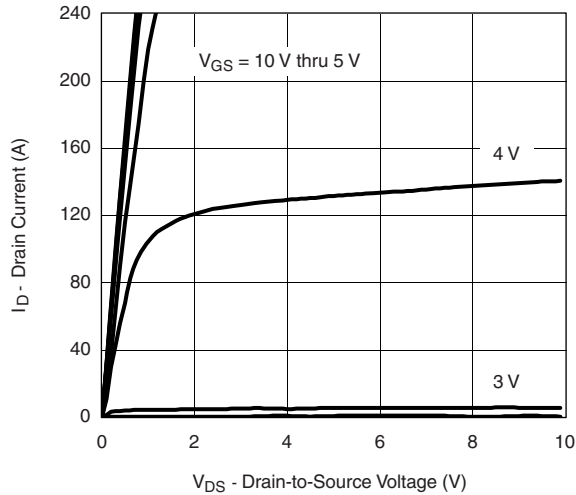
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

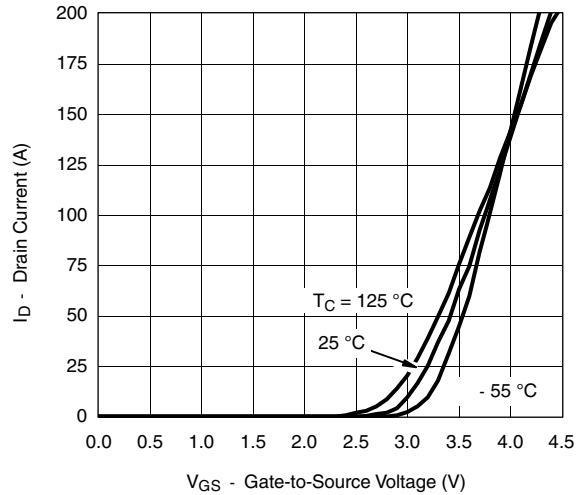
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



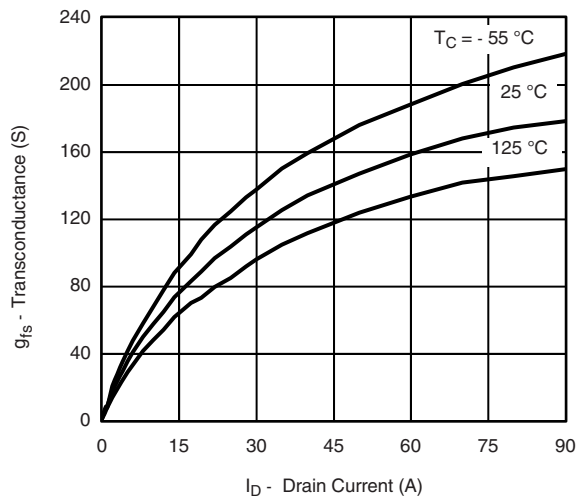
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



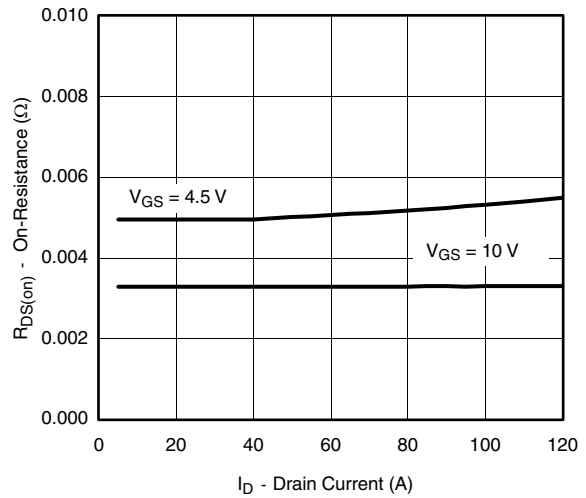
Output Characteristics



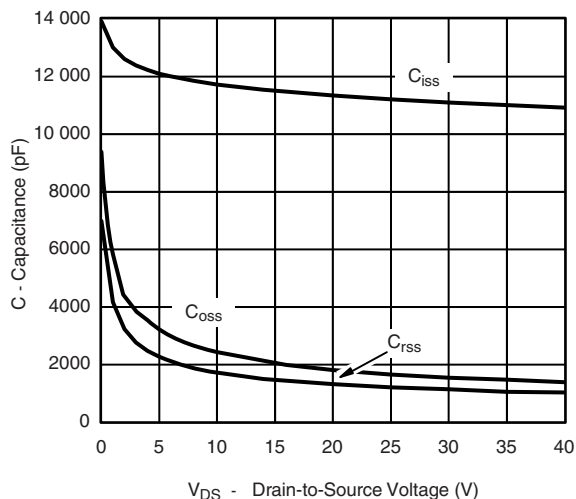
Transfer Characteristics



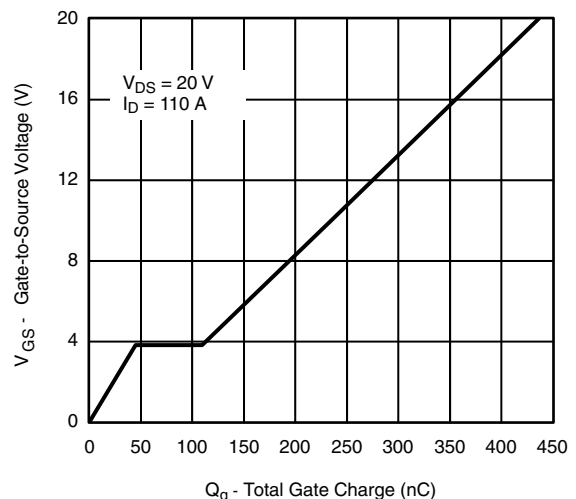
Transconductance



On-Resistance vs. Drain Current



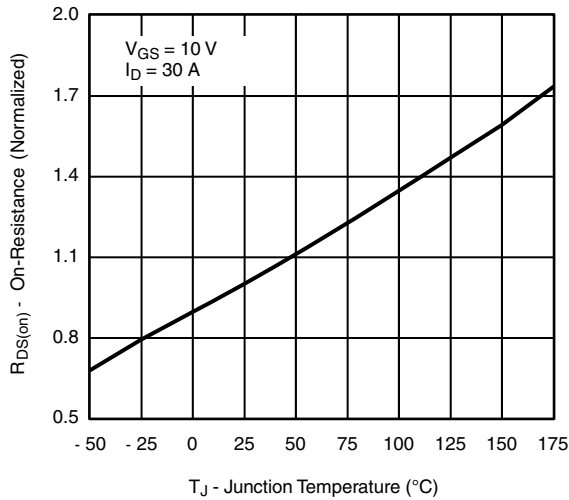
Capacitance



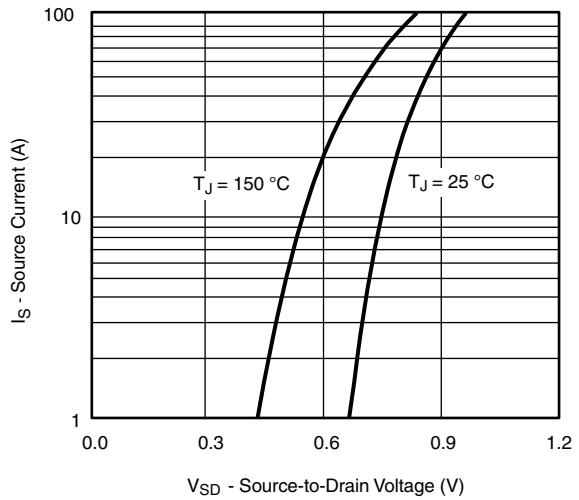
Gate Charge



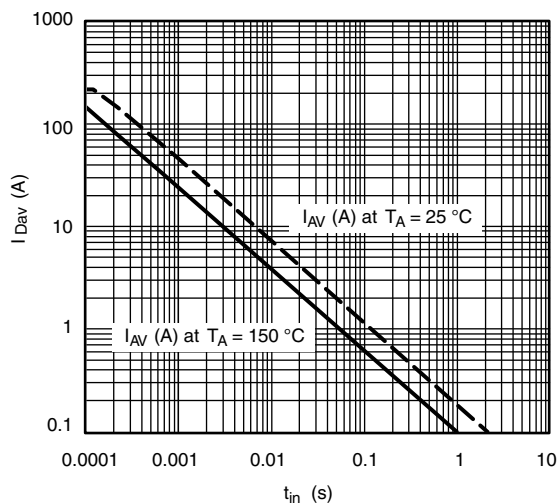
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



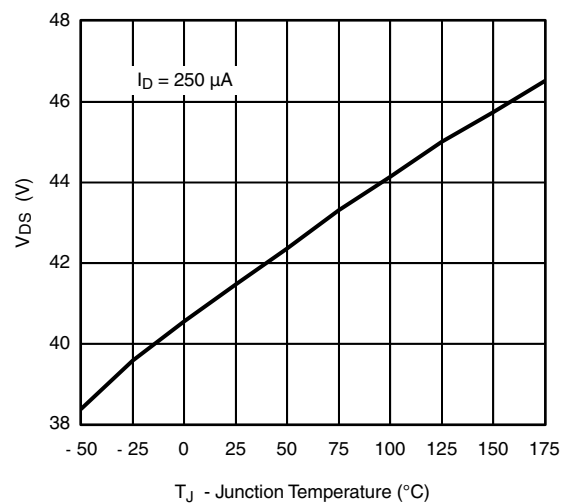
**On-Resistance vs. Junction Temperature**



**Source-Drain Diode Forward Voltage**



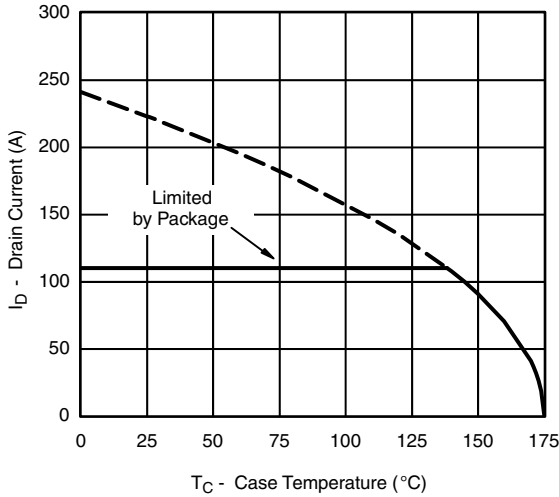
**Avalanche Current vs. Time**



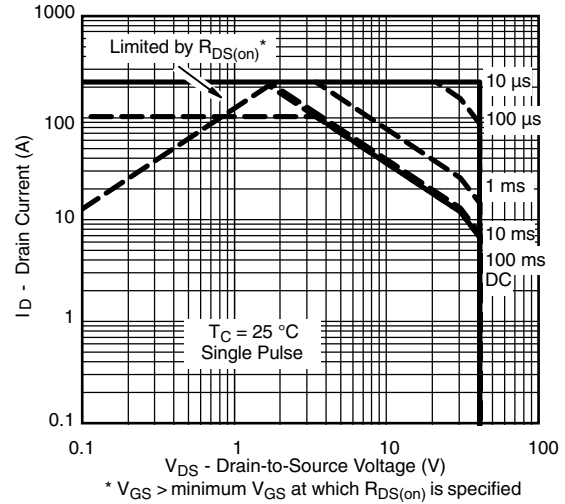
**Drain Source Breakdown vs. Junction Temperature**



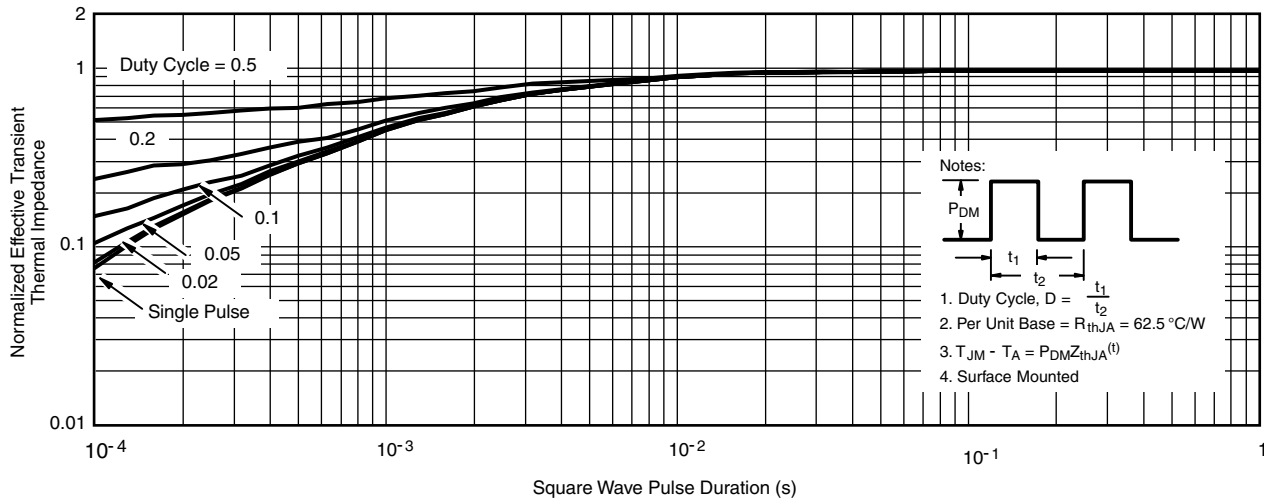
THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

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# TO-263 (D<sup>2</sup>PAK): 3-LEAD



DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

**Notes**

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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