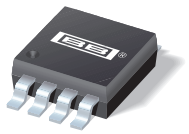
THE DATASHEET OF

ADS7823E/2K5



SBAS180B – JUNE 2001 - REVISED SEPTEMBER 2003

12-Bit, Sampling A/D Converter with I²C™ INTERFACE

FEATURES

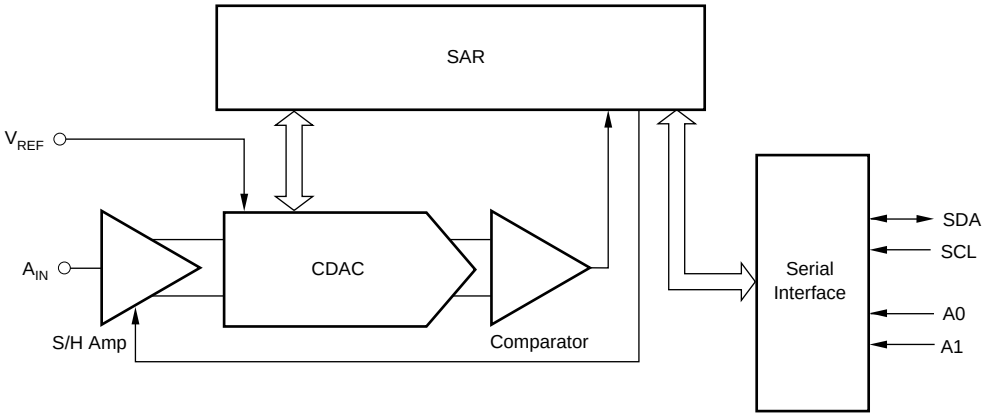
- 50kHz SAMPLING RATE
- NO MISSING CODES
- 2.7V TO 5V OPERATION
- FOUR-WORD FILO
- A0, A1 ADDRESS PINS
- I²C INTERFACE SUPPORTS: Standard, Fast, and High-Speed Modes
- MSOP-8 PACKAGE

DESCRIPTION

The ADS7823 is a single-supply, low-power, 12-bit data acquisition device that features a serial I²C interface. The Analog-to-Digital (A/D) converter features a sample-and-hold amplifier and internal, asynchronous clock. The combination of an I²C serial two-wire interface and micropower consumption makes the ADS7823 ideal for applications requiring the A/D converter to be close to the input source in remote locations and for applications requiring isolation. The ADS7823 is available in an MSOP-8 package.

APPLICATIONS

- VOLTAGE SUPPLY MONITORING
- ISOLATED DATA ACQUISITION
- TRANSDUCER INTERFACE
- BATTERY-OPERATED SYSTEMS
- REMOTE DATA ACQUISITION



ABSOLUTE MAXIMUM RATINGS[1]

$+V_{DD}$ to GND	–0.3V to +6V
Digital Input Voltage to GND	–0.3V to $+V_{DD}$ + 0.3V
Analog Input Voltage to GND	–0.3V to +6.0V
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature (T_J max)	+150°C
TSSOP Package	
Power Dissipation	(T_J max – T_A)/θ_{JA}
θ_{JA} Thermal Impedance	+240°C/W
Lead Temperature, Soldering	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7823E	±2	–40°C to +85°C	MSOP-8	DGK	B23	ADS7823E/250	Tape and Reel, 250
"	"	"	"	"	"	ADS7823E/2K5	Tape and Reel, 2500
ADS7823EB	±1	–40°C to +85°C	MSOP-8	DGK	B23	ADS7823EB/250	Tape and Reel, 250
"	"	"	"	"	"	ADS7823EB/2K5	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS: +2.7V

At T_A = –40°C to +85°C, $+V_{DD}$ = +2.7V, V_{REF} = +2.5V, SCL Clock Frequency = 3.4MHz (High Speed Mode) unless otherwise noted.

		ADS7823E			ADS7823EB			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Full-Scale Input Range		0		V_{REF}	*		*	V
Input Capacitance			25			*		pF
Input Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
No Missing Codes		12			*			Bits
Integral Linearity Error			±1.0	±2		±0.5	±1	LSB[1]
Differential Linearity Error			–0.5, +1.0	–1.0, +3.0		±0.5	*	LSB
Offset Error			±1.0	±4		±0.75	±3	LSB
Gain Error			±1.0	±4		±0.75	±3	LSB
Noise			33			*		µVrms
Power Supply Rejection			82			*		dB
SAMPLING DYNAMICS								
Throughput Frequency	High Speed Mode: SCL = 3.4MHz			50			*	kHz
	Fast Mode: SCL = 400kHz			8			*	kHz
	Standard Mode, SCL = 100kHz			2			*	kHz
Conversion Time			8			*		µs
AC ACCURACY								
Total Harmonic Distortion	V_{IN} = 2.5V_{PP} at 10kHz		–82			*		dB[2]
Signal-to-Ratio	V_{IN} = 2.5V_{PP} at 10kHz		72			*		dB
Signal-to-(Noise+Distortion) Ratio	V_{IN} = 2.5V_{PP} at 10kHz		71			*		dB
Spurious Free Dynamic Range	V_{IN} = 2.5V_{PP} at 10kHz		86			*		dB
VOLTAGE REFERENCE INPUT								
Range		0.05		V_{DD}	*		*	V
Resistance	All Modes		1.0			*		GΩ
Current Drain	At Code 800H, HS Mode: SCL = 3.4MHz		9.0			*		µA

ELECTRICAL CHARACTERISTICS: +2.7V (Cont.)

At T_A = –40°C to +85°C, $+V_{DD}$ = +2.7V, V_{REF} = +2.5V, SCL Clock Frequency = 3.4MHz (High Speed Mode) unless otherwise noted.

PARAMETER	CONDITIONS	ADS7823E MIN	ADS7823E TYP	ADS7823E MAX	ADS7823EB MIN	ADS7823EB TYP	ADS7823EB MAX	UNITS
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels: V_{IH}		$+V_{DD}$ • 0.7		$+V_{DD}$ + 0.5	*		*	V
V_{IL}		–0.3		$+V_{DD}$ • 0.3	*		*	V
V_{OL}	At min 3mA Sink Current			0.4			*	V
Input Leakage: I_{IH}	V_{IH} = $+V_{DD}$ +0.5			10			*	µA
I_{IL}	V_{IL} = -0.3	-10			*			µA
Data Format			Straight Binary			*		
ADS7823 HARDWARE ADDRESS			10010			*		Binary
POWER SUPPLY REQUIREMENTS								
Power Supply Voltage, $+V_{DD}$	Specified Performance	2.7		3.6	*		*	V
Quiescent Current	High Speed Mode: SCL = 3.4MHz		250	370		*	*	µA
	Fast Mode: SCL = 400kHz		137			*		µA
	Standard Mode, SCL = 100kHz		109			*		µA
Power Dissipation	High Speed Mode: SCL = 3.4MHz		680	1000		*	*	µW
	Fast Mode: SCL = 400kHz		370			*		µW
	Standard Mode, SCL = 100kHz		290			*		µW
Powerdown Mode	High Speed Mode: SCL = 3.4MHz		60			*		µA
w/Wrong Address Selected	Fast Mode: SCL = 400kHz		23			*		µA
	Standard Mode, SCL = 100kHz		5.4			*		µA
Full Powerdown	SCL Pulled HIGH, SDA Pulled HIGH		2	3000		*	*	nA
TEMPERATURE RANGE								
Specified Performance		–40		85	*		*	°C

* Specifications same as ADS7823E.

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to 2.5V, 1LSB is 610µV. (2) THD measured out to the 9th-harmonic.

ELECTRICAL CHARACTERISTICS: +5V

At T_A = –40°C to +85°C, $+V_{DD}$ = +5.0V, V_{REF} = +5.0V, SCL Clock Frequency = 3.4MHz (High Speed Mode) unless otherwise noted.

PARAMETER	CONDITIONS	ADS7823E MIN	ADS7823E TYP	ADS7823E MAX	ADS7823EB MIN	ADS7823EB TYP	ADS7823EB MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Full-Scale Input Range		0		V_{REF}	*		*	V
Input Capacitance			25			*		pF
Input Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
No Missing Codes		12			*			Bits
Integral Linearity Error			±1.0	±2		±0.5	±1	LSB(1)
Differential Linearity Error			–0.5, +1.0	–1, +3		±0.5	*	LSB
Offset Error			±1.0	±4		±0.75	±3	LSB
Gain Error			±1.0	±4		±0.75	±3	LSB
Noise			33			*		µVrms
Power Supply Rejection			82			*		dB
SAMPLING DYNAMICS								
Throughput Frequency	High Speed Mode: SCL = 3.4MHz			50			*	kHz
	Fast Mode: SCL = 400kHz			8			*	kHz
	Standard Mode, SCL = 100kHz			2			*	kHz
Conversion Time			8			*		µs
AC ACCURACY								
Total Harmonic Distortion	V_{IN} = $2.5V_{PP}$ at 10kHz		–82			*		dB(2)
Signal-to-Ratio	V_{IN} = $2.5V_{PP}$ at 10kHz		72			*		dB
Signal-to-(Noise+Distortion) Ratio	V_{IN} = $2.5V_{PP}$ at 10kHz		71			*		dB
Spurious Free Dynamic Range	V_{IN} = $2.5V_{PP}$ at 10kHz		86			*		dB
VOLTAGE REFERENCE INPUT								
Range		0.05		V_{DD}	*		*	V
Resistance	All Modes		1.0			*		GΩ
Current Drain	At Code 800H, HS Mode: SCL = 3.4MHz		20			*		µA

ELECTRICAL CHARACTERISTICS: +5V (Cont.)

At T_A = –40°C to +85°C, $+V_{DD}$ = +5.0V, V_{REF} = +5.0V, SCL Clock Frequency = 3.4MHz (High Speed Mode) unless otherwise noted.

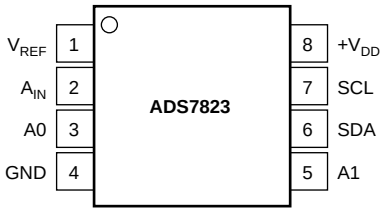
PARAMETER	CONDITIONS	ADS7823E			ADS7823EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels: V_{IH}			$+V_{DD}$ • 0.7		$+V_{DD}$ + 0.5	*		*	V
V_{IL}			–0.3		$+V_{DD}$ • 0.3	*		*	V
V_{OL}	At min 3mA Sink Current				0.4			*	V
Input Leakage: I_{IH}	V_{IH} = $+V_{DD}$ +0.5				10			*	µA
I_{IL}	V_{IL} = -0.3		-10			*			µA
Data Format				Straight Binary			*		
ADS7823 HARDWARE ADDRESS				10010			*		Binary
POWER SUPPLY REQUIREMENTS								
Power Supply Voltage, $+V_{DD}$	Specified Performance	4.75	5	5.25	*		*	V
Quiescent Current	High Speed Mode: SCL= 3.4MHz		0.72	1.0		*	*	mA
	Fast Mode: SCL= 400kHz		380			*		µA
	Standard Mode, SCL=100kHz		240			*		µA
Power Dissipation	High Speed Mode: SCL= 3.4MHz		3.6	5.0		*	*	mW
	Fast Mode: SCL= 400kHz		1.9			*		mW
	Standard Mode, SCL=100kHz		1.2			*		mW
Powerdown Mode	High Speed Mode: SCL= 3.4MHz		346			*		µA
w/Wrong Address Selected	Fast Mode: SCL= 400kHz		136			*		µA
	Standard Mode, SCL=100kHz		34			*		µA
Full Powerdown	SCL Pulled HIGH, SDA Pulled HIGH		3	3000		*	*	nA
TEMPERATURE RANGE								
Specified Performance		–40		85	*		*	°C

* Specifications same as ADS7823E.

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to 2.5V, 1LSB is 610µV. (2) THD measured out to the 9th-harmonic.

PIN CONFIGURATION

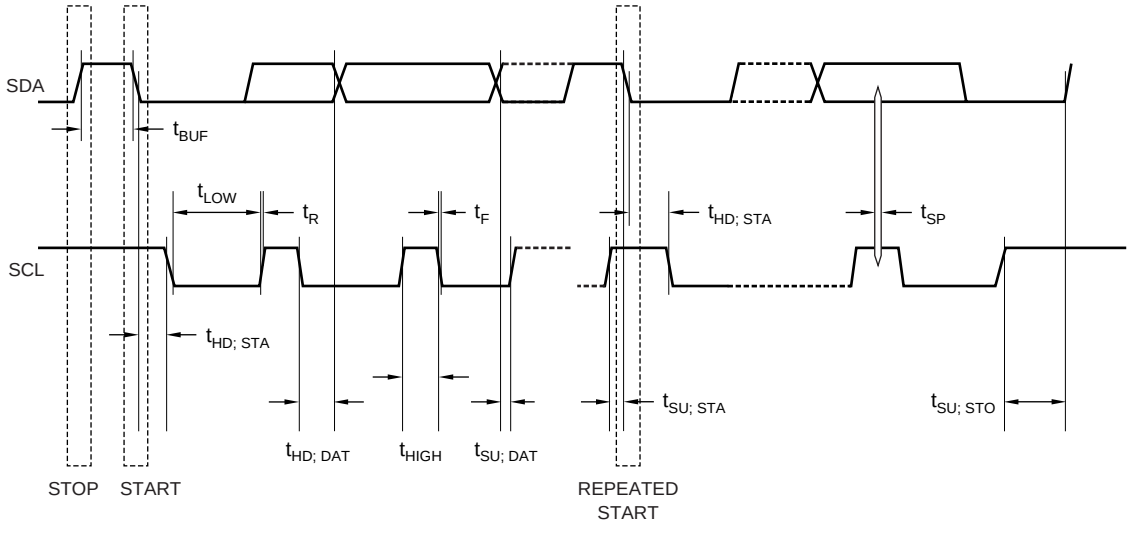
Top View **MSOP**



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V_{REF}	Reference Input, 2.5V Nominal
2	A_{IN}	Analog Input.
3	A0	Slave Address Bit 0
4	GND	Ground
5	A1	Slave Address Bit 1
6	SDA	Serial Data
7	SCL	Serial Clock
8	$+V_{DD}$	Power Supply, 3.3V Nominal

TIMING DIAGRAM



TIMING CHARACTERISTICS[1]

At T_A = –40°C to +85°C, $+V_{DD}$ = +2.7V, unless otherwise noted.

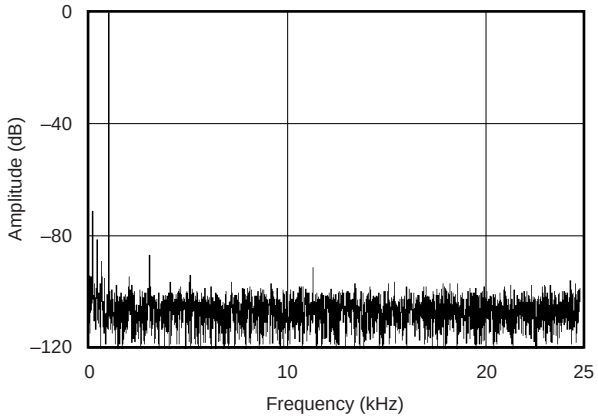
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard Mode		100	kHz
		Fast Mode		400	kHz
		High-Speed Mode, C_B = 100pF max		3.4	MHz
		High-Speed Mode, C_B = 400pF max		1.7	MHz
Bus Free Time Between a STOP and START Condition	t_{BUF}	Standard Mode	4.7		µs
		Fast Mode	1.3		µs
Hold Time (Repeated) START Condition	$t_{HD;STA}$	Standard Mode	4.0		µs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
LOW Period of the SCL Clock	t_{LOW}	Standard Mode	4.7		µs
		Fast Mode	1.3		µs
		High-Speed Mode, C_B = 100pF max[2]	160		ns
		High-Speed Mode, C_B = 400pF max[2]	320		ns
HIGH Period of the SCL Clock	t_{HIGH}	Standard Mode	4.0		µs
		Fast Mode	600		ns
		High-Speed Mode, C_B = 100pF max[2]	60		ns
		High-Speed Mode, C_B = 400pF max[2]	120		ns
Setup Time for a Repeated START Condition	$t_{SU;STA}$	Standard Mode	4.7		µs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
Data Setup Time	$t_{SU;DAT}$	Standard Mode	250		ns
		Fast Mode	100		ns
		High-Speed Mode	10		ns
Data Hold Time	$t_{HD;DAT}$	Standard Mode	0	3.45	µs
		Fast Mode	0	0.9	µs
		High-Speed Mode, C_B = 100pF max[2]	0[3]	70	ns
		High-Speed Mode, C_B = 400pF max[2]	0[3]	150	ns
Rise Time of SCL Signal	t_{RCL}	Standard Mode		1000	ns
		Fast Mode	$20 + 0.1C_B$	300	ns
		High-Speed Mode, C_B = 100pF max[2]	10	40	ns
		High-Speed Mode, C_B = 400pF max[2]	20	80	ns
Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit	t_{RCL1}	Standard Mode		1000	ns
		Fast Mode	$20 + 0.1C_B$	300	ns
		High-Speed Mode, C_B = 100pF max[2]	10	80	ns
		High-Speed Mode, C_B = 400pF max[2]	20	160	ns
Fall Time of SCL Signal	t_{FCL}	Standard Mode		300	ns
		Fast Mode	$20 + 0.1C_B$	300	ns
		High-Speed Mode, C_B = 100pF max[2]	10	40	ns
		High-Speed Mode, C_B = 400pF max[2]	20	80	ns
Rise Time of SDA Signal	t_{RDA}	Standard Mode		1000	ns
		Fast Mode	$20 + 0.1C_B$	300	ns
		High-Speed Mode, C_B = 100pF max[2]	10	80	ns
		High-Speed Mode, C_B = 400pF max[2]	20	160	ns
Fall Time of SDA Signal	t_{FDA}	Standard Mode		300	ns
		Fast Mode	$20 + 0.1C_B$	300	ns
		High-Speed Mode, C_B = 100pF max[2]	10	80	ns
		High-Speed Mode, C_B = 400pF max[2]	20	160	ns
Setup Time for STOP Condition	$t_{SU;STO}$	Standard Mode	4.0		µs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
Capacitive Load for SDA and SCL Line	C_B			400	pF
Pulse Width of Spike Suppressed	t_{SP}	Fast Mode		50	ns
		High-Speed Mode		10	ns
Noise Margin at the HIGH Level for Each Connected Device (Including Hysteresis)	V_{NH}	Standard Mode Fast Mode High-Speed Mode	$0.2V_{DD}$		V
Noise Margin at the LOW Level for Each Connected Device (Including Hysteresis)	V_{NL}	Standard Mode Fast Mode High-Speed Mode	$0.1V_{DD}$		V

NOTES: (1) All values referred to V_{IHMIN} and V_{ILMAX} levels. (2) For bus line loads C_B between 100pF and 400pF the timing parameters must be linearly interpolated. (3) A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

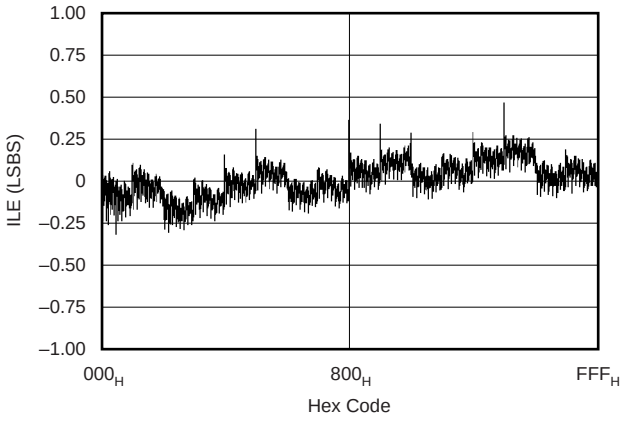
TYPICAL CHARACTERISTICS

At T_A = +25°C, $+V_{DD}$ = +2.7V, V_{REF} = External +2.5V, f_{SAMPLE} = 50kHz, unless otherwise noted.

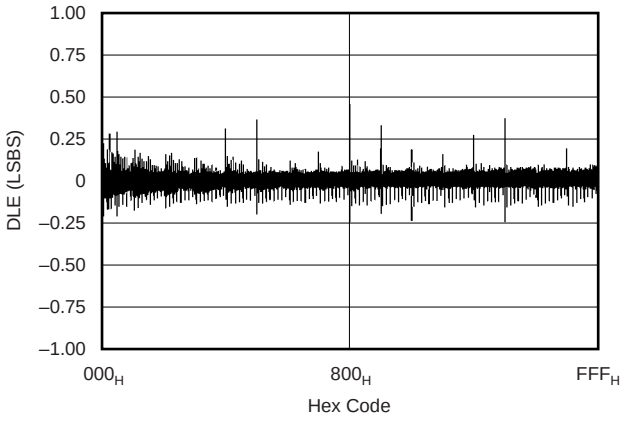
FREQUENCY SPECTRUM
(4096 Point FFT, f_{IN} = 1kHz, 0dB)



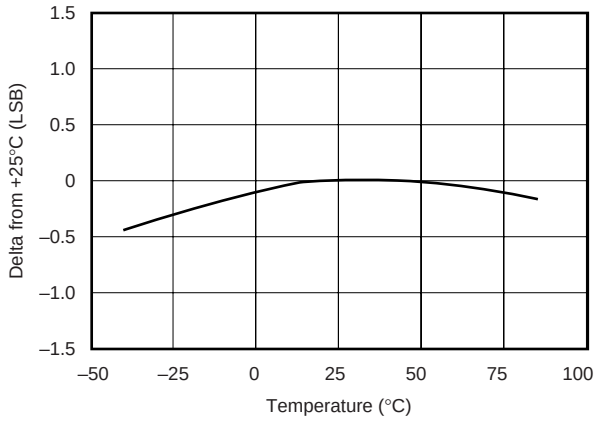
INTEGRAL LINEARITY ERROR vs CODE (+25°C)



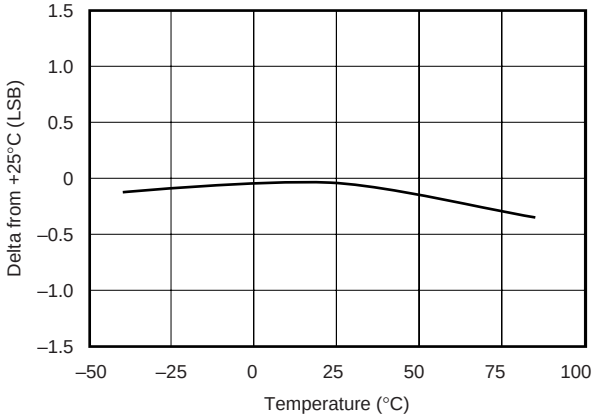
DIFFERENTIAL LINEARITY ERROR vs CODE (+25°C)



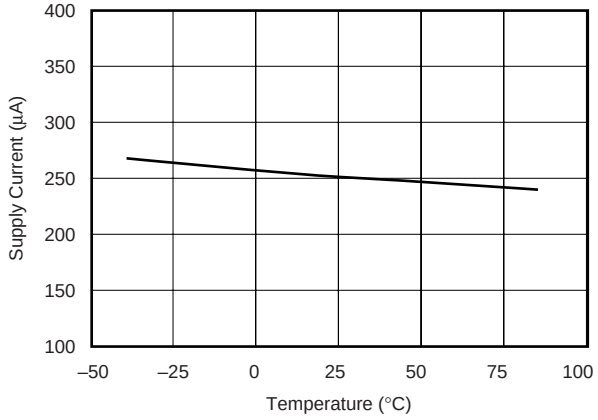
CHANGE IN OFFSET vs TEMPERATURE



CHANGE IN GAIN vs TEMPERATURE



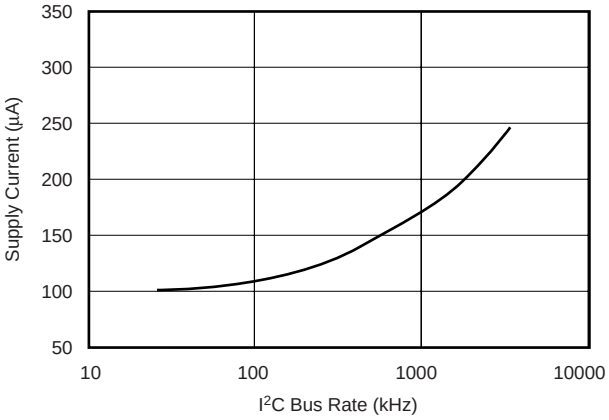
SUPPLY CURRENT vs TEMPERATURE



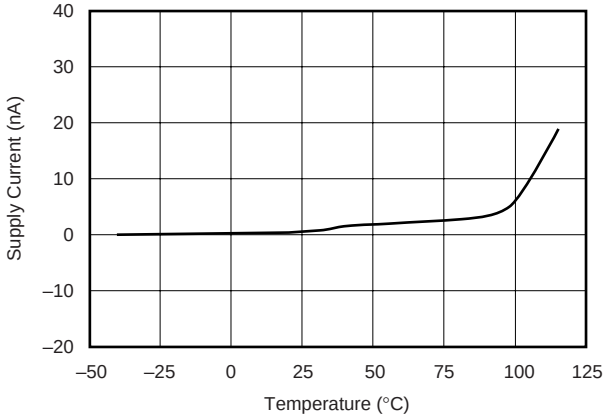
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_{DD}$ = +2.7V, V_{REF} = External +2.5V, f_{SAMPLE} = 50kHz, unless otherwise noted.

SUPPLY CURRENT vs I^2C BUS RATE



POWER DOWN SUPPLY CURRENT vs TEMPERATURE



THEORY OF OPERATION

The ADS7823 is a classic Successive Approximation Register (SAR) A/D converter. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µ CMOS process.

The ADS7823 core is controlled by an internally-generated free-running clock. When the ADS7823 is not performing conversions or being addressed, it keeps the A/D converter core powered off, and the internal clock does not operate.

The ADS7823 has an internal 4-word first-in last-out buffer (FILO) that stores the results of up to four conversions while they are waiting to be read out over the I^2C bus.

The simplified diagram of input and output for the ADS7823 is shown in Figure 1.

ANALOG INPUT

When the converter enters the hold mode, the voltage on the A_{IN} pin is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The amount of charge transfer from the analog source to the converter is a function of conversion rate.

REFERENCE INPUT

The external reference sets the analog input range. The ADS7823 will operate with a reference in the range of 50mV to V_{DD}. There are several important implications of this.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced.

The noise inherent in the converter will also appear to increase with lower LSB size. With a 2.5V reference, the internal noise of the converter typically contributes only 0.32LSB peak-to-peak of potential error to the output code. When the external reference is 50mV, the potential error contribution from the internal noise will be 50 times larger—16LSBs. The errors due to the internal noise are Gaussian in nature and can be reduced by averaging consecutive conversion results.

DIGITAL INTERFACE

The ADS7823 supports the I^2C serial bus and data transmission protocol, in all three defined modes: standard, fast, and high-speed. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver.

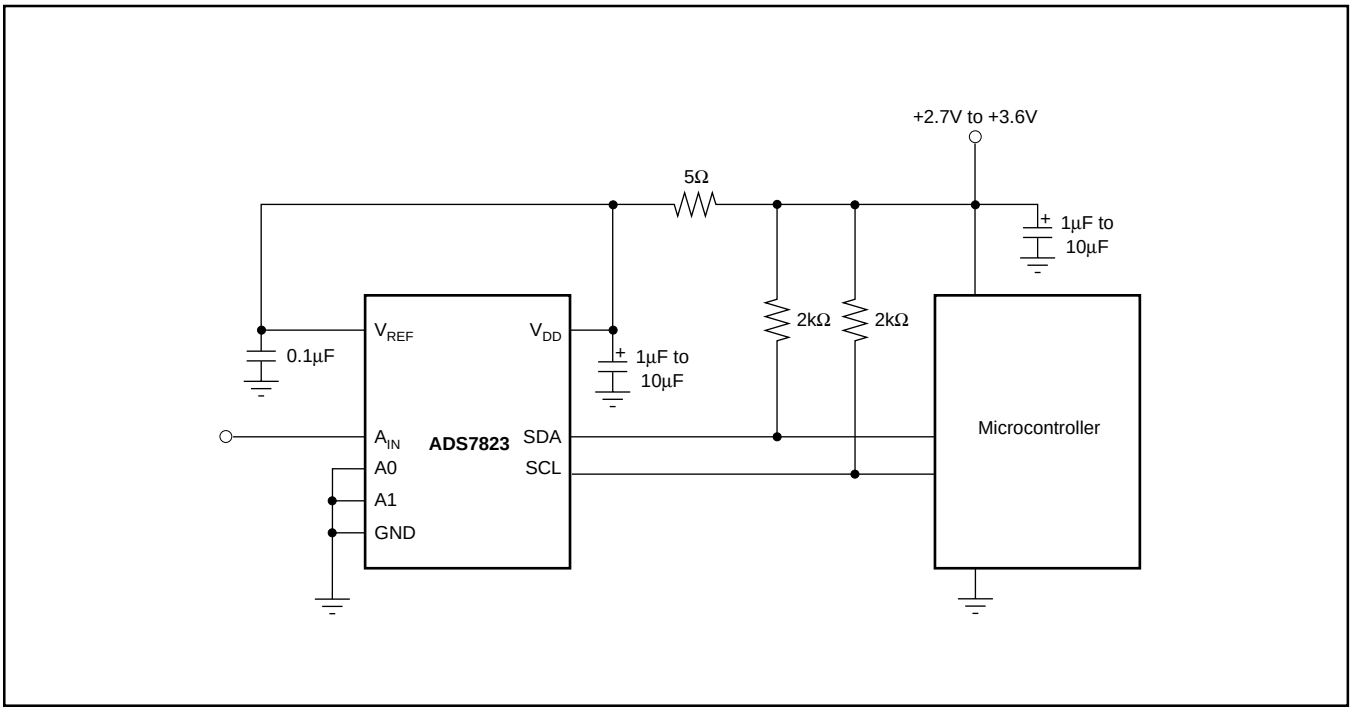


FIGURE 1. Simplified I/O of the ADS7823.

The device that controls the message is called a “master.” The devices that are controlled by the master are “slaves.” The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The ADS7823 operates as a slave on the I^2C bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (as shown in Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain HIGH.

Start Data Transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid: The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the I^2C bus specifications a standard mode (100kHz clock rate), a fast mode (400kHz clock rate), and a high-speed mode (3.4MHz clock rate) are defined. The ADS7823 works in all three modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 2 details how data transfer is accomplished on the I^2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The ADS7823 may operate in the following two modes:

- **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- **Slave Transmitter Mode:** The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the ADS7823 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

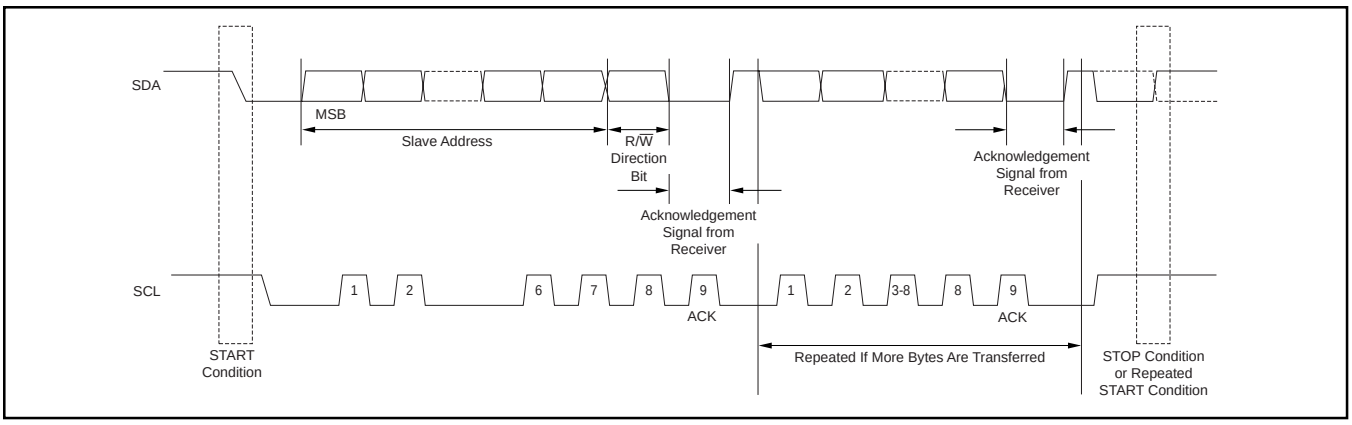


FIGURE 2. Basic Operation of the ADS7823.

ADDRESS BYTE

MSB	6	5	4	3	2	1	LSB
1	0	0	1	0	A1	A0	R/$\overline{W}$

The address byte is the first byte received following the START condition from the master device. The first five bits (MSBs) of the slave address are factory pre-set to 10010. The next two bits of the address byte are the device select bits, A1 and A0. Input pins (A1-A0) on the ADS7823 determine these two bits of the device address for a particular ADS7823. A maximum of four devices with the same pre-set code can therefore be connected on the same bus at one time.

The A1-A0 Address Inputs can be connected to V_{DD} or digital ground. The device address is set by the state of these pins upon power-up of the ADS7823.

The last bit of the address byte (R/$\overline{W}$) defines the operation to be performed. When set to a "1" a read operation is selected; when set to a "0" a write operation is selected. Following the START condition the ADS7823 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving the 10010 code, the appropriate device select bits, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

COMMAND BYTE

MSB	6	5	4	3	2	1	LSB
0	0	0	X	X	X	X	X

The ADS7823 operating mode is determined by a command byte.

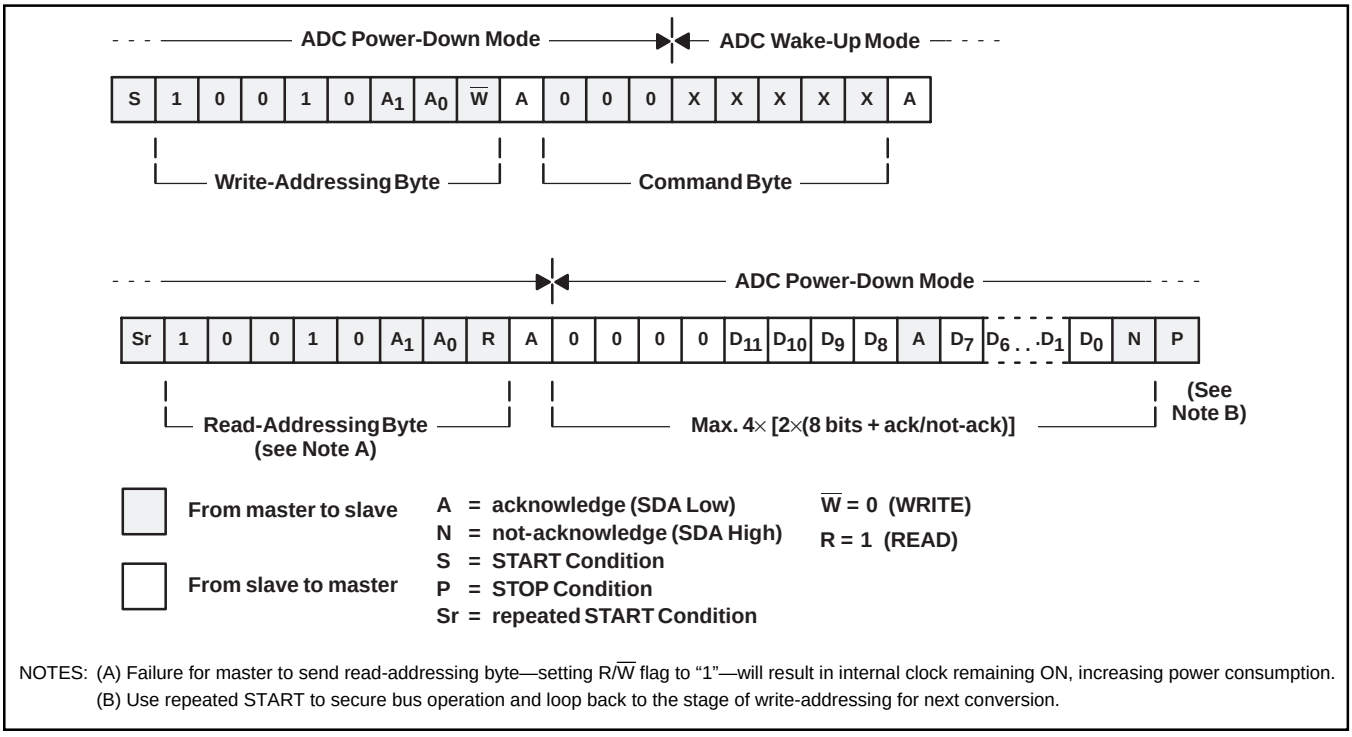
The ADS7823 command byte simply consists of three zeros in the most significant bits, while the remaining 5 bits are don't cares.

INITIATING CONVERSION

Provided the master has write-addressed it, the ADS7823 turns on the A/D converter section and begins conversions when it receives bit 5 of the command byte shown in the Command Byte. If the command byte is correct, the ADS7823 will return an ACK condition.

The converter will ignore any wrong command byte (that is, setting any of the top three MSBs to 1), remain in the A/D converter power-down mode, and reset the internal 4-word stack.

The ADS7823 will ignore a second valid command byte if two valid commands are issued consecutively. The ADS7823 will respond with a not-acknowledge, and will go to the A/D converter power-down mode after the responded not-acknowledge.



NOTES: (A) Failure for master to send read-addressing byte—setting R/$\overline{W}$ flag to "1"—will result in internal clock remaining ON, increasing power consumption.
(B) Use repeated START to secure bus operation and loop back to the stage of write-addressing for next conversion.

FIGURE 3. Typical Read Sequence in F/S Mode.

READING DATA

Data can be read from the ADS7823 by read-addressing the part (LSB of address byte set to 1) and receiving the transmitted bytes. Converted data can only be read from the ADS7823 once a conversion has been initiated as described in the preceding section.

Each 12-bit data word is returned in two bytes, as shown below, where D11 is the MSB of the data word, and D0 is the LSB. Byte 0 is sent first, followed by Byte 1.

	MSB	6	5	4	3	2	1	LSB
BYTE0	0	0	0	0	D11	D10	D9	D8
BYTE1	D7	D6	D5	D4	D3	D2	D1	D0

READING IN F/S MODE

In Fast and Standard (F/S) modes, the A/D converter has time to make four complete conversions between the reception of bit 5 of the command byte and the complete reception of the read address, even when operating in Fast mode.

Because the ADS7823 can perform these conversions much faster than they can be transmitted in F/S mode, data is stored in a four-level FILO. During the read operation, the A/D converter is powered down and the contents of the stack are read out one by one in the correct order.

A typical transfer sequence for reading four words of data in F/S mode (see Figure 3). Note that the master sends a not-acknowledge after the fourth data word has been read. This tells the ADS7823 that no further reads will be performed. No more than four data words should be read at a time; further reads will return undefined data.

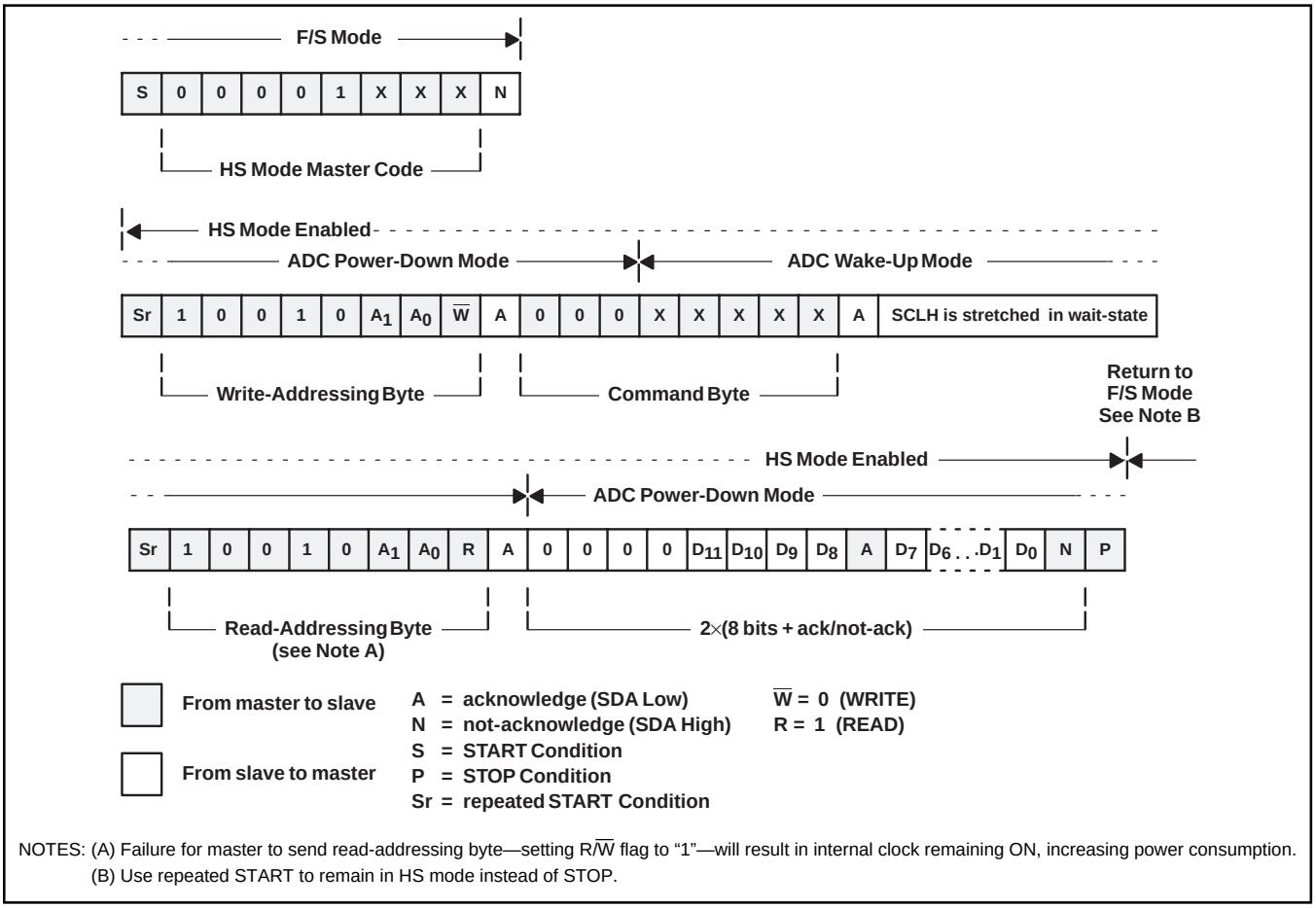
Although a STOP condition is shown at the end of the figure, it is permissible to issue a repeated START; this will have the same effect.

READING IN HS MODE

High Speed (HS) mode is fast enough that codes can be read out one at a time, without employing the FILO. In HS mode there is not enough time for a single conversion to complete between the reception of command bit 5 and the read address byte, so the ADS7823 stretches the clock after the command byte has been fully received, holding it LOW until the conversion is complete.

A typical read sequence for HS mode is shown in Figure 4. Included in the read sequence is the shift from F/S to HS modes. It may be desirable to remain in HS mode after reading a code; to do this, issue a repeated START instead of a STOP at the end of the read sequence, since a STOP causes the part to return to F/S mode.

It is very important not to read more than one code at a time from the ADS7823 during HS mode. If codes are read out more than one at a time, as in F/S mode, the results for all codes (except the first) are undefined, and the data stream will be corrupt.



NOTES: (A) Failure for master to send read-addressing byte—setting R/$\overline{W}$ flag to "1"—will result in internal clock remaining ON, increasing power consumption.
(B) Use repeated START to remain in HS mode instead of STOP.

FIGURE 4. Typical Read Sequence in HS Mode.

TERMINATING A CONVERSION

There are three methods to terminate the conversion of the A/D converter in the ADS7823 after the master initiates conversion:

1) In normal operation sequence (see Figures 3 and 4). The conversion is terminated after the read-addressing has been received.
2) A STOP condition will always terminate a conversion. It will also terminate the HS mode returning the ADS7823 to the F/S mode.
3) A not-acknowledge by the ADS7823 following a second command byte will end a conversion.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7823 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an "n-bit" SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices.

With this in mind, power to the ADS7823 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. A 1µF to 10µF capacitor may also be needed if the impedance of the connection between $+V_{DD}$ and the power supply is high.

The ADS7823 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7823E/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B23	Samples
ADS7823E/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		B23	Samples
ADS7823EB/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		B23	Samples
ADS7823EB/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		B23	Samples
ADS7823EB/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		B23	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

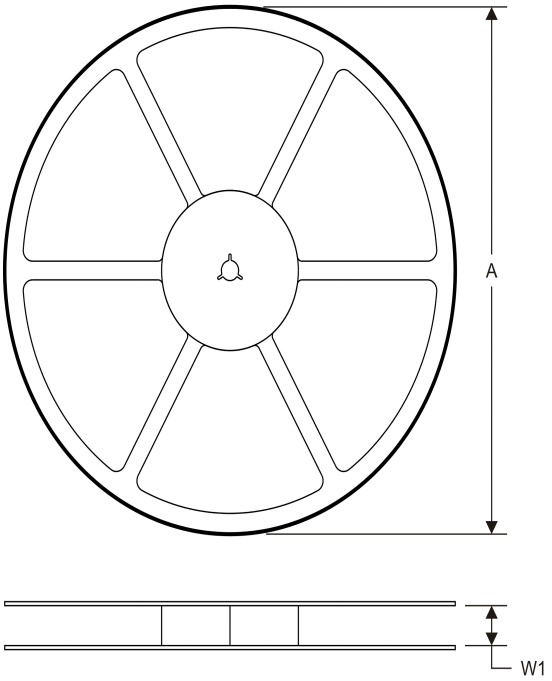
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

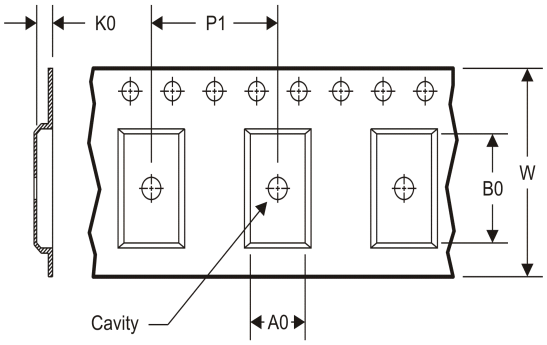
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



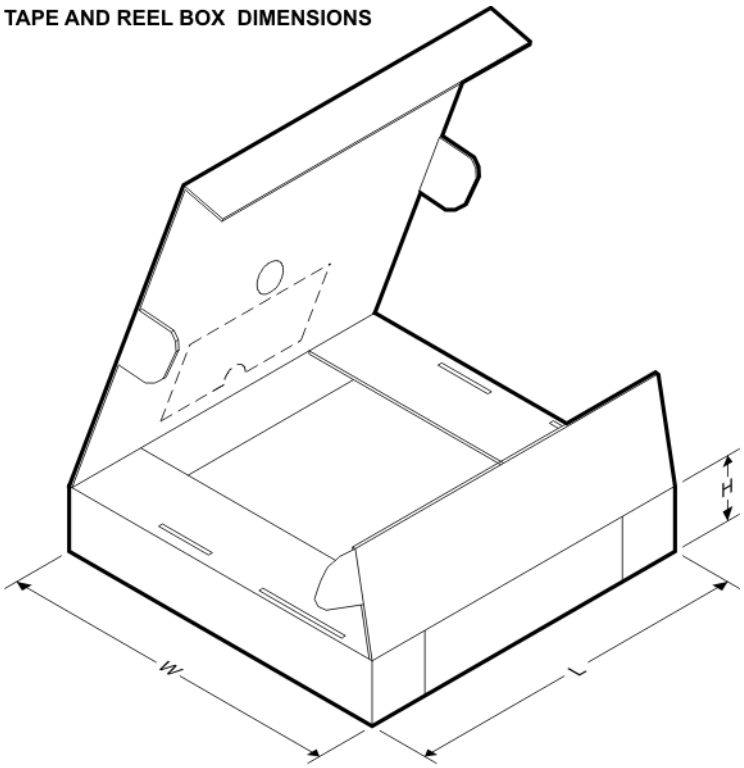
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7823E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7823E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7823EB/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7823EB/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

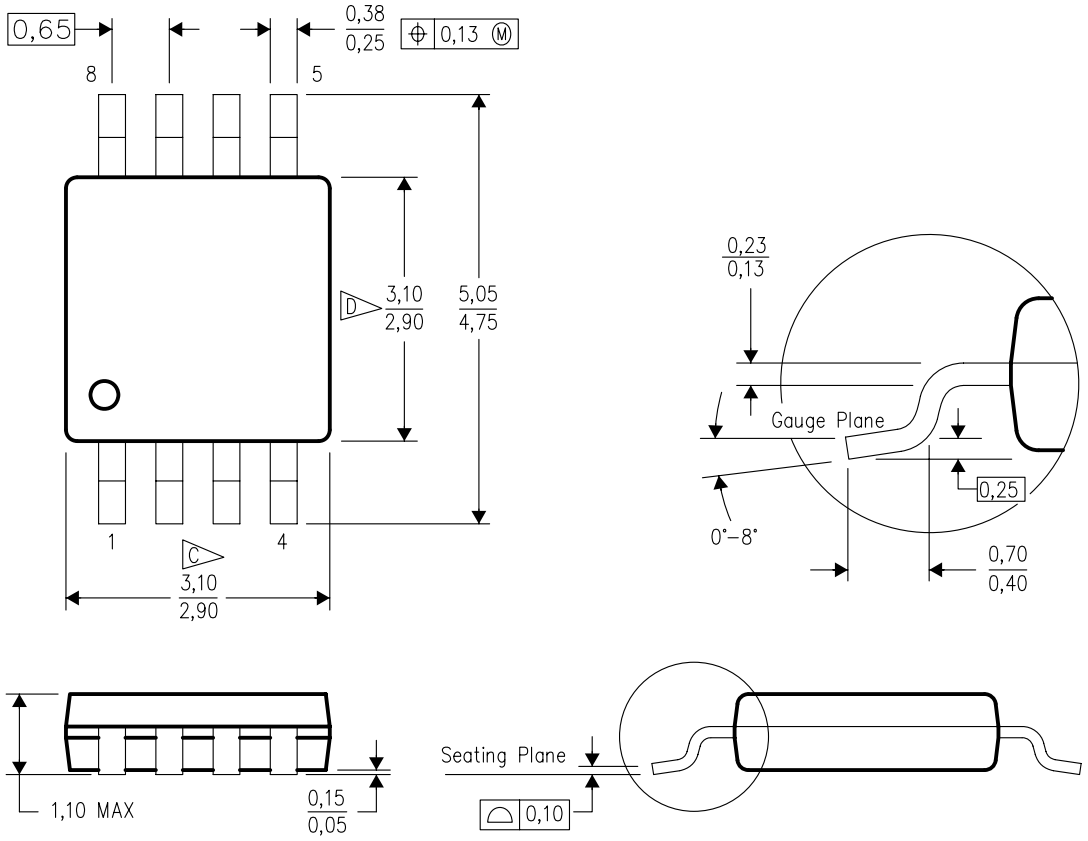
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7823E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS7823E/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
ADS7823EB/250	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS7823EB/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0

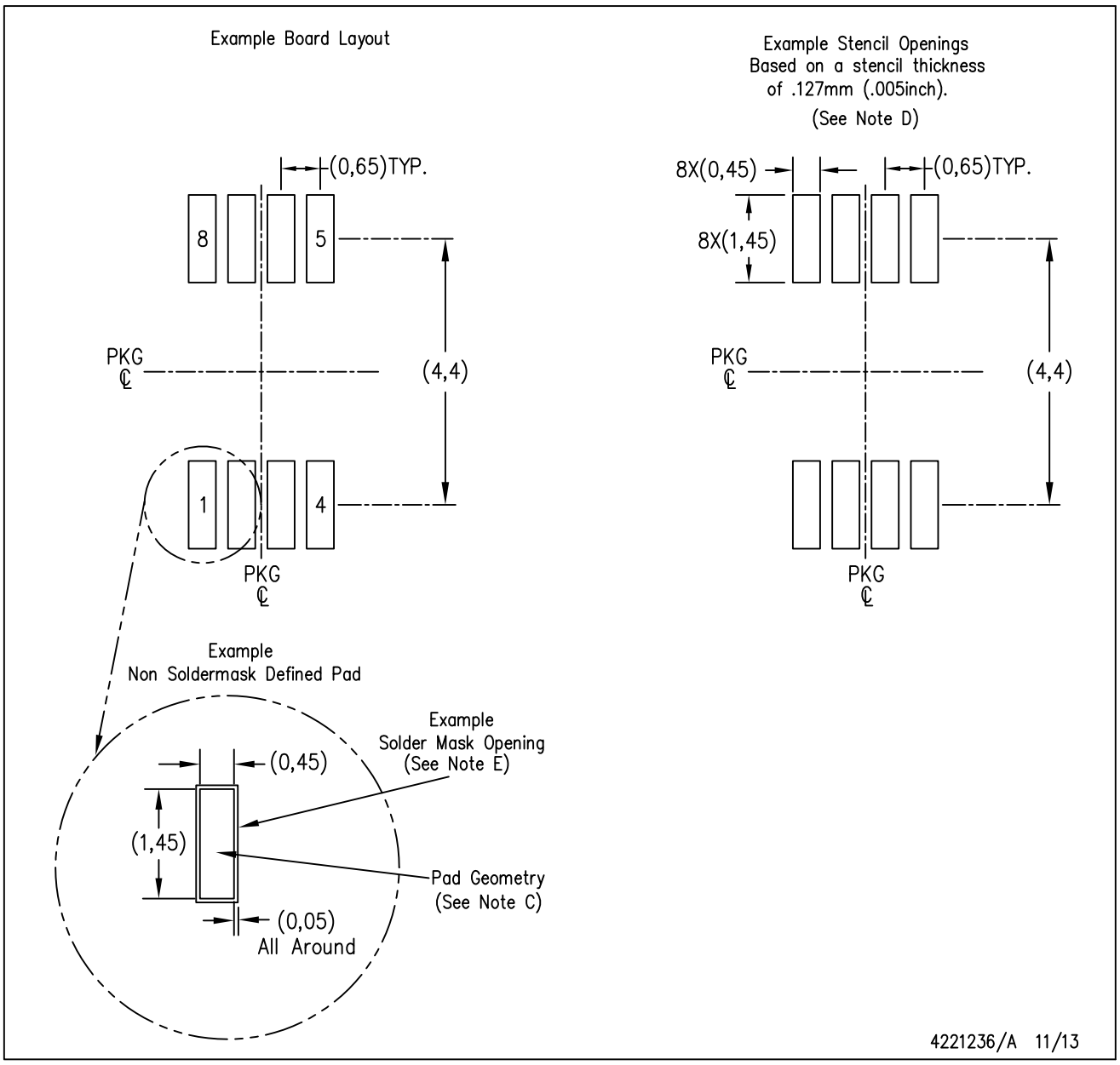
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View ADS7823E/2K5 on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management