THE DATASHEET OF

IXDN409SI

IXDD409PI / 409SI / 409YI / 409CI IXDI409PI / 409SI / 409YI / 409CI IXDN409PI / 409SI / 409YI / 409CI

9 Ampere Low-Side Ultrafast MOSFET Driver

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes.
- Latch Up Protected
- High Peak Output Current: 9A Peak
- Operates from 4.5V to 35V
- -55° C to 125° C Extended Operating Temperature Standard
- Ability to Disable Output under Faults
- High Capacitive Load Drive Capability: 2500pF in <15ns
- Matched Rise And Fall Times
- Low Propagation Delay Time
- Low Output Impedance
- Low Supply Current

Applications

- Driving MOSFETs and IGBTs
- Motor Controls
- Line Drivers
- Pulse Generators
- Local Power ON/OFF Switch
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Pulse Transformer Driver
- Limiting di/dt under Short Circuit
- Class D Switching Amplifiers

General Description

The IXDD409/IXDI409/IXDN409 are high speed high current gate drivers specifically designed to drive the largest MOSFETs and IGBTs to their minimum switching time and maximum practical frequency limits. The IXDD409/IXDI409/IXDN409 can source and sink 9A of peak current while producing voltage rise and fall times of less than 30ns. The input of the drivers are compatible with TTL or CMOS and are fully immune to latch up over the entire operating range. Designed with small internal delays, cross conduction/current shoot-through is virtually eliminated in the IXDD409/IXDI409/IXDN409. Their features and wide safety margin in operating voltage and power make the drivers unmatched in performance and value.

The IXDD409 incorporates a unique ability to disable the output under fault conditions. When a logical low is forced into the Enable input, both final output stage MOSFETs (NMOS and PMOS) are turned off. As a result, the output of the IXDD409 enters a tristate mode and achieves a Soft Turn-Off of the MOSFET/IGBT when a short circuit is detected. This helps prevent damage that could occur to the MOSFET/IGBT if it were to be switched off abruptly due to a dv/dt over-voltage transient.

The IXDN409 is configured as a non-inverting gate driver, and the IXDI409 is an inverting gate driver.

The IXDD409/IXDI409/IXDN409 are available in the standard 8-pin P-DIP (PI), SOIC-8 (SI), 5-pin TO-220 (CI) and in the TO-263 (YI) surface-mount packages.

Figure 1A - IXDD409 (Non Inverting With Enable) Diagram

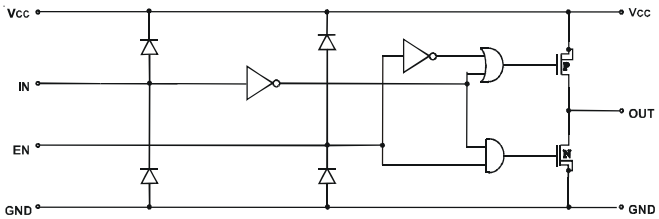


Figure 1B - IXDN409 (Non-Inverting) Diagram

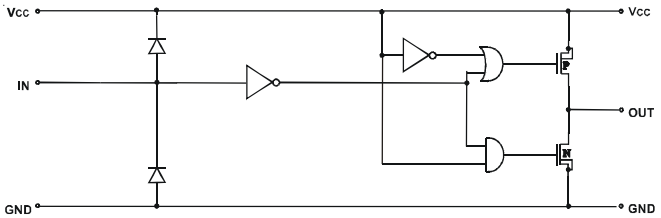
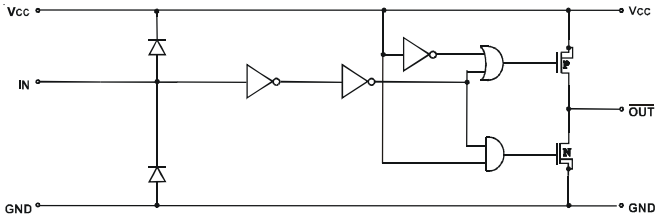


Figure 1C - IXDI409 (Inverting) Diagram



Ordering Information

Part Number	Package Type	Temp. Range	Configuration
IXDD409PI	8-Pin PDIP	-55°C to +125°C	Non Inverting With Enable Line
IXDD409SI	8-Pin SOIC		
IXDD409YI	5-Pin TO-263		
IXDD409CI	5-Pin TO-220		
IXDI409PI	8-Pin PDIP	-55°C to +125°C	Inverting
IXDI409SI	8-Pin SOIC		
IXDI409YI	5-Pin TO-263		
IXDI409CI	5-Pin TO-220		
IXDN409PI	8-Pin PDIP	-55°C to +125°C	Non Inverting
IXDN409SI	8-Pin SOIC		
IXDN409YI	5-Pin TO-263		
IXDN409CI	5-Pin TO-220		

Absolute Maximum Ratings (Note 1)

Parameter	Value
Supply Voltage	40V
All Other Pins	-0.3V to V_{CC} + 0.3V
Junction Temperature	150°C
Storage Temperature	-55°C to 150°C
Soldering Lead Temperature (10s)	300°C
Tab Temperature (10s)	260°C

Thermal Resistance (Junction to Case) (θ_{JC})

8 Pin PDIP (PI)	70 K/W
8 Pin SOIC (SI)	10 K/W
TO-220 (CI), TO-263 (YI)	2.5 K/W

Operating Ratings

Parameter	Value
Operating Temperature Range	-55 °C to 125 °C
Thermal Resistance (To Ambient)	
8 Pin PDIP (PI) (θ_{JA})	120 K/W
8 Pin SOIC (SIA)	110 K/W
TO-220 (CI)	50 K/W
θ_{JA} with heat sink **	
Heat sink area of 1 cm^2	
8 Pin SOIC	95 K/W
TO-263	95 K/W
Heat sink area of 3 cm^2	
8 Pin SOIC	85 K/W
TO-263	85 K/W

** Device soldered to metal back pane. Heat sink area is 1 oz. copper on 1 side of 0.06" thick FR4 PC board.

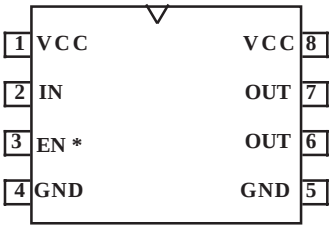
Electrical Characteristics

Unless otherwise noted, T_A = 25 °C, 4.5V ≤ V_{CC} ≤ 35V .
All voltage measurements with respect to GND. IXDD409 configured as described in *Test Conditions*.

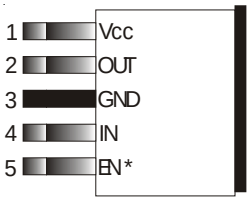
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage	4.5V ≤ V_{CC} ≤ 18V	3.5			V
V_{IL}	Low input voltage	4.5V ≤ V_{CC} ≤ 18V			0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	0V ≤ V_{IN} ≤ V_{CC}	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output high	I_{OUT} = 10mA, V_{CC} = 18V		0.8	1.5	Ω
R_{OL}	Output resistance @ Output Low	I_{OUT} = 10mA, V_{CC} = 18V		0.8	1.5	Ω
I_{PEAK}	Peak output current	V_{CC} is 18V		9		A
I_{DC}	Continuous output current	Limited by package power dissipation			2	A
V_{EN}	Enable voltage range	IXDD409 Only	- .3		Vcc + 0.3	V
V_{ENH}	High En Input Voltage	IXDD409 Only	2/3 Vcc			V
V_{ENL}	Low En Input Voltage	IXDD409 Only			1/3 Vcc	V
t_R	Rise time	C_L=2500pF Vcc=18V	8	10	15	ns
t_F	Fall time	C_L=2500pF Vcc=18V	8	10	15	ns
t_{ONDLY}	On-time propagation delay	C_L=2500pF Vcc=18V	33	36	40	ns
t_{OFFDLY}	Off-time propagation delay	C_L=2500pF Vcc=18V	31	33	36	ns
t_{ENOH}	Enable to output high delay time	IXDD409 Only, Vcc=18V			52	ns
t_{DOLD}	Disable to output low Disable delay time	IXDD409 Only, Vcc=18V			30	ns
V_{CC}	Power supply voltage		4.5	18	35	V
I_{CC}	Power supply current	V_{IN} = 3.5V V_{IN} = 0V V_{IN} = + V_{CC}		1 0	3 10 10	mA µA µA

Specifications Subject To Change Without Notice

Pin Configurations



8 PIN DIP (PI)
SO8 (SI)



TO220 (CI)
TO263 (YI)

Pin Description

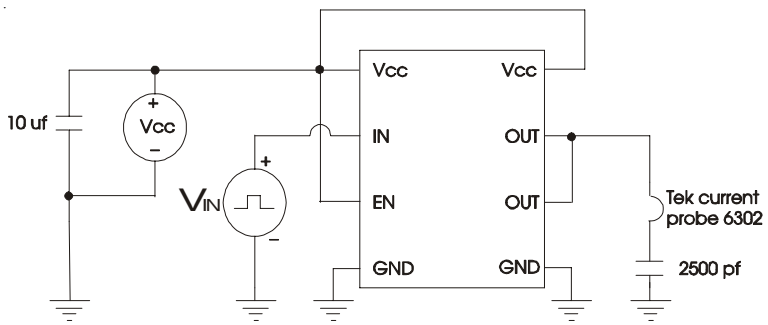
SYMBOL	FUNCTION	DESCRIPTION
VCC	Supply Voltage	Positive power-supply voltage input. This pin provides power to the entire chip. The range for this voltage is from 4.5V to 35V.
IN	Input	Input signal-TTL or CMOS compatible.
EN *	Enable	The system enable pin. This pin, when driven low, disables the chip, forcing high impedance state to the output (IXDD409 Only).
OUT	Output	Driver Output. For application purposes, this pin is connected, through a resistor, to Gate of a MOSFET/IGBT.
GND	Ground	The system ground pin. Internally connected to all circuitry, this pin provides ground reference for the entire chip. This pin should be connected to a low noise analog ground plane for optimum performance.

* This pin is used only on the IXDD409, and is N/C on the IXDI409 and IXDN409.

Note 1: Operating the device beyond parameters with listed "absolute maximum ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling this component.

Figure 2 - Characteristics Test Diagram



Typical Performance Characteristics

Fig. 3 Rise Times vs. Supply Voltage

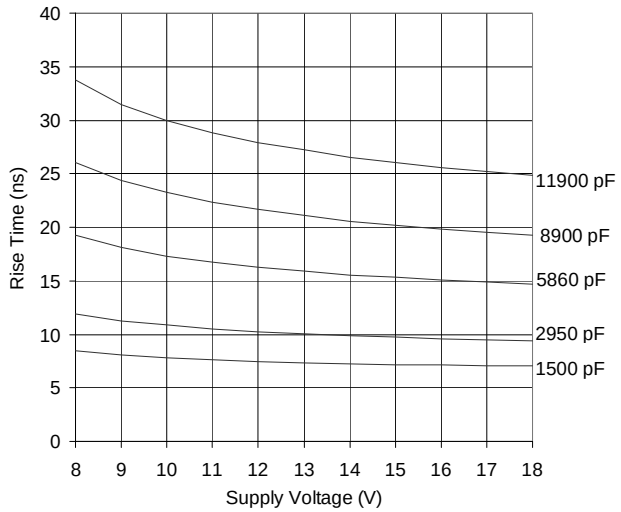


Fig. 4 Fall Times vs. Supply Voltage

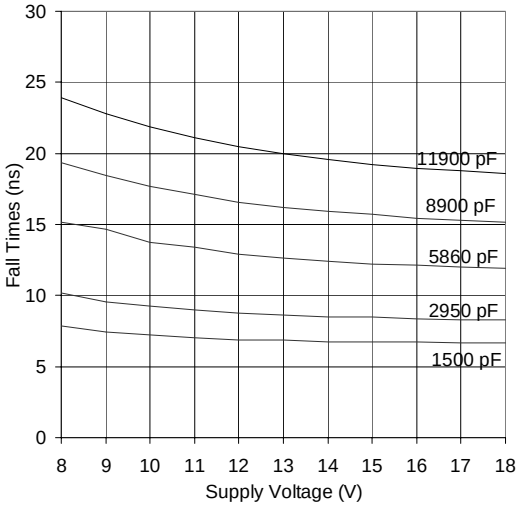


Fig. 5 Rise And Fall Times vs. Temperature
CL=2500pF, Vcc=18V

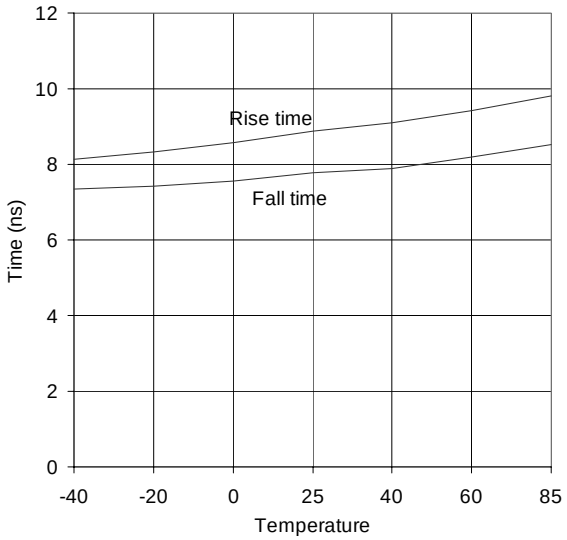


Fig. 6 Rise Time vs. Load Capacitance

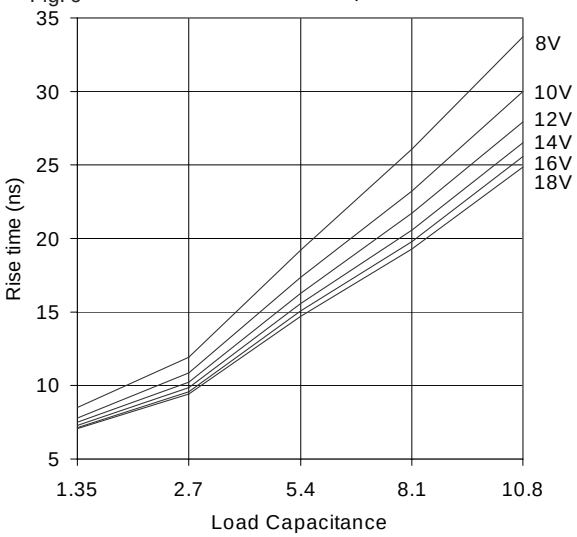


Fig. 7 Fall Time vs. Load Capacitance

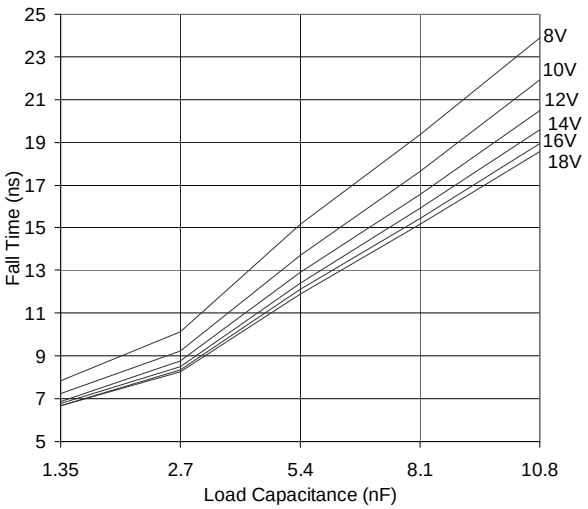


Fig. 8 Max / Min Input vs. Temperature

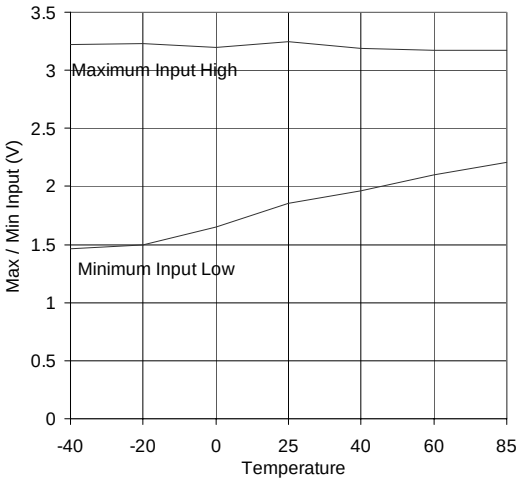


Fig. 9 Supply Current vs. Load Capacitance
Vcc = 18V

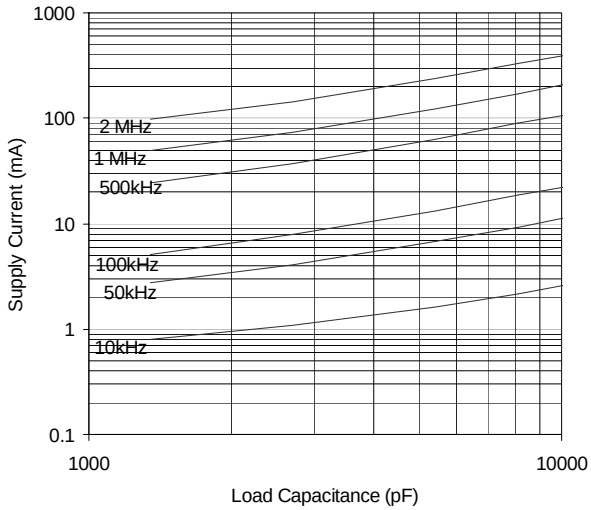


Fig. 10 Supply Current vs. Frequency
Vcc = 18V

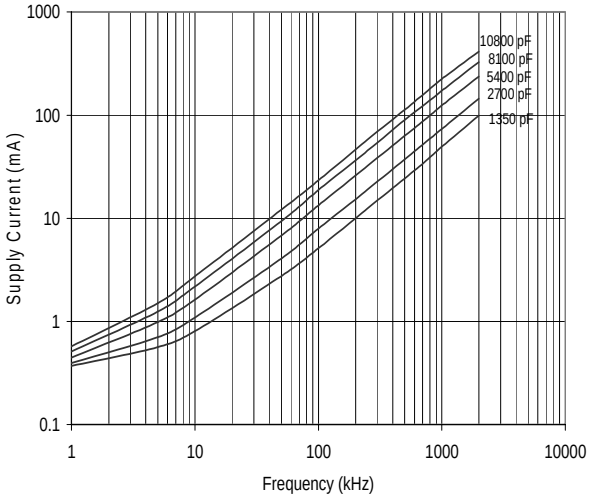


Fig. 11 Supply Current vs. Load Capacitance
Vcc = 12V

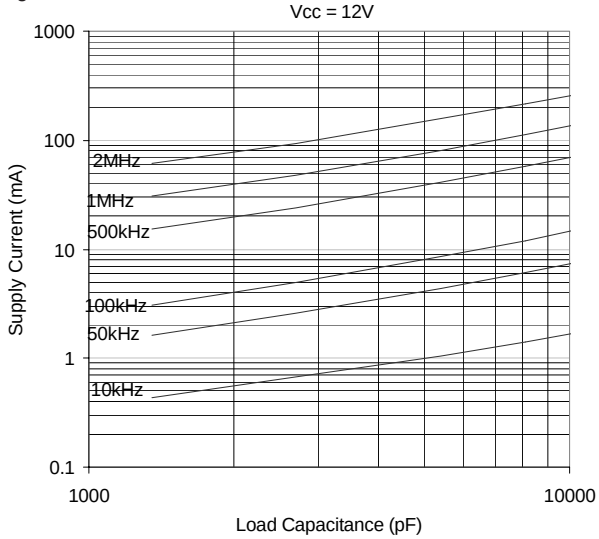


Fig. 12 Supply Current vs. Frequency
Vcc = 12V

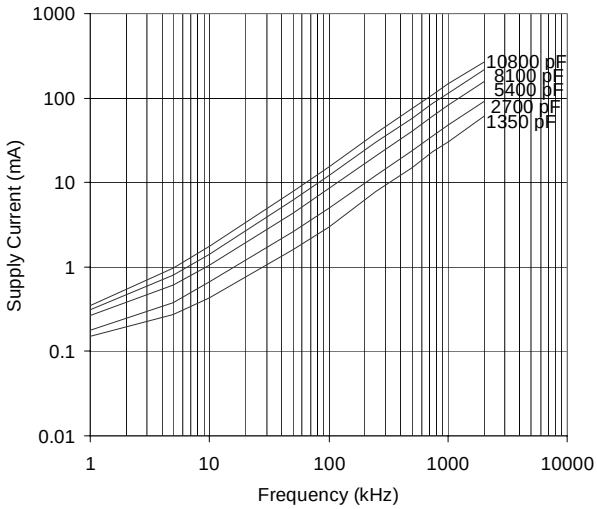


Fig. 13 Supply Current vs. Load Capacitance
Vcc = 8V

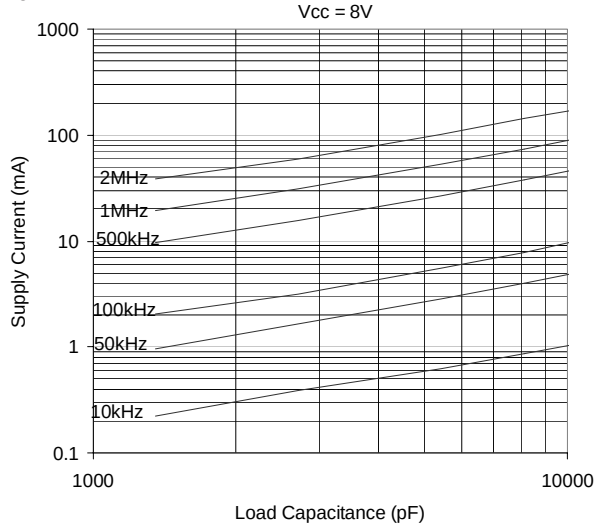


Fig. 14 Supply Current vs. Frequency
Vcc = 8V

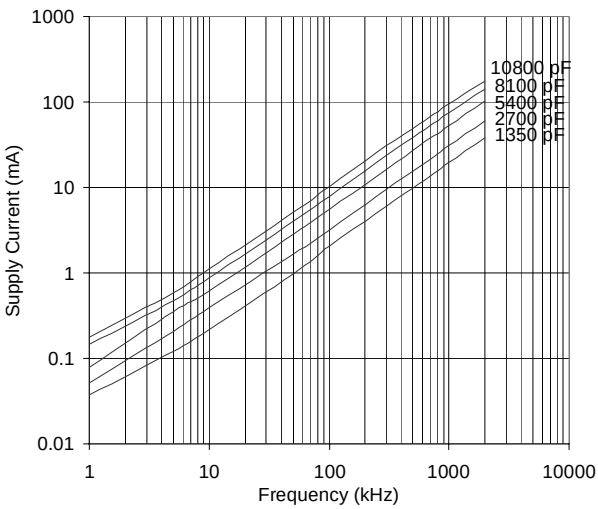


Fig. 15 Propagation Delay vs. Supply Voltage

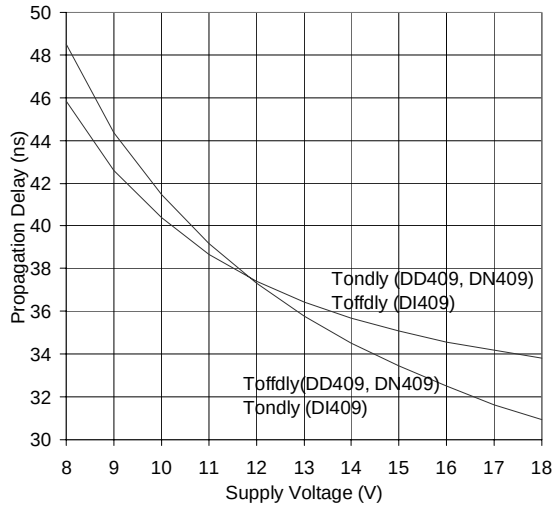


Fig. 16 Propagation Delay vs. Input Voltage

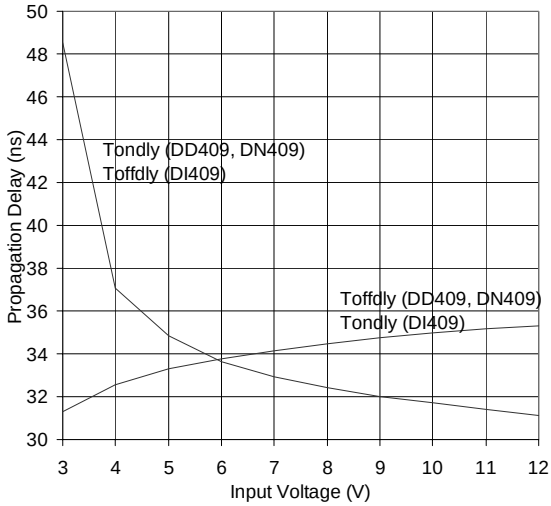


Fig. 17 Propagation Delay Times vs. Junction Temperature

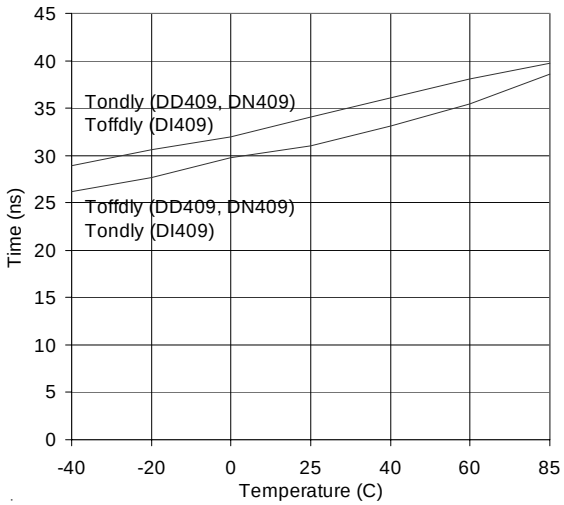


Fig. 18 Quiescent Supply Current vs. Junction Temperature
Vcc=18v Vin=5v@1kHz

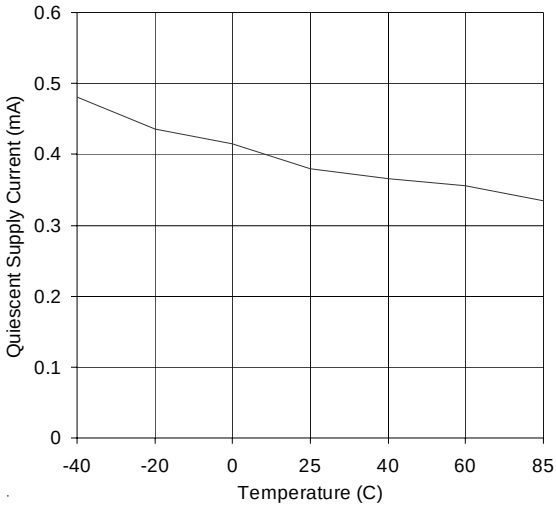


Fig. 19 Vcc vs. P Channel Peak Output Current
CL = 10 nF

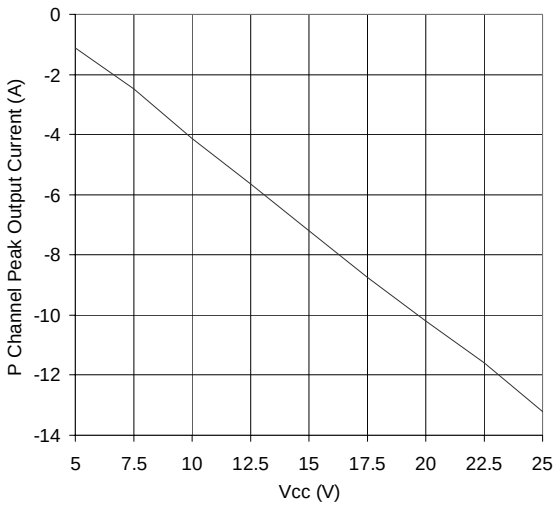


Fig. 20 Vcc vs. N Channel Peak Output Current
CL=10 nF

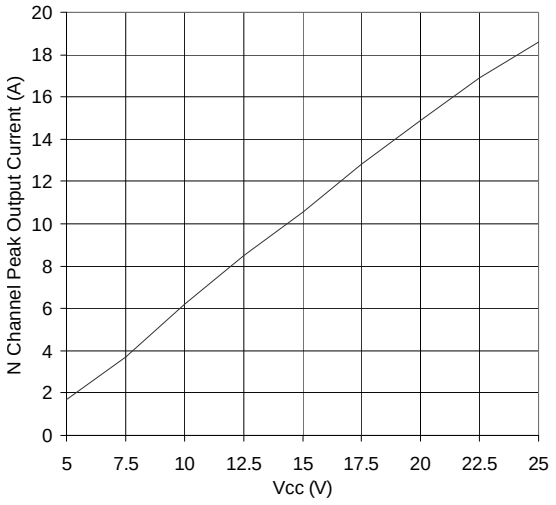


Fig. 21 P Channel Output Current vs. Temperature
Vcc = 18V CL = 10 nF

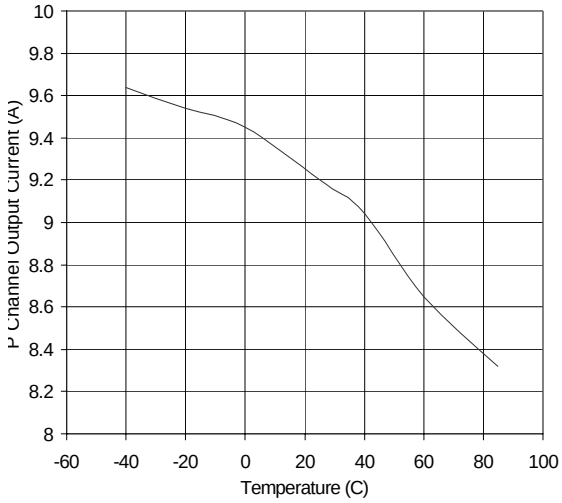


Fig. 22 N Channel Peak Ouput Current vs. Temperature
Vcc = 18V CL = 10 nF

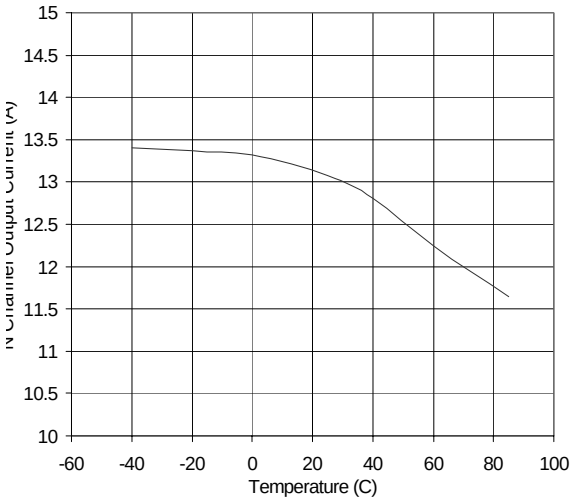


Fig. 23 High State Output Resistance vs. Supply Voltage

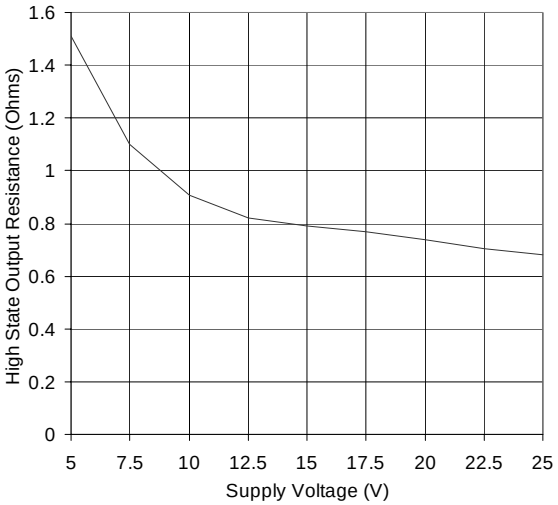


Fig. 24 Low State Output Resistance vs. Supply Voltage

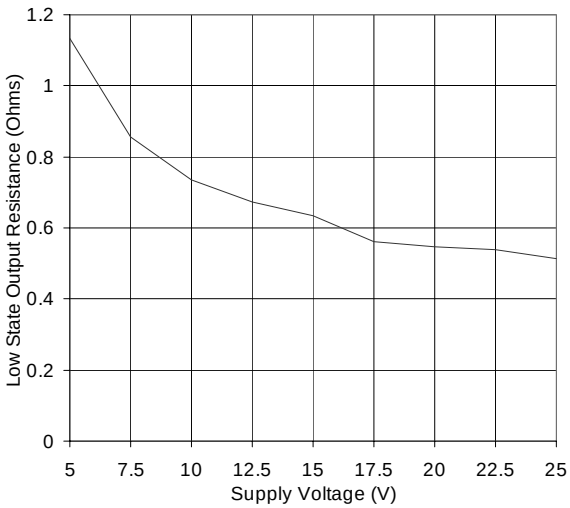
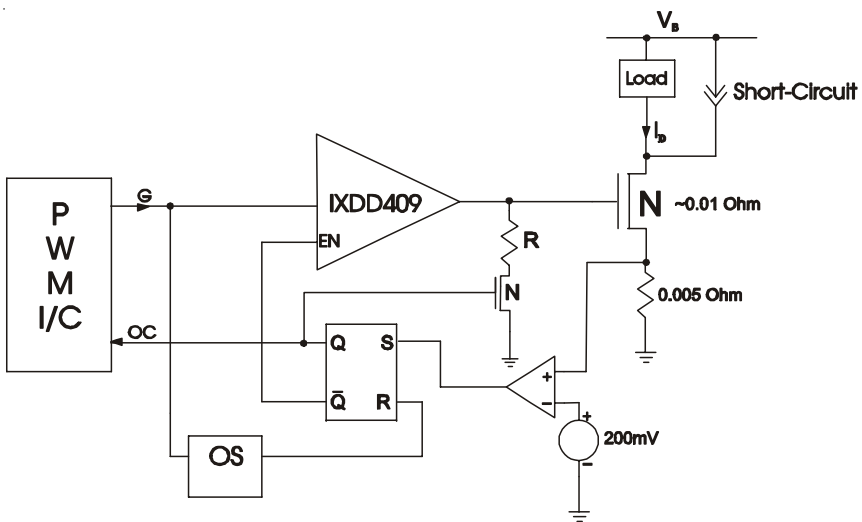


Figure 25 - Typical Application Short Circuit di/dt Limit



APPLICATIONS INFORMATION

Short Circuit di/dt Limit

A short circuit in a high-power MOSFET module such as the VM0580-02F, (580A, 200V), as shown in Figure 25, can cause the current through the module to flow in excess of 1500A for 10µs or more prior to self-destruction due to thermal runaway. For this reason, some protection circuitry is needed to turn off the MOSFET module. However, if the module is switched off too fast, there is a danger of voltage transients occuring on the drain due to Ldi/dt, (where L represents total inductance in series with drain). If these voltage transients exceed the MOSFET's voltage rating, this can cause an avalanche breakdown.

The IXDD409 has the unique capability to softly switch off the high-power MOSFET module, significantly reducing these Ldi/dt transients.

Thus, the IXDD409 helps to prevent device destruction from *both* dangers; over-current, and avalanche breakdown due to di/dt induced over-voltage transients.

The IXDD409 is designed to not only provide ±9A under normal conditions, but also to allow it's output to go into a high impedance state. This permits the IXDD409 output to control a separate weak pull-down circuit during detected overcurrent shutdown conditions to limit and separately control d_{VGS}/dt gate turnoff. This circuit is shown in Figure 26.

Referring to Figure 26, the protection circuitry should include a comparator, whose positive input is connected to the source of the VM0580-02. A low pass filter should be added to the input of the comparator to eliminate any glitches in voltage caused by the inductance of the wire connecting the source resistor to ground. (Those glitches might cause false triggering of the comparator).

The comparator's output should be connected to a SRFF(Set Reset Flip Flop). The flip-flop controls both the Enable signal, and the low power MOSFET gate. Please note that CMOS 4000-series devices operate with a V_{CC} range from 3 to 15 VDC, (with 18 VDC being the maximum allowable limit).

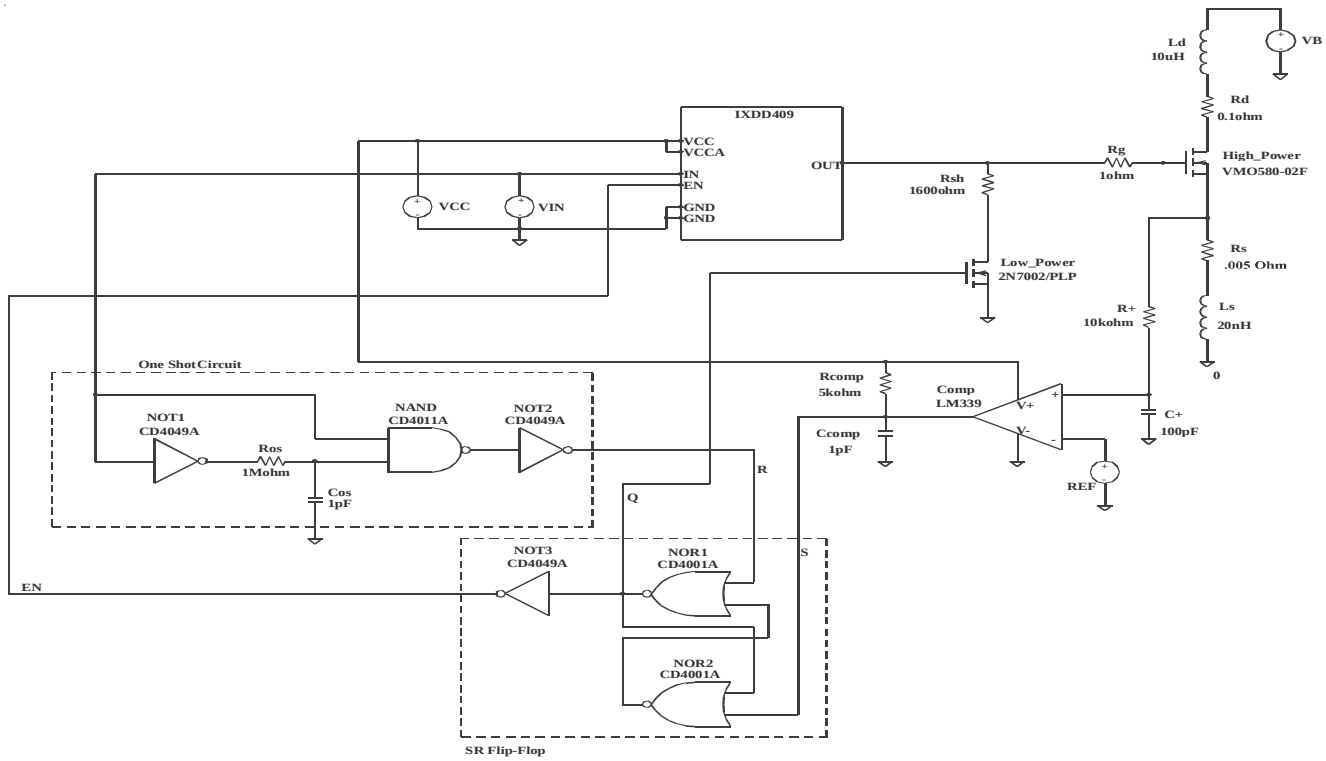
A low power MOSFET, such as the 2N7000, in series with a resistor, will enable the VMO580-02F gate voltage to drop gradually. The resistor should be chosen so that the RC time constant will be 100us, where "C" is the Miller capacitance of the VMO580-02F.

For resuming normal operation, a Reset signal is needed at the SRFF's input to enable the IXDD409 again. This Reset can be generated by connecting a One Shot circuit between the IXDD409 Input signal and the SRFF restart input. The One Shot will create a pulse on the rise of the IXDD409 input, and this pulse will reset the SRFF outputs to normal operation.

When a short circuit occurs, the voltage drop across the low-value, current-sensing resistor, (Rs=0.005 Ohm), connected between the MOSFET Source and ground, increases. This triggers the comparator at a preset level. The SRFF drives a low input into the Enable pin disabling the IXDD409 output. The SRFF also turns on the low power MOSFET, (2N7000).

In this way, the high-power MOSFET module is softly turned off by the IXDD409, preventing its destruction.

Figure 26 - Application Test Diagram



Supply Bypassing and Grounding Practices, Output Lead inductance

When designing a circuit to drive a high speed MOSFET utilizing the IXDD409/IXDI409/IXDN409, it is very important to keep certain design criteria in mind, in order to optimize performance of the driver. Particular attention needs to be paid to **Supply Bypassing**, **Grounding**, and minimizing the **Output Lead Inductance**.

Say, for example, we are using the IXDD409 to charge a 5000pF capacitive load from 0 to 25 volts in 25ns…

Using the formula: I= ΔV C / Δt, where ΔV=25V C=5000pF & Δt=25ns we can determine that to charge 5000pF to 25 volts in 25ns will take a constant current of 5A. (In reality, the charging current won't be constant, and will peak somewhere around 8A).

SUPPLY BYPASSING

In order for our design to turn the load on properly, the IXDD409 must be able to draw this 5A of current from the power supply in the 25ns. This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is a magnitude larger than the load capacitance. Usually, this would be achieved by placing two different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected, low inductance, low resistance, high-pulse current-service capacitors). Lead lengths may radiate at high frequency due to inductance, so care should be taken to keep the lengths of the leads between these bypass capacitors and the IXDD409 to an absolute minimum.

GROUNDING

In order for the design to turn the load off properly, the IXDD409 must be able to drain this 5A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the IXDD409 and it's load. Path #2 is between the IXDD409 and it's power supply. Path #3 is between the IXDD409 and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical. In addition, every effort should be made to keep these three ground paths distinctly separate. Otherwise, (for instance), the returning ground current from the load may develop a voltage that would have a detrimental effect on the logic line driving the IXDD409.

OUTPUT LEAD INDUCTANCE

Of equal importance to Supply Bypassing and Grounding are issues related to the Output Lead Inductance. Every effort should be made to keep the leads between the driver and it's load as short and wide as possible. If the driver must be placed farther than 2" from the load, then the output leads should be treated as transmission lines. In this case, a twisted-pair should be considered, and the return line of each twisted pair should be placed as close as possible to the ground pin of the driver, and connect directly to the ground terminal of the load.

TTL to High Voltage CMOS Level Translation (IXDD409 Only)

The enable (EN) input to the IXDD409 is a high voltage CMOS logic level input where the EN input threshold is ½ V_{CC}, and may not be compatible with 5V CMOS or TTL input levels. The IXDD409 EN input was intentionally designed for enhanced noise immunity with the high voltage CMOS logic levels. In a typical gate driver application, V_{CC} =15V and the EN input threshold at 7.5V, a 5V CMOS logical high input applied to this typical IXDD409 application's EN input will be misinterpreted as a logical low, and may cause undesirable or unexpected results. The note below is for optional adaptation of TTL or 5V CMOS levels.

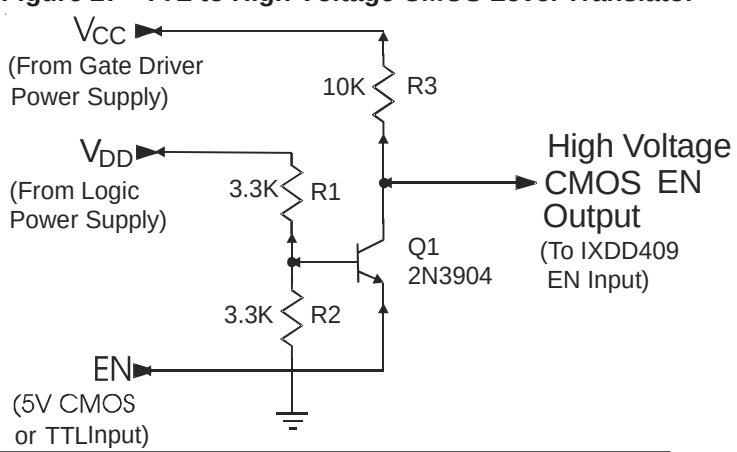
The circuit in Figure 27 alleviates this potential logic level misinterpretation by translating a TTL or 5V CMOS logic input to high voltage CMOS logic levels needed by the IXDD409 EN input. From the figure, V_{CC} is the gate driver power supply, typically set between 8V to 20V, and V_{DD} is the logic power supply, typically between 3.3V to 5.5V. Resistors R1 and R2 form a voltage divider network so that the Q1 base is positioned at the midpoint of the expected TTL logic transition levels.

A TTL or 5V CMOS logic low, V_{TTLLOW}=~<0.8V, input applied to the Q1 emitter will drive it on. This causes the level translator output, the Q1 collector output to settle to $V_{CESATQ1}$ + V_{TTLLOW}=<~2V, which is sufficiently low to be correctly interpreted as a high voltage CMOS logic low (<1/3V_{CC}=5V for V_{CC} =15V given in the IXDD409 data sheet.)

A TTL high, $V_{TTLHIGH}$=>~2.4V, or a 5V CMOS high, $V_{5VCMOSHIGH}$=~>3.5V, applied to the EN input of the circuit in Figure 27 will cause Q1 to be biased off. This results in Q1 collector being pulled up by R3 to V_{CC}=15V, and provides a high voltage CMOS logic high output. The high voltage CMOS logical EN output applied to the IXDD409 EN input will enable it, allowing the gate driver to fully function as an 8 Amp output driver.

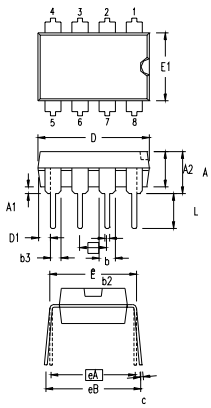
The total component cost of the circuit in Figure 27 is less than $0.10 if purchased in quantities >1K pieces. It is recommended that the physical placement of the level translator circuit be placed close to the source of the TTL or CMOS logic circuits to maximize noise rejection.

Figure 27 - TTL to High Voltage CMOS Level Translator



Package Outlines

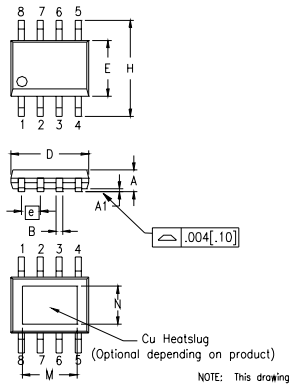
8-PIN PDIP (IXD_409PI)



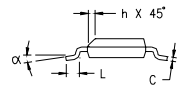
SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.140	.180	3.56	4.57
A1	.015	.040	0.38	1.02
A2	.125	.145	3.18	3.68
b	.015	.020	0.38	0.51
b2	.055	.065	1.40	1.65
b3	.035	.045	0.89	1.14
c	.009	.012	0.23	0.30
D	.355	.400	9.02	10.16
D1	.010	.040	0.25	1.02
E	.300	.325	7.62	8.26
E1	.240	.270	6.10	6.86
e	.100 BSC		2.54 BSC	
eA	.300 BSC		7.62 BSC	
eB	.300	.430	7.62	10.92
L	.120	.140	3.05	3.56

NOTE: THIS DRAWING MEETS ALL REQUIREMENT OF JEDEC OUTLINES MS-001 BA.

8-PIN SOP (IXD_409SI)

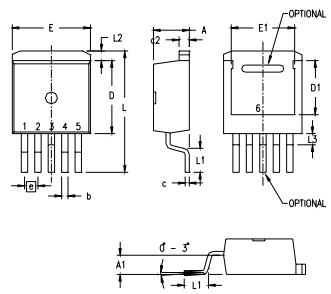


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
B	.013	.020	0.33	0.51
C	.008	.010	0.19	0.25
D	.189	.197	4.80	5.00
E	.150	.157	3.80	4.00
e	.050BSC		1.27BSC	
H	.228	.244	5.80	6.20
h	.010	.020	0.25	0.50
L	.016	.050	0.40	1.27
M	.135	.155	3.43	3.94
N	.095	.115	2.41	2.92
α	0°	8°	0°	8°



NOTE: This drawing will meet all dimensions requirement of JEDEC MS-012 AA.

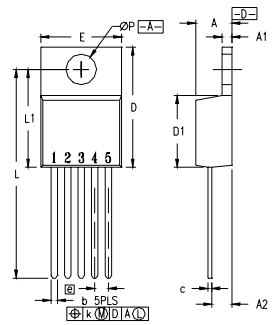
5-Lead TO-263 (IXD_409YI)



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.165	.189	4.20	4.80
A1	.083	.106	2.10	2.70
b	.024	.039	0.60	0.99
c	.016	.028	0.40	0.70
c2	.047	.055	1.20	1.40
D	.346	.374	8.80	9.50
D1	.260	.283	6.60	7.20
E	.390	.406	9.65	10.30
E1	.295	.323	7.50	8.20
e	.067 BSC		1.70 BSC	
L	.583	.622	14.80	15.80
L1	.088	.112	2.24	2.84
L2	.039	.055	1.00	1.40
L3	.047	.067	1.20	1.70

NOTE:
1. All metal surface are solder plated except trimmed area.
2. Short lead of No. 3 is optional of IXYS.
3. No. 3 lead is connected to No. 6 lead (bottom heat sink) internally.

5-Lead TO-220 (IXD_409CI)



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.170	.190	4.32	4.83
A1	.045	.055	1.14	1.40
A2	.090	.115	2.29	2.92
b	.025	.040	0.64	1.02
c	.015	.025	0.38	0.64
D	.580	.620	14.73	15.75
D1	.340	.370	8.64	9.40
E	.390	.415	9.91	10.54
e	.067 BSC		1.70 BSC	
k	0	.014	0	0.36
L	.995	1.045	25.27	26.54
L1	.470	.510	11.94	12.95
P	.139	.156	3.53	3.96

NOTE: This drawing will meet all dimensions requirement of JEDEC outlines TS-001AA and 5 lead version TO-220AB.

NOTE: Mounting or solder tabs on all packages are connected to ground

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