THE DATASHEET OF

ADS6149IRGZ

www.win-source.net 0086-755-83957316

14/12-Bit, 250/210 MSPS ADCs With DDR LVDS and Parallel CMOS Outputs

FEATURES

- **Maximum Sample Rate: 250 MSPS**
- **14-Bit Resolution – ADS614X**
- **12-Bit Resolution – ADS612X**
- **687 mW Total Power Dissipation at 250 MSPS**
- **Double Data Rate (DDR) LVDS and Parallel CMOS Output Options**
- **Programmable Fine Gain up to 6dB for SNR/SFDR Trade-Off**
- **DC Offset Correction**
- **Supports Input Clock Amplitude Down to 400 mV_{PP} Differential**
- **Internal and External Reference Support**
- **48-QFN Package (7mm × 7mm)**
- **Pin Compatible with ADS5547 Family**

APPLICATIONS

- **Multicarrier, Wide Band-Width Communications**
- **Wireless Multi-carrier Communications Infrastructure**
- **Software Defined Radio**
- **Power Amplifier Linearization**
- **802.16d/e**
- **Test and Measurement Instrumentation**
- **High Definition Video**
- **Medical Imaging**
- **Radar Systems**

DESCRIPTION

ADS614X (ADS612X) is a family of 14-bit (12-bit) A/D converters with sampling rates up to 250 MSPS. It combines high dynamic performance and low power consumption in a compact 48 QFN package. This makes it well-suited for multicarrier, wide band-width communications applications.

ADS614X/2X has fine gain options that can be used to improve SFDR performance at lower full-scale input ranges. It includes a dc offset correction loop that can be used to cancel the ADC offset. Both DDR LVDS (Double Data Rate) and parallel CMOS digital output interfaces are available. At lower sampling rates, the ADC automatically operates at scaled down power with no loss in performance.

It includes internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. Nevertheless, the device can also be driven with an external reference. The device is specified over the industrial temperature range (–40°C to 85°C).

	250 MSPS	210 MSPS
ADS614X 14-Bit Family	ADS6149	ADS6148
ADS612X 12-Bit Family	ADS6129	ADS6128

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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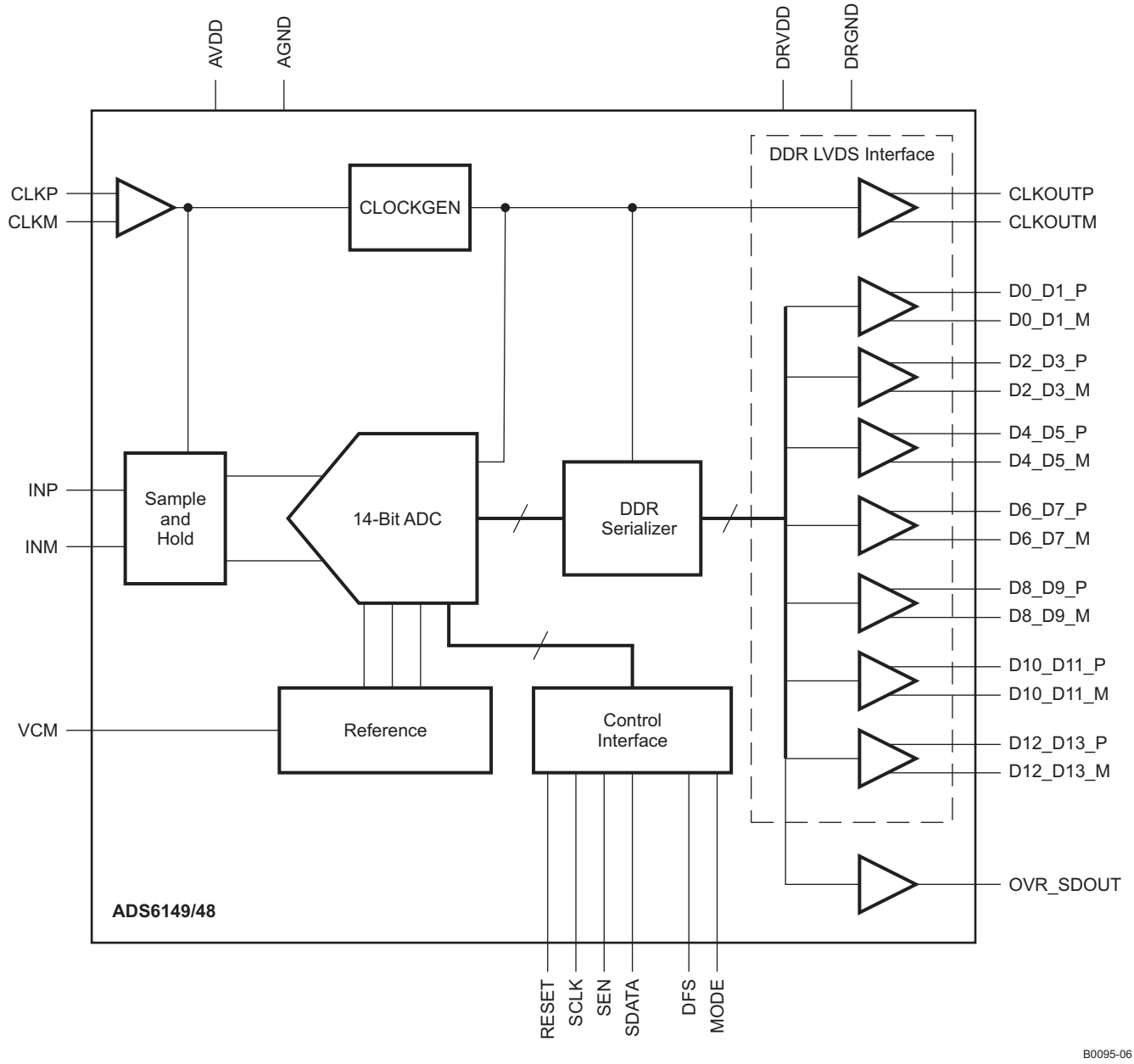
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ADS614X BLOCK DIAGRAM



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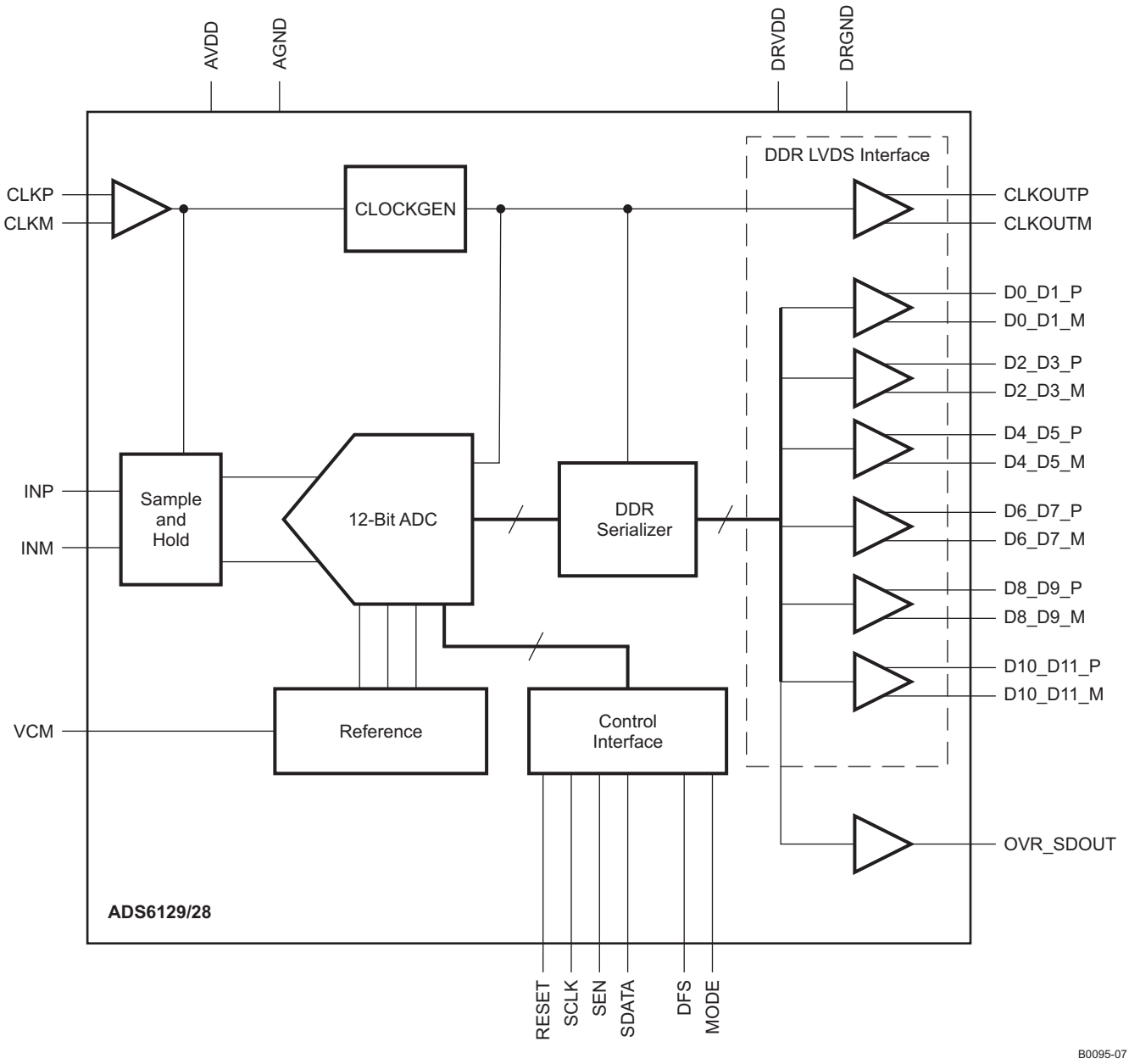
ADS612X BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION(1)(2)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS614x							
ADS6149	QFN-48	RGZ	–40°C to 85°C	Cu NiPdAu	AZ6149	ADS6149IRGZR	Tape and reel
						ADS6149IRGZT	
ADS6148					AZ6148	ADS6148IRGZR	
						ADS6148IRGZT	
ADS612x							
ADS6129	QFN-48	RGZ	–40°C to 85°C	Cu NiPdAu	AZ6129	ADS6129IRGZR	Tape and reel
						ADS6129IRGZT	
ADS6128					AZ6128	ADS6128IRGZR	
						ADS6128IRGZT	

(1) For thermal pad size on the package, see the mechanical drawings at the end of this data sheet. θ_{JA} = 25.41° C/W (0LFM air flow), θ_{JC} = 16.5°C/W when used with 2oz. copper trace and pad soldered directly to a JEDEC standard four layer 3 in x 3 in (7.62 cm x 7.62 cm) PCB.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
V_I	Supply voltage range, AVDD	–0.3 V to 3.9	V
	Supply voltage range, DRVDD	–0.3 V to 2.2	V
	Voltage between AGND and DRGND	–0.3 to 0.3	V
	Voltage between AVDD to DRVDD (when AVDD leads DRVDD)	0 to 3.3	V
	Voltage between DRVDD to AVDD (when DRVDD leads AVDD)	–1.5 to 1.8	V
	Voltage applied to external pin, VCM (in external reference mode)	–0.3 to 2.0	V
	Voltage applied to analog input pins - INP, INM	–0.3V to minimum (3.6, AVDD + 0.3V)	V
	Voltage applied to input pins - CLKP, CLKM(2), RESET, SCLK, SDATA, SEN, DFS and MODE	–0.3V to AVDD + 0.3V	V
T_A	Operating free-air temperature range	–40 to 85	°C
T_J	Operating junction temperature range	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is < |0.3V|. This prevents the ESD protection diodes at the clock input pins from turning on.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		3	3.3	3.6	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
	Differential input voltage range			2		V_{pp}
	Input common-mode voltage			1.5 ±0.1		V
	Voltage applied on CM in external reference mode			1.5 ± 0.05		V
	Maximum analog input frequency with 2 V_{PP} input amplitude(1)			500		MHz
	Maximum analog input frequency with 1 V_{PP} input amplitude(1)			800		MHz
CLOCK INPUT						
	Input clock sample rate	ADS6149 / ADS6129	1		250	MSPS
		ADS6148 / ADS6128	1		210	
	Input Clock amplitude differential (V_{CLKP}–V_{CLKM})	Sine wave, ac-coupled	0.3	1.5		V_{pp}
		LVPECL, ac-coupled		1.6		
		LVDS, ac-coupled		0.7		
		LVCMOS, single-ended, ac-coupled		3.3		V
	Input clock duty cycle		40%	50%	60%	
DIGITAL OUTPUTS						
C_L	Maximum external load capacitance from each output pin to DRGND			5		pF
R_L	Differential load resistance between the LVDS output pairs (LVDS mode)			100		Ω
T_A	Operating free-air temperature		–40		85	°C

(1) See the Theory of Operation in the application section.

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ELECTRICAL CHARACTERISTICS – ADS614X and ADS612X

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode unless otherwise noted.

Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 1.8 V

PARAMETER		ADS6149/ADS6129 250 MSPS			ADS6148/ADS6128 210 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
	Differential input voltage range		2			2		V_{PP}
	Differential input resistance (at dc), See Figure 97		>1			>1		MΩ
	Differential input capacitance, See Figure 98		3.5			3.5		pF
	Analog Input Bandwidth		700			700		MHz
	Analog Input common mode current (per input pin)		2			2		µA/MSPS
	VCM Common mode output voltage		1.5			1.5		V
	VCM output current capability		±4			±4		mA
DC ACCURACY								
	Offset error	–15	±2	15	–15	±2	15	mV
	Temperature coefficient of offset error		0.005			0.005		mV/°C
	Variation of offset error with supply		0.3			0.3		mV/V
E_{GREF}	Gain error due to internal reference inaccuracy alone	–1.25	±0.2	1.25	–1.25	±0.2	1.25	%FS
E_{GCHAN}	Gain error of channel alone		0.2			0.2		%FS
	Temperature coefficient of E_{GCHAN}		.001			.001		Δ%/°C
POWER SUPPLY								
I_{AVDD}	Analog supply current		170			155		mA
I_{DRVDD}	Output buffer supply current, LVDS interface with 100 Ω external termination		70			65		mA
	Output buffer supply current, CMOS interface Fin = 3 MHz(1), 10-pF external load capacitance		56			48		mA
	Analog power		561	630		510	570	mW
	Digital power LVDS interface		126	160		118	153	mW
	Digital power CMOS interface, Fin = 3 MHz(2), 10-pF external load capacitance		101			87		mW
	Global power down		20	50		20	50	mW
	Standby		120			120		mW

(1) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency and the supply voltage (see Figure 91 and CMOS interface power dissipation in application section).

(2) The maximum DRVDD current with CMOS interface depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance on each digital output line is 10 pF.

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ELECTRICAL CHARACTERISTICS – ADS6149 and ADS6148

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode unless otherwise noted.

Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 1.8 V

PARAMETER		ADS6149 250 MSPS			ADS6148 210 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SNR Signal to noise ratio, **LVDS**	Fin = 20 MHz		73.4			73.4		dBFS
	Fin = 80 MHz		72.7			72.7		
	Fin = 100 MHz		72.3			72.3		
	Fin = 170 MHz	69	71.3		69.7	71.2		
	Fin = 300 MHz		69			69		
SINAD Signal to noise and distortion ratio, **LVDS**	Fin = 20 MHz		73.2			73.3		dBFS
	Fin = 80 MHz		72.4			72.4		
	Fin = 100 MHz		71.9			71.8		
	Fin = 170 MHz	68	70.6		68.7	70.9		
	Fin = 300 MHz		68			68.2		
ENOB Effective number of bits	Fin = 170 MHz	11	11.4		11.1	11.5		LSB
DNL Differential non-linearity		–0.95	±0.4	2	–0.95	±0.4	2	LSB
INL Integrated non-linearity		–5	±2	5	–5	±2	5	LSB

ELECTRICAL CHARACTERISTICS – ADS6129 and ADS6128

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode unless otherwise noted.

Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 1.8 V

PARAMETER		ADS6129 250 MSPS			ADS6128 210 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SNR, Signal to noise ratio, **LVDS**	Fin = 20 MHz		70.7			70.9		dBFS
	Fin = 80 MHz		70.5			70.5		
	Fin = 100 MHz		70.1			70.1		
	Fin = 170 MHz	67.5	69.5		67.7	69.5		
	Fin = 300 MHz		67.8			67.9		
SINAD Signal to noise and distortion ratio, **LVDS**	Fin = 20 MHz		70.6			70.8		dBFS
	Fin = 80 MHz		70.4			70.4		
	Fin = 100 MHz		69.8			69.8		
	Fin = 170 MHz	66.5	69.2		66.7	69.3		
	Fin = 300 MHz		67.2			67.3		
ENOB, Effective number of bits	Fin = 170 MHz	10.8	11.2		10.8	11.2		LSB
DNL Differential non-linearity		–0.5	±0.2	1	–0.5	±0.2	1.0	LSB
INL Integrated non-linearity		–2.5	±1	2.5	–2.5	±1	2.5	LSB

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ELECTRICAL CHARACTERISTICS – ADS614x and ADS612x

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode unless otherwise noted.

Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 1.8 V

PARAMETER		ADS6149/ADS6129 250 MSPS			ADS6148/ADS6128 210 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SFDR Spurious Free Dynamic Range	Fin = 20 MHz		92			92		dBc
	Fin = 80 MHz		86			82		
	Fin = 100 MHz		85			81		
	Fin = 170 MHz	74	82		74	83		
	Fin = 300 MHz		76			76		
THD Total Harmonic Distortion	Fin = 10 MHz		89			88.5		dBc
	Fin = 20 MHz		83			80		
	Fin = 80 MHz		82			79		
	Fin = 170 MHz	71	79		71	80		
	Fin = 300 MHz		73			73		
HD2, Second Harmonic Distortion	Fin = 20 MHz		94			94		dBc
	Fin = 80 MHz		90			88		
	Fin = 100 MHz		88			88		
	Fin = 170 MHz	74	84		74	84		
	Fin = 300 MHz		76			76		
HD3 Third Harmonic Distortion	Fin = 20 MHz		93			92		dBc
	Fin = 80 MHz		86			82		
	Fin = 100 MHz		85			81		
	Fin = 170 MHz	74	82		74	83		
	Fin = 300 MHz		76			76		
Worst Spur Other than second, third harmonics	Fin = 20 MHz		96			96		dBc
	Fin = 80 MHz		94			94		
	Fin = 100 MHz		94			94		
	Fin = 170 MHz		92			92		
	Fin = 300 MHz		90			90		
IMD 2-Tone inter-modulation distortion	F1 = 46 MHz, F2 = 50 MHz, Each tone at –7 dBFS		94			95		dBFS
	F1 = 185 MHz, F2 = 190 MHz, Each tone at –7 dBFS		90			90		
Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine wave input		1			1		clock cycles
PSRR AC power supply rejection ratio	For 100 mV_{PP} signal on AVDD supply		25			25		dB

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DIGITAL CHARACTERISTICS – ADS614x and ADS612x

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 3.3 V, DRVDD = 1.8 V

PARAMETER		TEST CONDITIONS	ADS6149/ADS6148/ ADS6129/ADS6128			UNIT
			MIN	TYP	MAX	
DIGITAL INPUTS – RESET, SCLK, SDATA, SEN(1)						
High-level input voltage		All digital inputs support 1.8V and 3.3V CMOS logic levels	1.3			V
Low-level input voltage					0.4	V
High-level input current	SDATA, SCLK(2)	VHIGH = 3.3V		16		µA
	SEN(3)	VHIGH = 3.3V		10		
Low-level input current	SDATA, SCLK	VLOW = 0V		0		µA
	SEN	VLOW = 0V		–20		
Input capacitance				4		pF
DIGITAL OUTPUTS – CMOS INTERFACE (Pins D0 to D13 and OVR_SDOUT)						
High-level output voltage				DRVDD		V
Low-level output voltage				0		V
Output capacitance (internal to device)				2		pF
DIGITAL OUTPUTS – LVDS INTERFACE (Pins D0_D1_P/M to D12_D13_P/M)(4)						
V_{ODH}, High-level output voltage(5)			275	350	425	mV
V_{ODL}, Low-level output voltage(5)			–425	–350	–275	mV
V_{OCM}, Output common-mode voltage			1	1.2	1.3	V
Output capacitance		Capacitance inside the device, from either output to ground		2		pF

(1) SCLK, SDATA, SEN function as digital input pins in serial configuration mode.
(2) SDATA, SCLK have internal 200 kΩ pull-down resistor
(3) SEN has internal 100 kΩ pull-up resistor to AVDD. Since the pull-up is weak, SEN can also be driven by 1.8V or 3.3V CMOS buffers.
(4) OVR_SDOUT has CMOS output logic levels, determined by DRVDD voltage.
(5) With external 100 Ω termination

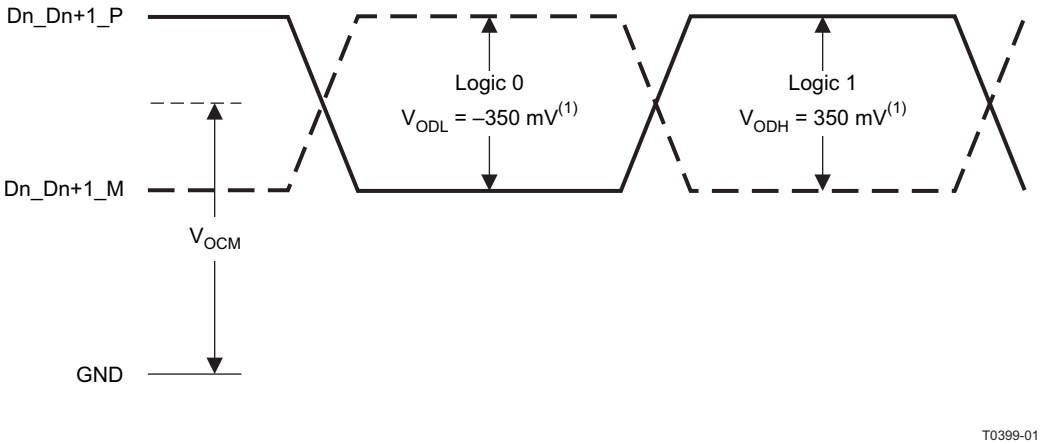

Figure 1. LVDS Voltage Levels

TIMING REQUIREMENTS – LVDS AND CMOS MODES(1)

Typical values are at 25°C, AVDD = 3.3V, DRVDD = 1.8V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 5pF(2), R_{LOAD} = 100Ω(3), LOW SPEED mode disabled, unless otherwise noted.
Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3V, DRVDD = 1.7V to 1.9V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay	The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs	0.7	1.2	1.7	ns
t_j	Aperture jitter			170		fs rms
	Wake-up time	Time to valid data after coming out of STANDBY mode		0.3	1	µs
		Time to valid data after coming out of PDN GLOBAL mode		25	100	
		Time to valid data after stopping and restarting the input clock		10		clock cycles
	ADC Latency(4)	Default, after reset		18		clock cycles
DDR LVDS MODE (5)						
t_{su}	Data setup time	Data valid (6) to zero-crossing of CLKOUTP	0.8	1.2		ns
t_h	Data hold time	Zero-crossing of CLKOUT to data becoming invalid(6)	0.25	0.6		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *100 MSPS ≤ Sampling frequency ≤ 250 MSPS*	0.2 × t_s + t_{delay}			ns
	t_{delay}		5.0	6.2	7.5	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP–CLKOUTM) *100 MSPS ≤ Sampling frequency ≤ 250 MSPS*		52%		
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from –100 mV to 100 mV Fall time measured from 100 mV to –100 mV *1 MSPS ≤ Sampling frequency ≤ 250 MSPS*	0.08	0.14	0.2	ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100 mV to 100 mV Fall time measured from 100 mV to –100 mV 1 MSPS ≤ Sampling frequency ≤ 250 MSPS	0.08	0.14	0.2	ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		40		ns
PARALLEL CMOS MODE (7)						
t_{START}	Input clock to data delay	Input clock rising edge cross-over to start of data valid(8)			3.2	ns
t_{DV}	Data valid time	Time interval of valid data(8)	0.7	1.5		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *100 MSPS ≤ Sampling frequency ≤ 150 MSPS*	0.78 × t_s + t_{delay}			
	t_{delay}		5	6.5	8	ns
	Output clock duty cycle	Duty cycle of differential clock, (CLKOUT) *100 MSPS ≤ Sampling frequency ≤ 150 MSPS*		50%		
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD, Fall time measured from 80% to 20% of DRVDD, *1 MSPS ≤ Sampling frequency ≤ 250 MSPS*	0.7	1.2	2	ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD, Fall time measured from 80% to 20% of DRVDD, *1 MSPS ≤ Sampling frequency ≤ 150 MSPS*	0.5	1	1.5	ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		20		ns

(1) Timing parameters are specified by design and characterization and not tested in production.
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) Data valid refers to LOGIC HIGH of +100mV and LOGIC LOW of –100mV.
(7) For Fs> 150 MSPS, it is recommended to use external clock for data capture and NOT the device output clock signal (CLKOUT).
(8) Data valid refers to LOGIC HIGH of 1.26V and LOGIC LOW of 0.54V.

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LVDS Timings at Lower Sampling Frequencies

SAMPLING FREQUENCY, MSPS	SETUP TIME, ns			HOLD TIME, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
210	1.0	1.4		0.4	0.8	
190	1.1	1.5		0.5	0.9	
170	1.3	1.7		0.7	1.1	
150	1.6	1.9		0.9	1.2	
125	1.9	2.2		1.1	1.4	
<100 *Enable LOW SPEED mode*	2.5			2.0		
1 ≤ Fs ≤ 100, *Enable LOW SPEED mode*				t_{PDI}, ns (1)		
				MIN	TYP	MAX
					8.2	

(1) Ts = 1/Sampling frequency

CMOS Timings at Lower Sampling Frequencies

SAMPLING FREQUENCY, MSPS	Timings specified with respect to input clock					
	t_{START}, ns			DATA VALID TIME, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
210			1.7	1.6	2.4	
190			0.4	2.2	3.0	
170			5.1	2.4	3.6	
150			4.8	3.0	4.3	

SAMPLING FREQUENCY, MSPS	Timings specified with respect to CLKOUT					
	SETUP TIME, ns			HOLD TIME, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
150	2.0	3.2		1.5	2.2	
125	2.9	4		2.2	2.7	
<100 *Enable LOW SPEED mode*	5.0			3.8		
1 ≤ Fs ≤ 100 *Enable LOW SPEED mode*				t_{PDI}, ns (1)		
				MIN	TYP	MAX
					14	

(1) Ts = 1/Sampling frequency

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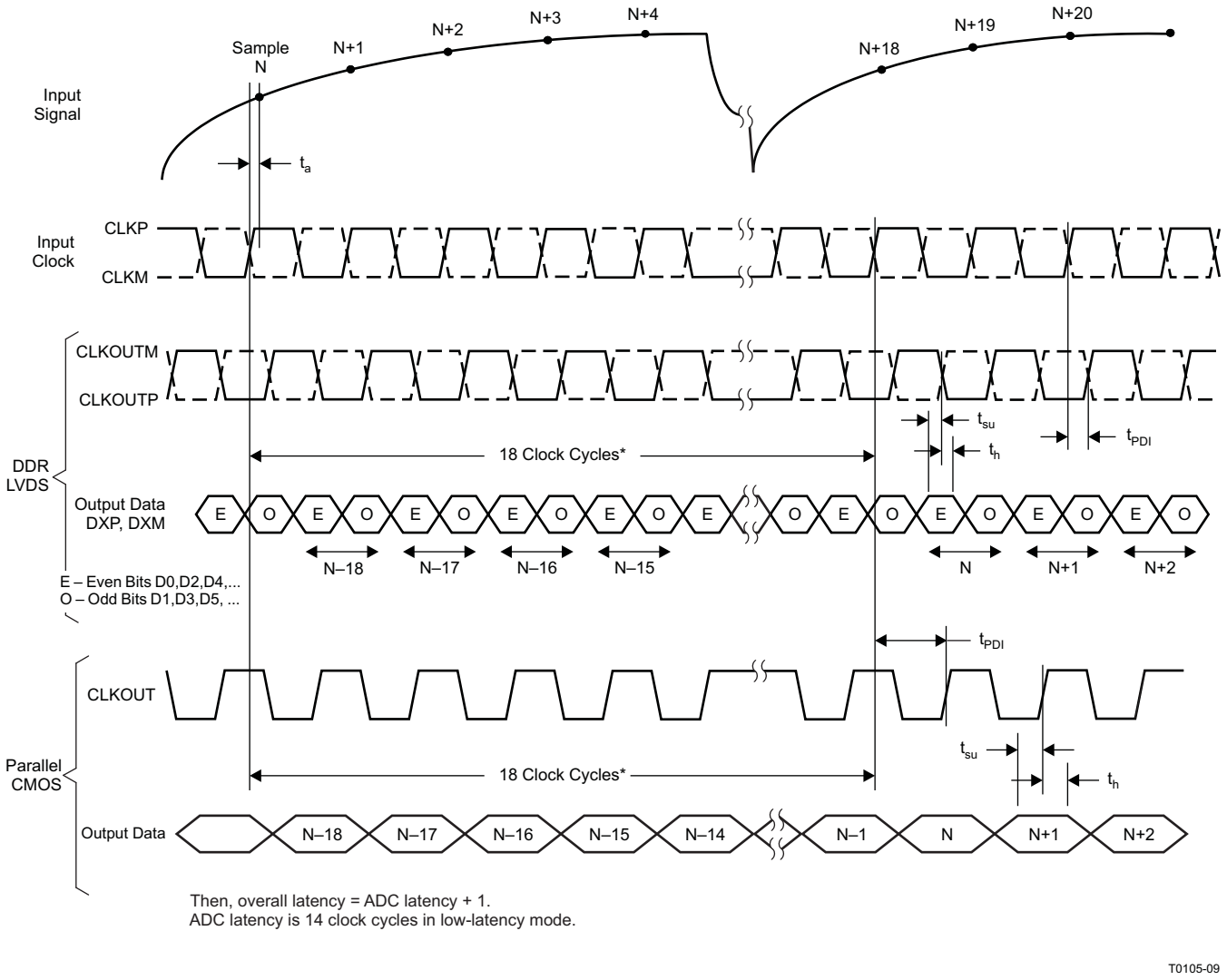

Figure 2. Latency Diagram

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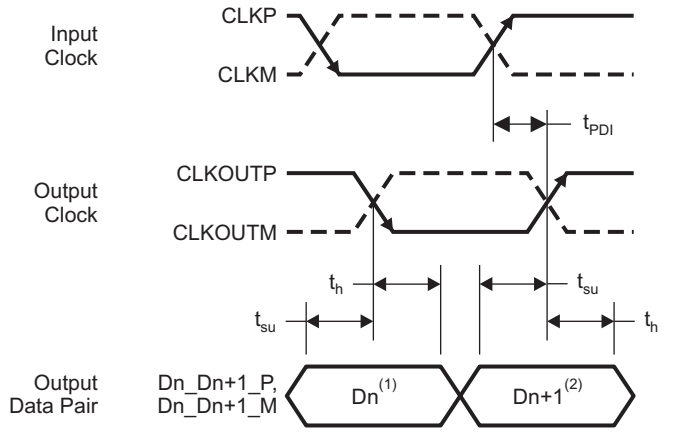

(1)Dn – Bits D0, D2, D4,...
(2)Dn+1 – Bits D1, D3, D5, ...

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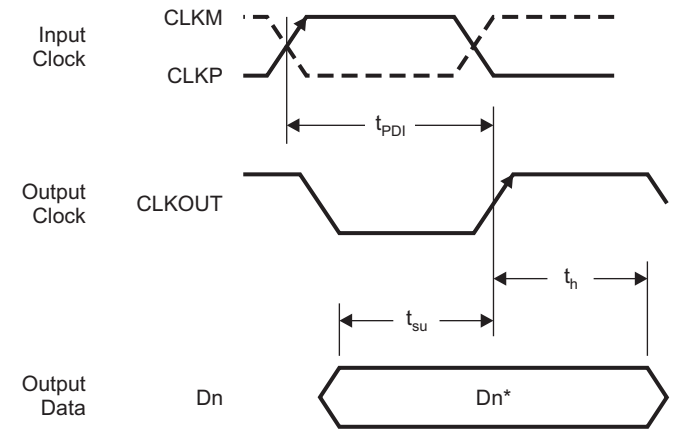
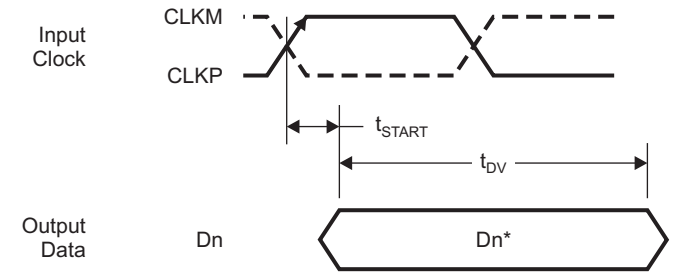
Figure 3. LVDS Mode Timing





*Dn – Bits D0, D1, D2, ...

T0107-05

Figure 4. CMOS Mode Timing

DEVICE CONFIGURATION

ADS614X/2X can be configured independently using either parallel interface control or serial interface programming.

PARALLEL CONFIGURATION ONLY

To put the device in parallel configuration mode, keep RESET tied to HIGH (DRVDD).

Now, pins DFS, MODE, SEN and SDATA can be used to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 3 to Table 6. There is no need to apply reset.

In this mode, SEN and SDATA function as parallel interface control pins. Frequently used functions can be controlled in this mode – standby, selection between LVDS/CMOS output format, internal/external reference, two's complement/straight binary output format and position of the output clock edge.

Table 1 briefly describes the modes controlled by the parallel pins.

Table 1. Parallel Pin Functions

PIN	TYPE OF CONTROL	CONTROLS MODES
DFS	Analog	Data format and LVDS/CMOS output interface.
MODE(1)	Analog	Internal or external reference, low speed mode enable
SEN	Analog	CLKOUT edge programmability.
SDATA	Digital	Global power-down (ADC, internal references and output buffers are powered down)

(1) In the next generation pin-compatible ADC family, MODE will be converted to a digital control pin for certain reserved functions. So, the selection of internal or external reference and low speed functions will not be supported using MODE. In the system board using ADS61x9/x8, the MODE pin can be routed to a digital controller. This will avoid board modification while migrating to the next generation ADC.

SERIAL INTERFACE CONFIGURATION ONLY

To exercise this mode, first the serial registers have to be reset to their default values and RESET pin has to be kept LOW.

SEN, SDATA and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC.

The registers can be reset either by applying a pulse on RESET pin or by setting HIGH the **<RESET>** bit (D7 in register 0x00). The serial interface section describes the register programming and register reset in more detail.

Since the parallel pins DFS and MODE are not to be used in this mode, they have to be tied to ground.

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CONFIGURATION USING BOTH THE SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, an additional configuration mode is supported wherein a combination of serial interface registers and parallel pin controls (DFS, MODE) can be used to configure the device.

To exercise this mode, the serial registers have to be reset to their default values and RESET pin has to be kept LOW.

SEN, SDATA and SCLK function as serial interface pins in this mode and can be used to access the internal registers of ADC. The registers can be reset either by applying a pulse on RESET pin or by setting HIGH the <RESET> bit (D7 in register 0x00). The serial interface section describes the register programming and register reset in more detail.

The parallel interface control pins DFS and MODE can be used and their function is determined by the appropriate voltage levels as described in Table 3. The voltage levels can be easily derived, by using a resistor string as illustrated with an example as shown in Figure 5.

Since some functions can be controlled using both the parallel pins and serial registers, the priority between the two is determined by a Priority Table as shown in Table 2.

Table 2. Priority Between Parallel Pins and Serial Registers

FUNCTION	PRIORITY
Internal/External reference	MODE pin controls this selection ONLY if the register bits **<REF>** = 00, otherwise **<REF>** controls the selection
Data format selection	DFS pin controls this selection ONLY if the register bits **<DATA FORMAT>** = 00, otherwise **<DATA FORMAT>** controls the selection
LVDS or CMOS interface selection	DFS pin controls this selection ONLY if the register bits **<LVDS CMOS>** = 00, otherwise **<LVDS CMOS>** controls the selection

DESCRIPTION OF PARALLEL PINS

Table 3. SDATA – DIGITAL CONTROL PIN

SDATA	DESCRIPTION
0	Normal operation (default)
AVDD	Global power-down. ADC, internal references and the output buffers are powered down.

Table 4. SEN – ANALOG CONTROL PIN(1)

SEN	DESCRIPTION – Output Clock Edge Programmability
0	**LVDS:** Data and output clock transitions are aligned **CMOS:** Setup time increases by (6xTs/26), Hold time reduces by (6xTs/26)
(3/8)AVDD	**LVDS:** Setup time decreases by (4xTs/26), Hold time increases by (4xTs/26) **CMOS:** Setup time increases by (9xTs/26), Hold time reduces by (9xTs/26)
(5/8)AVDD	**LVDS:** Setup time increases by (4xTs/26), Hold time reduces by (4xTs/26) **CMOS**: Setup time increases by (3xTs/26), Hold time reduces by (3xTs/26)
AVDD	Default output clock position (Setup/hold timings of output data with respect to this clock position is specified in the timing characteristics table).

(1) Ts = 1/Sampling frequency

Table 5. DFS – ANALOG CONTROL PIN

DFS	DESCRIPTION
0	2s complement data and DDR LVDS output
(3/8)AVDD	2s complement data and parallel CMOS output
(5/8)AVDD	Offset binary data and parallel CMOS output
AVDD	Offset binary data and DDR LVDS output

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Table 6. MODE – ANALOG CONTROL PIN

MODE	DESCRIPTION
0	Internal reference, LOW SPEED mode disabled (for Fs > 100 MSPS)
(3/8)AVDD	External reference, LOW SPEED mode disabled (for Fs > 100 MSPS)
(5/8)AVDD	External reference, LOW SPEED mode enabled (for Fs ≤ 100 MSPS)
AVDD	Internal reference, LOW SPEED mode enabled (for Fs ≤ 100 MSPS)

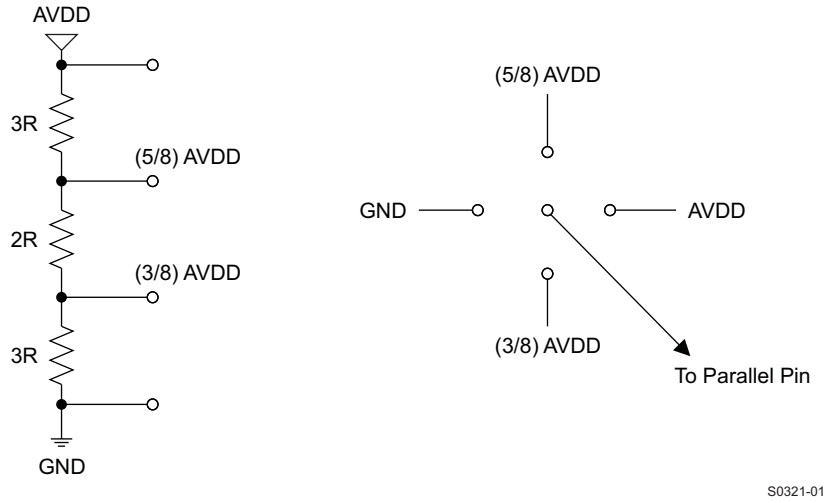

Figure 5. Simple Scheme to Configure Parallel Pins SEN and SCLK

SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock) and SDATA (Serial Interface Data).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiple of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address and the remaining 8 bits are the register data. The interface can work with SCLK frequency from 20 MHz down to low speeds (few Hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers MUST be initialized to their default values. This can be done in one of two ways:

1. Either through hardware reset by applying a high-going pulse on RESET pin (of width greater than 10ns) as shown in Figure 6.

   OR

2. By applying software reset. Using the serial interface, set the **<RESET>** bit (D7 in register 0x00) to HIGH. This initializes internal registers to their default values and then self-resets the **<RESET>** bit to LOW. In this case the RESET pin is kept LOW.

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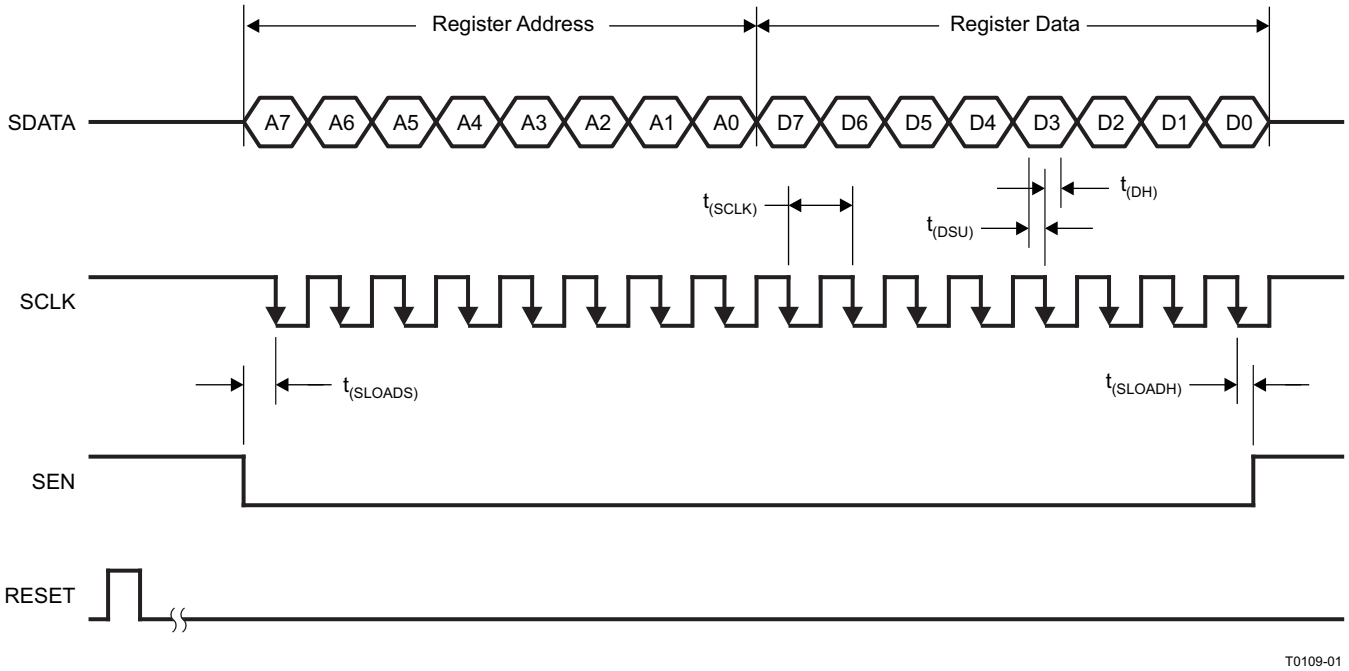

Figure 6. Serial Interface Timing

SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at 25°C, min and max values across the full temperature range
T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3V, DRVDD = 1.8V, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (= 1/ tSCLK)	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DS}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

SERIAL REGISTER READOUT

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

a. First, set register bit <SERIAL READOUT> = 1. This also disables any further writes into the registers (EXCEPT register bit <SERIAL READOUT> itself).
b. Initiate a serial interface cycle specifying the address of the register (A7-A0) whose content has to be read.
c. The device outputs the contents (D7-D0) of the selected register on OVR_SDOUT pin.
d. The external controller can latch the contents at the falling edge of SCLK.
e. To enable register writes, reset register bit <SERIAL READOUT> = 0.

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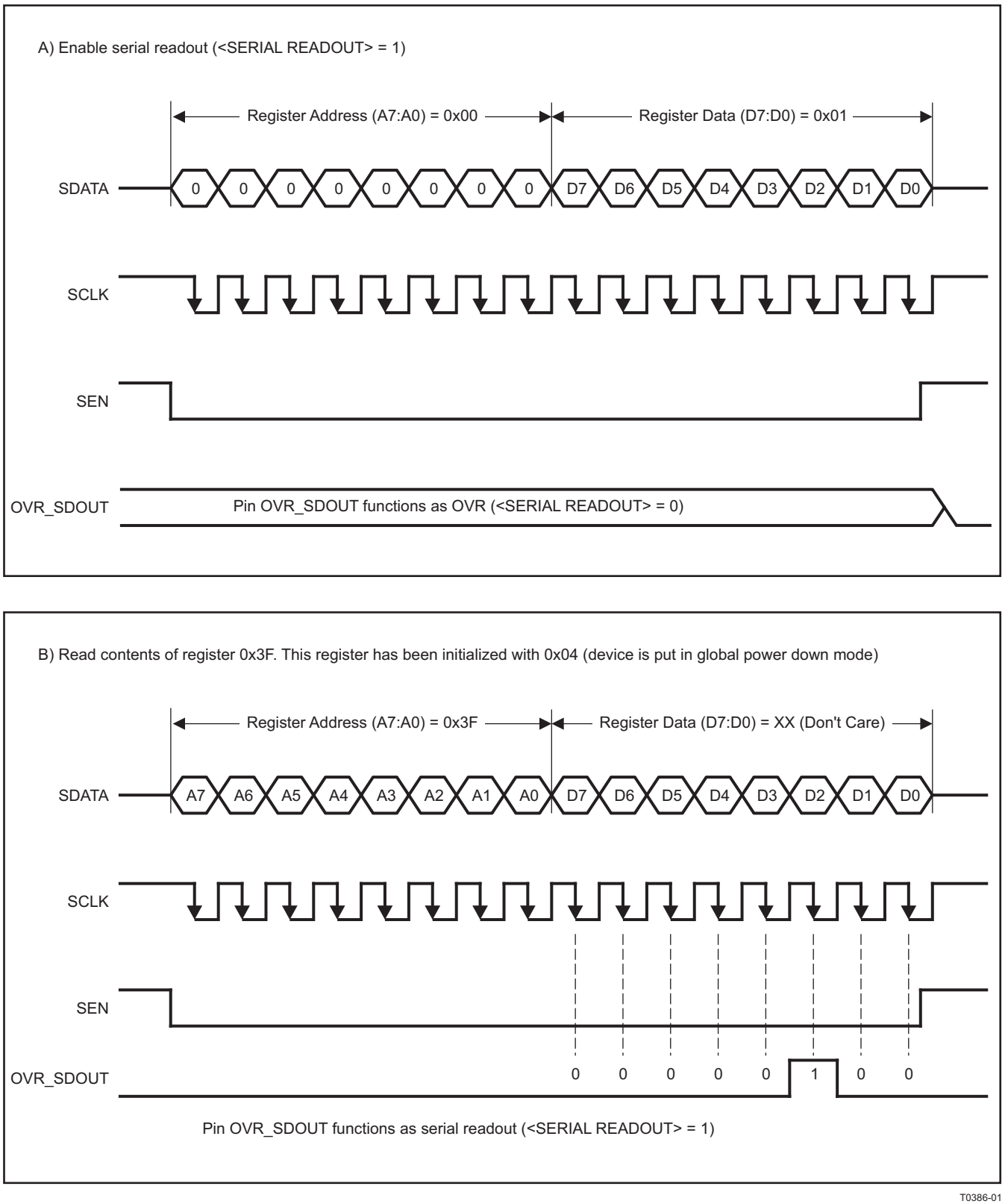

Figure 7. Serial Readout

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RESET TIMING

Typical values at 25°C, min and max values across the full temperature range
T_{MIN} = –40°C to T_{MAX} = 85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active		1		ms
t_2	Reset pulse width	Pulse width of active RESET signal that will reset the serial registers	10			ns
					1	µs
t_3		Delay from RESET disable to SEN active	100			ns

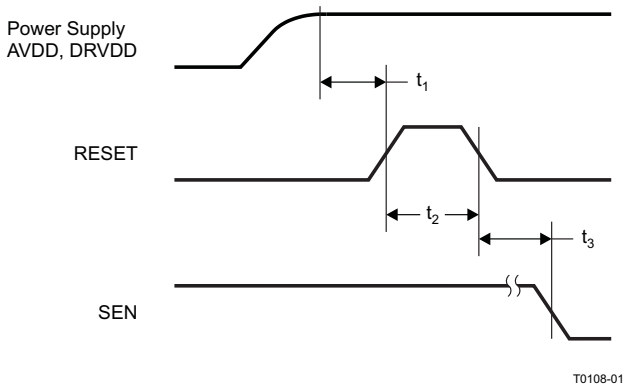

Figure 8. Reset Timing Diagram

SERIAL REGISTER MAP

Table 7. Summary of Functions Supported by Serial Interface(1)

REGISTER ADDRESS	REGISTER FUNCTIONS							
A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	<RESET> *Software Reset*	0	0	0	0	0	0	<SERIAL READOUT>
20	0	0	0	0	0	<ENABLE LOW SPEED MODE>	0	0
3F	0	REF> *Internal or external reference*		0	0	<PDN GLOBAL>	<STANDBY>	<PDN OBUF>
41	<LVDS CMOS> *Output interface*		0	0	0	0	0	0
44	<CLKOUT POSN> *Output clock position control*						0	0
50	0	0	0	0	0	<DATA FORMAT> *2s complement or offset binary*		0
51	<CUSTOM PATTERN LOW>							
52	0	0	CUSTOM PATTERN HIGH>					
53	0	ENABLE OFFSET CORR>	0	0	0	0	0	0
55	<FINE GAIN >					<OFFSET CORR TIME CONSTANT> Offset correction time constant		
62	0	0	0	0	0	TEST PATTERNS>		
63	0	0	PROGRAM OFFSET PEDESTAL >					

(1) Multiple functions in a register can be programmed in a single write operation.

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DESCRIPTION OF SERIAL REGISTERS

A)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	<RESET> *Software Reset*	0	0	0	0	0	0	<SERIAL READOUT>

D7 <RESET>

1 Software reset applied – resets all internal registers and self-clears to 0.

D0 <SERIAL READOUT>

0 Serial readout disabled

1 Serial readout enabled, Pin OVR_SDOUT functions as serial data readout.

A)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
20	0	0	0	0	0	<ENABLE LOW SPEED MODE>	0	0

D2 <ENABLE LOW SPEED MODE>

0 LOW SPEED mode disabled. Use for sampling frequency > 100 MSPS

1 Enable LOW SPEED mode for sampling frequencies ≤ 100 MSPS.

B)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
3F	0	<REF>		0	0	<PDN GLOBAL>	<STANDBY>	<PDN OBUF>

D0 <PDN OBUF> Power down output buffer

0 Output buffer enabled

1 Output buffer powered down

D1 <STANDBY>

0 Normal operation

1 ADC alone powered down. Internal references, output buffers are active. Quick wake-up time

D2 <PDN GLOBAL>

0 Normal operation

1 Total power down – ADC, internal references and output buffers are powered down. Slow wake-up time.

D6,D5 <REF> Internal or external reference selection

00 MODE pin controls reference selection

01 Internal reference enabled

11 External reference enabled

C)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
41	<LVDS CMOS>		0	0	0	0	0	0

D7,D6 <LVDS CMOS>

00 DFS pin controls LVDS or CMOS interface selection

10 DDR LVDS interface

11 Parallel CMOS interface

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D)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
44	<CLKOUT POSN> *Output clock position control*						0	0

LVDS Interface

D7-D5	<CLKOUT POSN> Output clock rising edge position
000	Default output clock position (refer to timing specification table)
100	Default output clock position (refer to timing specification table)
101	Rising edge shifted by + (4/26)Ts
110	Rising edge aligned with data transition
111	Rising edge shifted by - (4/26)Ts

D4-D2	<CLKOUT POSN> Output clock falling edge position
000	Default output clock position (refer to timing specification table)
100	Default output clock position (refer to timing specification table)
101	Falling edge shifted by + (4/26)Ts
110	Falling edge aligned with data transition
111	Falling edge shifted by - (4/26)Ts

CMOS Interface

D7-D5	<CLKOUT POSN> Output clock rising edge position
000	Default output clock position (refer to timing specification table)
100	Default output clock position (refer to timing specification table)
101	Rising edge shifted by + (4/26)Ts
110	Rising edge shifted by + (6/26)Ts
111	Rising edge aligned with data transition

D4-D2	<CLKOUT POSN> Output clock falling edge position
000	Default output clock position (refer to timing specification table)
100	Default output clock position (refer to timing specification table)
101	Falling edge shifted by + (4/26)Ts
110	Falling edge shifted by + (6/26)Ts
111	Falling edge aligned with data transition

T_s = 1/Sampling Frequency

E)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
50	0	0	0	0	0	<DATA FORMAT> *2s complement or offset binary*		0

D2,D1	<DATA FORMAT>
00	DFS pin controls data format selection
10	2's complement
11	Offset binary

F)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
51	<Custom Pattern>							
52	0	0	<Custom Pattern>					

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D7–D0 **<CUSTOM LOW>**

8 lower bits of custom pattern available at the output instead of ADC data.

D5–D0 **<CUSTOM HIGH>**

6 upper bits of custom pattern available at the output instead of ADC data

G)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
53	0	<ENABLE OFFSET CORR> *Offset correction enable*	0	0	0	0	0	0

D6 **<ENABLE OFFSET CORR>**

0 Offset correction disabled

1 Offset correction enabled

H)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
55	<FINE GAIN>				<OFFSET CORR TC> *Offset correction time constant*			

D3–D0 **<OFFSET CORR TC>** Time constant of correction loop in number of clock cycles. See "Offset Correction" in application section.

0000 256 k

0001 512 k

0010 1 M

0011 2 M

0100 4 M

0101 8 M

0110 16 M

0111 32 M

1000 64 M

1001 128 M

1010 256 M

1011 512 M

1100 to 1111 RESERVED

D7–D4 **<FINE GAIN>** Gain programmability in 0.5 dB steps

0000 0 dB gain, default after reset

0001 0.5 dB gain

0010 1.0 dB gain

0011 1.5 dB gain

0100 2.0 dB gain

0101 2.5 dB gain

0110 3.0 dB gain

0111 3.5 dB gain

1000 4.0 dB gain

1001 4.5 dB gain

1010 5.0 dB gain

1011 5.5 dB gain

1100 6.0 dB gain

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I)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
62	0	0	0	0	0	<TEST PATTERNS>		

D2–D0 **<TEST PATTERNS>** Test Patterns to verify data capture

000 Normal operation

001 Outputs all zeros

010 Outputs all ones

011 Outputs toggle pattern

ADS6149/8: Output data <D13:D0> alternates between 10101010101010 and 01010101010101 every clock cycle.

ADS6129/8: Output data <D11:D0> alternates between 101010101010 and 010101010101 every clock cycle.

100 Outputs digital ramp

ADS6149/8: Output data increments by one LSB (14-bit) every clock cycle from code 0 to code 16383

ADS6129/8: Output data increments by one LSB (124-bit) every 4^{th} clock cycle from code 0 to code 4095

101 Outputs custom pattern as specified in registers 0x51 and 0x52.

110 Unused

111 Unused

J)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
63			<OFFSET PEDESTAL>					

D5–D0 **<OFFSET PEDESTAL>** When the offset correction is enabled, the final converged value after the offset is corrected will be the ADC mid-code value.

A pedestal can be added to the final converged value by programming these bits. For example, See "Offset Correction" in application section.

011111 Mid-code + 31 LSB

011110 Mid-code + 30 LSB

011101 Mid-code + 29 LSB

....

000000 Mid-code

111111 Mid-code - 1 LSB

111110 Mid-code - 2 LSB

....

100000 Mid-code - 32 LSB

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DEVICE INFORMATION

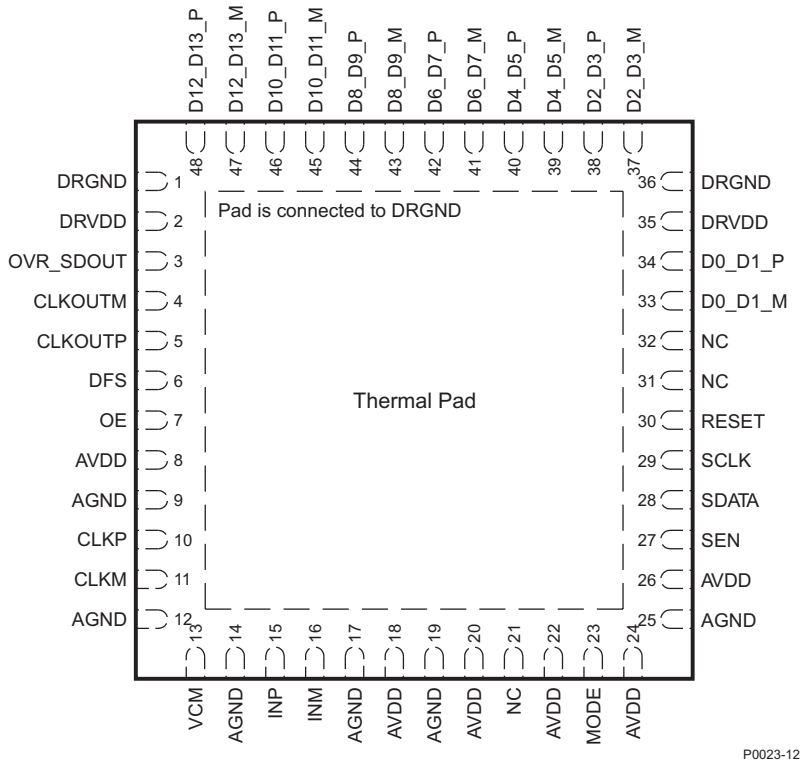

Figure 9. PIN CONFIGURATION (LVDS MODE) — ADS6149/48

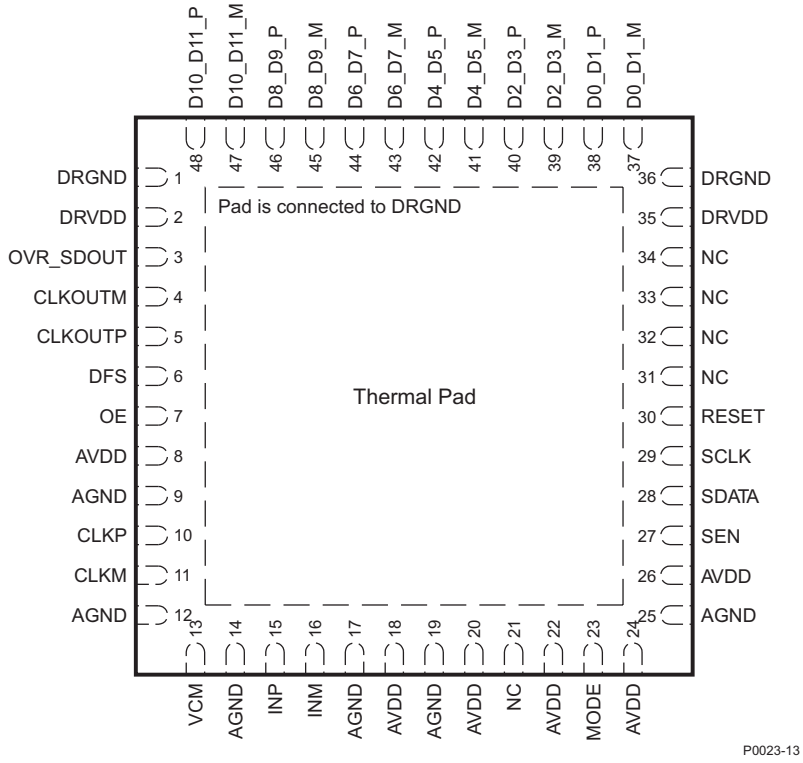

Figure 10. PIN CONFIGURATION (LVDS MODE) — ADS6129/28

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Table 8. PIN ASSIGNMENTS (LVDS MODE) — ADS6149/48 and ADS6129/28

PIN		I/O	NO. of PINS	DESCRIPTION
NAME	NO.			
AVDD	8, 18, 20, 22, 24, 26	I	6	3.3-V Analog power supply
AGND	9, 12, 14, 17, 19, 25	I	6	Analog ground
CLKP, CLKM	10, 11	I	2	Differential clock input
INP, INM	15, 16	I	2	Differential analog input
VCM	13	IO	1	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references
RESET	30	I	1	Serial interface RESET input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to *SERIAL INTERFACE* section. In parallel interface mode, the user has to tie RESET pin permanently HIGH. (SDATA and SEN are used as parallel pin controls in this mode) The pin has an internal 100 kΩ pull-down resistor.
SCLK	29	I	1	Serial interface clock input. The pin has an internal 100 kΩ pull-down resistor.
SDATA	28	I	1	This pin functions as serial interface data input when RESET is LOW. It functions as power down control pin when RESET is tied high. See Table 3 for detailed information. The pin has an internal 100 kΩ pull-down resistor.
SEN	27	I	1	This pin functions as serial interface enable input when RESET is low. It functions as output clock edge control when RESET is tied high. See Table 4 for detailed information. The pin has an internal 100 kΩ pull-up resistor to AVDD.
OE	7	I	1	Output buffer enable input, active high. The pin has an internal 100 kΩ pull-up resistor to AVDD.
DFS	6	I	1	Data Format Select input. This pin sets the DATA FORMAT (2s complement or Offset binary) and the LVDS/CMOS output interface type. See Table 5 for detailed information.
MODE(1)	23	I	1	Internal or external reference selection and low speed mode control. control. See Table 6 for detailed information.
CLKOUTP	5	O	1	Differential output clock, true
CLKOUTM	4	O	1	Differential output clock, complement
D0_D1_P	See Figure 9 and Figure 10	O	1	Differential output data D0 and D1 multiplexed, true
D0_D1_M		O	1	Differential output data D0 and D1 multiplexed, complement
D2_D3_P		O	1	Differential output data D2 and D3 multiplexed, true
D2_D3_M		O	1	Differential output data D2 and D3 multiplexed, complement
D4_D5_P		O	1	Differential output data D4 and D5 multiplexed, true
D4_D5_M		O	1	Differential output data D4 and D5 multiplexed, complement
D6_D7_P		O	1	Differential output data D6 and D7 multiplexed, true
D6_D7_M		O	1	Differential output data D6 and D7 multiplexed, complement
D8_D9_P		O	1	Differential output data D8 and D9 multiplexed, true
D8_D9_M		O	1	Differential output data D8 and D9 multiplexed, complement
D10_D11_P		O	1	Differential output data D10 and D11 multiplexed, true
D10_D11_M		O	1	Differential output data D10 and D11 multiplexed, complement
D12_D13_P		O	1	Differential output data D12 and D13 multiplexed, true
D12_D13_M		O	1	Differential output data D12 and D13 multiplexed, complement
OVR_SDOUT	3	O	1	It is a CMOS output with logic levels determined by DRVDD supply. It functions as out-of-range indicator after reset and when register bit <SERIAL READOUT> = 0. It functions as serial register readout pin when register bit <SERIAL READOUT> = 1.

(1) In the next generation pin-compatible ADC family, MODE will be converted to a digital control pin for certain reserved functions. So, the selection of internal or external reference and low speed functions will not be supported using MODE. In the system board using ADS61x9/x8, the MODE pin can be routed to a digital controller. This will avoid board modification while migrating to the next generation ADC.

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Table 8. PIN ASSIGNMENTS (LVDS MODE) — ADS6149/48 and ADS6129/28 (continued)

PIN		I/O	NO. of PINS	DESCRIPTION
NAME	NO.			
DRVDD	2, 35	I	2	1.8 V Digital and output buffer supply
DRGND	1, 36, PAD	I	2	Digital and output buffer ground
NC	See Figure 9 and Figure 10			Do not connect

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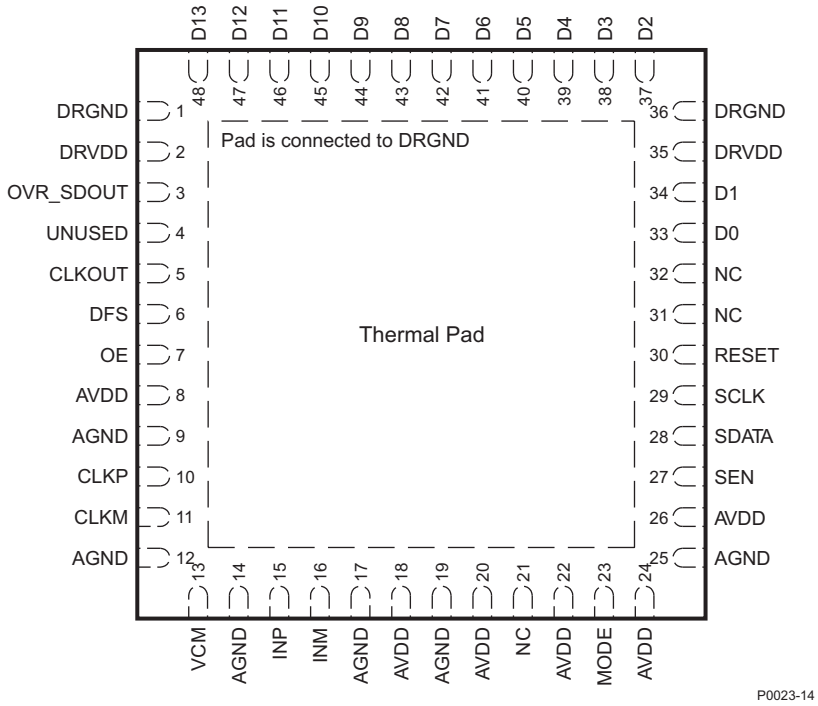

Figure 11. PIN CONFIGURATION (CMOS MODE) – ADS6149/48

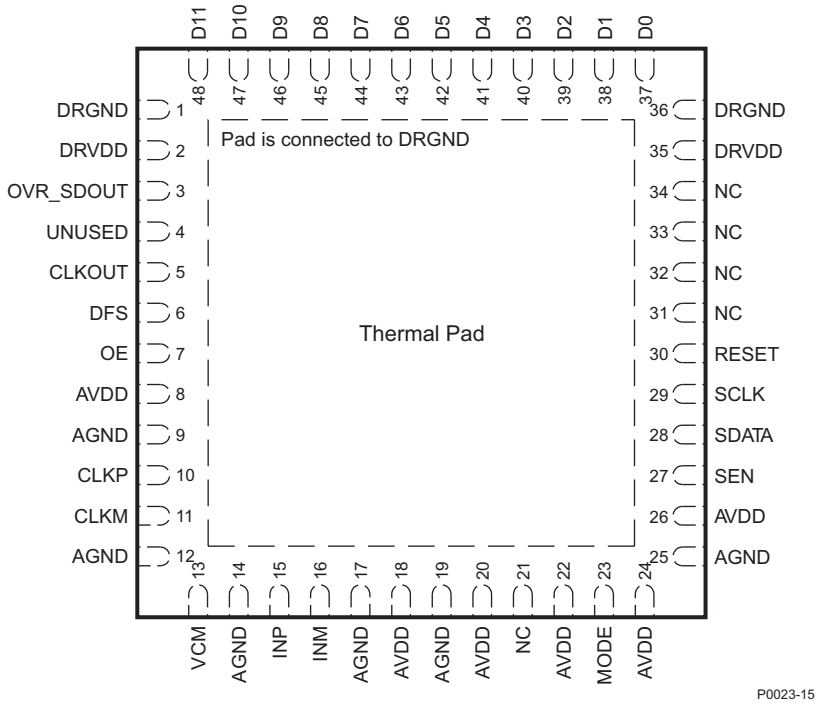

Figure 12. PIN CONFIGURATION (CMOS MODE) – ADS6129/28

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PIN ASSIGNMENTS (CMOS MODE) – ADS6149/48 and ADS6129/28

PIN		I/O	NO. of PINS	DESCRIPTION
NAME	NO.			
AVDD	8, 18, 20, 22, 24, 26	I	6	3.3-V Analog power supply
AGND	9, 12, 14, 17, 19, 25	I	6	Analog ground
CLKP, CLKM	10, 11	I	2	Differential clock input
INP, INM	15, 16	I	2	Differential analog input
VCM	13	IO	1	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references
RESET	30	I	1	Serial interface RESET input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to *SERIAL INTERFACE* section. In parallel interface mode, the user has to tie RESET pin permanently HIGH. (SDATA and SEN are used as parallel pin controls in this mode) The pin has an internal 100 kΩ pull-down resistor.
SCLK	29	I	1	Serial interface clock input. The pin has an internal 100 kΩ pull-down resistor.
SDATA	28	I	1	This pin functions as serial interface data input when RESET is LOW. It functions as power down control pin when RESET is tied high. See Table 3 for detailed information. The pin has an internal 100 kΩ pull-down resistor.
SEN	27	I	1	This pin functions as serial interface enable input when RESET is low. It functions as output clock edge control when RESET is tied high. See Table 4 for detailed information. The pin has an internal 100 kΩ pull-up resistor to AVDD.
DFS	6	I	1	Data Format Select input. This pin sets the DATA FORMAT (2s complement or Offset binary) and the LVDS/CMOS output interface type. See Table 5 for detailed information.
MODE	23	I	1	Internal or external reference selection control and low speed mode control. See Table 6 for detailed information.
CLKOUT	5	O	1	CMOS output clock
OE	7	I	1	Output buffer enable input, active high. The pin has an internal 100 kΩ pull-up resistor to AVDD.
CLKOUTM	4	O	1	Differential output clock, complement
D0–D13	See Figure 11 and Figure 12	O	14/12	14 bit/12 bit CMOS output data
OVR_SDOUT	3	O	1	It is a CMOS output with logic levels determined by DRVDD supply. It functions as out-of-range indicator after reset and when register bit <SERIAL READOUT> = 0. It functions as serial register readout pin when <SERIAL READOUT> = 1.
DRVDD	2, 35	I	2	1.8 V Digital and output buffer supply
DRGND	1, 36, PAD	I	2	Digital and output buffer ground
UNUSED	4		1	Unused pin in CMOS mode
NC	See Figure 11 and Figure 12			Do not connect

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TYPICAL CHARACTERISTICS - ADS6149

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

FFT for 20 MHz INPUT SIGNAL

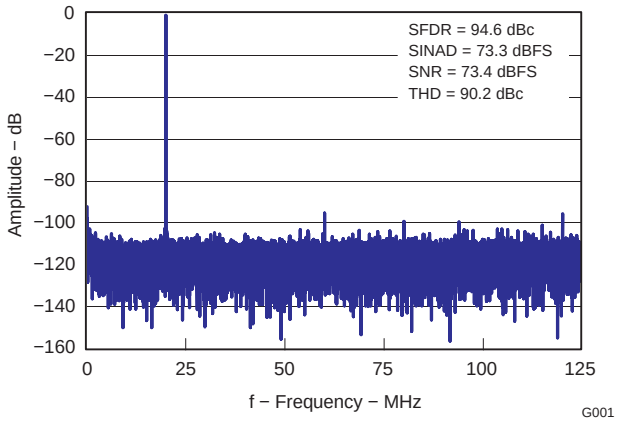

Figure 13.

FFT for 60 MHz INPUT SIGNAL

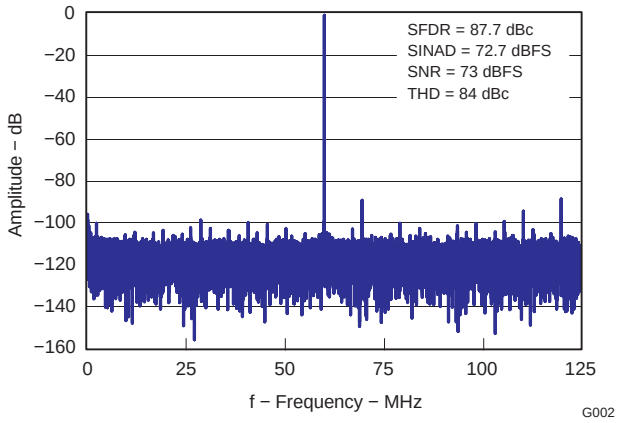

Figure 14.

FFT for 170 MHz INPUT SIGNAL

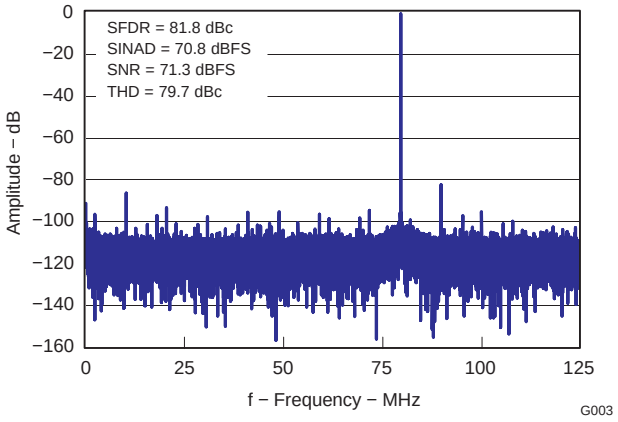

Figure 15.

FFT for 300 MHz INPUT SIGNAL

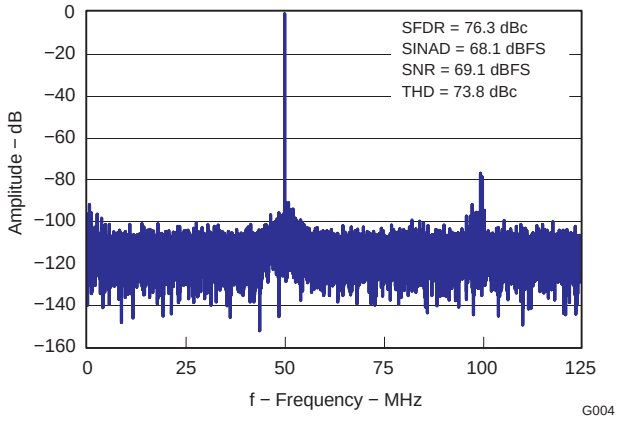

Figure 16.

FFT for 2-TONE INPUT SIGNAL (IMD)

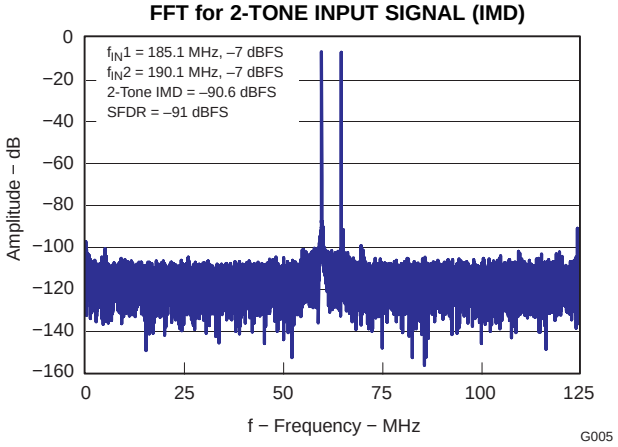

Figure 17.

FFT for 2-TONE INPUT SIGNAL (IMD)

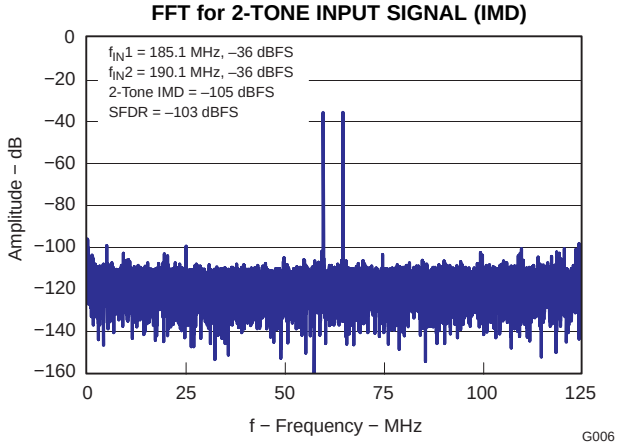

Figure 18.

TYPICAL CHARACTERISTICS - ADS6149 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

SFDR vs INPUT FREQUENCY

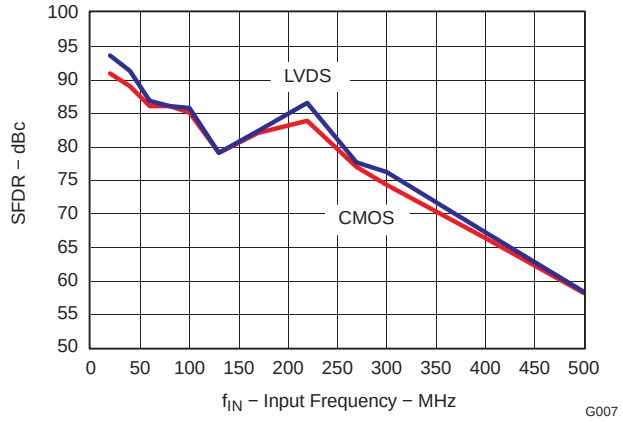

Figure 19.

SNR vs INPUT FREQUENCY

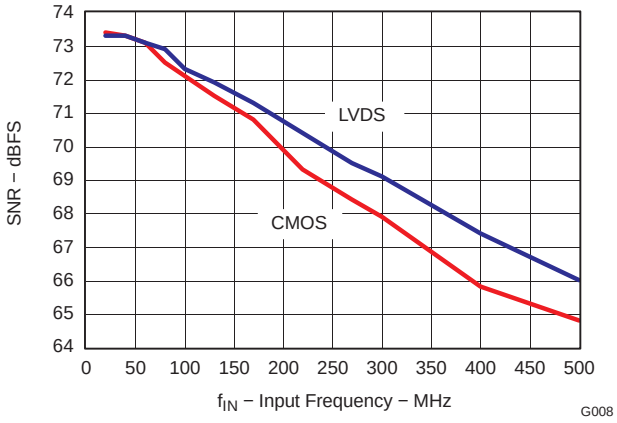

Figure 20.

SFDR vs GAIN

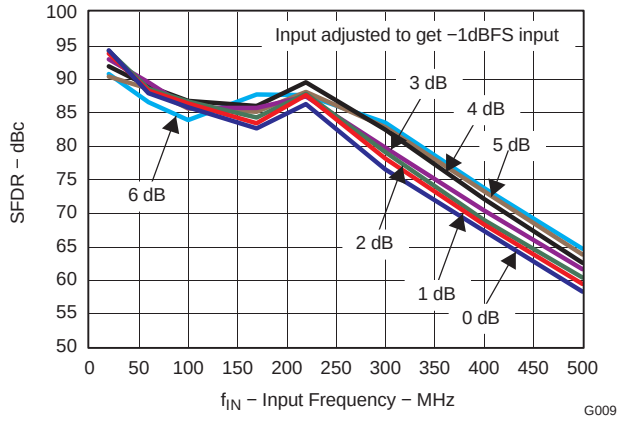

Figure 21.

SINAD vs GAIN

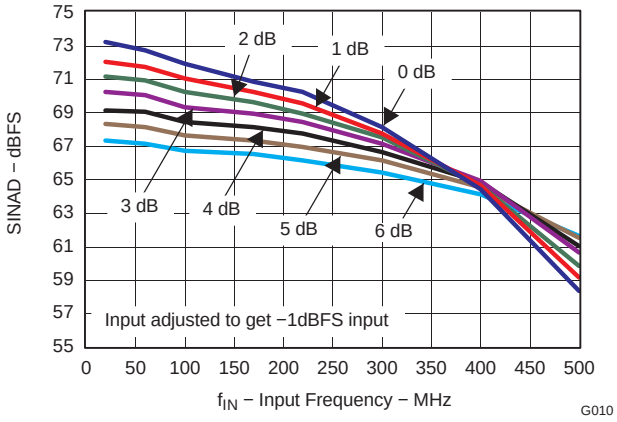

Figure 22.

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TYPICAL CHARACTERISTICS - ADS6149 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

PERFORMANCE vs INPUT AMPLITUDE

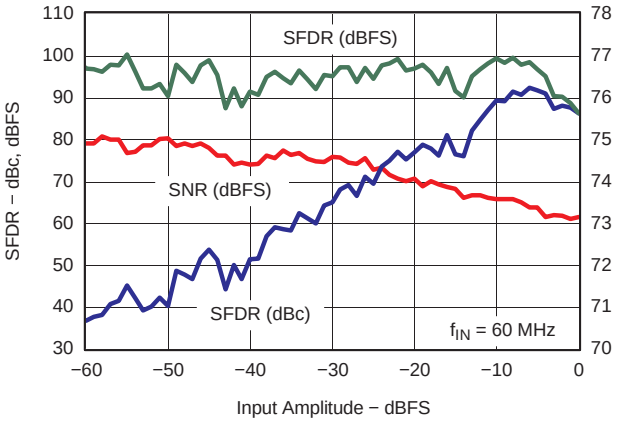

Figure 23.

PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

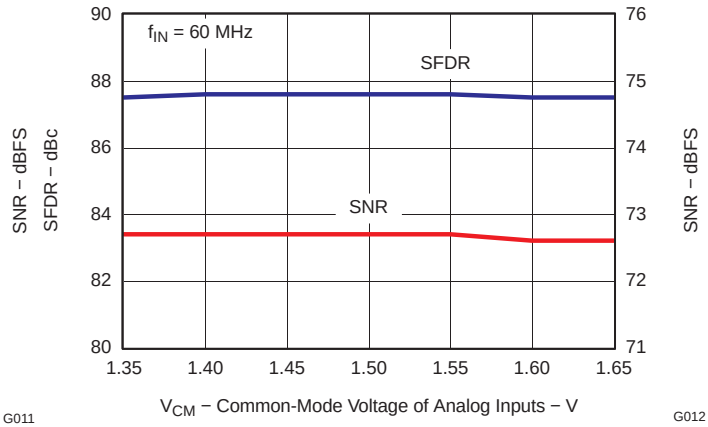

Figure 24.

PERFORMANCE vs AVDD SUPPLY

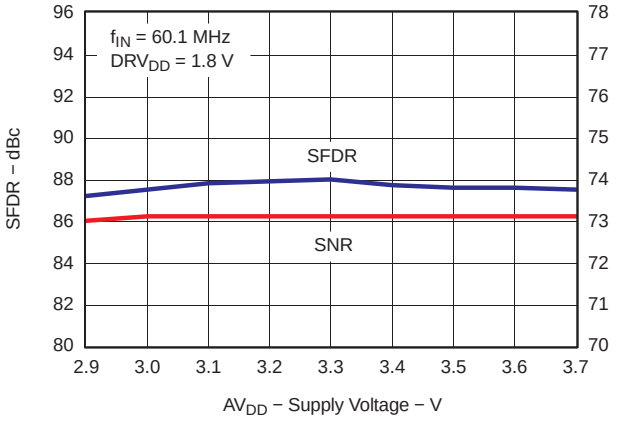

Figure 25.

PERFORMANCE vs DRVDD SUPPLY

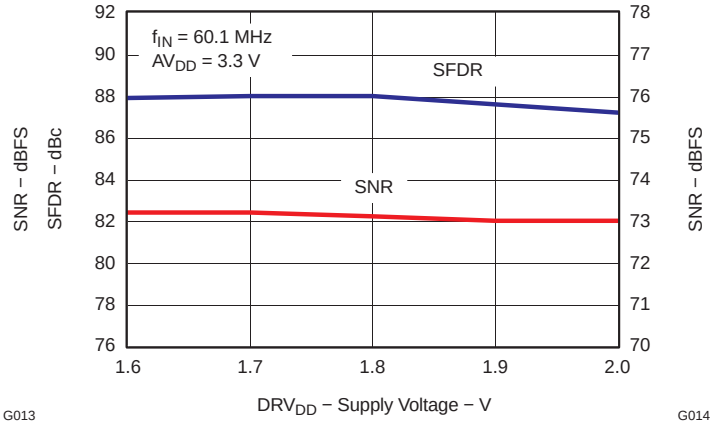

Figure 26.

TYPICAL CHARACTERISTICS - ADS6149 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

PERFORMANCE vs TEMPERATURE

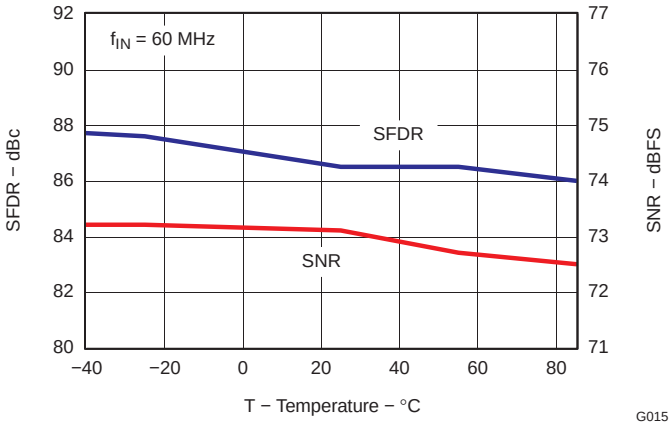

Figure 27.

PERFORMANCE vs INPUT CLOCK AMPLITUDE

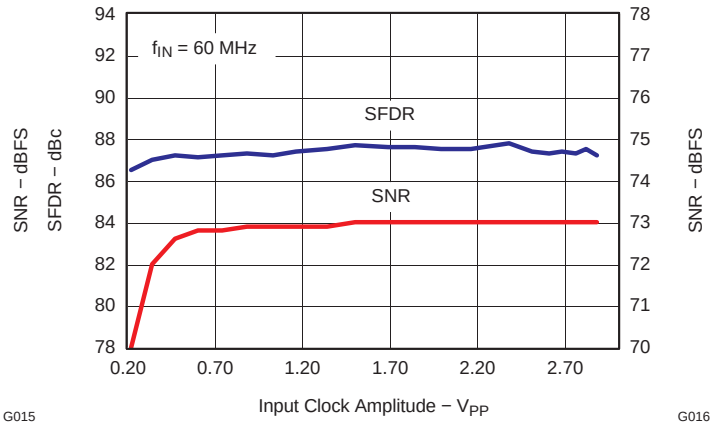

Figure 28.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

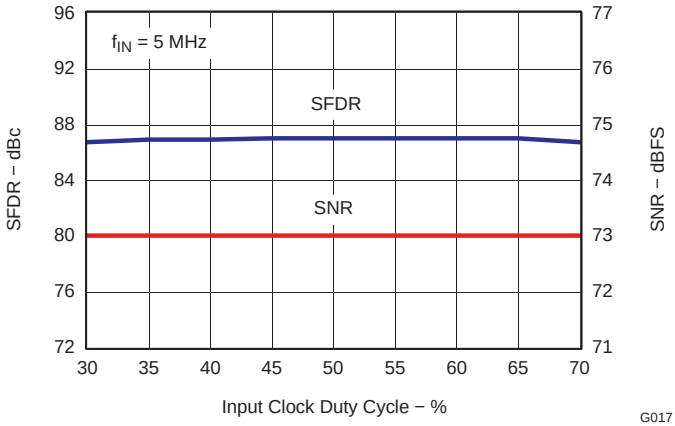

Figure 29.

PERFORMANCE vs VCM VOLTAGE

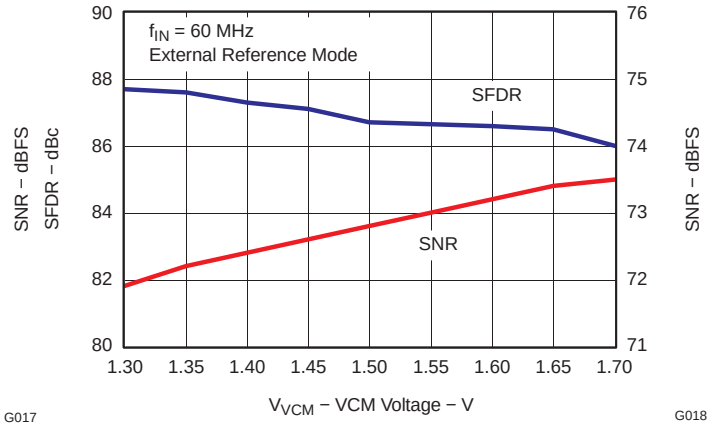

Figure 30.

OUTPUT NOISE HISTOGRAM

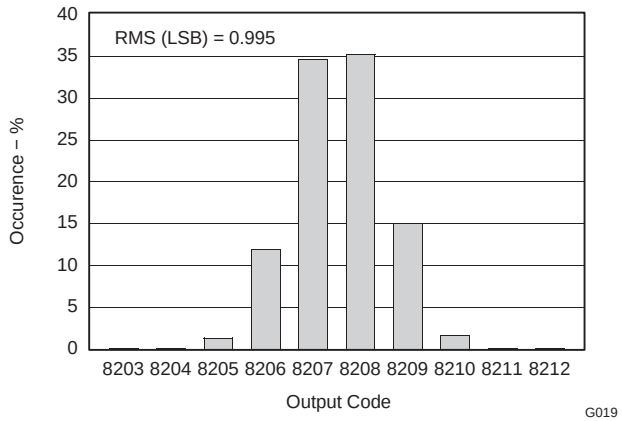

Figure 31.

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TYPICAL CHARACTERISTICS - ADS6148

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

FFT for 20 MHz INPUT SIGNAL

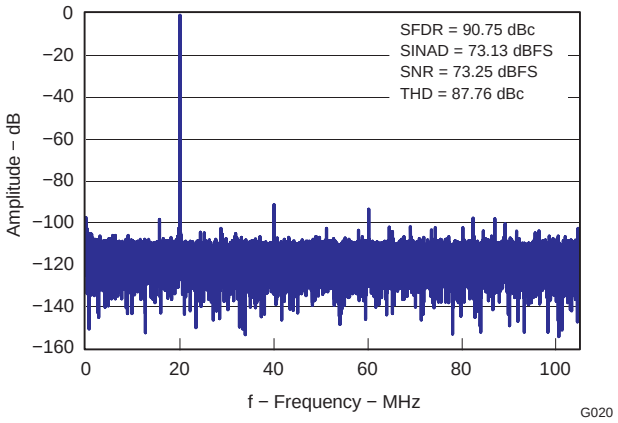

Figure 32.

FFT for 60 MHz INPUT SIGNAL

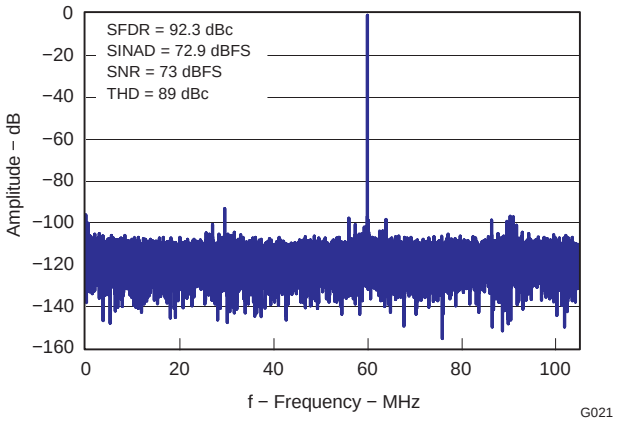

Figure 33.

FFT for 170 MHz INPUT SIGNAL

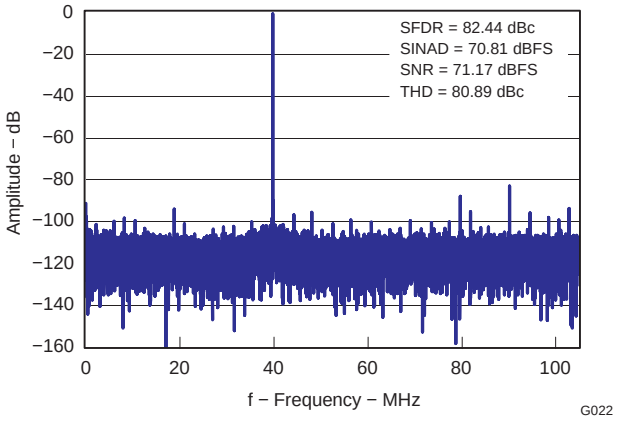

Figure 34.

FFT for 300 MHz INPUT SIGNAL

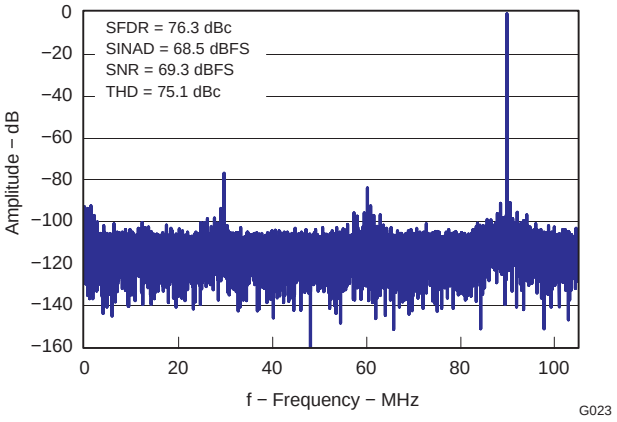

Figure 35.

FFT for 2-TONE INPUT SIGNAL (IMD)

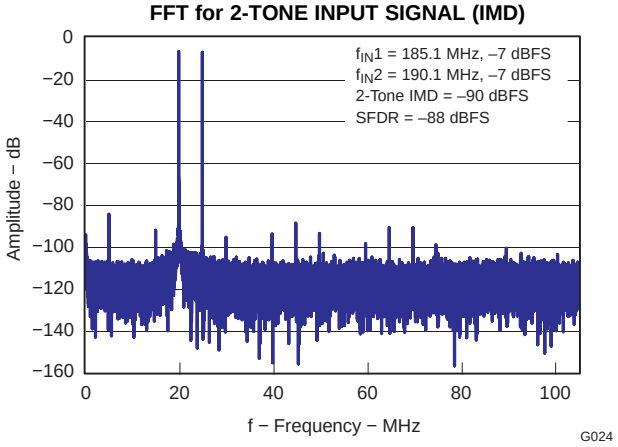

Figure 36.

FFT for 2-TONE INPUT SIGNAL (IMD)

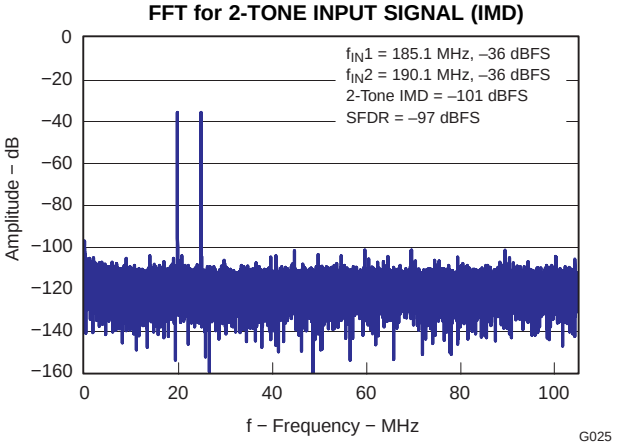

Figure 37.

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TYPICAL CHARACTERISTICS - ADS6148 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

SFDR vs INPUT FREQUENCY

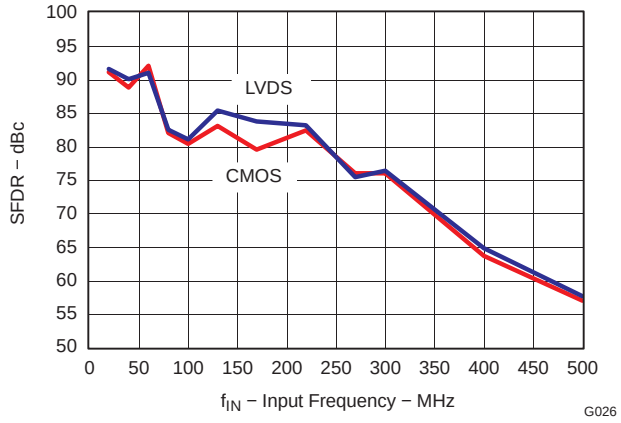

Figure 38.

SNR vs INPUT FREQUENCY

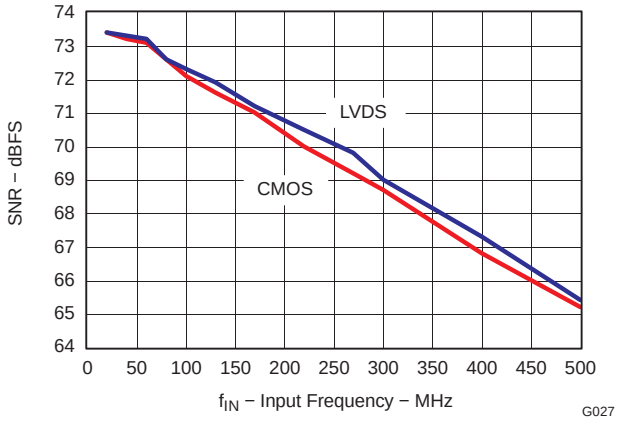

Figure 39.

SFDR vs GAIN

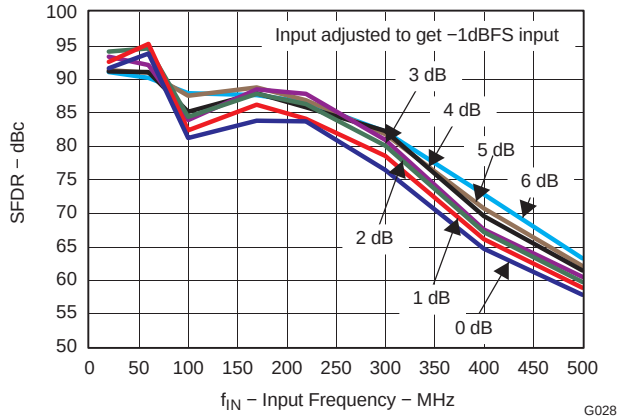

Figure 40.

SINAD vs GAIN

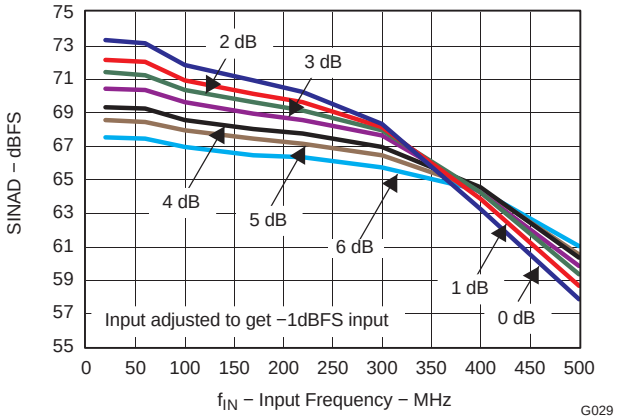

Figure 41.

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TYPICAL CHARACTERISTICS - ADS6148 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

PERFORMANCE vs INPUT AMPLITUDE

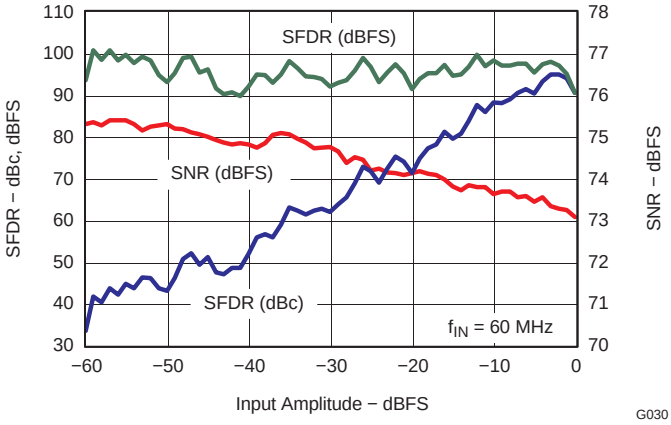

Figure 42.

PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

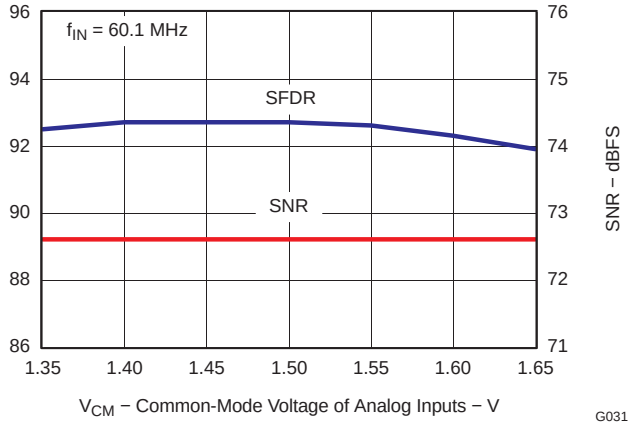

Figure 43.

PERFORMANCE vs AVDD SUPPLY

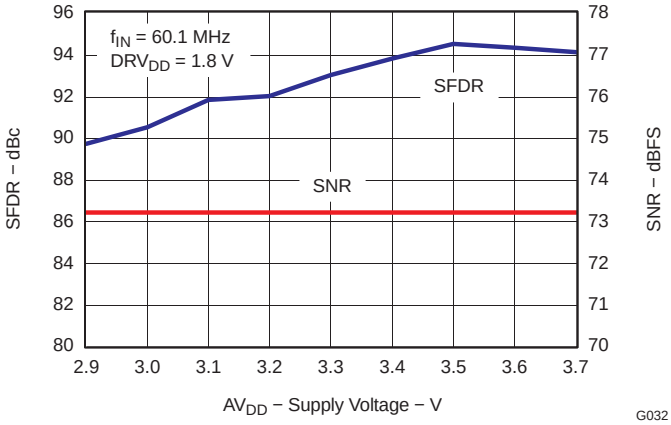

Figure 44.

PERFORMANCE vs DRVDD SUPPLY

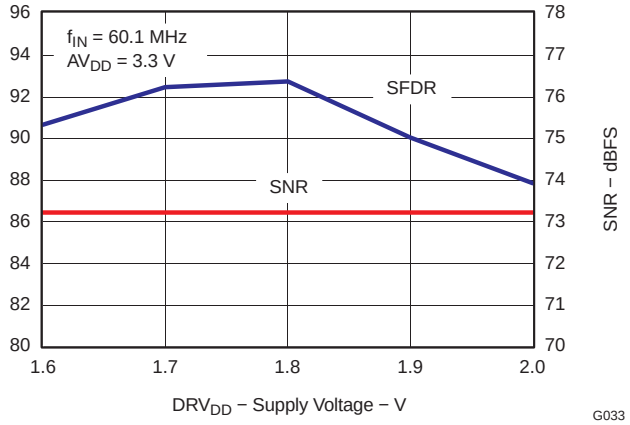

Figure 45.

TYPICAL CHARACTERISTICS - ADS6148 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

PERFORMANCE vs TEMPERATURE

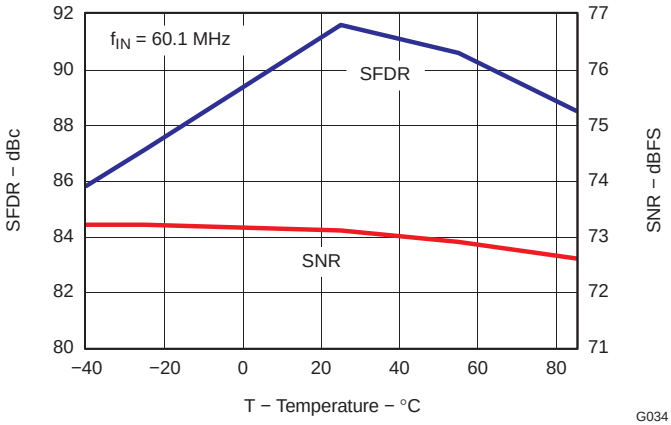

Figure 46.

PERFORMANCE vs INPUT CLOCK AMPLITUDE

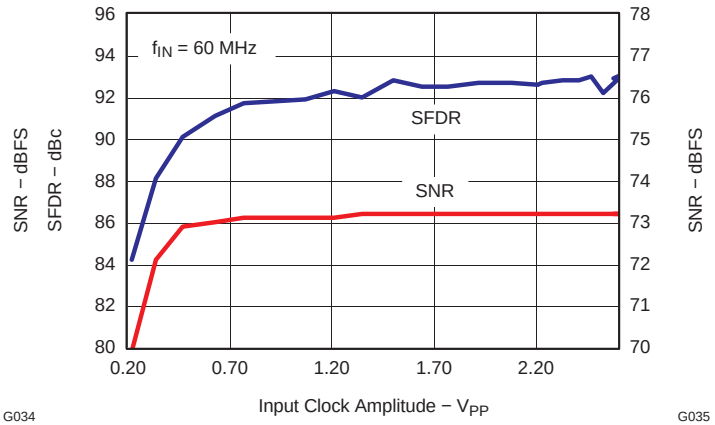

Figure 47.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

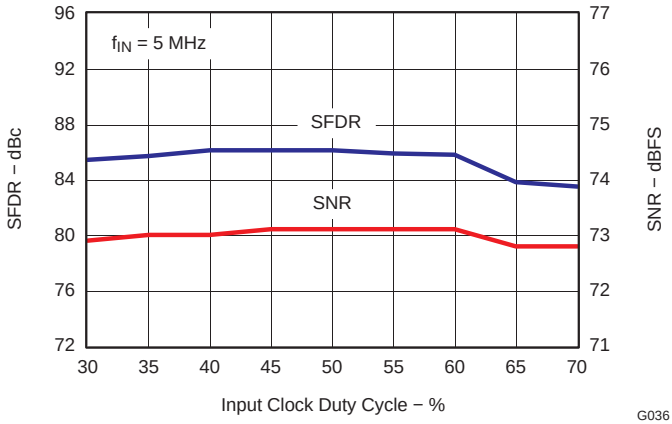

Figure 48.

PERFORMANCE vs VCM VOLTAGE

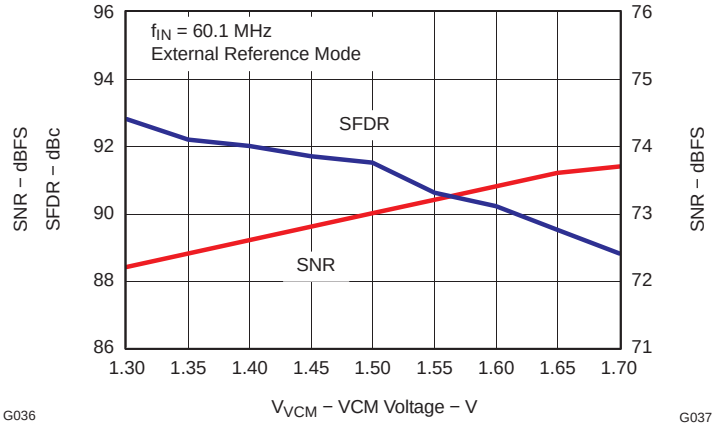

Figure 49.

OUTPUT NOISE HISTOGRAM

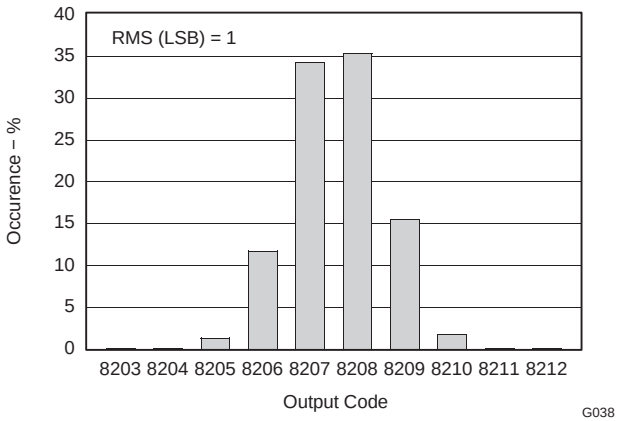

Figure 50.

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TYPICAL CHARACTERISTICS - ADS6129

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

FFT for 20 MHz INPUT SIGNAL

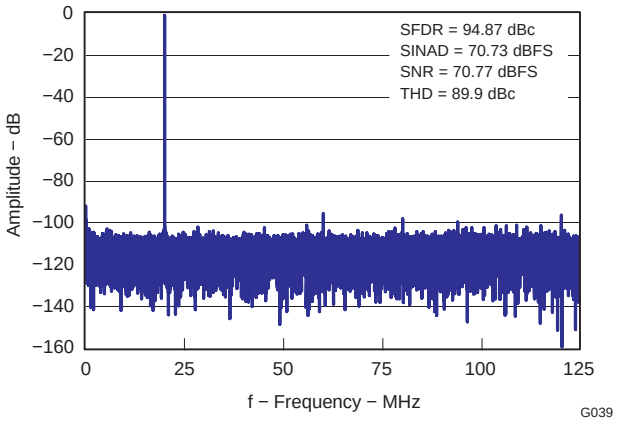

Figure 51.

FFT for 60 MHz INPUT SIGNAL

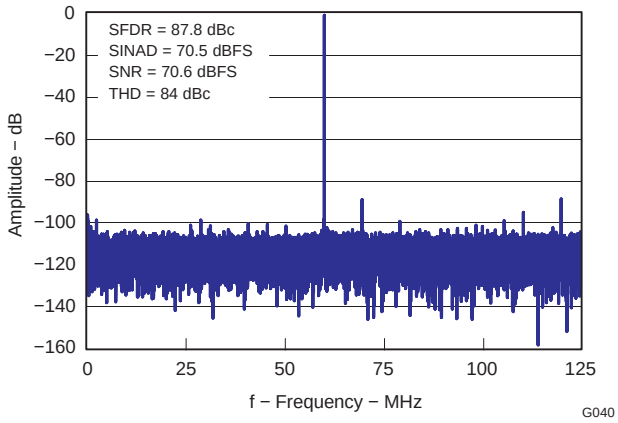

Figure 52.

FFT for 170 MHz INPUT SIGNAL

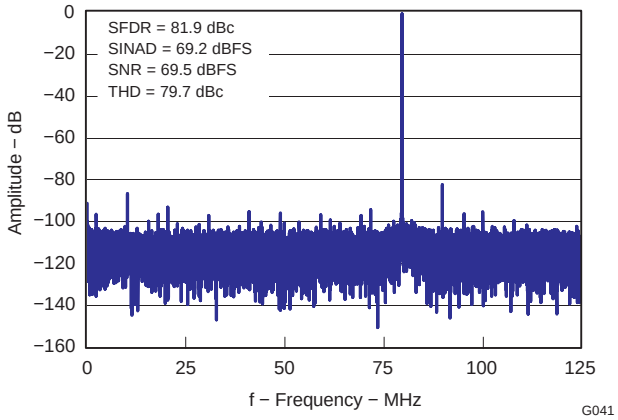

Figure 53.

FFT for 300 MHz INPUT SIGNAL

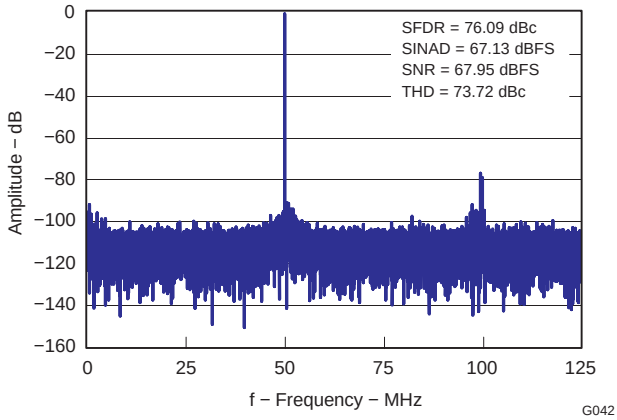

Figure 54.

FFT for 2-TONE INPUT SIGNAL (IMD)

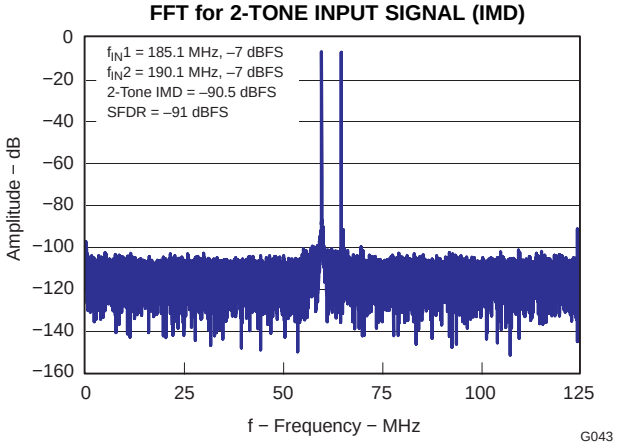

Figure 55.

FFT for 2-TONE INPUT SIGNAL (IMD)

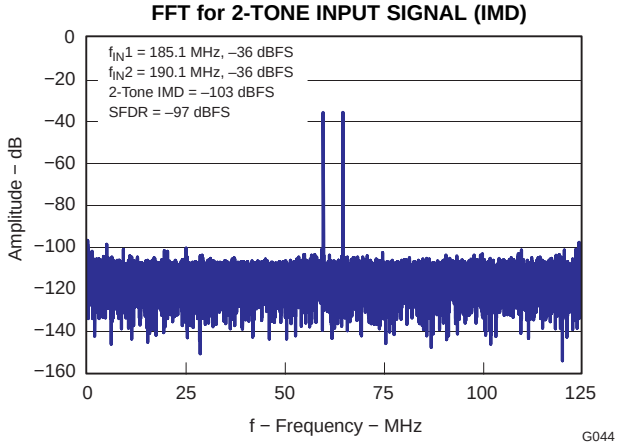

Figure 56.

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TYPICAL CHARACTERISTICS - ADS6129 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

SFDR vs INPUT FREQUENCY

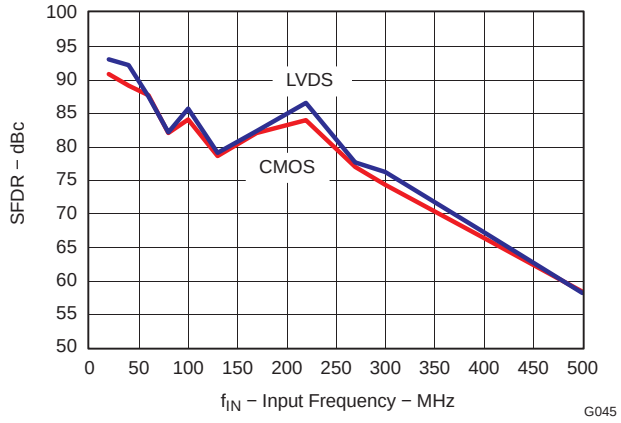

Figure 57.

SNR vs INPUT FREQUENCY

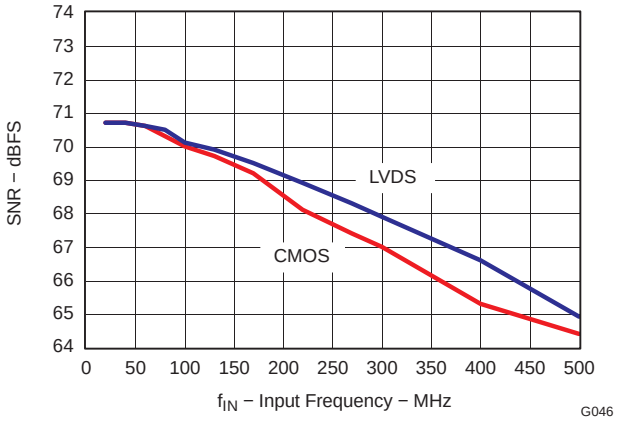

Figure 58.

SFDR vs GAIN

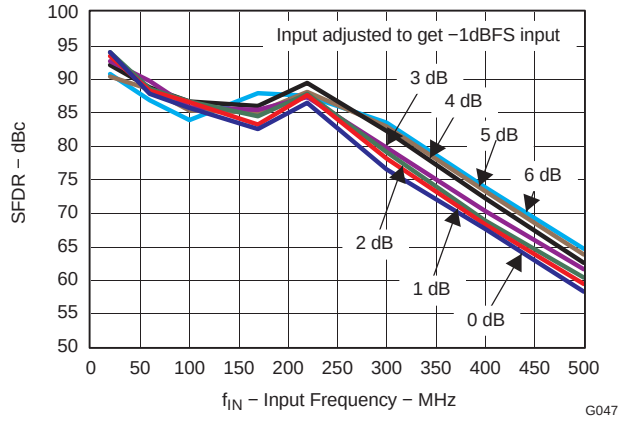

Figure 59.

SINAD vs GAIN

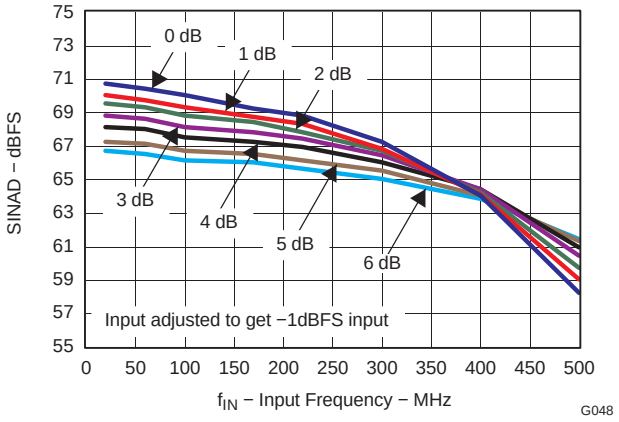

Figure 60.

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TYPICAL CHARACTERISTICS - ADS6129 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

PERFORMANCE vs INPUT AMPLITUDE

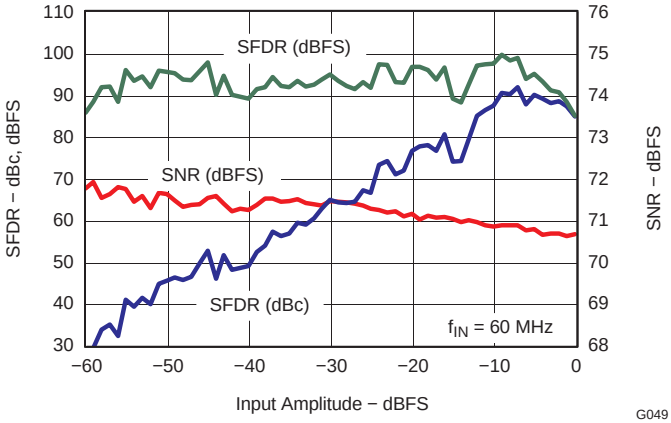

Figure 61.

PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

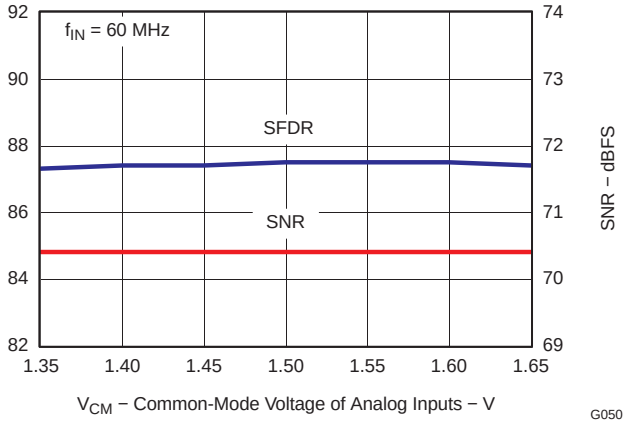

Figure 62.

PERFORMANCE vs AVDD SUPPLY

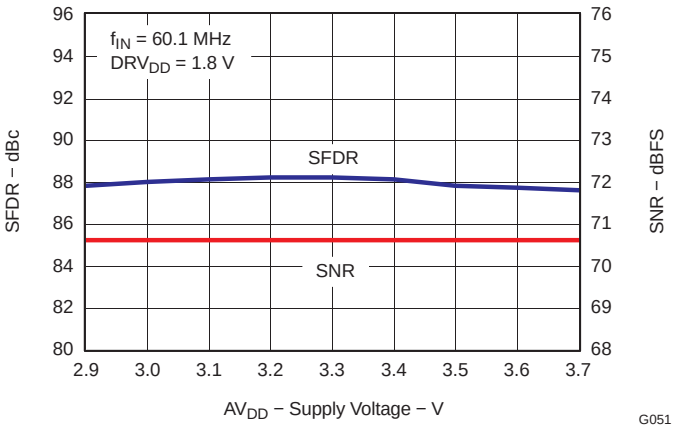

Figure 63.

PERFORMANCE vs DRVDD SUPPLY

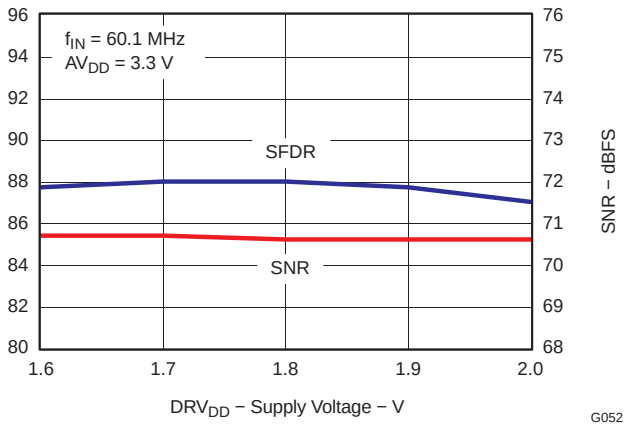

Figure 64.

TYPICAL CHARACTERISTICS - ADS6129 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

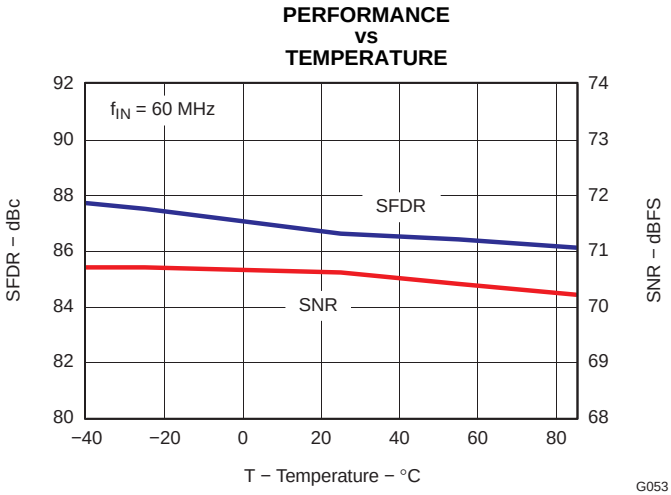

Figure 65.

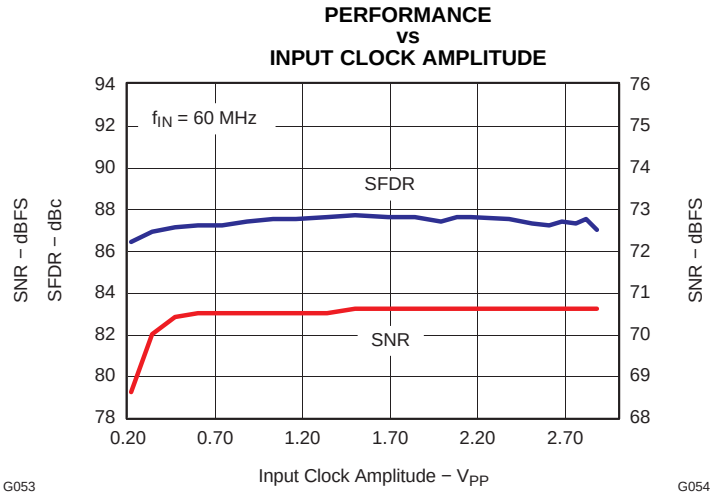

Figure 66.

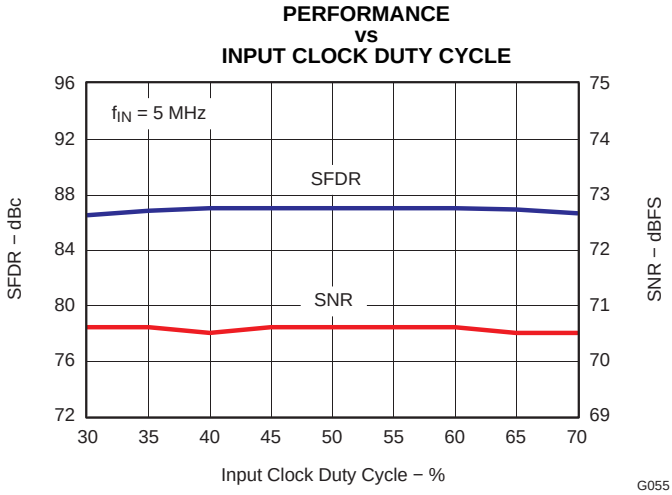

Figure 67.

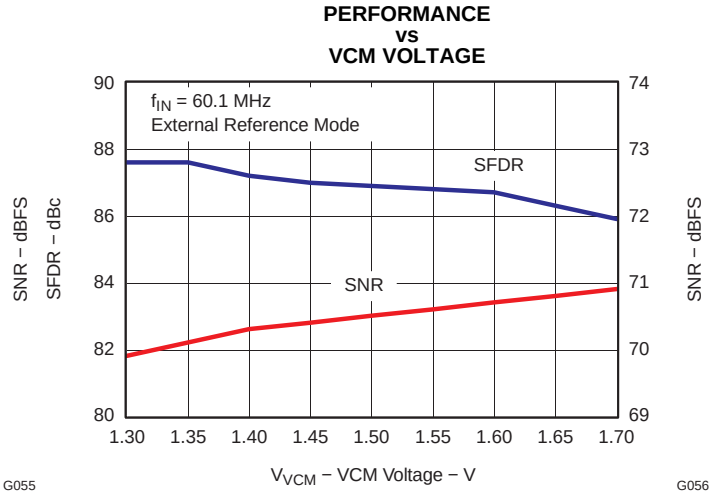

Figure 68.

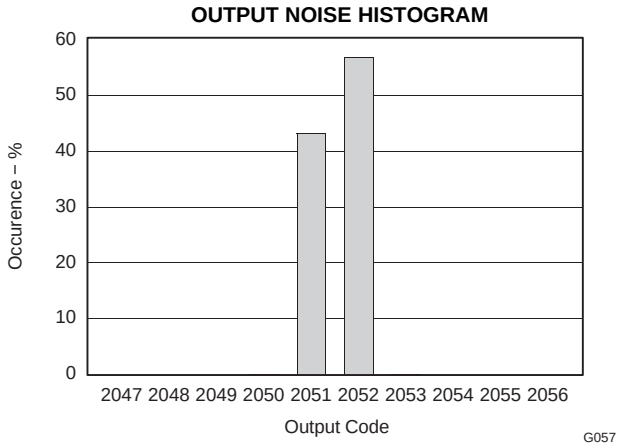

Figure 69.

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TYPICAL CHARACTERISTICS - ADS6128

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

FFT for 20 MHz INPUT SIGNAL

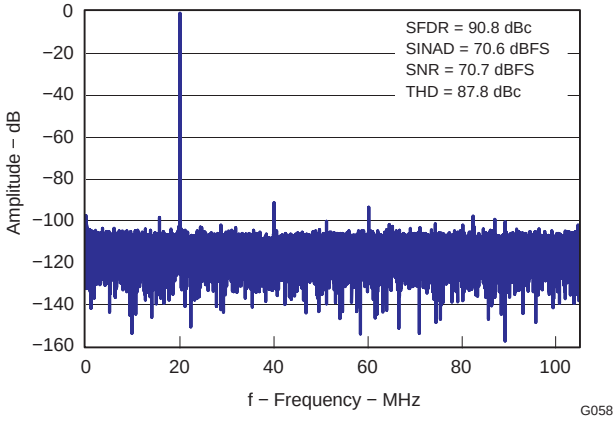

Figure 70.

FFT for 60 MHz INPUT SIGNAL

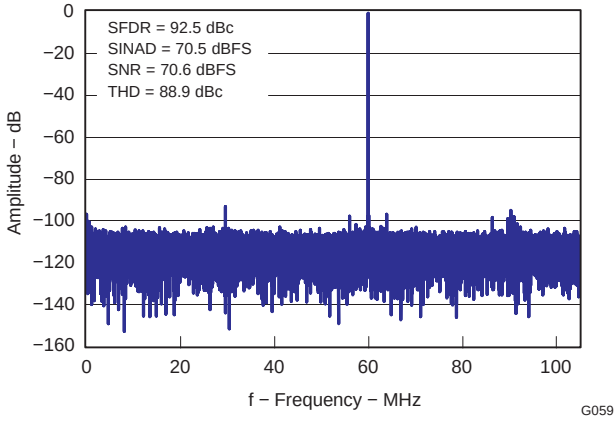

Figure 71.

FFT for 170 MHz INPUT SIGNAL

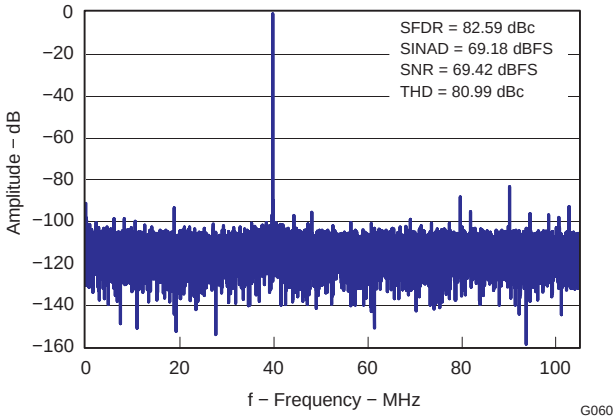

Figure 72.

FFT for 300 MHz INPUT SIGNAL

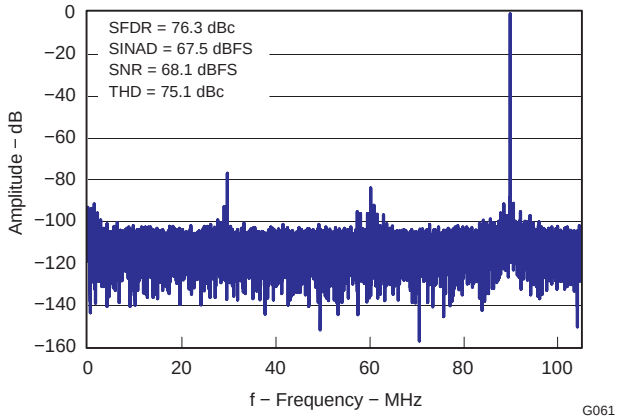

Figure 73.

FFT for 2-TONE INPUT SIGNAL (IMD)

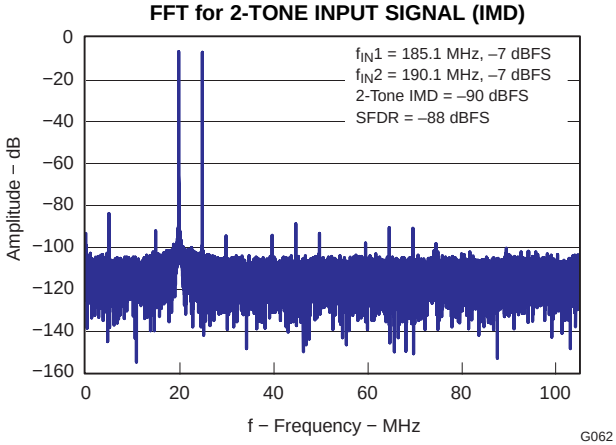

Figure 74.

FFT for 2-TONE INPUT SIGNAL (IMD)

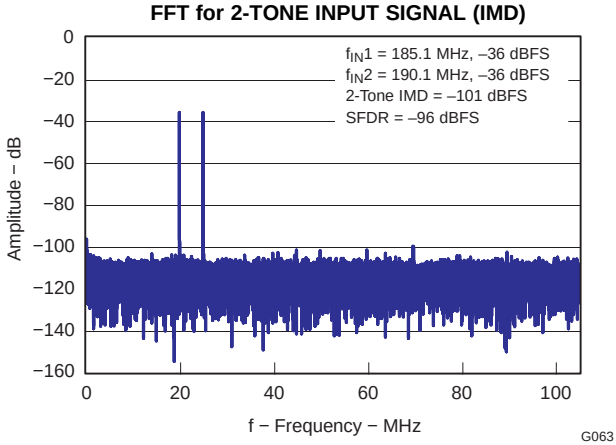

Figure 75.

TYPICAL CHARACTERISTICS - ADS6128 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

SFDR vs INPUT FREQUENCY

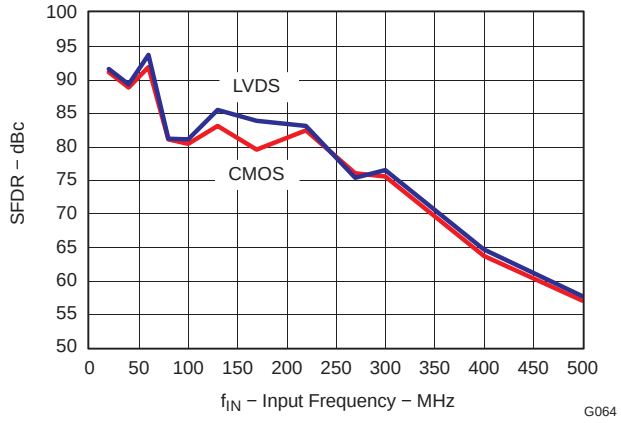

Figure 76.

SNR vs INPUT FREQUENCY

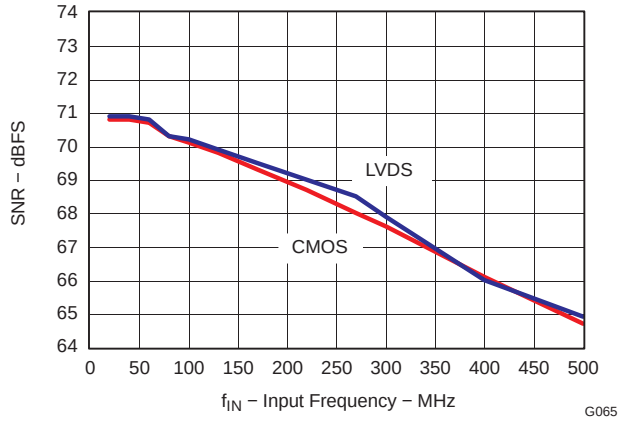

Figure 77.

SFDR vs GAIN

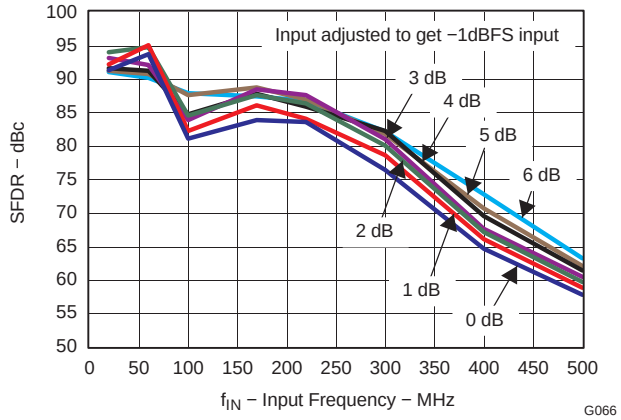

Figure 78.

SINAD vs GAIN

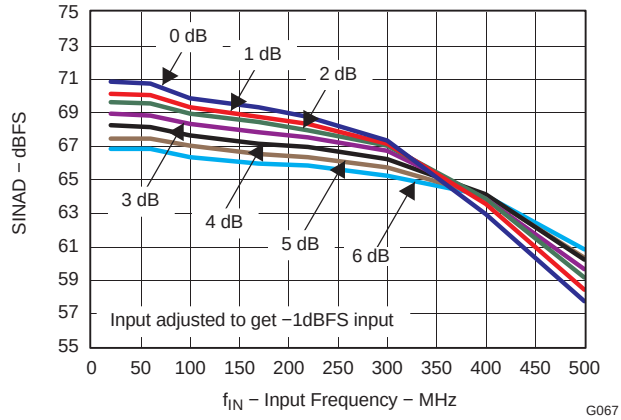

Figure 79.

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TYPICAL CHARACTERISTICS - ADS6128 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

PERFORMANCE vs INPUT AMPLITUDE

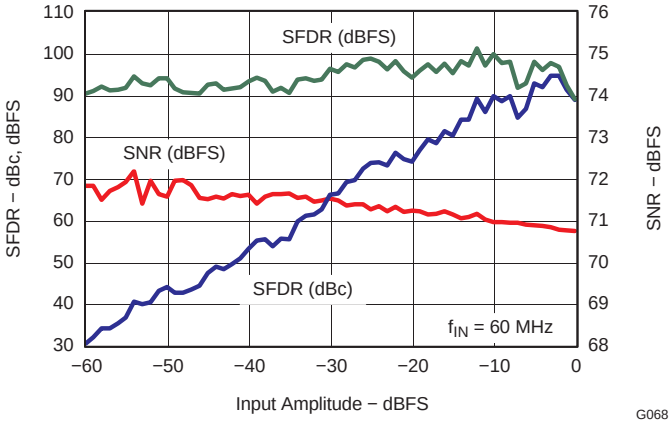

Figure 80.

PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

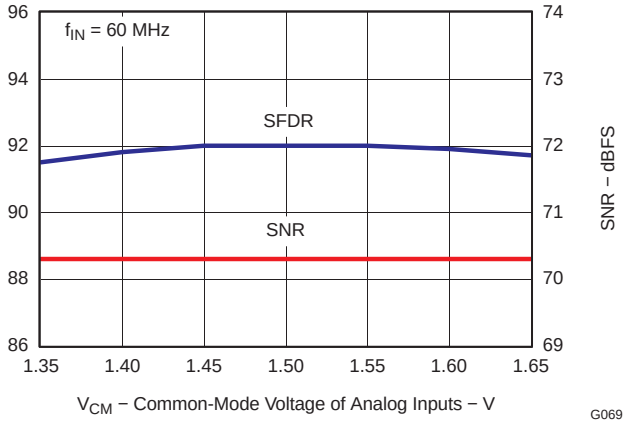

Figure 81.

PERFORMANCE vs AVDD SUPPLY

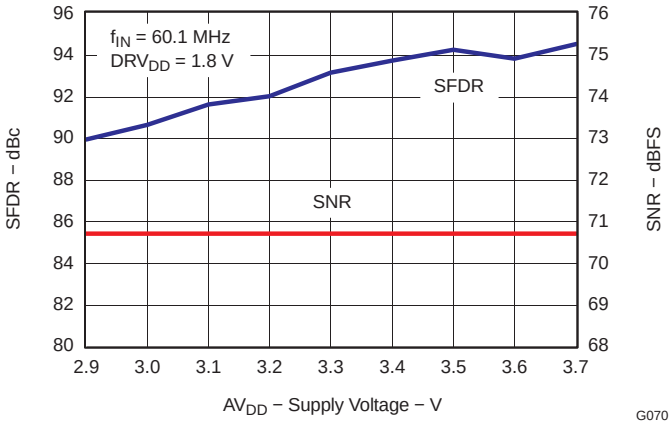

Figure 82.

PERFORMANCE vs DRVDD SUPPLY

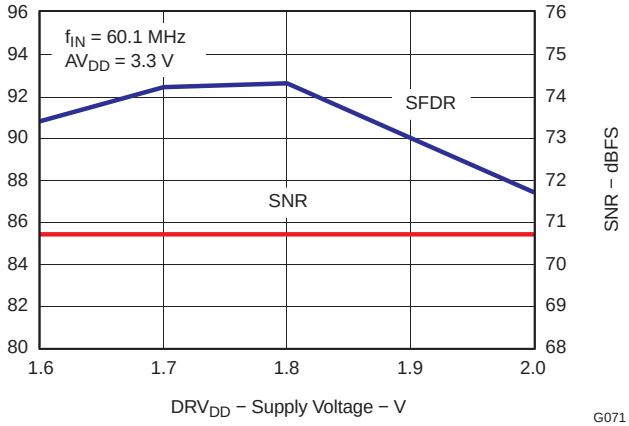

Figure 83.

TYPICAL CHARACTERISTICS - ADS6128 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

PERFORMANCE vs TEMPERATURE

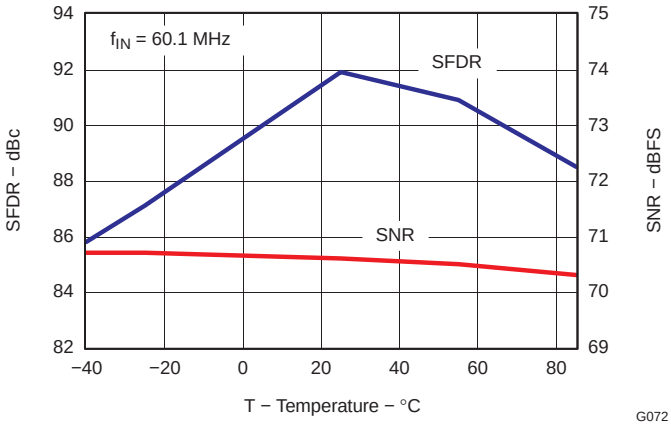

Figure 84.

PERFORMANCE vs INPUT CLOCK AMPLITUDE

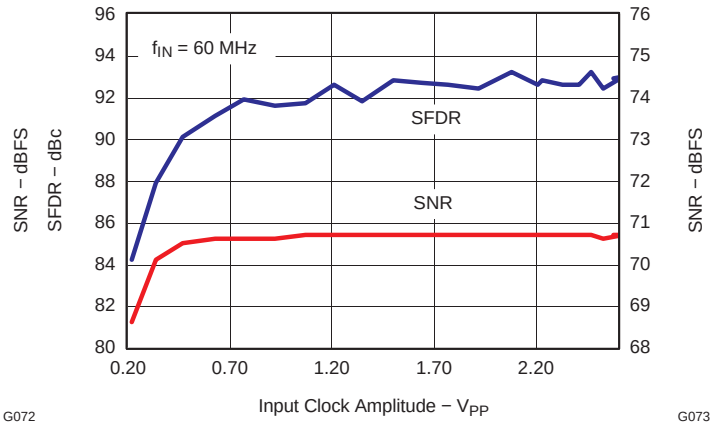

Figure 85.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

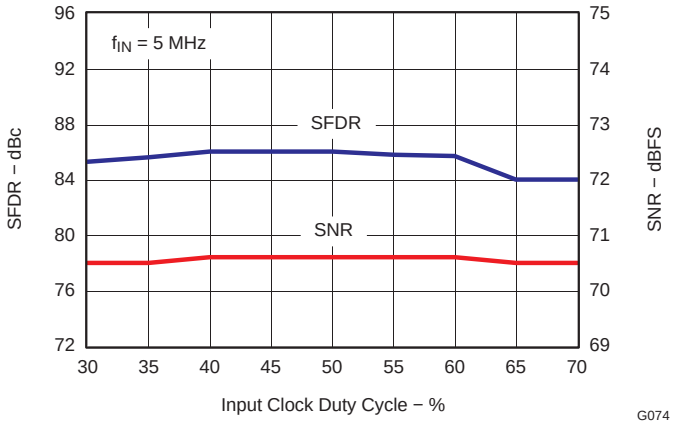

Figure 86.

PERFORMANCE vs VCM VOLTAGE

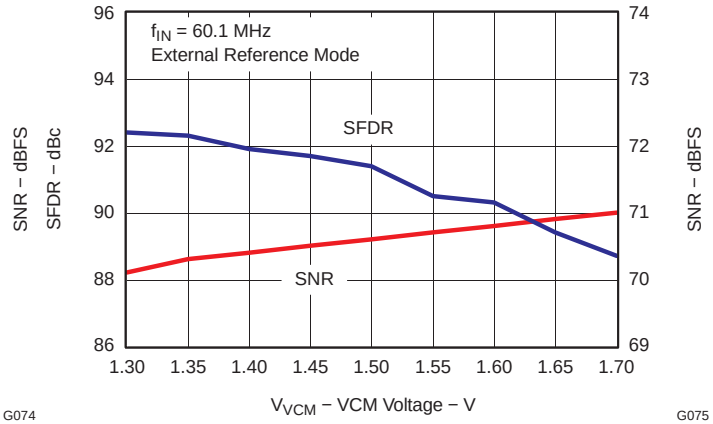

Figure 87.

OUTPUT NOISE HISTOGRAM

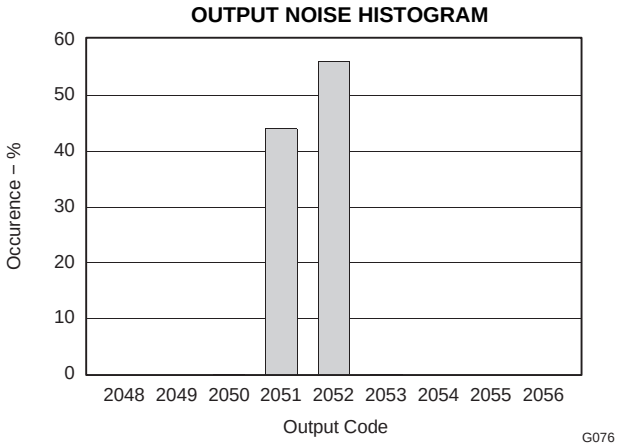

Figure 88.

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TYPICAL CHARACTERISTICS - COMMON PLOTS

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 DBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

CMRR vs INPUT FREQUENCY

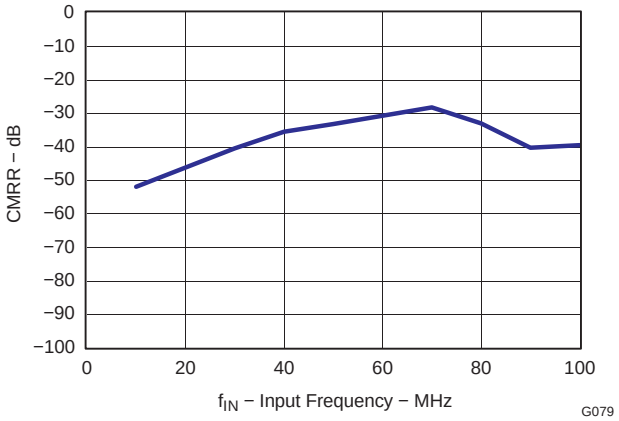

Figure 89.

TOTAL POWER vs SAMPLING FREQUENCY

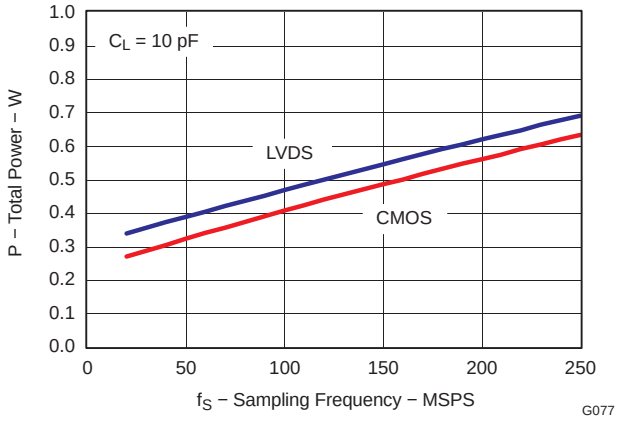

Figure 90.

DRVDD CURRENT vs SAMPLING FREQUENCY

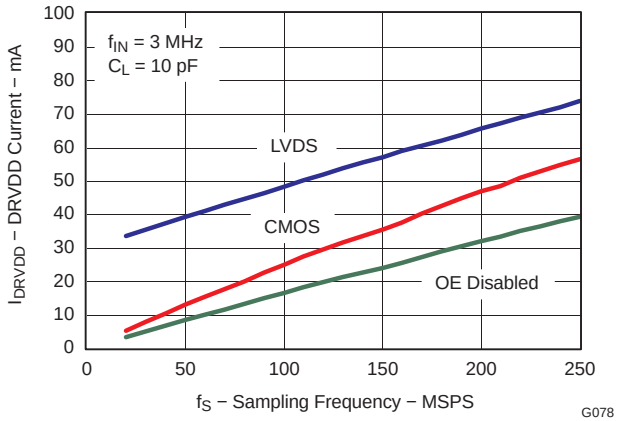

Figure 91.

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CONTOUR PLOTS - ADS6149/ADS6148/ADS6129/ADS6128

Plots are at 25°C, AVDD = 3.3V, DRVDD = 1.8 V, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

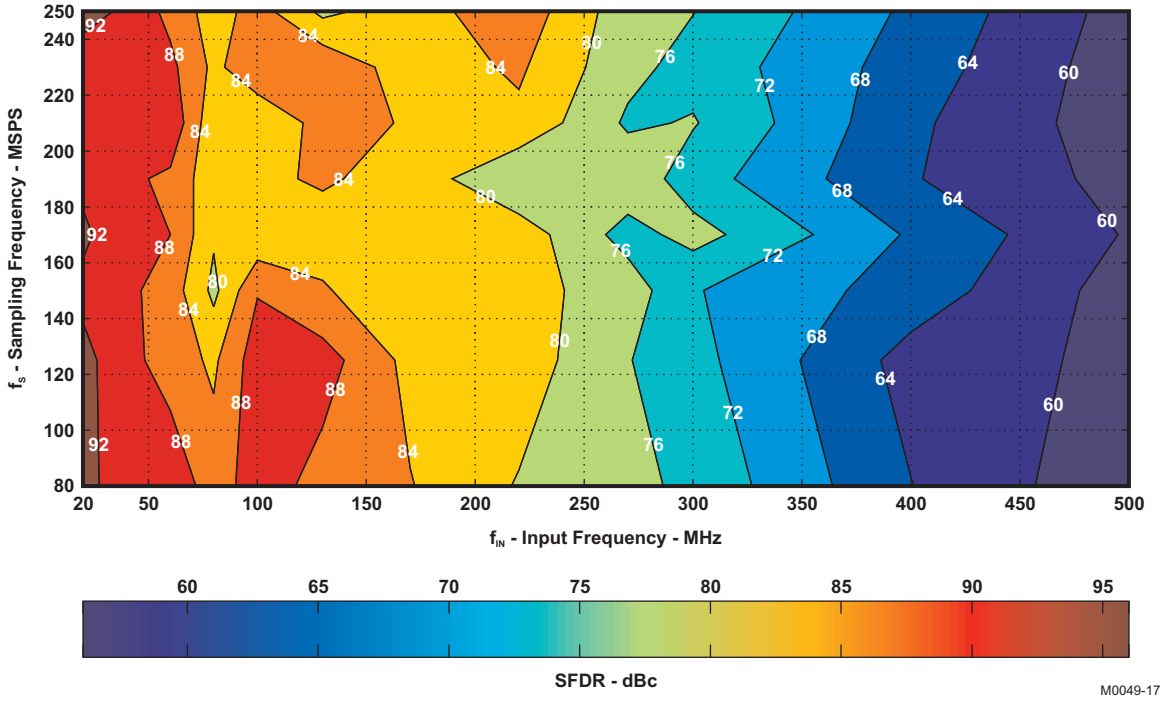

Figure 92. SFDR Contour Plot (0 dB gain)

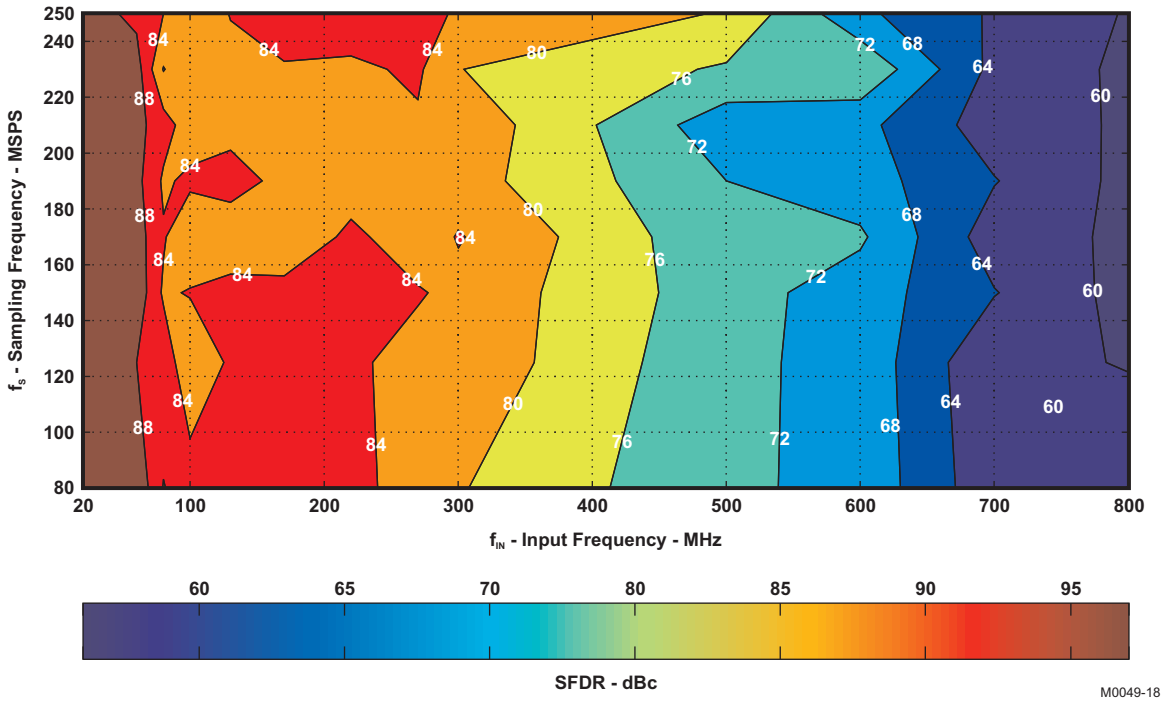

Figure 93. SFDR Contour Plot (6 dB gain)

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CONTOUR PLOTS - ADS6149/ADS6148

Plots are at 25°C, AVDD = 3.3V, DRVDD = 1.8 V, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface (unless otherwise noted)

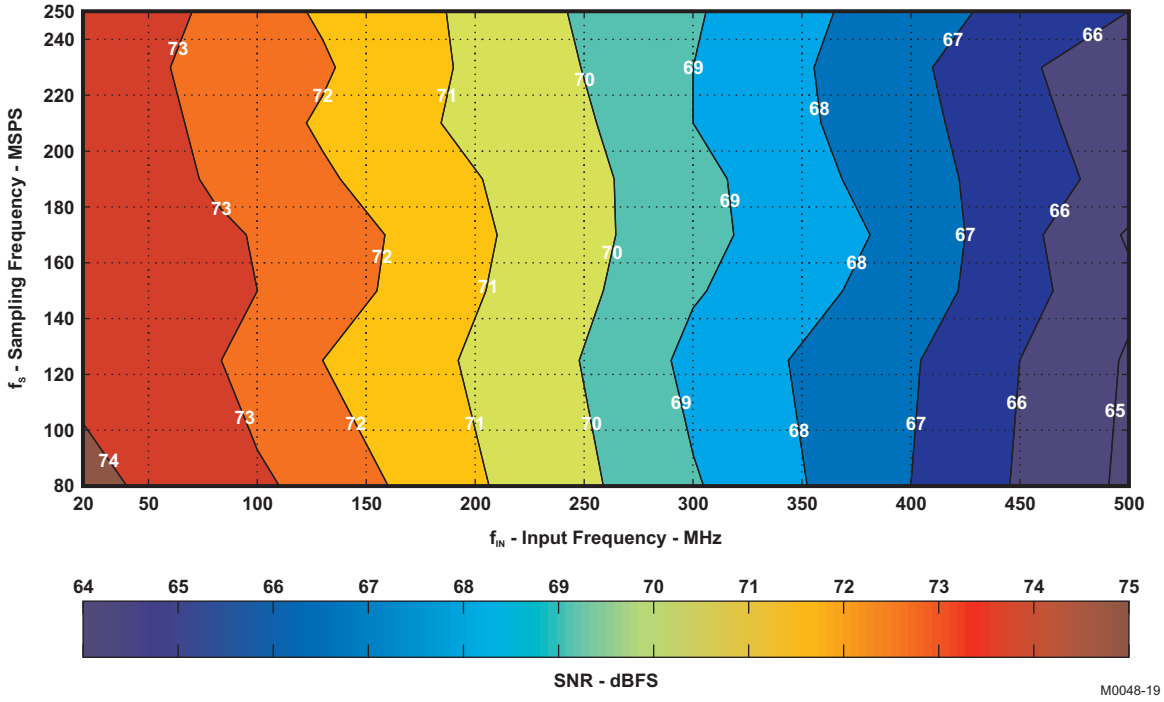

Figure 94. SNR Contour Plot (0 dB gain)

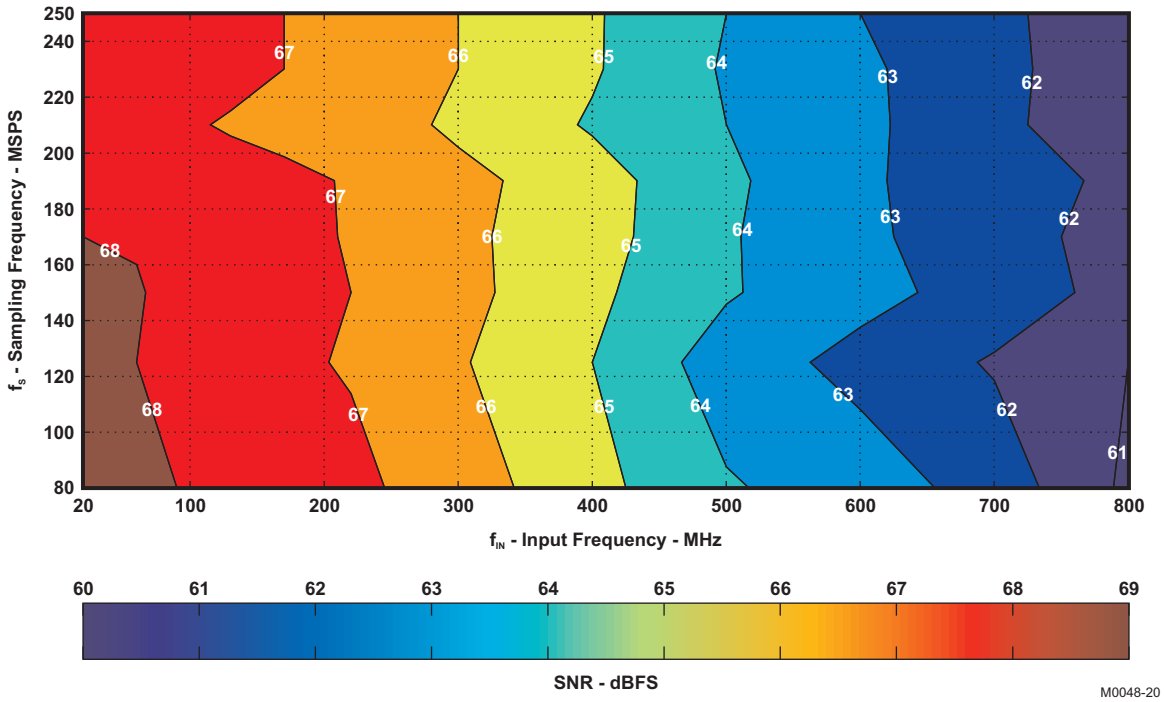

Figure 95. SNR Contour Plot (6 dB gain)

APPLICATION INFORMATION

THEORY OF OPERATION

ADS6149/48 and ADS6129/28 is a family of high performance, low power 14-bit and 12-bit pipeline A/D converters with maximum sampling rate up to 250 MSPS.

At every rising edge of the input clock, the analog input signal is sampled and sequentially converted by a pipeline of low resolution stages. In each stage, the sampled and held signal is converted by a high speed, low resolution flash sub-ADC. The difference (residue) between the stage input and its quantized equivalent is gained and propagates to the next stage. At every clock, each succeeding stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block to create the final 14 or 12 bit code, after a data latency of 18 clock cycles.

The digital output is available as either DDR LVDS or parallel CMOS and coded in either straight offset binary or binary 2s complement format.

The dynamic offset of the first stage sub-ADC limits the maximum analog input frequency to about 500MHz (with $2V_{PP}$ amplitude) and about 800MHz (with $1V_{PP}$ amplitude).

ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture.

This differential topology results in a good AC performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5V, available on VCM pin. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.5V and VCM – 0.5V, resulting in a 2Vpp differential input swing.

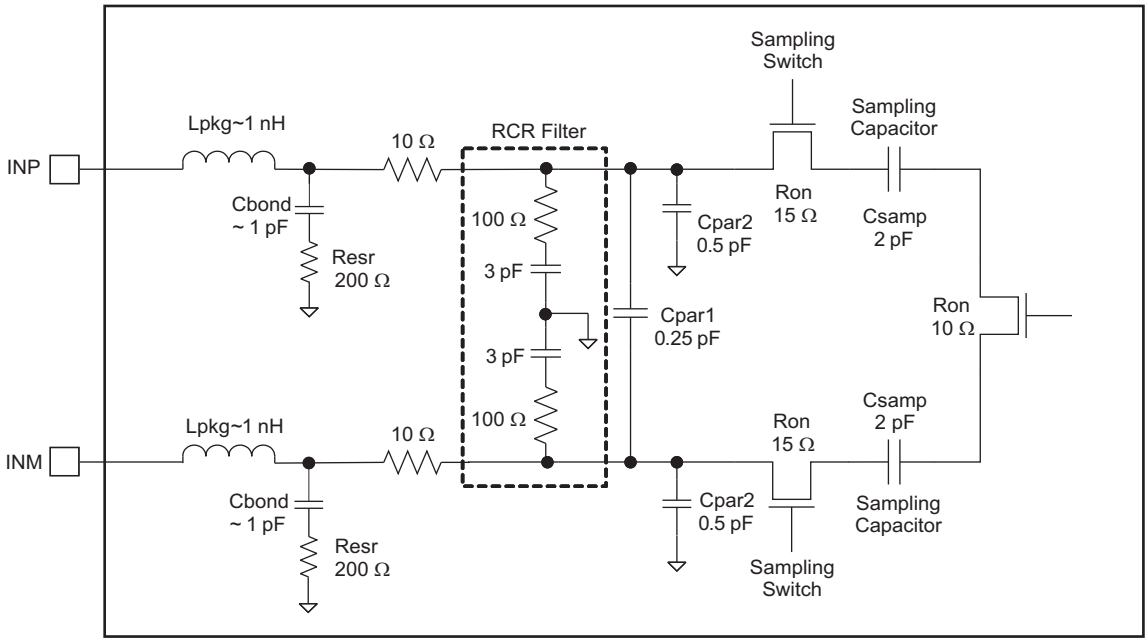

Figure 96. Analog Input Equivalent Circuit

The input sampling circuit has a high 3-dB bandwidth that extends up to 700 MHz (measured from the input pins to the sampled voltage).

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Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. A 5 Ω to 15 Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics. It is also necessary to present low impedance (< 50 Ω) for the common mode switching currents. This can be achieved by using two resistors from each input terminated to the common mode voltage (VCM).

Note that the device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the glitches caused by the opening and closing of the sampling capacitors. The cut-off frequency of the R-C filter involves a trade-off. A lower cut-off frequency (larger C) absorbs glitches better, but also reduces the input bandwidth and the maximum input frequency that can be supported. On the other hand, with no internal R-C filter, high input frequency can be supported, but now the sampling glitches need to be supplied by the external driving circuit. This has limitations due to the presence of the package bond-wire inductance.

In ADS61x9/x8, the R-C component values have been optimized while supporting high input bandwidth (up to 750 MHz). However, in applications where high input frequency support is not required, the filtering of the glitches can be improved further using an external R-C-R filter (as shown in Figure 99 and Figure 100).

In addition to the above, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance must be considered. Figure 97 and Figure 98 show the impedance (Zin = Rin || Cin) looking into the ADC input pins.

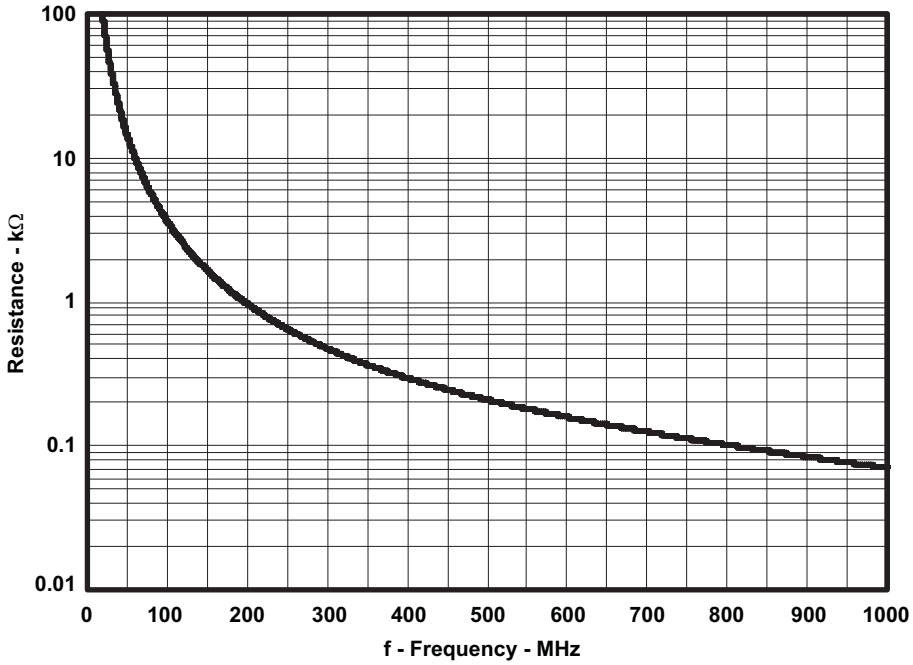

Figure 97. ADC Analog Input Resistance (Rin) Across Frequency

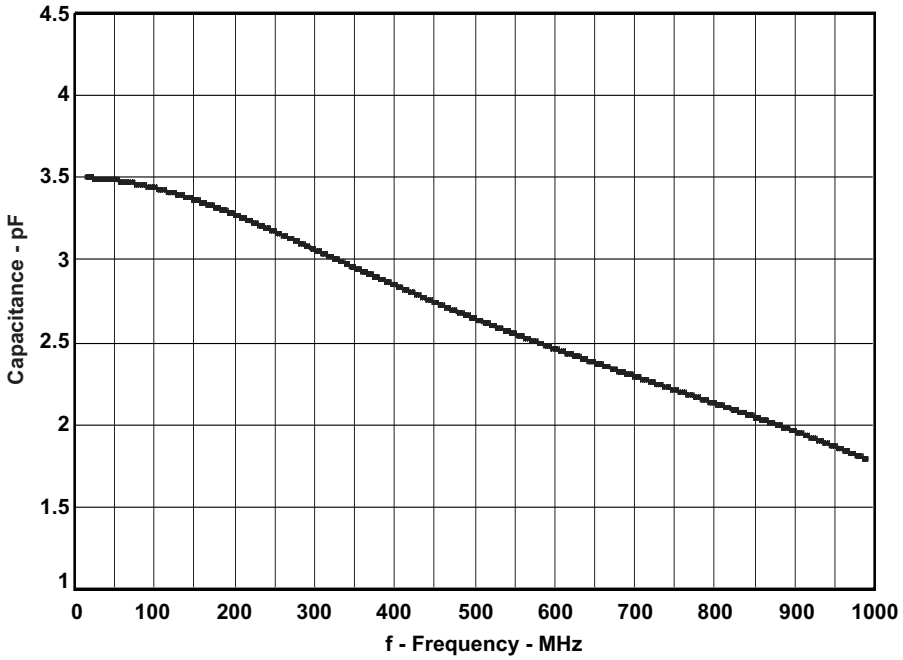

Figure 98. ADC Analog Input Capacitance (Cin) Across Frequency

Driving Circuit

Two example driving circuit configurations are shown in Figure 99 and Figure 100 – one optimized for low bandwidth (low input frequencies) and the other one for high bandwidth to support higher input frequencies.

In Figure 99, an external R-C-R filter using 22pF has been used. Together with the series inductor (39nH), this combination forms a filter and absorbs the sampling glitches. Due to the large capacitor (22pF) in the R-C-R and the 15Ω resistors in series with each input pin, the drive circuit has low bandwidth, and supports low input frequencies (< 100MHz)..

To support high input frequencies (up to about 300MHz, see Figure 100), the capacitance used in the R-C-R is reduced to 3.3pF and the series inductors are shorted out. Together with the lower series resistors (5Ω), this drive circuit provides high bandwidth and supports high input frequencies.

A transformer such as ADT1-1WT or ETC1-1-13 can be used up to 300MHz.

In Figure 100, by dropping the external R-C-R filter, the drive circuit has high bandwidth and can support high input frequencies (> 300MHz). For example, a transformer such as the ADTL2-18 can be used.

Note that both the drive circuits have been terminated by 50Ω near the ADC side. The termination is accomplished using a 25Ω resistor from each input to the 1.5V common-mode (VCM) from the device. This biases the analog inputs around the required common-mode voltage.

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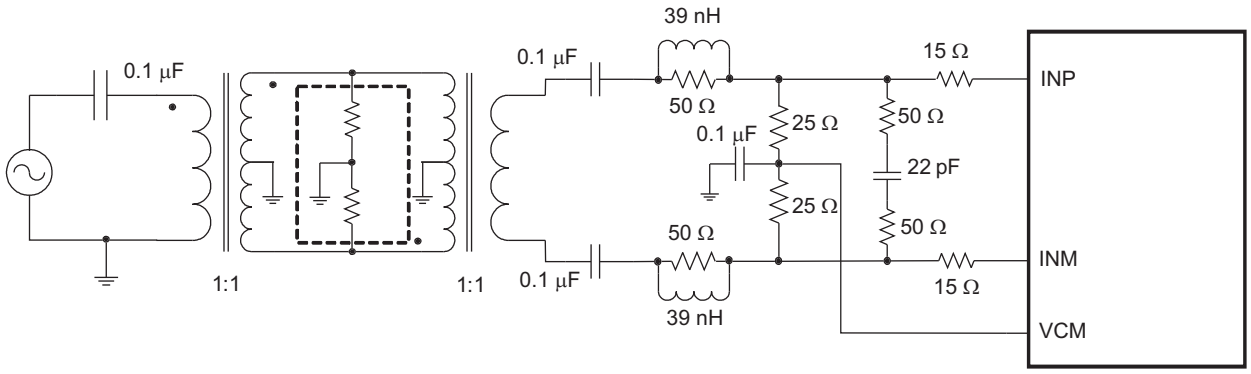

Figure 99. Drive Circuit with Low Bandwidth (for low input frequencies)

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back to back helps minimize this mismatch and good performance is obtained for high frequency input signals. An additional termination resistor pair may be required between the two transformers as shown in the figures. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side have to be chosen to get an effective 50Ω (in the case of 50Ω source impedance).

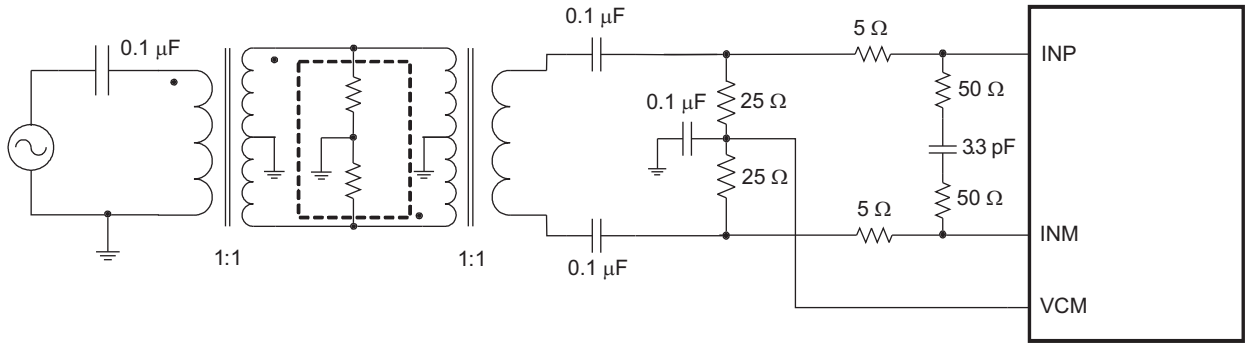

Figure 100. Drive Circuit with High Bandwidth (for high input frequencies)

Input Common-Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1µF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. The input stage of the ADC sinks a common-mode current in the order of 500µA (per input pin, at 250 MSPS). Equation 1 describes the dependency of the common-mode current and the sampling frequency.

$$\frac{500\ \mu A \times Fs}{250\ MSPS} \quad (1)$$

This equation helps to design the output capability and impedance of the CM driving circuit accordingly.

REFERENCE

ADS614X/2X has built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the on-chip integration of the requisite reference capacitors eliminates the need for external decoupling. The full-scale input range of the converter can be controlled in the external reference mode as explained below. The internal or external reference modes can be selected by programming the serial interface register bit **<REF>**.

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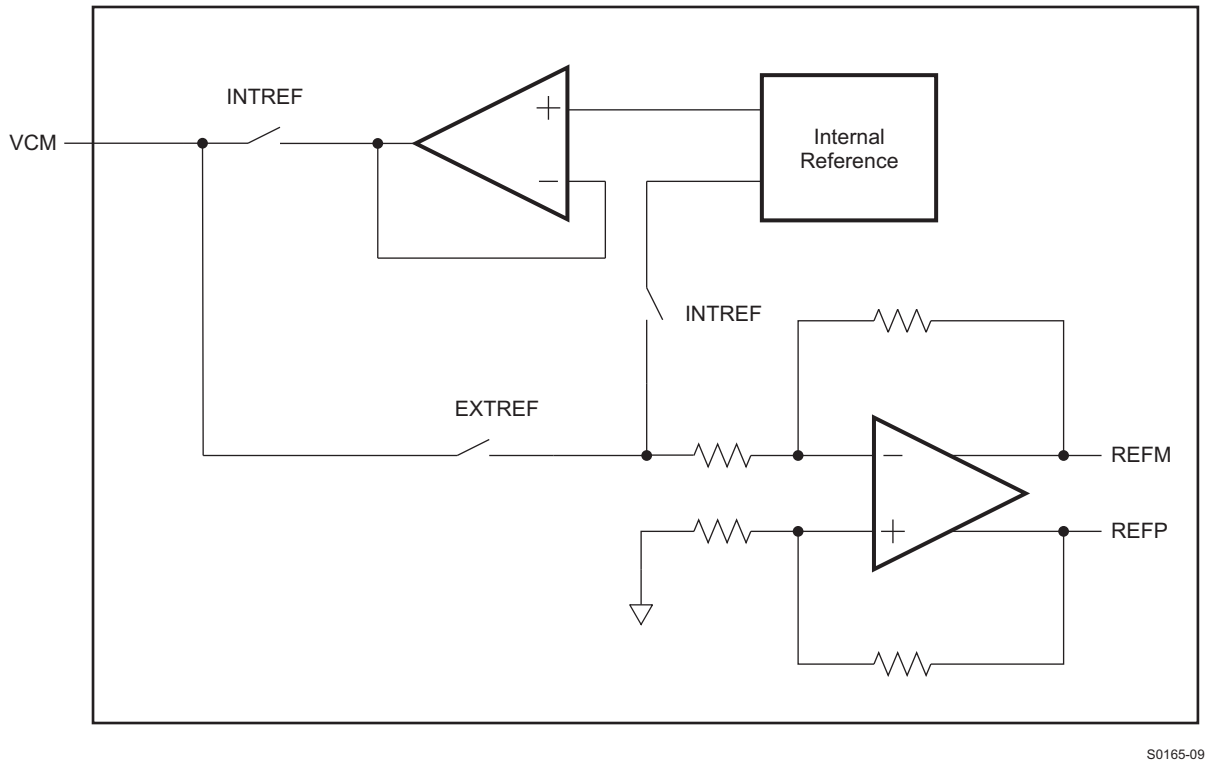

Figure 101. Reference Section

Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5V nominal) is output on VCM pin, which can be used to externally bias the analog input pins.

External Reference

When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by Equation 2.

Full-scale differential input pp = (Voltage forced on VCM) × 1.33 (2)

In this mode, the 1.5V common-mode voltage to bias the input pins has to be generated externally.

CLOCK INPUT

ADS614X/2X clock inputs can be driven differentially (sine, LVPECL or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This allows using transformer-coupled drive circuits for sine wave clock or ac-coupling for LVPECL, LVDS clock sources.

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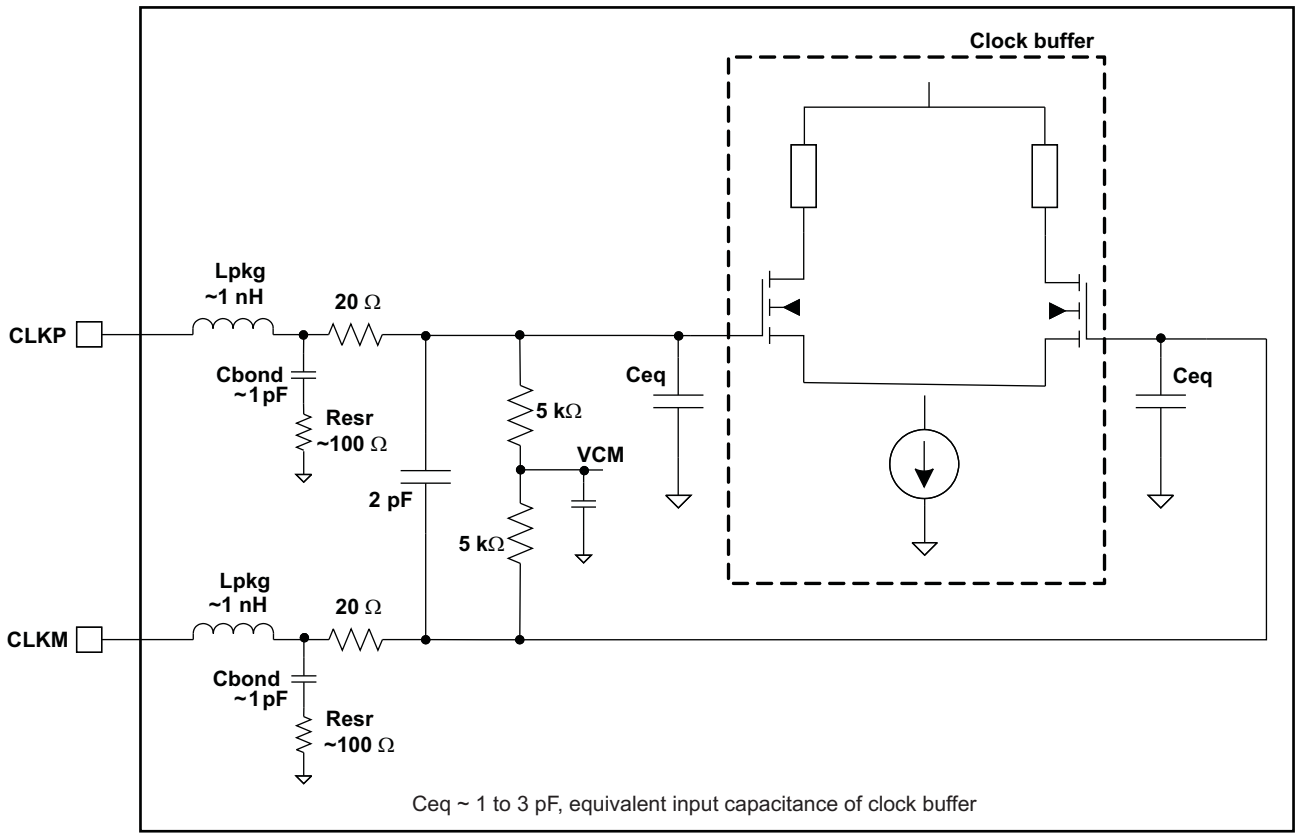

Figure 102. Internal Clock Buffer

Single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-μF capacitor, as shown in Figure 104. For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with low jitter. Band-pass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input.

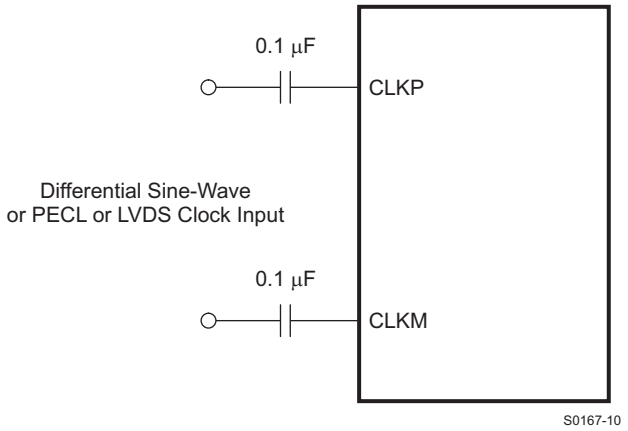

Figure 103. Differential Clock Driving Circuit

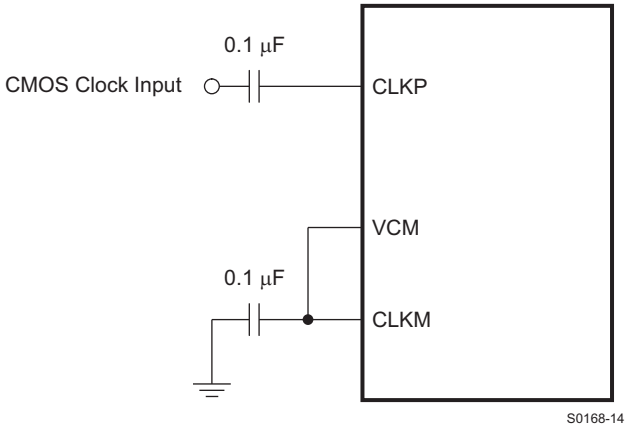

Figure 104. Single-Ended Clock Driving Circuit

FINE GAIN CONTROL

ADS614X/2X includes gain settings that can be used to get improved SFDR performance (compared to no gain). The gain is programmable from 0dB to 6dB (in 0.5 dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 9.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades about 0.5–1dB. The SNR degradation is less at high input frequencies. As a result, the gain is useful at high input frequencies as the SFDR improvement is significant with marginal degradation in SNR.

So, the gain can be used to trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB.

Table 9. Full-Scale Range Across Gains

Gain, dB	Type	Full-Scale, V_{PP}
0	Default after reset	2V
1	Fine, programmable	1.78
2		1.59
3		1.42
4		1.26
5		1.12
6		1.00

OFFSET CORRECTION

ADS61x9/x8 has an internal offset correction algorithm that estimates and corrects the dc offset up to ±10mV. The correction can be enabled using the serial register bit <ENABLE OFFSET CORR>. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using register bits <OFFSET CORR TIME CONSTANT> as described inTable 10.

After the offset is estimated, the correction can be locked in by setting <OFFSET CORR TIME CONSTANT> = 0. Once locked, the last estimated value is used for offset correction every clock cycle. Note that offset correction is disabled by default after reset.

Figure 105 shows the time response of the offset correction algorithm, after it is enabled.

Table 10. Time Constant of Offset Correction Algorithm

<OFFSET CORR TIME CONSTANT> D3-D0	Time constant (TCCLK), number of clock cycles	Time constant, sec (=TCCLK x 1/Fs) (1)
0000	256 k	1 ms
0001	512 k	2 ms
0010	1 M	4 ms
0011	2 M	8 ms
0100	4 M	17 ms
0101	8 M	33 ms
0110	16 M	67 ms
0111	32 M	134 ms
1000	64 M	268 ms
1001	128 M	536 ms
1010	256 M	1.1 s
1011	512 M	2.2 s
1100	RESERVED	–
1101	RESERVED	–
1110	RESERVED	–
1111	RESERVED	–

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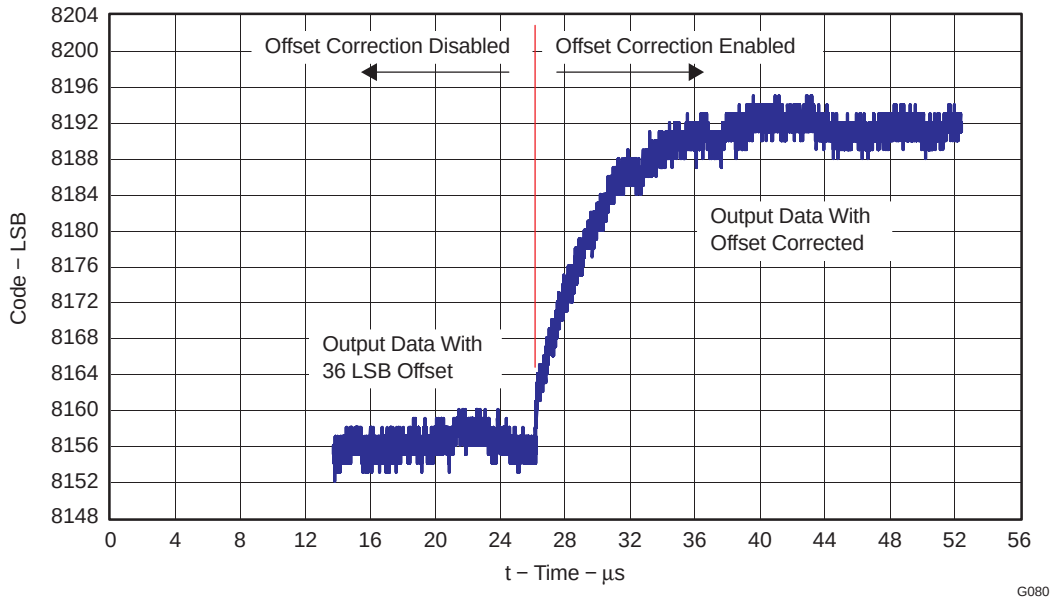

Figure 105. Output Code Time Response With Offset Correction Enabled

POWER DOWN

ADS614X/2X has three power down modes – power down global, standby and output buffer disable.

Power Down Global

In this mode, the entire chip including the A/D converter, internal reference and the output buffers are powered down resulting in reduced total power dissipation of about 20 mW. The output buffers are in high impedance state. The wake-up time from global power down to data becoming valid in normal mode is typically 25 µs.

This can be controlled using register bit **<PDN GLOBAL>** or using SDATA pin (in parallel configuration mode).

Standby

Here, only the A/D converter is powered down and internal references are active, resulting in fast wake-up time of 300 ns. The total power dissipation in standby is about 120 mW.

This can be controlled using register bit **<STANDBY>**.

Output Buffer Disable

The output buffers can be disabled and put in high impedance state – wakeup time from this mode is fast, about 40 ns. This can be controlled using register bit **<PDN OBUF>**.

Input Clock Stop

In addition to the above, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is about 120 mW.

POWER SUPPLY SEQUENCE

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated in the device. Externally, they can be driven from separate supplies or from a single supply.

DIGITAL OUTPUT INFORMATION

ADS614X/2X provides 14-bit/12-bit data and an output clock synchronized with the data.

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Output Interface

Two output interface options are available – Double Data Rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit **<ODI>** or using DFS pin in parallel configuration mode.

DDR LVDS Outputs

In this mode, the data bits and clock are output using LVDS (Low Voltage Differential Signal) levels. Two data bits are multiplexed and output on each LVDS differential pair.

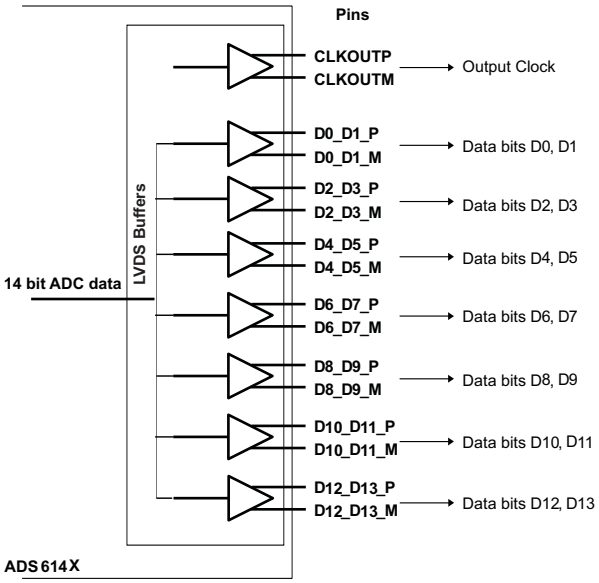

Figure 106. 14-Bit ADC LVDS Outputs

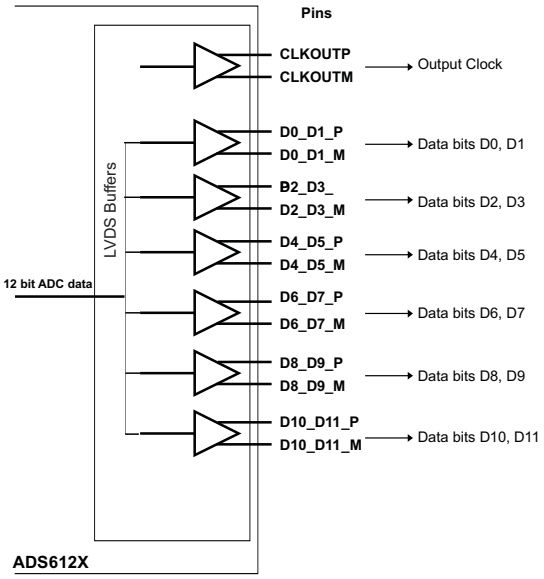

Figure 107. 12-Bit ADC LVDS Outputs

Even data bits D0, D2, D4… are output at the falling edge of CLKOUTP and the odd data bits D1, D3, D5… are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP have to be used to capture all of the data bits (see Figure 108).

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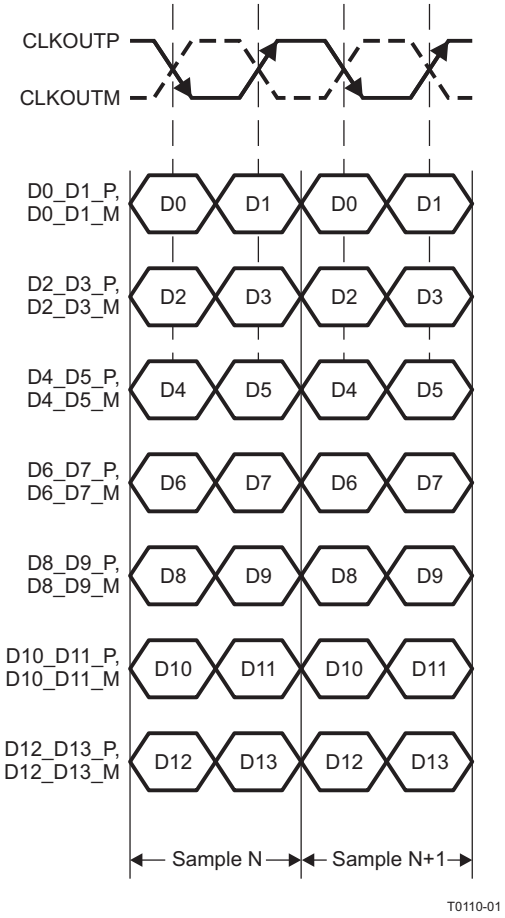

Figure 108. DDR LVDS Interface

LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 109. The buffer is designed to present an output impedance of 100 Ω (Rout). The differential outputs can be terminated at the receive end by a 100 Ω termination. The buffer output impedance behaves like a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity. Note that this internal termination cannot be disabled and its value cannot be changed.

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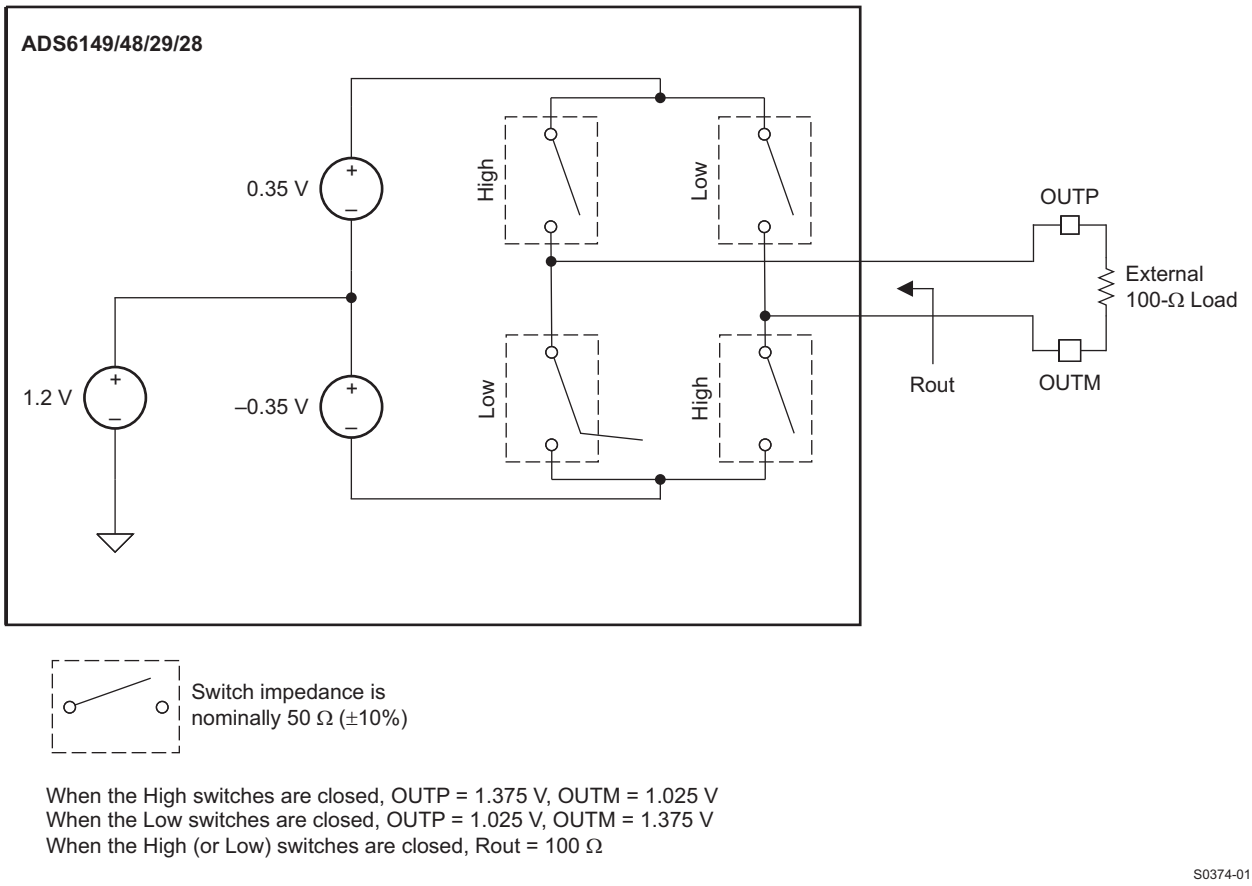

Figure 109. LVDS Buffer Equivalent Circuit

Parallel CMOS Interface

In the CMOS mode, each data bit is output on separate pin as CMOS voltage level, every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver ***(for sampling frequencies up to 150 MSPS)***.

Up to 150 MSPS, the setup and hold timings of the output data with respect to CLKOUT are specified. It is recommended to minimize the load capacitance seen by data and clock output pins by using short traces to the receiver. Also, match the output data and clock traces to minimize the skew between them.

For sampling frequencies > 150 MSPS, it is recommended to use an external clock to capture data. The delay from input clock to output data and the data valid times are specified for the higher sampling frequencies. These timings can be used to delay the input clock appropriately and use it to capture the data (see Figure 4).

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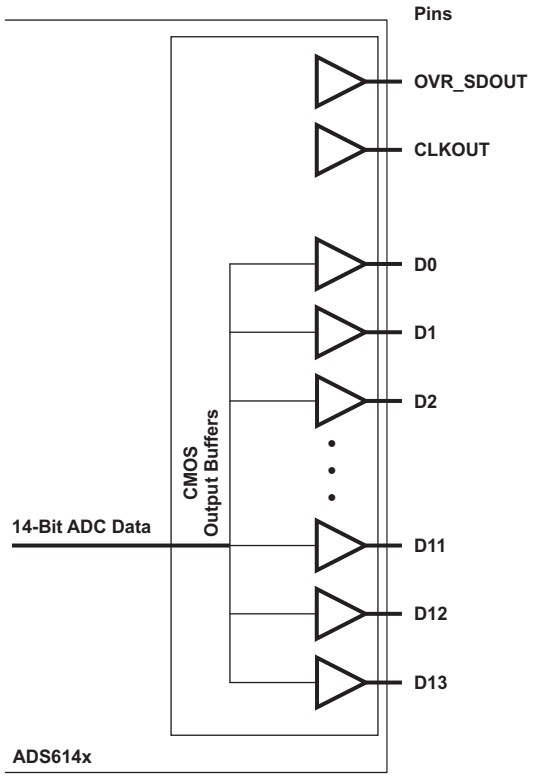

Figure 110. CMOS Output Interface

Output Buffer Strength Programmability

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs during the instant of sampling and degrade the SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this, the CMOS output buffers are designed with controlled drive strength to get best SNR. The default drive strength also ensures wide data stable window for load capacitances up to 5 pF.

CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In an actual application, the DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

$$\text{Digital current due to CMOS output switching} = C_L \times \text{DRVDD} \times (N \times F_{AVG}),$$

where

C_L = load capacitance,

$N \times F_{AVG}$ = average number of output bits switching.

Figure 91 shows the current across sampling frequencies at 2 MHz analog input frequency.

Output Data Format

Two output data formats are supported – 2s complement and offset binary. They can be selected using the serial interface register bit **<DATA FORMAT>** or controlling the DFS pin in parallel configuration mode.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full scale level. For a positive overdrive, the output code is 0x3FFF in offset binary output format, and 0x1FFF in 2s complement output format. For a negative input overdrive, the output code is 0x0000 in offset binary output format and 0x2000 in 2s complement output format.

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BOARD DESIGN CONSIDERATIONS

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the EVM User Guide (SLWU061) for details on layout and grounding.

Supply Decoupling

As the ADS61x9/x8 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power supply noise, so the optimum number of capacitors would depend on the actual application. The decoupling capacitors should be placed close to the converter supply pins.

Exposed Pad

In addition to providing a path for heat dissipation, the pad is also electrically connected to digital ground internally. So, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance.

For detailed information, see the application notes for QFN Layout Guidelines (SLOA122) and QFN/SON PCB Attachment (SLUA271).

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DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay will be different across channels. The maximum variation is specified as aperture delay variation (channel-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error due to reference inaccuracy and error due to the channel. Both these errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first order approximation, the total gain error will be $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from (1-0.5/100) x FS_{ideal} to (1 + 0.5/100) x FS_{ideal}.

Offset Error – The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}–T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (PS) to the noise floor power (PN), excluding the power at DC and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (3)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (4)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB) – The ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

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$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (5)$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (PD).

$$THD = 10Log^{10} \frac{P_S}{P_N} \quad (6)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ratio (DC PSRR) – The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

AC Power Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔVout is the resultant change of the ADC output code (referred to the input), then

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (7)$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from their expected values) is noted.

Common Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔVcm_in is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (8)$$

Cross-Talk (only for multi-channel ADC)– This is a measure of the internal coupling of a signal from adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Cross-talk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS6128IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6128	Samples
ADS6128IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6128	Samples
ADS6129IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6129	Samples
ADS6129IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6129	Samples
ADS6148IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6148	Samples
ADS6148IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6148	Samples
ADS6149IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6149	Samples
ADS6149IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6149	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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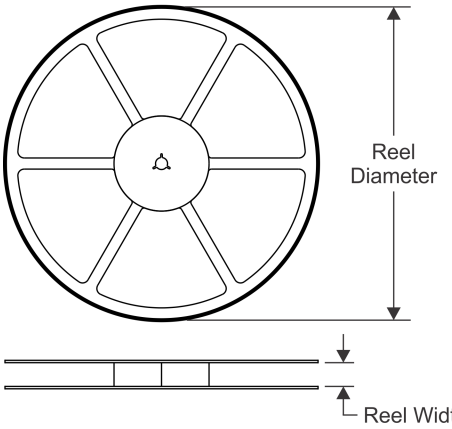
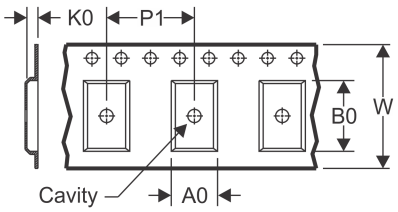
TAPE AND REEL INFORMATION

REEL DIMENSIONS

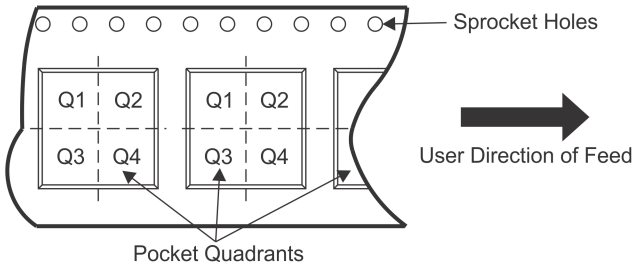


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

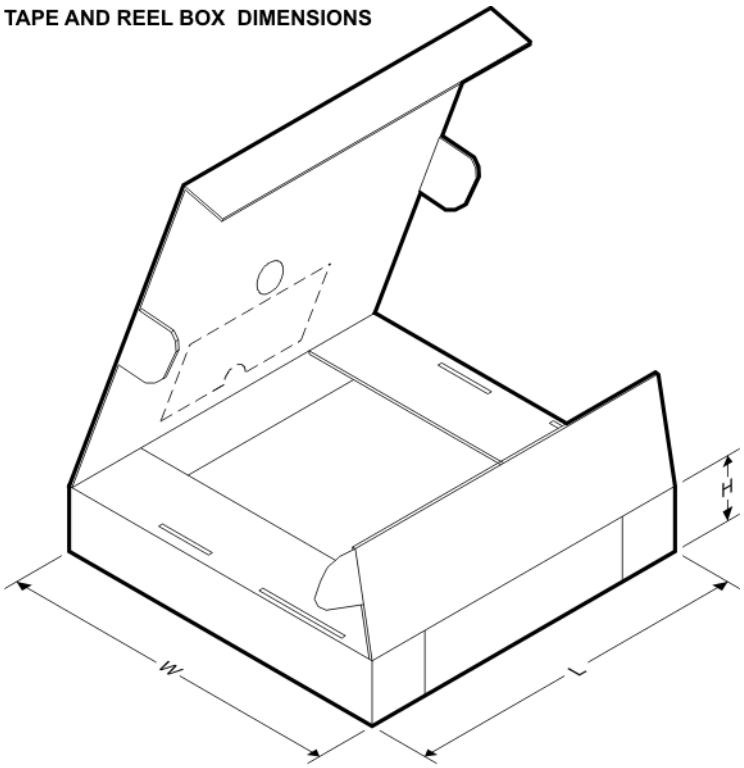
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS6128IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS6128IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS6129IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS6129IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS6148IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS6148IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS6149IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS6149IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS6128IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADS6128IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADS6129IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADS6129IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADS6148IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADS6148IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADS6149IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADS6149IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

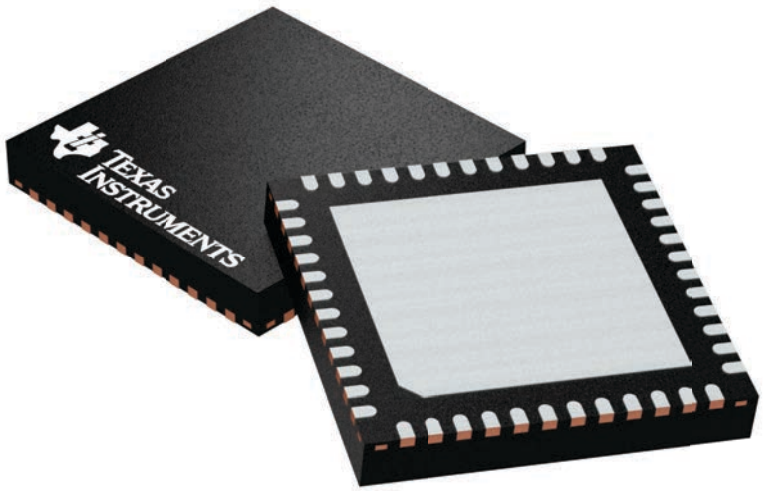
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

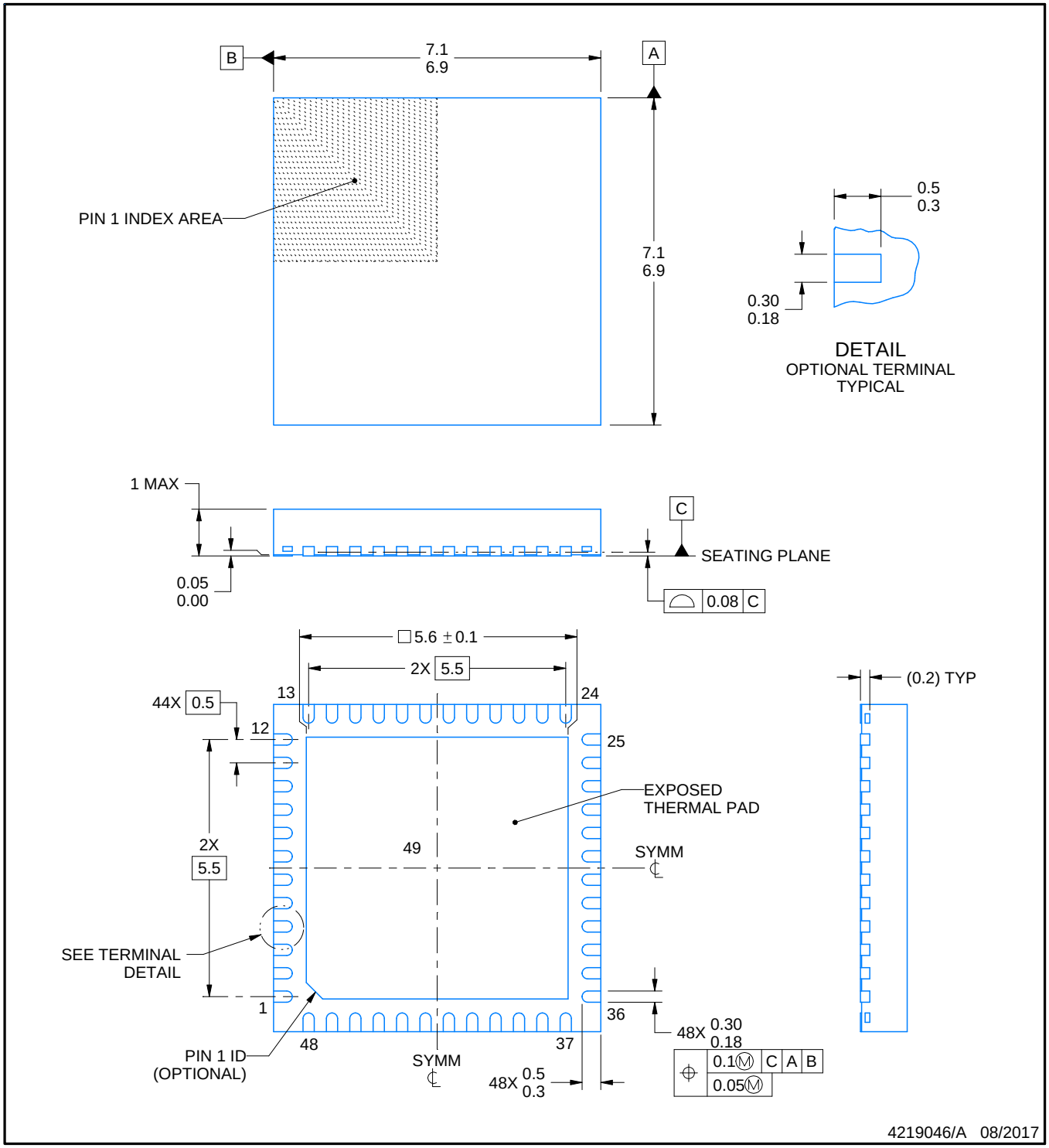
4224671/A

PACKAGE OUTLINE

RGZ0048D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

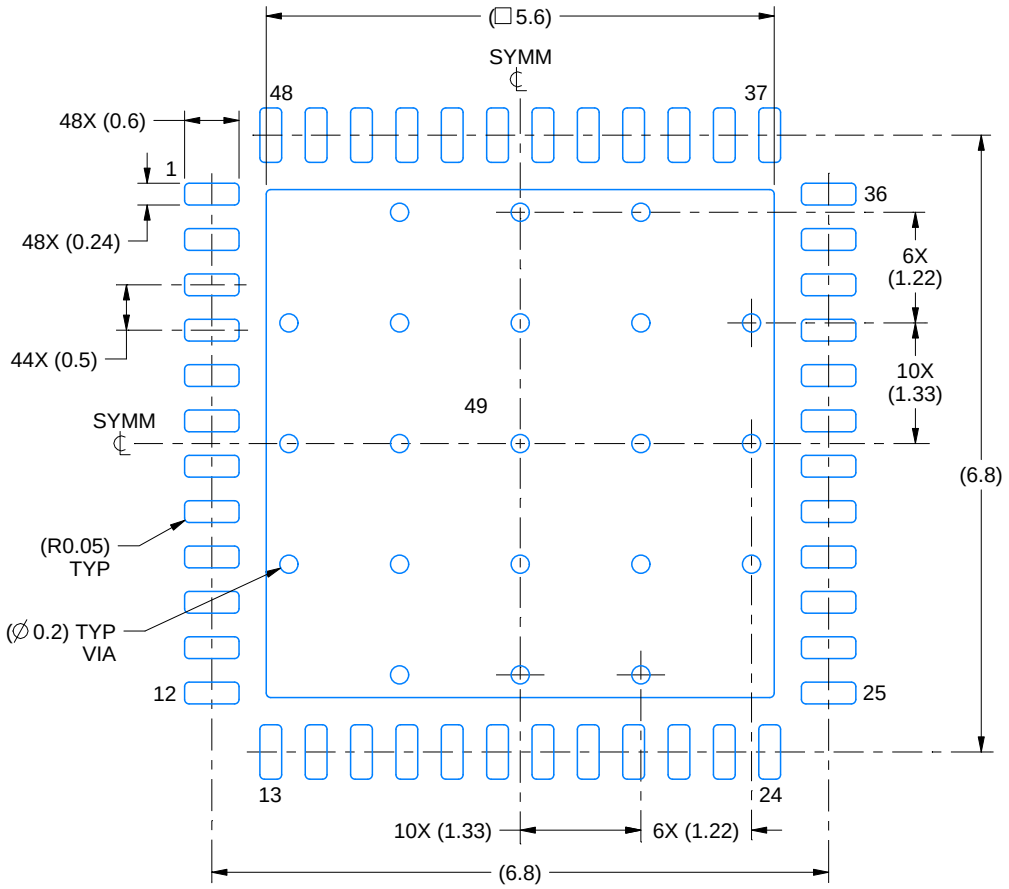
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

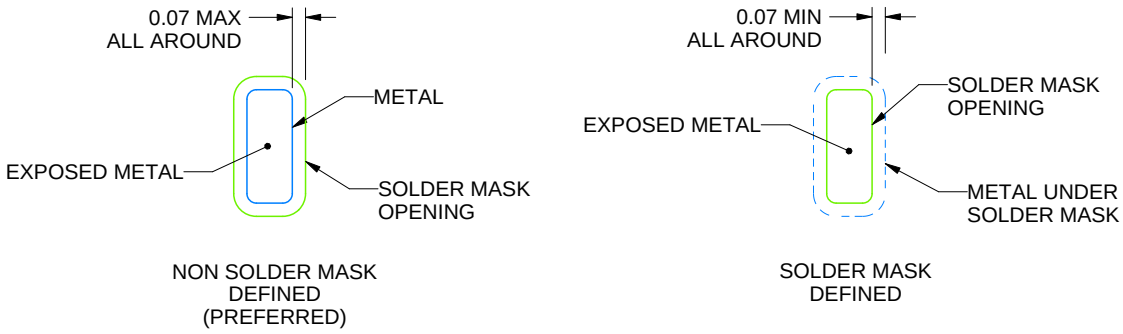
RGZ0048D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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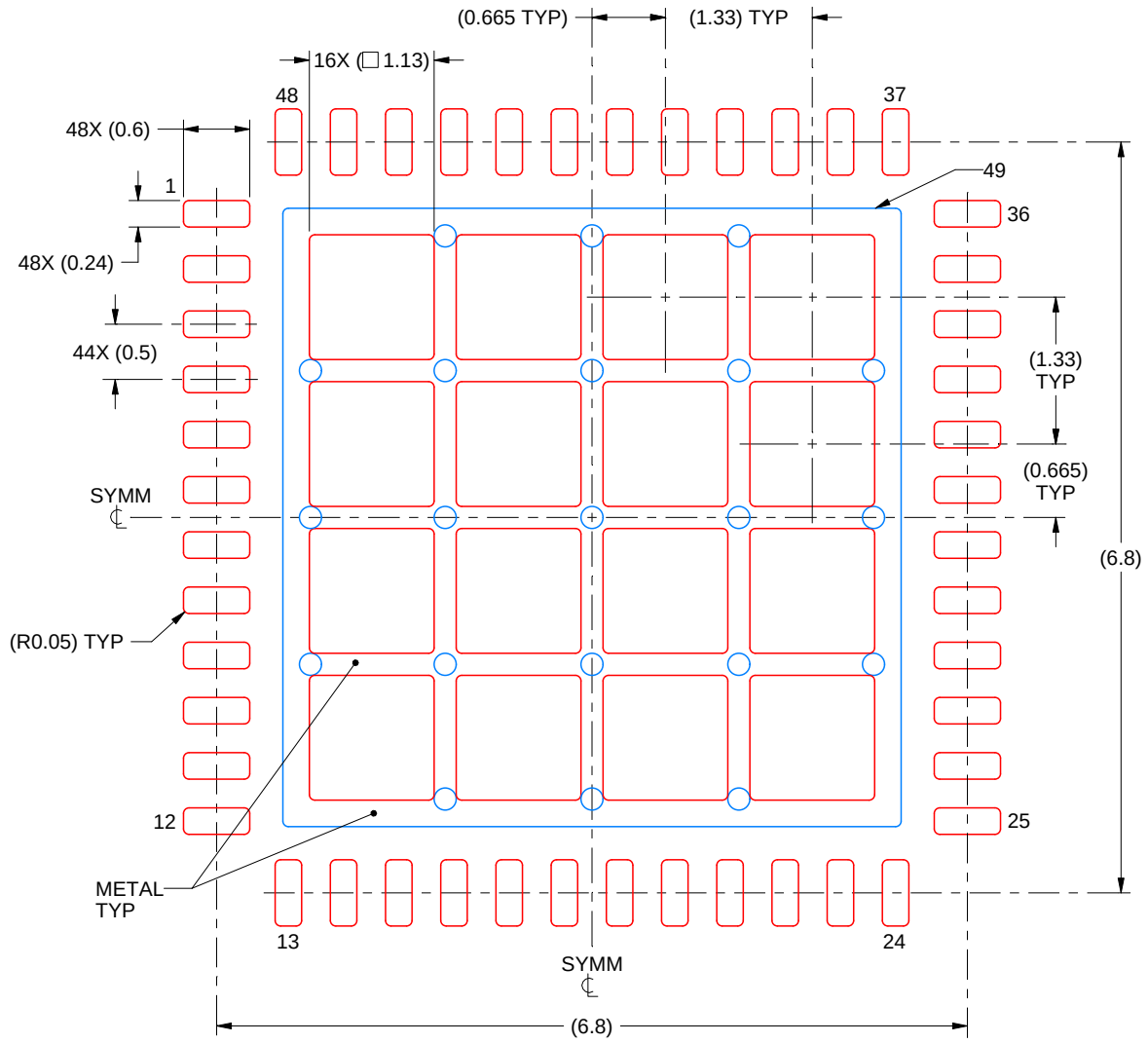
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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