



**THE DATASHEET OF
ADS5203IPFB**





Dual 10-Bit 40MSPS Low-Power ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 3.3V Single-Supply Operation
- Dual Simultaneous Sample-and-Hold Inputs
- Differential or Single-Ended Analog Inputs
- Single or Dual Parallel Bus Output
- 60dB SNR at $f_{IN} = 10.5\text{MHz}$
- 73dB SFDR at $f_{IN} = 10.5\text{MHz}$
- Low Power: 240mW
- 300MHz Analog Input Bandwidth
- 3.3V TTL/CMOS-Compatible Digital I/O
- Internal or External Reference
- Adjustable Reference Input Range
- Power-Down (Standby) Mode
- TQFP-48 Package

APPLICATIONS

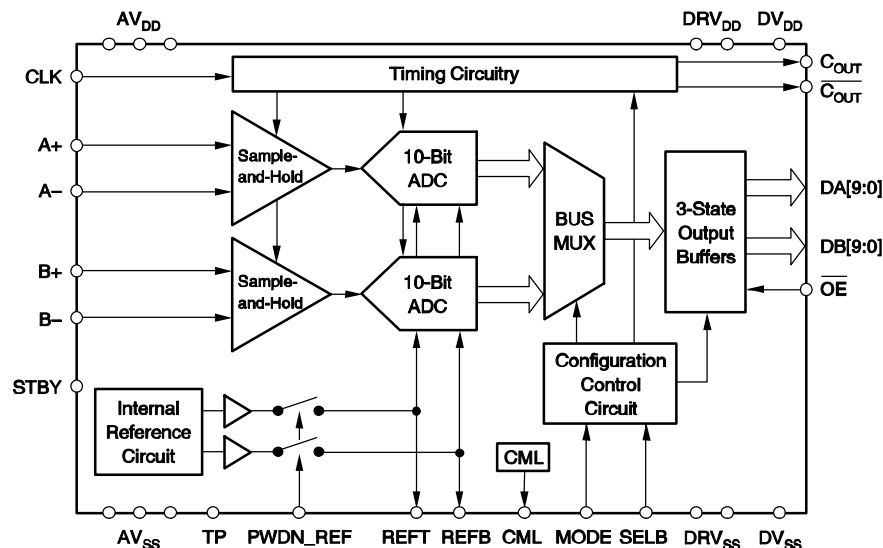
- Digital Communications (Baseband Sampling)
- Video Processing
- Portable Instrumentation
- Ultrasound

DESCRIPTION

The ADS5203 is a dual 10-bit, 40MSPS Analog-to-Digital Converter (ADC). It simultaneously converts each analog input signal into a 10-bit, binary coded digital word up to a maximum sampling rate of 40MSPS per channel. All digital inputs and outputs are 3.3V TTL/CMOS compatible.

An innovative dual-pipeline architecture implemented in a CMOS process and the 3.3V supply results in very low power dissipation. In order to provide maximum flexibility, both top and bottom voltage references can be set from user-supplied voltages. Alternatively, if no external references are available, the on-chip internal references can be used. Both ADCs share a common reference to improve offset and gain matching. If external reference voltage levels are available, the internal references can be powered down independently from the rest of the chip, resulting in even greater power savings.

The ADS5203 is characterized for operation from -40°C to $+85^{\circ}\text{C}$ and is available in a TQFP-48 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5203	TQFP-48	PFB	-40°C to +85°C	AZ5203	ADS5203IPFB	Tray, 250
ADS5203	TQFP-48	PFB	-40°C to +85°C	AZ5203	ADS5203IPFBR	Tape and Reel, 1000

(1) For the most current specifications and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾.

Supply Voltage: AV _{DD} to AGND, DV _{DD} to DGND	-0.5V to 3.6V
Supply Voltage: AV _{DD} to DV _{DD} , AGND to DGND	-0.5V to 0.5V
Digital Input Voltage Range to DGND	-0.5V to DV _{DD} + 0.5V
Analog Input Voltage Range to AGND	-0.5V to AV _{DD} + 0.5V
Digital Output Voltage Applied from Ext. Source to DGND	-0.5V to DV _{DD} + 0.5V
Reference Voltage Input Range to AGND: V _{REFT} , V _{REFB}	-0.5V to AV _{DD} + 0.5V
Operating Free-Air Temperature Range, T _A (ADS5203I)	-40°C to +85°C
Storage Temperature Range, T _{STG}	-65°C to +150°C
Soldering Temperature 1.6mm (1/16 inch) from case for 10 seconds	300°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, T_A, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply						
Supply Voltage	AV _{DD}		3.0	3.3	3.6	V
	DV _{DD}					
	DRV _{DD}					
Analog and Reference Inputs						
Reference Input Voltage (top)	V _{REFT}	f _{CLK} = 1MHz to 80MHz	1.9	2.0	2.15	V
Reference Input Voltage (bottom)	V _{REFB}	f _{CLK} = 1MHz to 80MHz	0.95	1.0	1.1	V
Reference Voltage Differential	V _{REFT} - V _{REFB}	f _{CLK} = 1MHz to 80MHz	0.95	1.0	1.1	V
Reference Input Resistance	R _{REF}	f _{CLK} = 80MHz		1650		Ω
Reference Input Current	I _{REF}	f _{CLK} = 80MHz		0.62		mA
Analog Input Voltage, Differential	V _{IN}		-1		1	V
Analog Input Voltage, Single-Ended ⁽¹⁾	V _{IN}		CML - 1.0		CML + 1.0	V
Analog Input Capacitance	C _I			8		pF
Clock Input ⁽²⁾			0		AV _{DD}	V
Analog Outputs						
CML Voltage				AV _{DD} /2		V
CML Output Resistance				2.3		kΩ
Digital Inputs						
High-Level Input Voltage	V _{IH}		2.4		DV _{DD}	V
Low-Level Input Voltage	V _{IL}		DGND		0.8	V
Input Capacitance				5		pF
Clock Period	t _C (80MHz)		12.5			ns
Pulse Duration	t _w (CLKH), t _w (CLKL) (80MHz)	Clock HIGH or LOW	5.25			ns
Clock Period	t _C (40MHz)		25			ns
Pulse Duration	t _w (CLKH), t _w (CLKL) (40MHz)	Clock HIGH or LOW	11.25			ns

(1) Applies only when the signal reference input connects to CML.

(2) Clock pin is referenced to AV_{DD}/AV_{SS}.

ELECTRICAL CHARACTERISTICS

 over recommended operating conditions with $f_{CLK} = 80\text{MHz}$ and use of internal voltage references, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Power Supply							
I _{DD} Operating Supply Current	AV _{DD}	AV _{DD} = DV _{DD} = DRV _{DD} = 3.3V, C _L = 10pF, f _{IN} = 3.5MHz, -1dBFS		56	62	mA	
	DV _{DD}			1.7	2.2		
	DRV _{DD}			15	26		
Power Dissipation	P _D	PWDN_REF = 'L'		240	290	mW	
		PWDN_REF = 'H'		220	240		
Standby Power	P _D (STBY)	STDBY = 'H', CLK Held HIGH or LOW		95	150	μW	
Power-Up Time for All References from Standby	t _{PD}			550		ms	
Wake Up Time	t _{WU}	External Reference		40		μs	
Digital Inputs							
High-Level Input Current on Digital Inputs incl. CLK	I _{IH}	AV _{DD} = DV _{DD} = DRV _{DD} = 3.6V	-1		1	μA	
Low-Level Input Current on Digital Inputs incl. CLK	I _{IL}		-1		1	μA	
Digital Outputs							
High-Level Output Voltage	V _{OH}	AV _{DD} = DV _{DD} = DRV _{DD} = 3.0V at I _{OH} = 50μA, Digital Outputs Forced HIGH	2.8	2.96		V	
Low-Level Output Voltage	V _{OL}	AV _{DD} = DV _{DD} = DRV _{DD} = 3.0V at I _{OL} = 50μA, Digital Outputs Forced LOW		0.04	0.2	V	
Output Capacitance	C _O			5		pF	
High-Impedance State Output Current to High-Level	I _{OZH}	AV _{DD} = DV _{DD} = DRV _{DD} = 3.6V	-1		+1	μA	
High-Impedance State Output Current to Low-Level	I _{OZL}		-1		+1	μA	
Data Output Rise-and-Fall Time		C _{LOAD} = 10pF, Single-Bus Mode		3		ns	
		C _{LOAD} = 10pF, Dual-Bus Mode		5		ns	
Reference Outputs							
Reference Top Voltage	V _{REFTO}	Absolute Min/Max Values Valid and Tested for AV _{DD} = 3.3V	1.9	2	2.1	V	
Reference Bottom Voltage	V _{REFBO}		0.95	1	1.05	V	
Differential Reference Voltage	REFT – REFB		0.95	1.0	1.05	V	
DC Accuracy							
Integral Nonlinearity, End Point	INL	Internal References(1)	T _A = -40°C to +85°C	-1.5	±0.4	+1.5	LSB
Differential Nonlinearity	DNL	Internal References(2)	T _A = -40°C to +85°C	-0.9	±0.5	+1	LSB
Missing Codes		No Missing Codes Assured					
Zero Error(3)		AV _{DD} = DV _{DD} = DRV _{DD} = 3.3V External References (3)		0.12	±1.5	%FS	
Full-Scale Error				0.28	±1.5	%FS	
Gain Error				0.24	±1.5	%FS	

(1) Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full-scale. The point used as zero occurs ½LSB before the first code transition. The full-scale point is defined as a level ½LSB beyond the last code transition. The deviation is measured from the center of each particular code to the best-fit line between these two endpoints.

(2) An ideal ADC exhibits code transitions that are exactly 1LSB apart. DNL is the deviation from this ideal value. Therefore, this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test, (i.e., (last transition level – first transition level)/(2ⁿ – 2)). Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than -1LSB ensures no missing codes.

(3) Zero error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that will switch the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to ½LSB to the bottom reference level. The voltage corresponding to 1LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024). Full-scale error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that will switch the ADC output from code 1022 to code 1023. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5LSB from the top reference level. The voltage corresponding to 1LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

DYNAMIC PERFORMANCE(1)

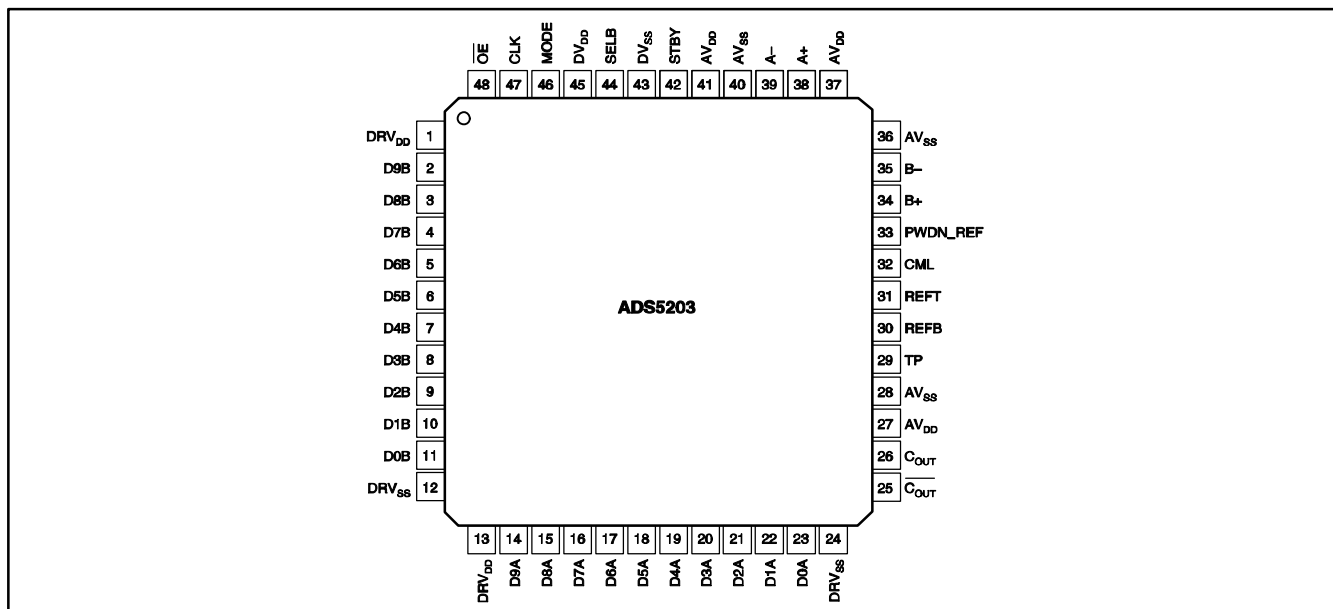
$T_A = T_{MIN}$ to T_{MAX} , $AV_{DD} = DV_{DD} = DRV_{DD} = 3.3V$, $f_{IN} = -1dBFS$, Internal Reference, $f_{CLK} = 80MHz$, $f_S = 40MSPS$, and Differential Input Range = $2V_{p-p}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Effective Number of Bits	ENOB	$f_{IN} = 3.5MHz$		9.7		Bits
		$f_{IN} = 10.5MHz$	9.3	9.7		Bits
		$f_{IN} = 20MHz$		9.6		Bits
Total Harmonic Distortion	THD	$f_{IN} = 3.5MHz$		-71		dB
		$f_{IN} = 10.5MHz$		-71	-66	dB
		$f_{IN} = 20MHz$		-68		dB
Signal-to-Noise Ratio	SNR	$f_{IN} = 3.5MHz$		60.5		dB
		$f_{IN} = 10.5MHz$		60.5		dB
		$f_{IN} = 20MHz$		60		dB
Signal-to-Noise Ratio + Distortion	SINAD	$f_{IN} = 3.5MHz$		60		dB
		$f_{IN} = 10.5MHz$	57	60		dB
		$f_{IN} = 20MHz$		60		dB
Spurious-Free Dynamic Range	SFDR	$f_{IN} = 3.5MHz$		75		dB
		$f_{IN} = 10.5MHz$	69	73		dB
		$f_{IN} = 20MHz$		70.5		dB
Analog Input Bandwidth		See Note (2)		300		MHz
2-Tone Intermodulation Distortion	IMD	$f_1 = 9.5MHz$, $f_2 = 9.9MHz$		-68		dBc
A/B Channel Crosstalk				-75		dBc
A/B Channel Offset Mismatch				0.016	1.75	% FS
A/B Channel Full-Scale Error Mismatch				0.016	1.0	% FS

(1) These specifications refer to a 25Ω series resistor and 15pF differential capacitor between A/B+ and A/B- inputs; any source impedance will bring the bandwidth down.

(2) Analog input bandwidth is defined as the frequency at which the sampled input signal is 3dB down on unity gain and is limited by the input switch impedance.

PIN CONFIGURATION



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
DRVDD	1,13	I	Supply Voltage for Output Drivers
DRVSS	12, 24	I	Digital Ground for Output Drivers
DA 9..0	14-23	O	Data Outputs for Bus A. D9 is MSB. This is the primary bus. Data from both input channels can be output on this bus or data from the A channel only. Pins SELB and MODE select the output mode. The data outputs are in tri-state during power-down (refer to Timing Options table).
DB 9..0	2-11	O	Data Outputs for Bus B. D9 is MSB. This is the second bus. Data is output from the B-channel when dual bus output mode is selected. The data outputs are in tri-state during power-down and single-bus modes (refer to Timing Options table).
OE	48	I	Output Enable. A LOW on this terminal will enable the data output bus, COUT and COUT.
COUT	26	O	Latch Clock for the Data Outputs. COUT is in tri-state during power-down.
COUT	25	O	Inverted Latch Clock or multiplexer control for the Data Outputs. COUT is in tri-state during power-down.
SELB	44	I	Selects either single-bus data output or dual-bus data output. A LOW selects dual-bus data output.
DVSS	43	I	Digital Ground
CLK	47	I	Clock Input. The input is sampled on each rising edge of CLK when using a 40MHz input and alternate rising edges when using an 80MHz input. The clock pin is referenced to AVDD and AVSS to reduce noise coupling from digital logic.
DVDD	45	I	Digital Supply Voltage
AVDD	27,37,41	I	Analog Supply Voltage
MODE	46	I	Selects the COUT and COUT output mode.
AVSS	28,36,40	I	Analog Ground
B-	35	I	Negative Input for the Analog B Channel
B+	34	I	Positive Input for the Analog B Channel
REFT	31	I/O	Reference Voltage Top. The voltage at this terminal defines the top reference voltage for the ADC. Sufficient filtering should be applied to this input: the use of 0.1µF capacitor between REFT and AVSS is recommended. Additionally a 0.1µF capacitor should be connected between REFT and REFB.
REFB	30	I/O	Reference Voltage Bottom. The voltage at this terminal defines the bottom reference voltage for the ADC. Sufficient filtering should be applied to this input: the use of 0.1µF capacitor between REFB and AVSS is recommended. Additionally a 0.1µF capacitor should be connected between REFT and REFB.
CML	32	O	Common-Mode Level. This voltage is equal to (AVDD - AVSS)/2. An external capacitor of 0.1µF should be connected between this terminal and AVSS when CML is used as a bias voltage. No capacitor is required if CML is not used.
PDOWN_REF	33	I	Power-Down for Internal Reference Voltages. A HIGH on this terminal disables the internal reference circuit.
STBY	42	I	Standby Input. A HIGH on this terminal will power down the device.
A-	39	I	Negative Input for the Analog A Channel
A+	38	I	Positive Input for Analog A Channel
TP	29		This pin must be connected to DVDD. It should not be left floating.

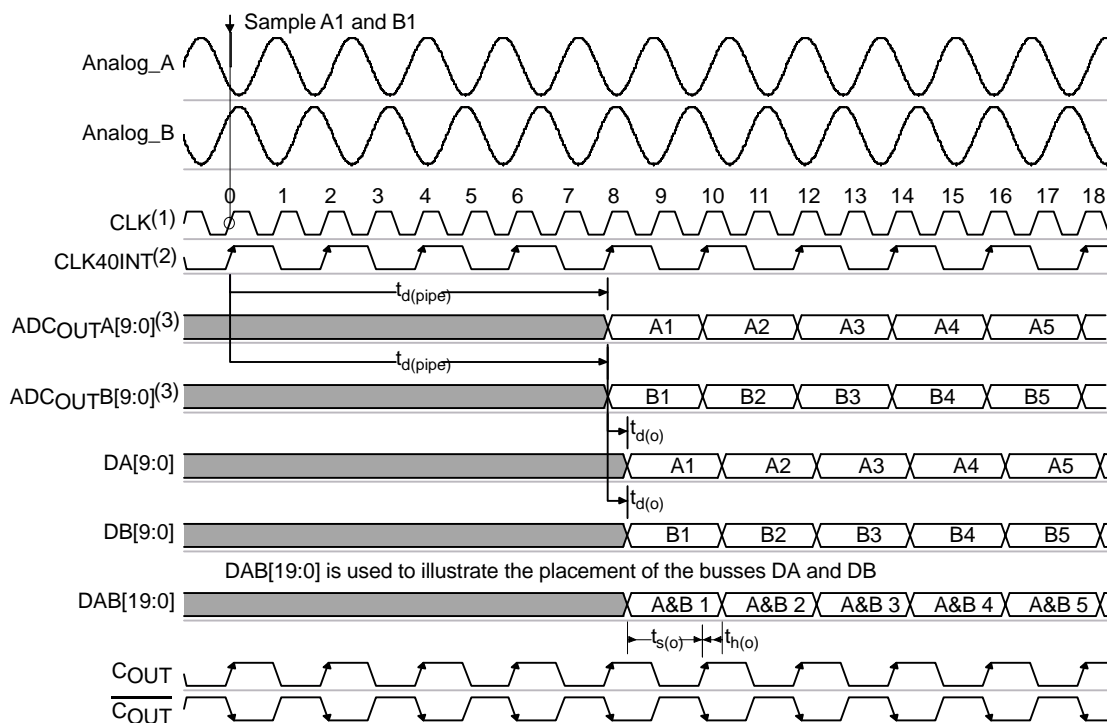
TIMING REQUIREMENTS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Clock Rate	f_{CLK}	1		80	MHz
Conversion Rate		1		40	MSPS
Clock Duty Cycle (40MHz)		45	50	55	%
Clock Duty Cycle (80MHz)		42	50	58	%
Output Delay Time	$t_{d(o)}$ $C_L = 10pF$		9	14	ns
Mux Setup Time	$t_{s(m)}$	9	10.4		ns
Mux Hold Time	$t_{h(m)}$	1.7	2.1		ns
Output Setup Time	$t_{s(o)}$ $C_L = 10pF$	9	10.4		ns
Output Hold Time	$t_{h(o)}$ $C_L = 10pF$	1.5	2.2		ns
Pipeline Delay (latency, channels A and B)	$t_{d(pipe)}$ MODE = 0, SELB = 0		8		CLK Cycles
Pipeline Delay (latency, channels A and B)	$t_{d(pipe)}$ MODE = 1, SELB = 0		4		CLK Cycles
Pipeline Delay (latency, channel A)	$t_{d(pipe)}$ MODE = 0, SELB = 1		8		CLK Cycles
Pipeline Delay (latency, channel B)	$t_{d(pipe)}$ MODE = 0, SELB = 1		9		CLK Cycles
Pipeline Delay (latency, channel A)	$t_{d(pipe)}$ MODE = 1, SELB = 1		8		CLK Cycles
Pipeline Delay (latency, channel B)	$t_{d(pipe)}$ MODE = 1, SELB = 1		9		CLK Cycles
Aperture Delay Time	$t_{d(a)}$		3		ns
Aperture Jitter	$t_{J(a)}$		1.5		ps, rms
Disable Time, \overline{OE} Rising to Hi-Z	t_{dis}		5	8	ns
Enable Time, \overline{OE} Falling to Valid Data	t_{en}		5	8	ns

TIMING OPTIONS

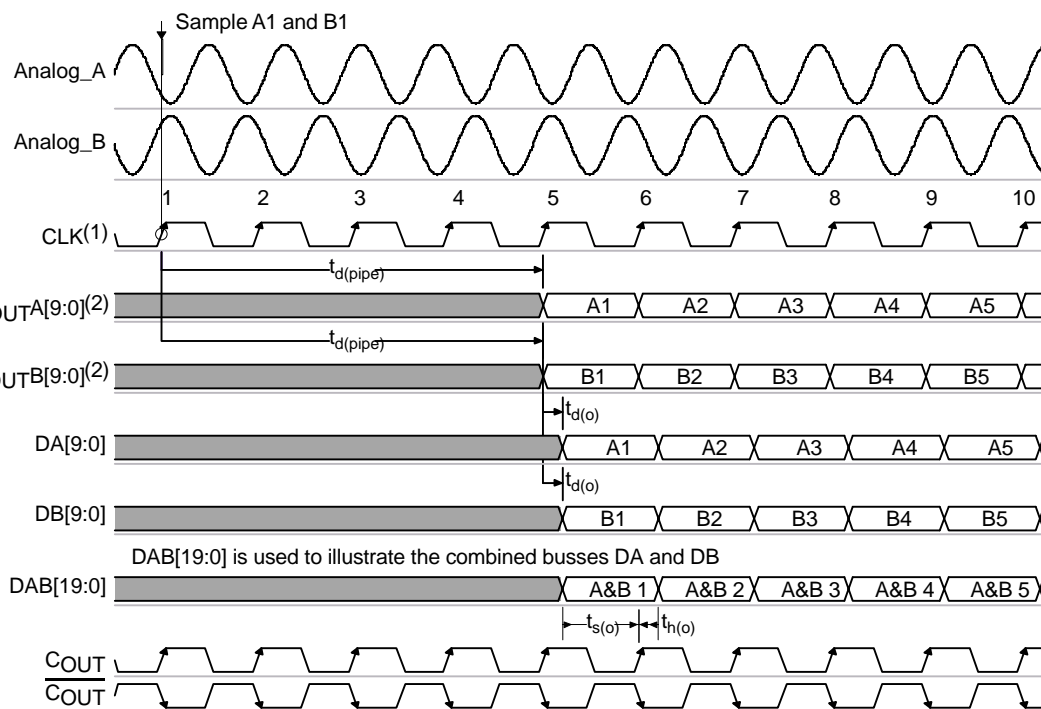
OPERATING MODE	MODE	SELB	TIMING DIAGRAM FIGURE
80MHz Input Clock, Dual-Bus Output, $C_{OUT} = 40MHz$	0	0	1
40MHz Input Clock, Dual-Bus Output, $C_{OUT} = 40MHz$	1	0	2
80MHz Input Clock, Single-Bus Output, $C_{OUT} = 40MHz$	0	1	3
80MHz Input Clock, Single-Bus Output, $C_{OUT} = 80MHz$	1	1	4

TIMING DIAGRAMS



NOTES: (1) In this option CLK = 80MHz. (2) CLK40INT refers to 40MHz Internal Clock, per channel. (3) Internal signal only.

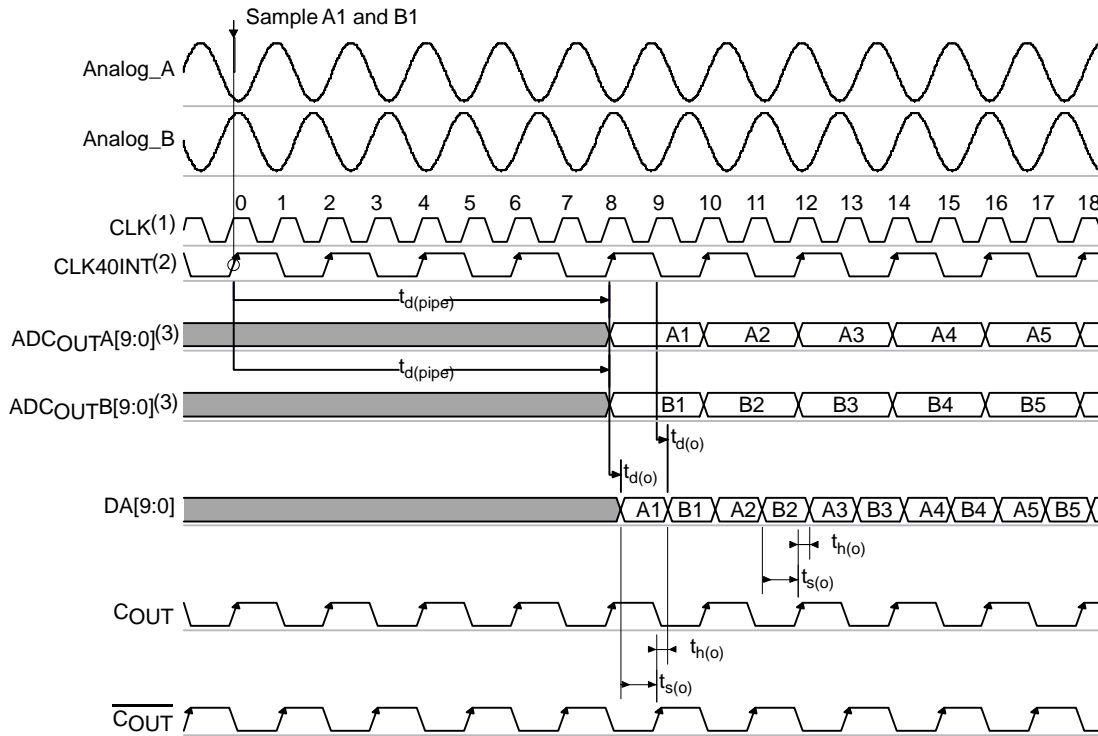
Figure 1. Dual Bus Output—Option 1.



NOTE: (1) In this option CLK = 40MHz, per channel. (2) Internal signal only

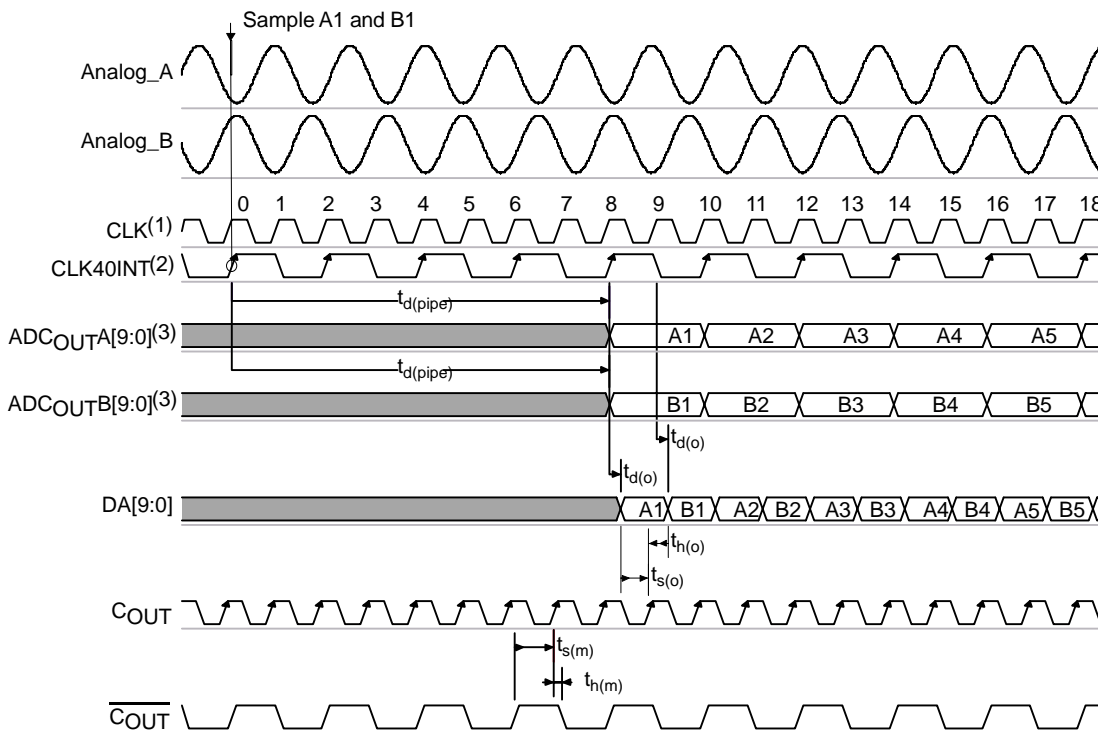
Figure 2. Dual Bus Output—Option 2.

TIMING DIAGRAMS (Cont.)



NOTES: (1) In this option CLK = 80MHz. (2) CLK40INT refers to 40MHz Internal Clock, per channel. (3) Internal signal only.

Figure 3. Single Bus Output—Option 1.

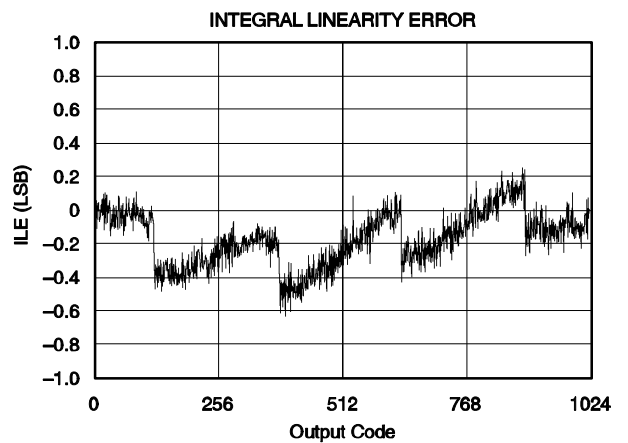
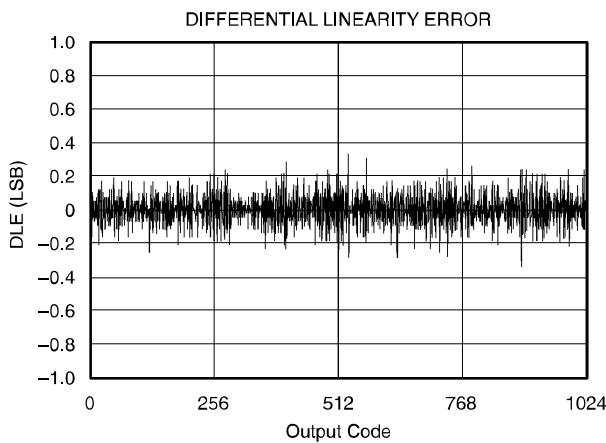
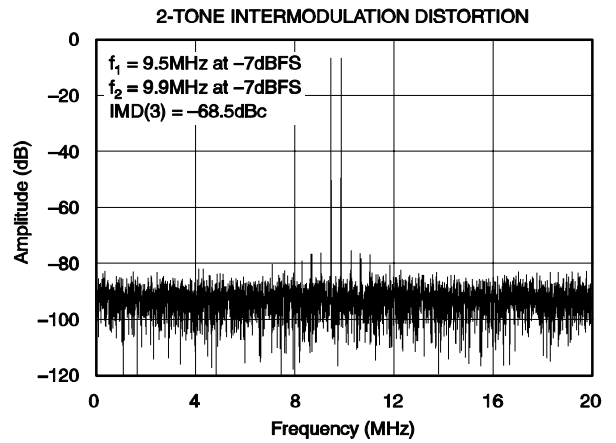
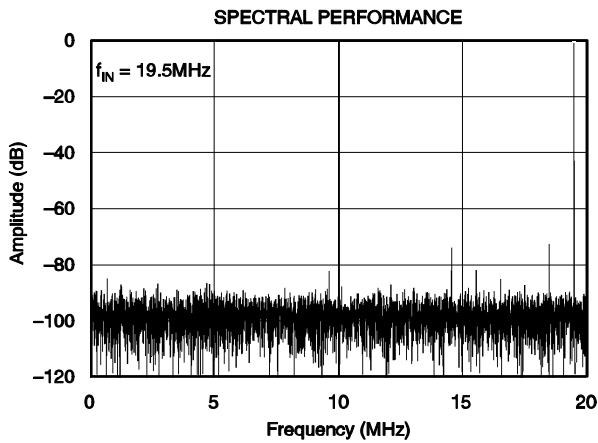
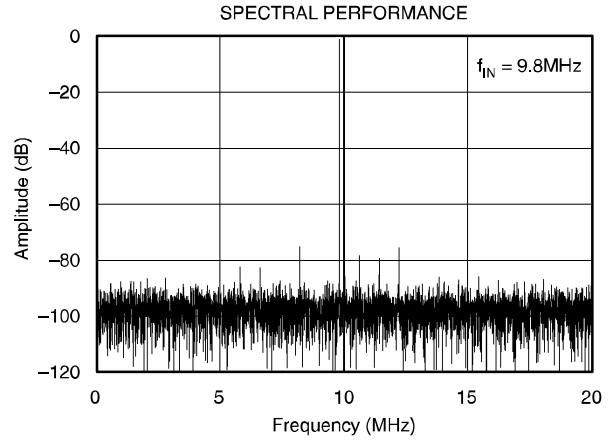
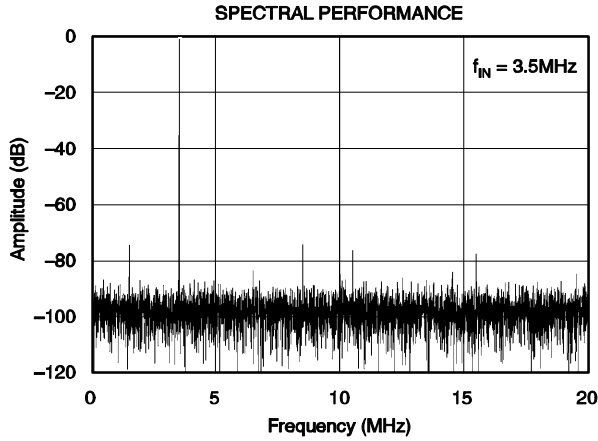


NOTES: (1) In this option CLK = 80MHz. (2) CLK40INT refers to 40MHz Internal Clock, per channel. (3) Internal signal only.

Figure 4. Single Bus Output—Option 2.

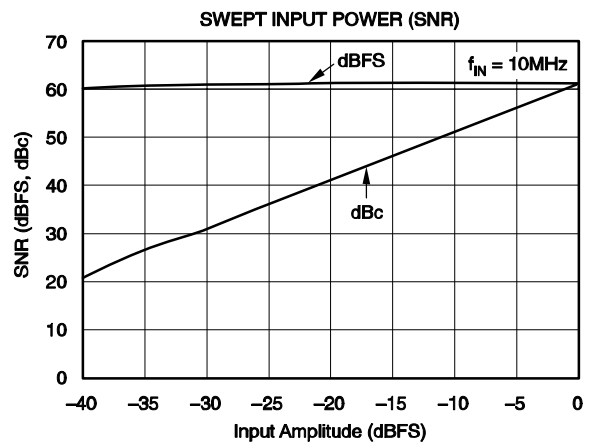
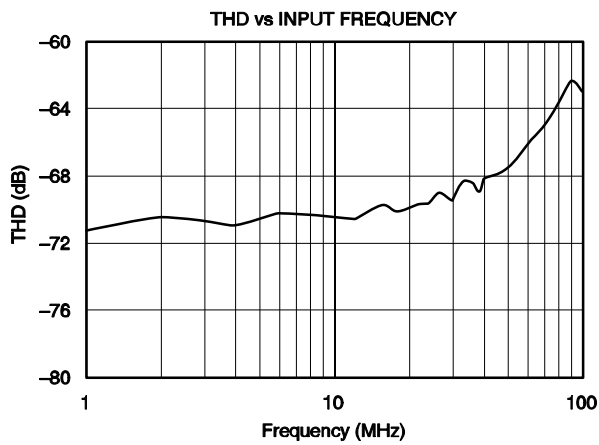
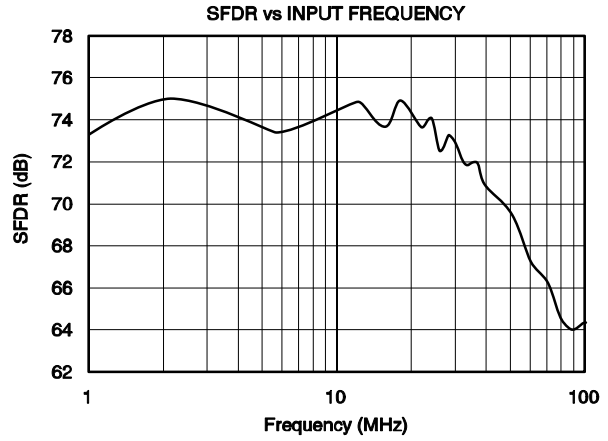
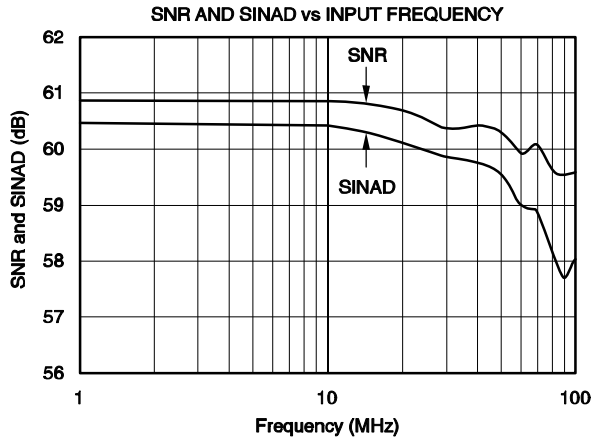
TYPICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = DRV_{DD} = 3.3\text{V}$, $f_{IN} = -0.5\text{dBFS}$, Internal Reference, $f_{CLK} = 80\text{MHz}$, $f_S = 40\text{MSPS}$, Differential Input Range = 2V_{p-p} , 25Ω series resistor, and 15pF differential capacitor at A/B+ and A/B- inputs, unless otherwise noted.



Typical Characteristics (Cont.)

At $T_A = 25^\circ\text{C}$, $AV_{DD} = DV_{DD} = DRV_{DD} = 3.3\text{V}$, $f_{IN} = -0.5\text{dBFS}$, Internal Reference, $f_{CLK} = 80\text{MHz}$, $f_S = 40\text{MSPS}$, Differential Input Range = 2Vp-p , 25Ω series resistor, and 15pF differential capacitor at A/B+ and A/B- inputs, unless otherwise noted.



PRINCIPLE OF OPERATION

The ADS5203 implements a dual high-speed, 10-bit, 40MSPS converter in a cost-effective CMOS process. The differential inputs on each channel are sampled simultaneously. Signal inputs are differential and the clock signal is single-ended. The clock signal is either 80MHz or 40MHz, depending on the device configuration set by the user. Powered from 3.3V, the dual-pipeline design architecture ensures low-power operation and 10-bit resolution. The digital inputs are 3.3V TTL/CMOS compatible. Internal voltage references are included for both bottom and top voltages. Alternatively, the user may apply externally generated reference voltages. In doing so, the input range can be modified to suit the application.

The ADC is a 5-stage pipelined ADC with 4 stages of fully-differential switched capacitor sub-ADC/MDAC pairs and a single sub-ADC in stage 5. All stages deliver 2 bits of the final conversion result. A digital error correction is used to compensate for modest comparator offsets in the sub-ADCs.

SAMPLE-AND-HOLD AMPLIFIER

Figure 5 shows the internal SHA architecture. The circuit is balanced and fully differential for good supply noise rejection. The sampling circuit has been kept as simple as possible to obtain good performance for high-frequency input signals.

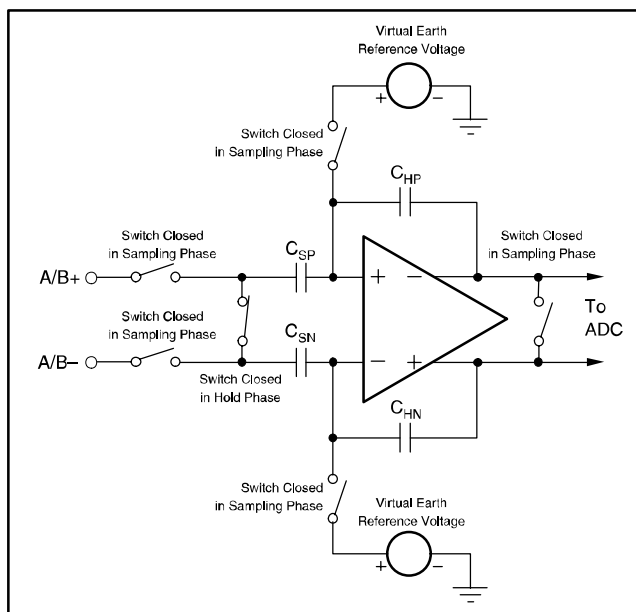


Figure 5. SHA Architecture.

The analog input signal is sampled on capacitors C_{SP} and C_{SN} while the internal device clock is low. The sampled voltage is transferred to capacitors C_{HP} and C_{HN} and held on these while the internal device clock is high. The SHA can sample both single-ended and differential input signals.

The load presented to the AIN pin consists of the switched input sampling capacitor C_S (approximately 2pF) and its various stray capacitances. A simplified equivalent circuit for the switched capacitor input is shown in Figure 6. The switched capacitor circuit is modeled as a resistor R_{IN} . f_{CLK} is the clock frequency, which is 40MHz at full speed, and C_S is the sampling capacitor. Using 25Ω series resistors and a differential 15pF capacitor at the A/B+ and A/B- inputs is recommended to reduce noise.

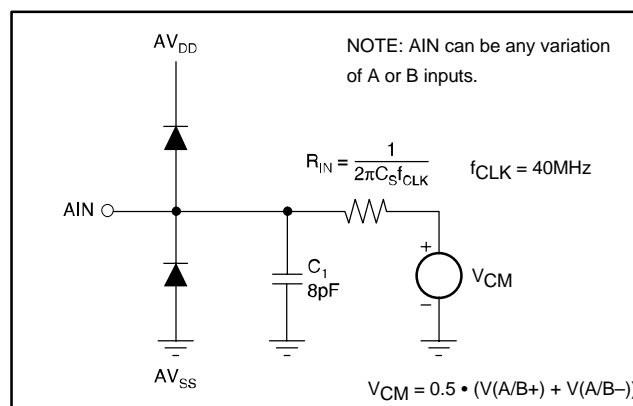


Figure 6. Equivalent Circuit for the Switched Capacitor Input.

ANALOG INPUT, DIFFERENTIAL CONNECTION

The analog input of the ADS5203 is a differential architecture that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection will deliver the best performance from the converter. The analog inputs must not go below AV_{SS} or above AV_{DD} . The inputs can be biased with any common-mode voltage provided that the minimum and maximum input voltages stay within the range AV_{SS} to AV_{DD} . It is recommended to bias the inputs with a common-mode voltage around $AV_{DD}/2$. This can be accomplished easily with the output voltage source CML, which is equal to $AV_{DD}/2$. CML is made available to the user to help simplify circuit design. This output voltage source is not designed to be a reference or to be loaded but makes an excellent DC bias source and stays well within the analog input common-mode voltage range over temperature.

Table 1 lists the digital outputs for the corresponding analog input voltages.

Table 1. Output Format for Differential Configuration

DIFFERENTIAL INPUT	
$V_{IN} = (A+/B+) - (A-/B-), REFT - REFB = 1V$	
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE
$V_{IN} = +1V$	3FF _H
$V_{IN} = 0$	200 _H
$V_{IN} = -1V$	000 _H

DC-COUPLED DIFFERENTIAL ANALOG INPUT CIRCUIT

Driving the analog input differentially can be achieved in various ways. Figure 7 gives an example where a single-ended signal is converted into a differential signal by using a fully differential amplifier such as the THS4141. The input voltage applied to V_{OCM} of the THS4141 shifts the output signal into the desired common-mode level. V_{OCM} can be connected to CML of the ADS5203, the common-mode level is shifted to $AV_{DD}/2$.

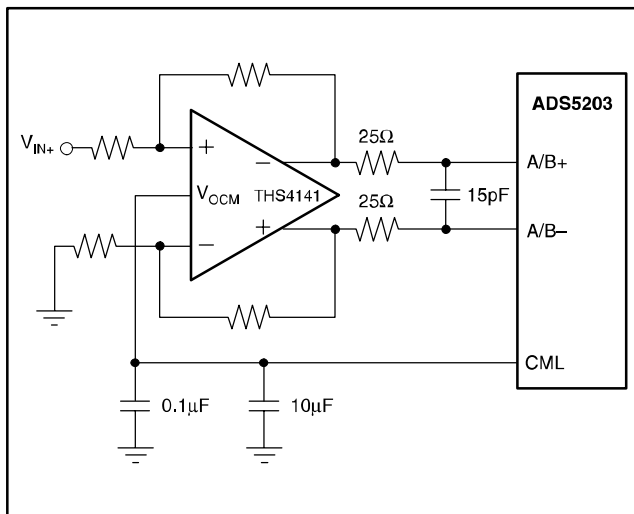


Figure 7. Single-Ended to Differential Conversion Using the THS4141.

AC-COUPLED DIFFERENTIAL ANALOG INPUT CIRCUIT

Driving the analog input differentially can be achieved by using a transformer-coupling, as illustrated in Figure 8. The center tap of the transformer is connected to the voltage source CML, which sets the common-mode voltage to $AV_{DD}/2$. No buffer is required at the output of CML since the circuit is balanced and no current is drawn from CML.

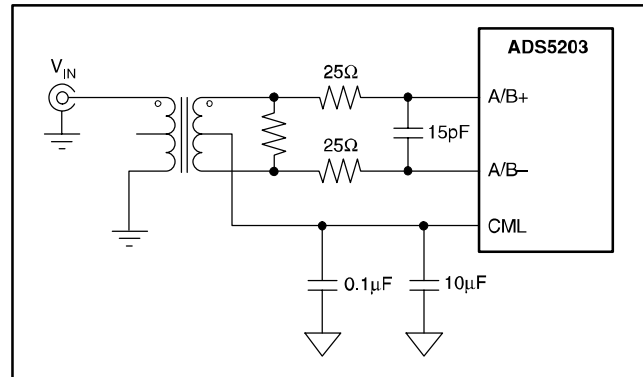


Figure 8. AC-Coupled Differential Input with Transformer.

ANALOG INPUT, SINGLE-ENDED CONFIGURATION

For a single-ended configuration, the input signal is applied to only one of the two inputs. The signal applied to the analog input must not go below AV_{SS} or above AV_{DD} . The inputs can be biased with any common-mode voltage provided that the minimum and maximum input voltage stays within the range AV_{SS} to AV_{DD} . It is recommended to bias the inputs with a common-mode voltage around $AV_{DD}/2$. This can be accomplished easily with the output voltage source CML, which is equal to $AV_{DD}/2$. An example for this is shown in Figure 9.

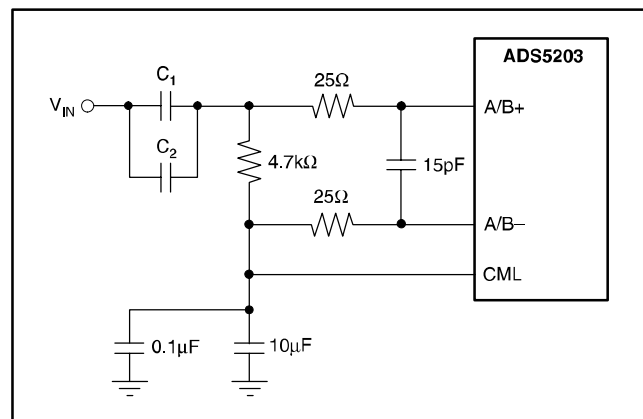


Figure 9. AC-Coupled, Single-Ended Configuration.

The signal amplitude to achieve full scale is 2Vp-p. The signal, which is applied at A/B+ is centered at the bias voltage. The input A/B- is also centered at the bias voltage. The CML output is connected via a 4.7kΩ resistor to bias the input signal. There is a direct DC-coupling from CML to A/B- while this input is AC-decoupled through the 10μF and 0.1μF capacitors. The decoupling minimizes the coupling of A/B+ into the A/B- path.

Table 2 lists the digital outputs for the corresponding analog input voltages.

Table 2. Output Format for Single-Ended Configuration.

SINGLE-ENDED INPUT, REFT – REFB = 1V	
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE
$V(A/B+) = V_{CML} + 1V$	3FF _H
$V(A/B+) = V_{CML}$	200 _H
$V(A/B+) = V_{CML} - 1V$	000 _H

REFERENCE TERMINALS

The ADS5203's input range is determined by the voltages on its REFB and REFT pins. The ADS5203 has an internal voltage reference generator that sets the ADC reference voltages REFB = 1V and REFT = 2V. The internal ADC references must be decoupled to the PCB AV_{SS} plane. The recommended decoupling scheme is shown in Figure 10. The internal reference voltages common-mode voltage is 1.5V.

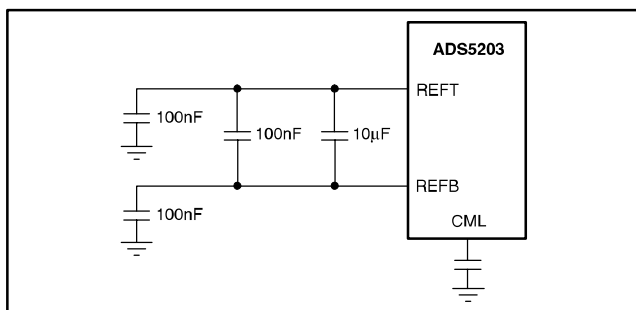


Figure 10. Recommended External Decoupling for the Internal ADC Reference.

External ADC references can also be chosen. The ADS5203 internal references must be disabled by tying PWDN_REF HIGH before applying the external reference sources to the REFT and REFB pins. The external reference voltages common-mode voltage should be 1.5V for best ADC performance.

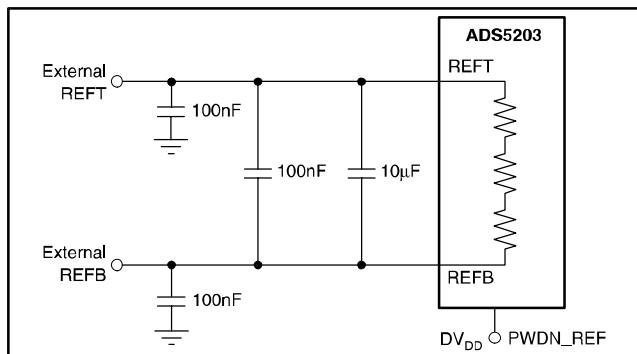


Figure 11. External ADC Reference Configuration.

DIGITAL INPUTS

Digital inputs are CLK, STDBY, PWDN_REF, \overline{OE} , MODE, and SELB. These inputs don't have a pull-down resistor to ground, therefore, they should not be left floating.

The CLK signal at high frequencies should be considered as an 'analog' input. CLK should be referenced to AV_{DD} and AV_{SS} to reduce noise coupling from the digital logic. Overshoot/undershoot should be minimized by proper termination of the signal close to the ADS5203. An important cause of performance degradation for a high-speed ADC is clock jitter. Clock jitter causes uncertainty in the sampling instant of the ADC, in addition to the inherent uncertainty on the sampling instant caused by the part itself, as specified by its aperture jitter. There is a theoretical relationship between the frequency f and resolution (2^N) of a signal that needs to be sampled on one hand, and on the other hand the maximum amount of aperture error dt_{max} that is tolerable. It is given by the following relation:

$$dt_{max} = 1/[\pi f 2^{(N+1)}]$$

As an example, for a 10-bit converter with a 20MHz input, the jitter needs to be kept less than 7.8ps in order not to have changes in the LSB of the ADC output due to the total aperture error.

DIGITAL OUTPUTS

The output of ADS5203 is an unsigned binary code. Capacitive loading on the output should be kept as low as possible (a maximum loading of 10pF is recommended) to ensure best performance. Higher output loading causes higher dynamic output currents and can, therefore, increase noise coupling into the part's analog front end. To drive higher loads, the use of an output buffer is recommended.

When clocking output data from ADS5203, it is important to observe its timing relation to C_{OUT}. Please refer to the timing section for detailed information on the pipeline latency in the different modes.

For safest system timing, C_{OUT} and $\overline{C_{OUT}}$ should be used to latch the output data, (see Figures 1 to 4). In Figure 4, $\overline{C_{OUT}}$ can be used by the receiving device to identify whether the data presently on the bus is from channel A or B.

LAYOUT, DECOUPLING, AND GROUNDING RULES

Proper grounding and layout of the PCB on which the ADS5203 is populated is essential to achieve the stated performance. It is advised to use separate analog and digital ground planes that are spliced underneath the IC. The ADS5203 has digital and analog pins on opposite sides of the package to make this easier. Since there is no connection internally between analog and digital grounds, they have to be joined on the PCB. It is advised to do this at one point in close proximity to the ADS5203.

As for power supplies, separate analog and digital supply pins are provided on the part (AV_{DD}/DV_{DD}). The supply to the digital output drivers is kept separate as well (DRV_{DD}). Lowering the voltage on this supply to 3.0V instead of the nominal 3.3V improves performance because of the lower switching noise caused by the output buffers.

Due to the high sampling rate and switched-capacitor architecture, the ADS5203 generates transients on the supply and reference lines. Proper decoupling of these lines is, therefore, essential.

NOTES

1. Integral Nonlinearity (INL)—Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full-scale. The point used as zero occurs $\frac{1}{2}$ LSB before the first code transition. The full-scale point is defined as a level $\frac{1}{2}$ LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two endpoints.

2. Differential Nonlinearity (DNL)—An ideal ADC exhibits code transitions that are exactly 1LSB apart. DNL is the deviation from this ideal value. Therefore, this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test (i.e., (last transition level – first transition level)/($2^n - 2$)). Using this definition for DNL separates the effects of gain and offset error.

A minimum DNL better than -1 LSB ensures no missing codes.

3. Zero and Full-Scale Error—Zero error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that will switch the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to $\frac{1}{2}$ LSB to the bottom reference level. The voltage corresponding to 1LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

Full-scale error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that will switch the ADC output from code 1022 to code 1023. The ideal voltage level is determined by subtracting the voltage corresponding to $\frac{1}{2}$ LSB from the top reference level. The voltage corresponding to 1LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

4. Analog Input Bandwidth—The analog input bandwidth is defined as the max. frequency of a 1dBFS input sine that can be applied to the device for which an extra 3dB attenuation is observed in the reconstructed output signal.

5. Output Timing—Output timing $t_{d(o)}$ is measured from the 1.5V level of the CLK input falling edge to the 10%/90% level of the digital output. The digital output load is not higher than 10pF.

Output hold time $t_{h(o)}$ is measured from the 1.5V level of the C_{OUT} input rising edge to the 10%/90% level of the digital output. The digital output load is not less than 2pF. Aperture delay $t_{d(A)}$ is measured from the 1.5V level of the CLK input to the actual sampling instant.

The \overline{OE} signal is asynchronous. \overline{OE} timing t_{dis} is measured from the $V_{IH(MIN)}$ level of \overline{OE} to the high-impedance state of the output data. The digital output load is not higher than 10pF. \overline{OE} timing t_{en} is measured from the $V_{IL(MAX)}$ level of \overline{OE} to the instant when the output data reaches $V_{OH(min)}$ or $V_{OL(max)}$ output levels. The digital output load is not higher than 10pF.

6. Pipeline Delay (latency)—The number of clock cycles between conversion initiation on an input sample and the corresponding output data being made available from the ADC pipeline. Once the data pipeline is full, new valid output data is provided on every clock cycle. The first valid data is available on the output pins after the latency time plus the output delay time $t_{d(o)}$ through the digital output buffers. Note that a minimum $t_{d(o)}$ is not guaranteed because data can transition before or after a CLK edge. It is possible to use CLK for latching data, but at the risk of the prop delay varying over temperature, causing data to transition one CLK cycle earlier or later. The recommended method is to use the latch signals C_{OUT} and $\overline{C_{OUT}}$ which are designed to provide reliable setup and hold times with respect to the data out.

7. Wake-Up Time—Wake-up time is from the power-down state to accurate ADC samples being taken, and is specified for external reference sources applied to the device and an 80MHz clock applied at the time of release of STDBY. Cells that need to power up are the bandgap, bias generator, SHAs, and ADCs.

8. Power-Up Time—Power-up time is from the power-down state to accurate ADC samples being taken with an 80MHz clock applied at the time of release of STDBY. Cells that need to power up are the bandgap, internal reference circuit, bias generator, SHAs, and ADCs.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5203IPFB	OBSOLETE	TQFP	PFB	48		TBD	Call TI	Call TI	-40 to 85	AZ5203	
ADS5203IPFBG4	OBSOLETE	TQFP	PFB	48		TBD	Call TI	Call TI	-40 to 85		
ADS5203IPFBR	OBSOLETE	TQFP	PFB	48		TBD	Call TI	Call TI	-40 to 85	AZ5203	
ADS5203IPFBG4	OBSOLETE	TQFP	PFB	48		TBD	Call TI	Call TI	-40 to 85		

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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

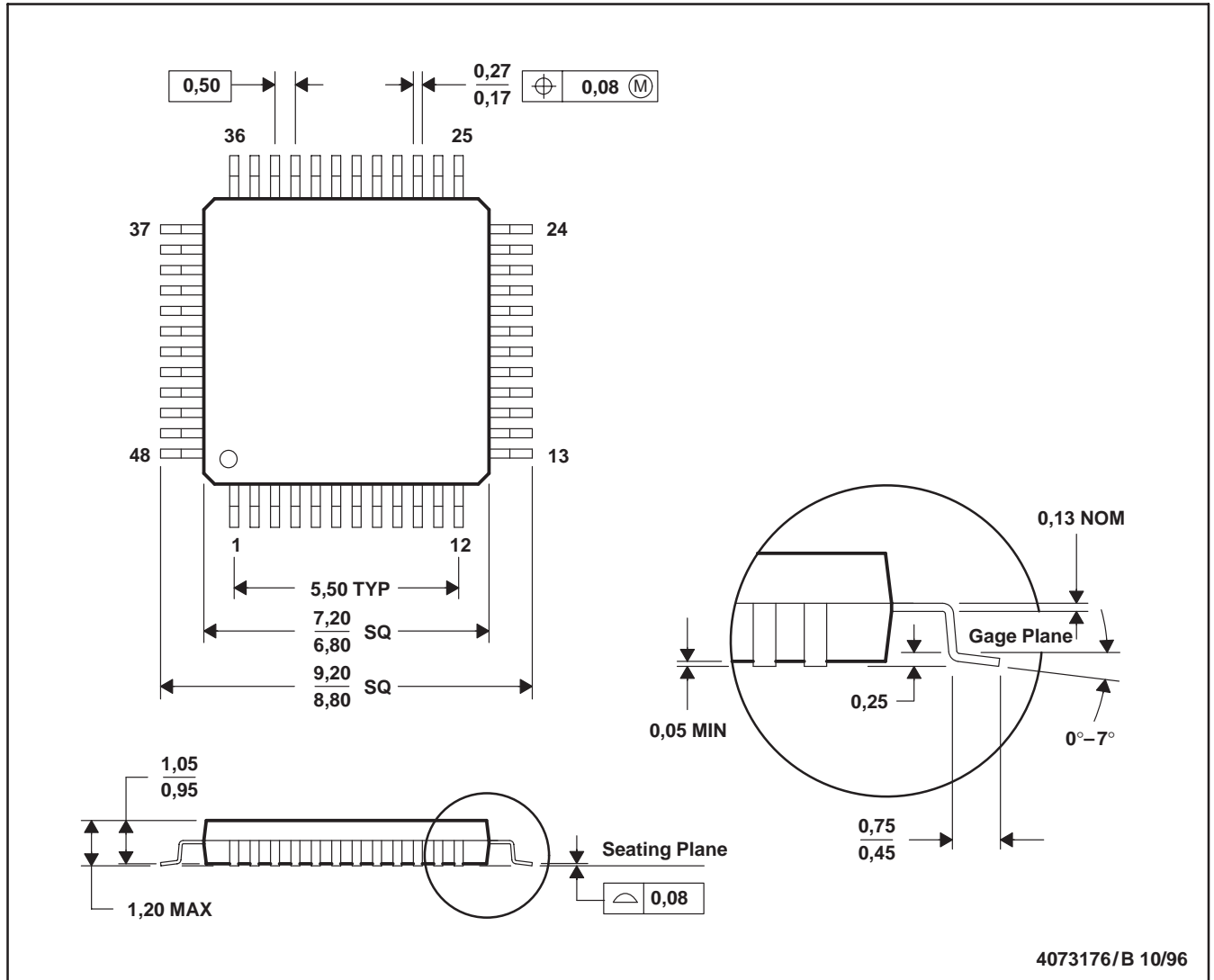
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PFB (S-PQFP-G48)

PLASTIC QUAD FLATPACK



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