THE DATASHEET OF

ADS1254E/2K5

SBAS213B – JUNE 2001 – REVISED JUNE 2006

24-Bit, 20kHz, Low Power ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 24 BITS—NO MISSING CODES
- 19 BITS EFFECTIVE RESOLUTION UP TO 20kHz DATA RATE
- LOW NOISE: 1.8ppm
- FOUR DIFFERENTIAL INPUTS
- INL: 15ppm (max)
- EXTERNAL REFERENCE (0.5V to 5V)
- POWER-DOWN MODE
- SYNC MODE
- LOW POWER: 4mW at 20kHz
- SEPARATE DIGITAL INTERFACE SUPPLY 1.8V to 3.6V

APPLICATIONS

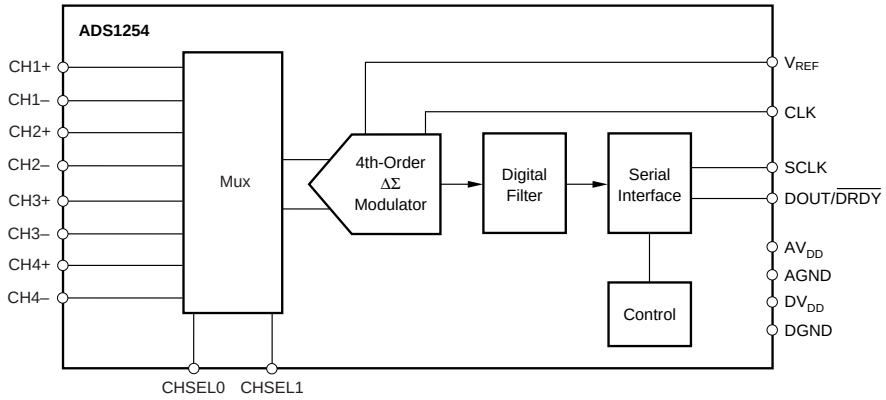
- CARDIAC DIAGNOSTICS
- DIRECT THERMOCOUPLE INTERFACES
- BLOOD ANALYSIS
- INFRARED PYROMETERS
- LIQUID/GAS CHROMATOGRAPHY
- PRECISION PROCESS CONTROL

DESCRIPTION

The ADS1254 is a precision, wide dynamic range, delta-sigma, Analog-to-Digital (A/D) converter with 24-bit resolution. The delta-sigma architecture is used for wide dynamic range and to ensure 24 bits of no missing codes performance. An effective resolution of 19 bits (1.8ppm of rms noise) is achieved for conversion rates up to 20kHz.

The ADS1254 is designed for high-resolution measurement applications in cardiac diagnostics, smart transmitters, industrial process control, weight scales, chromatography, and portable instrumentation. The converter includes a flexible, two-wire synchronous serial interface for low-cost isolation.

The ADS1254 is a multi-channel converter and is offered in an SSOP-20 package.



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ABSOLUTE MAXIMUM RATINGS[1]

Analog Input: Current (Momentary)	±100mA
(Continuous)	±10mA
Voltage	GND – 0.3V to V_{DD} + 0.3V
AV_{DD} to AGND	–0.3V to 6V
DV_{DD} to AV_{DD}	–6V to +6V
DV_{DD} to DGND	–0.3V to 6V
V_{REF} Voltage to AGND	–0.3V to V_{DD} + 0.3V
Digital Input Voltage to DGND	–0.3V to V_{DD} + 0.3V
Digital Output Voltage to DGND	–0.3V to V_{DD} + 0.3V
Lead Temperature (soldering, 10s)	+300°C
Power Dissipation (any package)	500mW

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

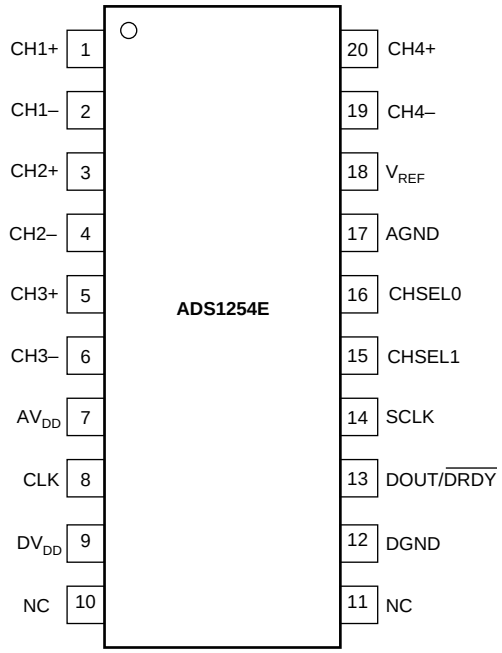
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

Top View **SSOP-20**



PIN DESCRIPTIONS

PIN	NAME	PIN DESCRIPTION
1	CH1+	Analog Input: Positive Input of the Differential Analog Input
2	CH1–	Analog Input: Negative Input of the Differential Analog Input
3	CH2+	Analog Input: Positive Input of the Differential Analog Input
4	CH2–	Analog Input: Negative Input of the Differential Analog Input
5	CH3+	Analog Input: Positive Input of the Differential Analog Input
6	CH3–	Analog Input: Negative Input of the Differential Analog Input
7	AV_{DD}	Input: Analog Power Supply Voltage, +5V
8	CLK	Digital Input: Device System Clock. The system clock is in the form of a CMOS-compatible clock. This is a Schmitt-Trigger input
9	DV_{DD}	Input: Digital Power Supply Voltage
10	NC	No Connection
11	NC	No Connection
12	DGND	Input: Digital Ground
13	DOUT/$\overline{DRDY}$	Digital Output: Serial Data Output/Data Ready. This output indicates that a new output word is available from the ADS1254 data output register. The serial data is clocked out of the serial data output shift register using SCLK.
14	SCLK	Digital Input: Serial Clock. The serial clock is in the form of a CMOS-compatible clock. The serial clock operates independently from the system clock; therefore, it is possible to run SCLK at a higher frequency than CLK. The normal state of SCLK is LOW. Holding SCLK HIGH will either initiate a modulator reset for synchronizing multiple converters or enter power-down mode. This is a Schmitt-Trigger input.
15	CHSEL1	Digital Input: Used to select analog input channel. This is a Schmitt-Trigger Input
16	CHSEL0	Digital Input: Used to select analog input channel. This is a Schmitt-Trigger Input
17	AGND	Input: Analog Ground
18	V_{REF}	Analog Input: Reference Voltage Input
19	CH4–	Analog Input: Negative Input of the Differential Analog Input
20	CH4+	Analog Input: Positive Input of the Differential Analog Input

ELECTRICAL CHARACTERISTICS

All specifications at T_{MIN} to T_{MAX}, AV_{DD} = +5V, DV_{DD} = +1.8V. CLK = 8MHz, and V_{REF} = 4.096, unless otherwise specified.

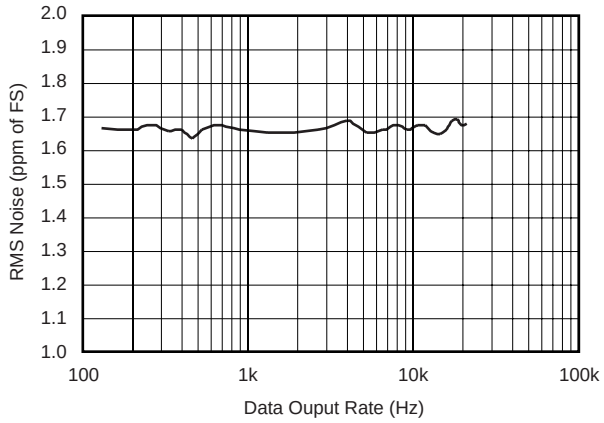
PARAMETER	CONDITIONS	ADS1254E MIN	ADS1254E TYP	ADS1254E MAX	UNITS
ANALOG INPUT					
Input Voltage Range		AGND		$\pm V_{REF}$	V
Input Impedance	CLK = 3,840Hz		260		MΩ
	CLK = 1MHz		1		MΩ
	CLK = 8MHz		125		kΩ
Input Capacitance			6		pF
Input Leakage	At +25°C		5	50	pA
	At T_{MIN} to T_{MAX}			1	nA
DYNAMIC CHARACTERISTICS					
Data Rate				20.8	kHz
Bandwidth	–3dB	4.24			kHz
Serial Clock (SCLK)				8	MHz
System Clock Input (CLK)				8	MHz
ACCURACY					
Integral Non-Linearity[1]			±0.0002	±0.0015	% of FSR
THD	1kHz Input; 0.1dB below FS		105		dB
Noise			1.8	2.7	ppm of FSR, rms
Resolution			24		Bits
No Missing Codes			24		Bits
Common-Mode Rejection	60Hz, AC	90	102		dB
Gain Error			0.1	1	% of FSR
Offset Error			±30	±100	ppm of FSR
Gain Sensitivity to V_{REF}			1:1		
Power-Supply Rejection Ratio		70	88		dB
PERFORMANCE OVER TEMPERATURE					
Offset Drift			0.07		ppm/°C
Gain Drift			0.4		ppm/°C
VOLTAGE REFERENCE					
V_{REF}		0.5	4.096	V_{DD}	V
Load Current			32		µA
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Level: V_{IH}		0.65 • DV_{DD}		DV_{DD} + 0.3	V
V_{IL}		–0.3		0.35 • DV_{DD}	V
V_{OH}	I_{OH} = –500µA	DV_{DD} –0.4			V
V_{OL}	I_{OL} = 500µA			0.4	V
Input (SCLK, CLK, CHSEL0, CHSEL1) Hysteresis			0.6		V
Data Format		Offset Binary Two's Complement			
POWER-SUPPLY REQUIREMENTS					
Power Supply Voltage	DV_{DD}	1.8		3.6	VDC
	AV_{DD}	4.75	5	5.25	VDC
Quiescent Current	AV_{DD} = +5V		0.8	1.15	mA
	DV_{DD} = +1.8V		0.2	0.4	mA
Operating Power			4.3	6.5	mW
Power-Down Current			0.4	1	µA
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+150	°C

NOTE: (1) Applies to full-differential signals.

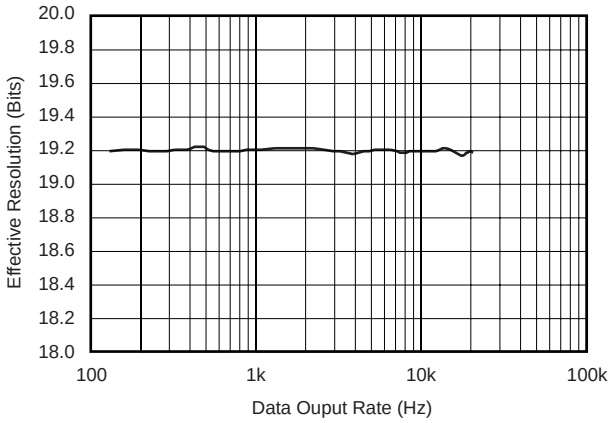
TYPICAL CHARACTERISTICS

At T_A = +25°C, AV_{DD} = +5V, DV_{DD} = +1.8V, CLK = 8MHz, and V_{REF} = 4.096, unless otherwise specified.

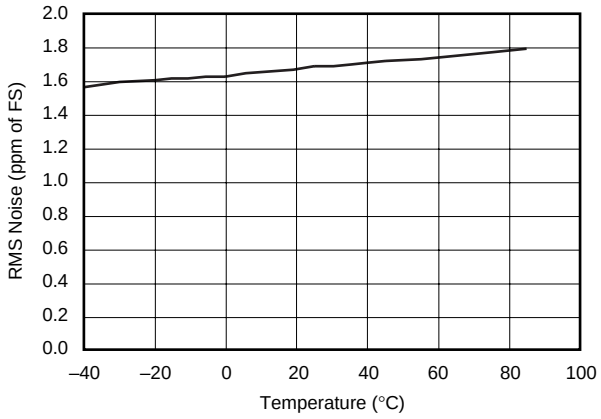
RMS NOISE vs DATA OUTPUT RATE



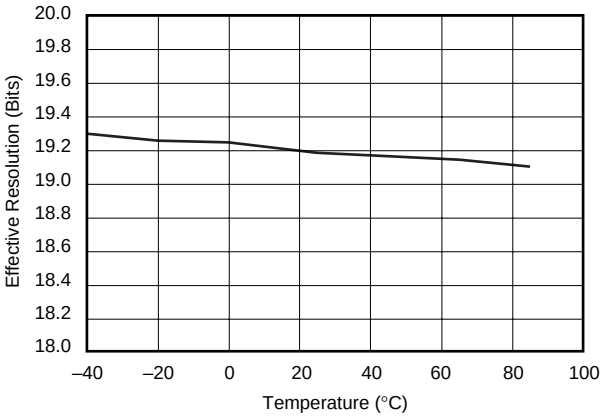
EFFECTIVE RESOLUTION vs DATA OUTPUT RATE



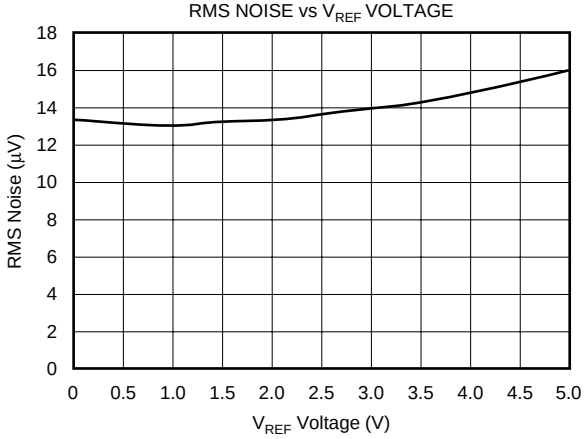
RMS NOISE vs TEMPERATURE



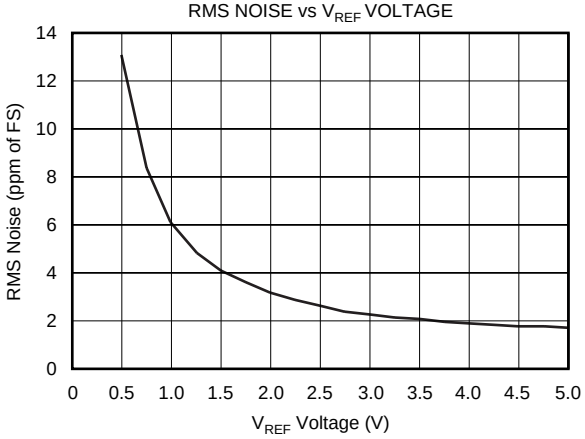
EFFECTIVE RESOLUTION vs TEMPERATURE



RMS NOISE vs V_{REF} VOLTAGE



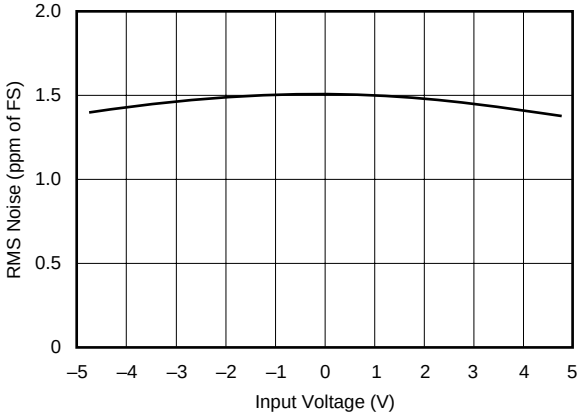
RMS NOISE vs V_{REF} VOLTAGE



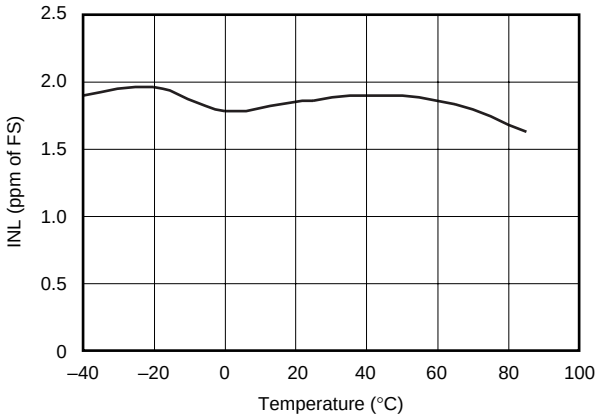
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, AV_{DD} = +5V, DV_{DD} = +1.8V, CLK = 8MHz, and V_{REF} = 4.096, unless otherwise specified.

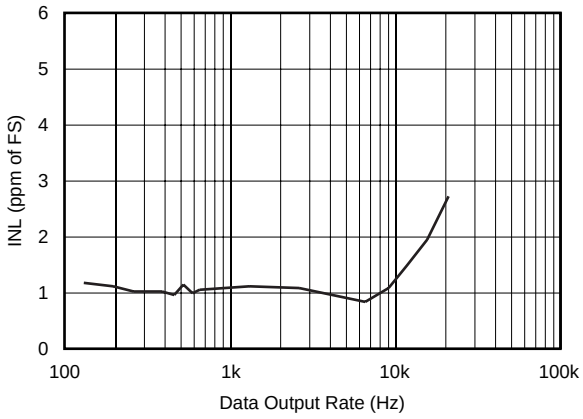
RMS NOISE vs INPUT VOLTAGE



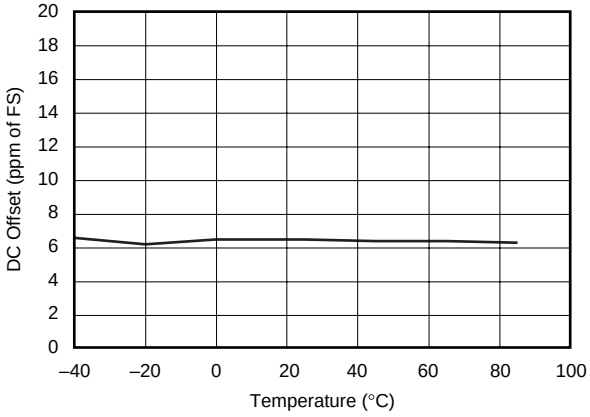
INTEGRAL NONLINEARITY vs TEMPERATURE



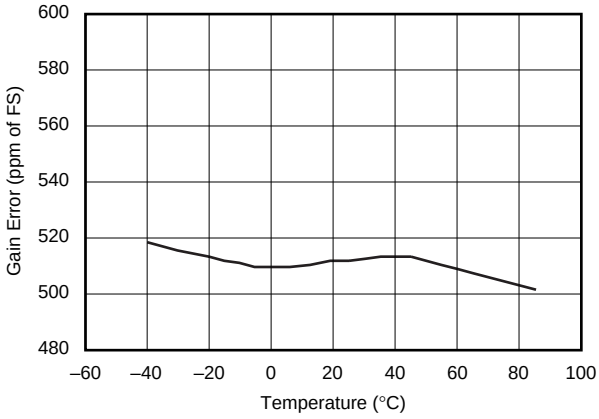
INTEGRAL NONLINEARITY vs DATA OUTPUT RATE



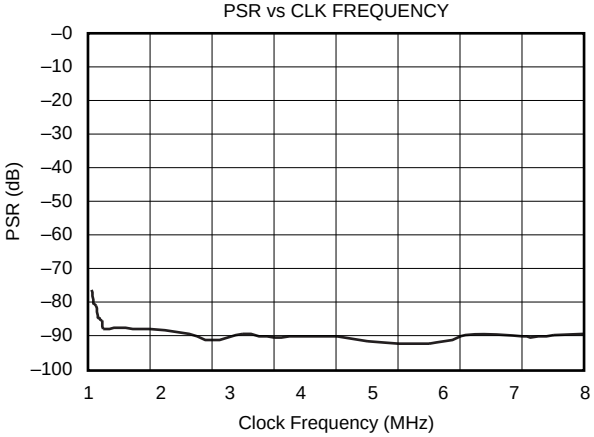
OFFSET vs TEMPERATURE



GAIN ERROR vs TEMPERATURE



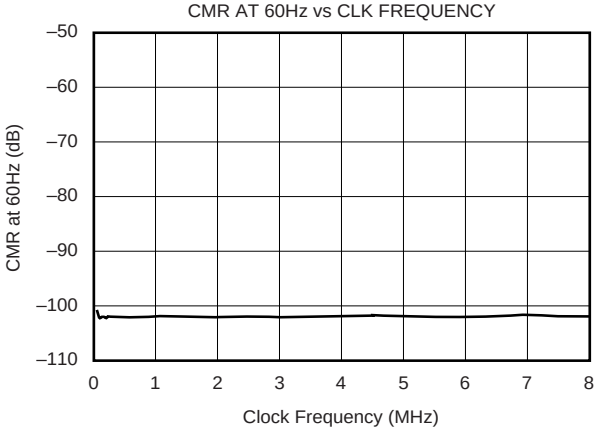
PSR vs CLK FREQUENCY



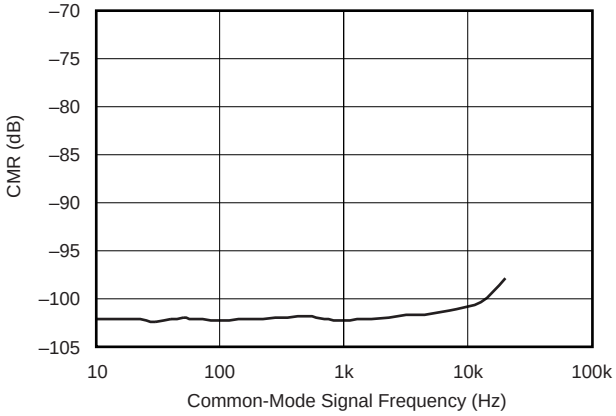
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, AV_{DD} = +5V, DV_{DD} = +1.8V, CLK = 8MHz, and V_{REF} = 4.096, unless otherwise specified.

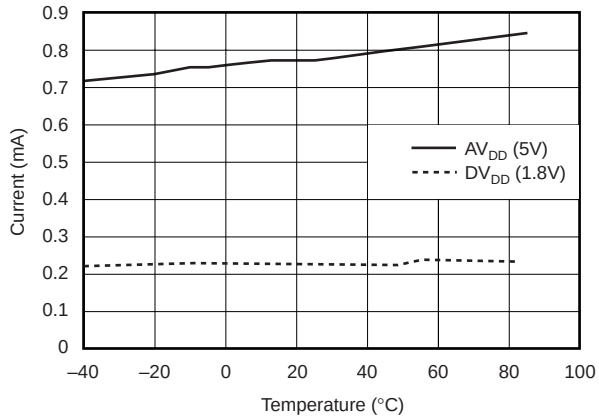
CMR AT 60Hz vs CLK FREQUENCY



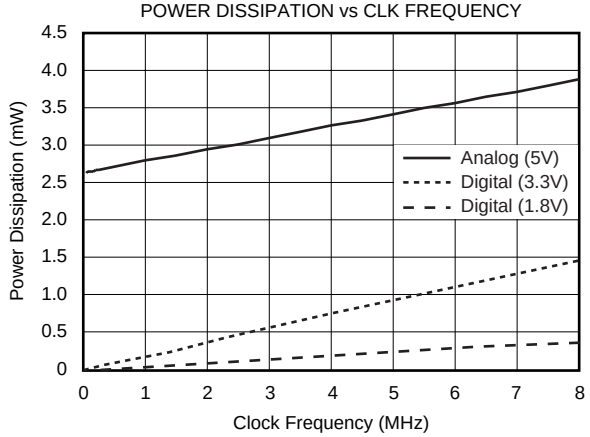
CMR vs COMMON-MODE FREQUENCY



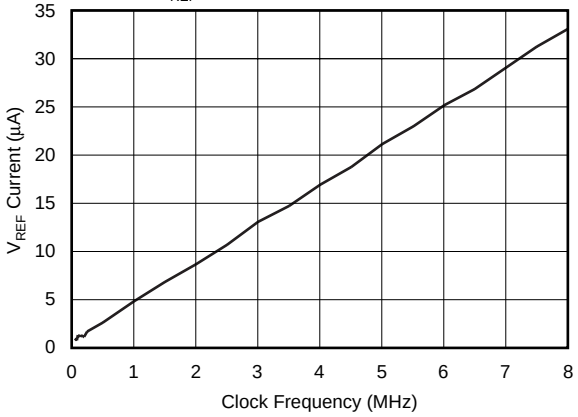
CURRENT vs TEMPERATURE



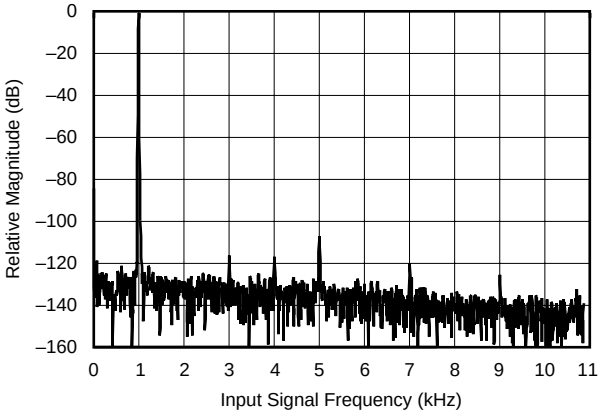
POWER DISSIPATION vs CLK FREQUENCY



V_{REF} CURRENT vs CLK FREQUENCY



TYPICAL FFT
(1kHz input at 0.1dB less than full-scale)



THEORY OF OPERATION

The ADS1254 is a precision, high-dynamic range, 24-bit, delta-sigma, A/D converter capable of achieving very high-resolution digital results at high data rates. The analog-input signal is sampled at a rate determined by the frequency of the system clock (CLK). The sampled analog input is modulated by the delta-sigma A/D modulator, which is followed by a digital filter. A $Sinc^5$ digital low-pass filter processes the output of the delta-sigma modulator and writes the result into the data-output register. The DOUT/$\overline{DRDY}$ pin is pulled LOW, indicating that new data is available to be read by the external microcontroller/microprocessor. As shown in the block diagram, the main functional blocks of the ADS1254 are the fourth-order delta-sigma modulator, a digital filter, control logic, and a serial interface. Each of these functional blocks is described below.

ANALOG INPUT

The ADS1254 contains a fully differential analog input. In order to provide low system noise, common-mode rejection of 102dB, and excellent power-supply rejection, the design topology is based on a fully differential switched-capacitor architecture. The bipolar input voltage range is from –4.096V to +4.096V, when the reference input voltage equals +4.096V. The bipolar range is with respect to $–V_{IN}$, and not with respect to GND.

Figure 1 shows the basic input structure of the ADS1254. The impedance is directly related to the sampling frequency of the input capacitor that is set by the CLK rate. Higher CLK rates result in lower impedance, and lower CLK rates result in higher impedance.

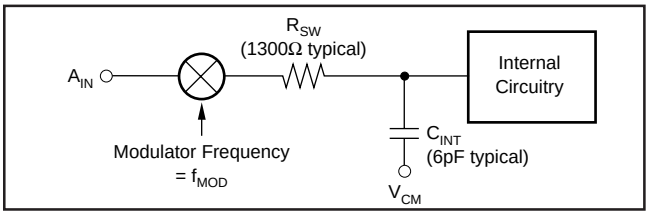


FIGURE 1. Analog-Input Structure.

The input impedance of the analog input changes with the ADS1254 system clock frequency (CLK). The relationship is:

$$A_{IN} \text{ Impedance } (\Omega) = (8\text{MHz/CLK}) \bullet 125{,}000$$

With regard to the analog-input signal, the overall analog performance of the device is affected by three items: first, the input impedance can affect accuracy. If the source impedance of the input signal is significant, or if there is passive filtering prior to the ADS1254, a significant portion of the signal can be lost across this external impedance. The magnitude of the effect is dependent on the desired system performance.

Second, the current into or out of the analog inputs must be limited. Under no conditions should the current into or out of the analog inputs exceed 10mA.

Third, to prevent aliasing of the input signal, the analog-input signal must be band limited. The bandwidth of the A/D converter is a function of the system clock frequency. With a system clock frequency of 8MHz, the data-output rate is 20.8kHz with a –3dB frequency of 4.24kHz. The –3dB frequency scales with the system clock frequency.

To ensure the best linearity of the ADS1254, a fully differential signal is recommended.

INPUT MULTIPLEXER

The CHSEL1 and CHSEL0 pins are used to select the analog input channel, as shown in Table I. The recommended method for changing channels is to change them after the conversion from the previous channel has been completed and read. When a channel is changed, internal logic senses the change on the falling edge of CLK and resets the conversion process. The conversion data from the new channel is valid on the first $\overline{DRDY}$ after the channel change.

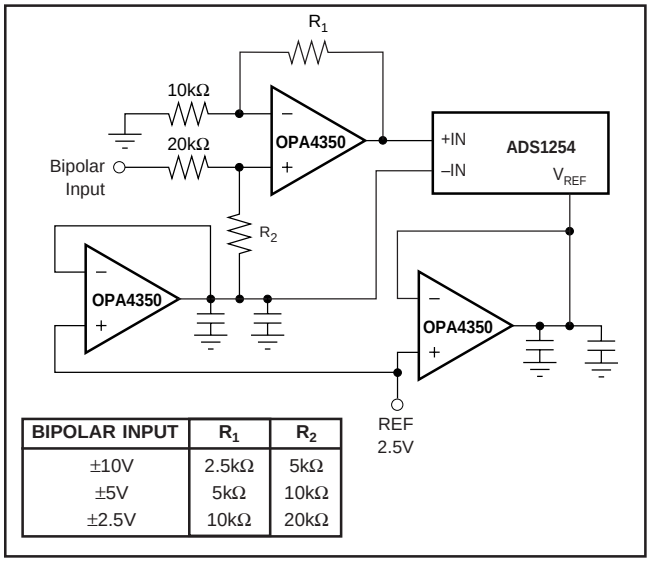
When multiplexing inputs, it is possible to achieve sample rates close to 4kHz. This is due to the fact that it requires five internal conversion cycles for the data to fully settle; the data also must be read before the channel is changed. The $\overline{DRDY}$ signal indicates a valid result after the five cycles have occurred.

BIPOLAR INPUT

CHSEL1	CHSEL0	CHANNEL
0	0	CH1
0	1	CH2
1	0	CH3
1	1	CH4

TABLE I. Channel Selection.

Each of the differential inputs of the ADS1254 must stay between AGND and AV_{DD}. With a reference voltage at less than half of AV_{DD}, one input can be tied to the reference voltage, and the other input can range from AGND to $2 \bullet V_{REF}$. By using a three op amp circuit featuring a single amplifier and four external resistors, the ADS1254 can be configured to accept bipolar inputs referenced to ground. The conventional ±2.5V, ±5V, and ±10V input ranges can be interfaced to the ADS1254 using the resistor values shown in Figure 2.



BIPOLAR INPUT	R_1	R_2
±10V	2.5kΩ	5kΩ
±5V	5kΩ	10kΩ
±2.5V	10kΩ	20kΩ

FIGURE 2. Level Shift Circuit for Bipolar Input Ranges.

DELTA-SIGMA MODULATOR

The ADS1254 operates from a nominal system clock frequency of 8MHz. The modulator frequency is fixed in relation to the system clock frequency. The system clock frequency is divided by 6 to derive the modulator frequency. Therefore, with a system clock frequency of 8MHz, the modulator frequency is 1.333MHz. Furthermore, the oversampling ratio of the modulator is fixed in relation to the modulator frequency. The oversampling ratio of the modulator is 64, and with the modulator frequency running at 1.333MHz, the data rate is 20.8kHz. Using a slower system clock frequency will result in a lower data output rate, as shown in Table II.

CLK (MHz)	DATA OUTPUT RATE (Hz)
8[1]	20,833
7.372800[1]	19,200
6.144000[1]	16,000
6.000000[1]	15,625
4.915200[1]	12,800
3.686400[1]	9,600
3.072000[1]	8,000
2.457600[1]	6,400
1.843200[1]	4,800
0.921600	2,400
0.460800	1,200
0.384000	1,000
0.192000	500
0.038400	100
0.023040	60
0.019200	50
0.011520	30
0.009600	25
0.007680	20
0.006400	16.67
0.005760	15
0.004800	12.50
0.003840	10

NOTE: (1) Standard Clock Oscillator.

TABLE II. CLK Rate versus Data Output Rate.

REFERENCE INPUT

Reference input takes an average current of 32µA with a 8MHz system clock. This current will be proportional to the system clock. A buffered reference is recommended for the ADS1254. The recommended reference circuit is shown in Figure 3.

Reference voltages higher than 4.096V will increase the full-scale range, while the absolute internal circuit noise of the converter remains the same. This will decrease the noise in terms of ppm of full scale, which increases the effective resolution (see the typical characteristic curve, *RMS Noise vs V_{REF} Voltage*).

DIGITAL FILTER

The digital filter of the ADS1254, referred to as a $sinc^5$ filter, computes the digital result based on the most recent outputs from the delta-sigma modulator. At the most basic level, the digital filter can be thought of as simply averaging the modulator results in a weighted form and presenting this average as the digital output. The digital output rate, or data rate, scales directly with the system CLK frequency. This allows the data output rate to be changed over a very wide range (five orders of magnitude) by changing the system CLK frequency. However, it is important to note that the –3dB point of the filter is 0.2035 times the data output rate, so the data output rate should allow for sufficient margin to prevent attenuation of the signal of interest.

Since the conversion result is essentially an average, the data-output rate determines the location of the resulting notches in the digital filter (see Figure 4). Note that the first notch is located at the data-output rate frequency, and subsequent notches are located at integer multiples of the data-output rate to allow for rejection of not only the fundamental frequency, but also harmonic frequencies. In this manner, the data-output rate can be used to set specific notch frequencies in the digital filter response.

For example, if the rejection of power-line frequencies is desired, then the data-output rate can simply be set to the power-line frequency. For 50Hz rejection, the system CLK

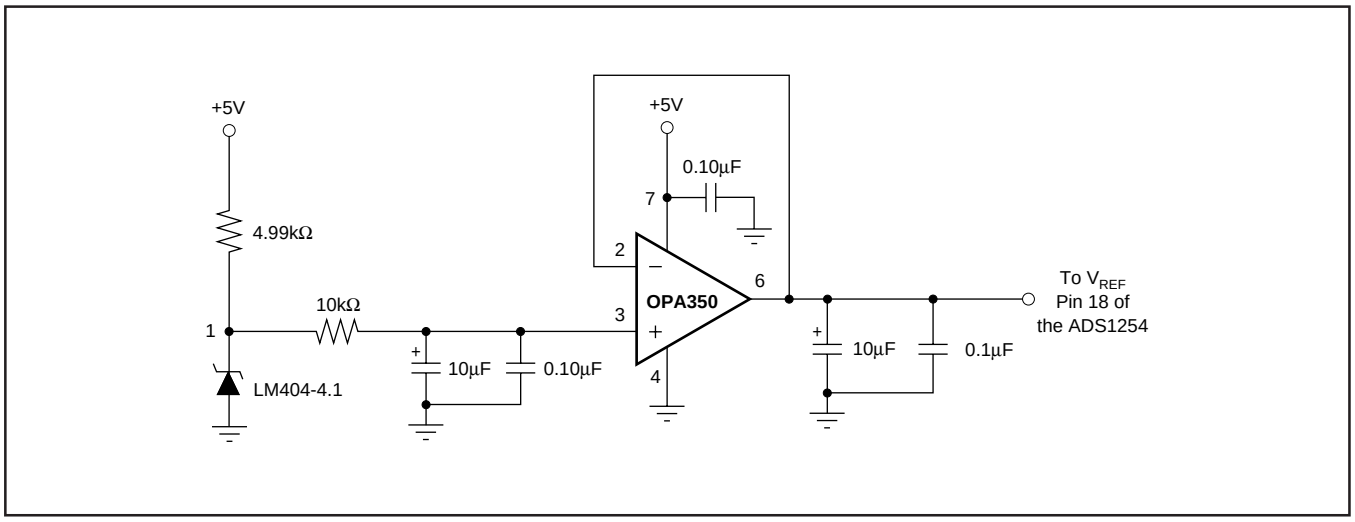


FIGURE 3. Recommended External Voltage Reference Circuit for Best Low-Noise Operation with the ADS1254.

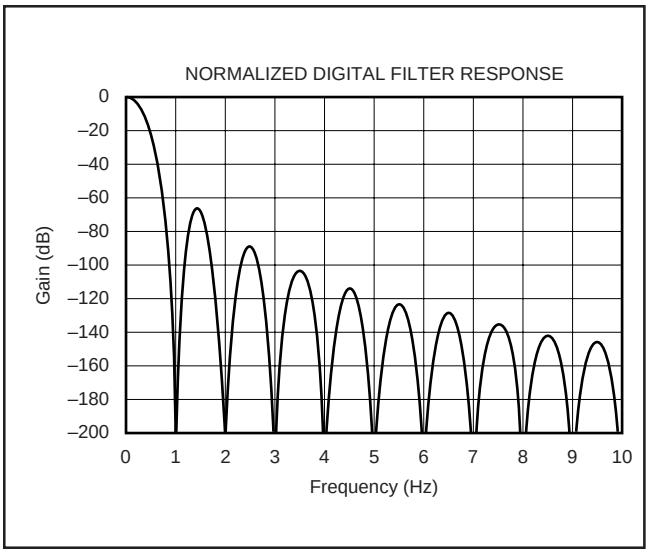


FIGURE 4. Normalized Digital Filter Response.

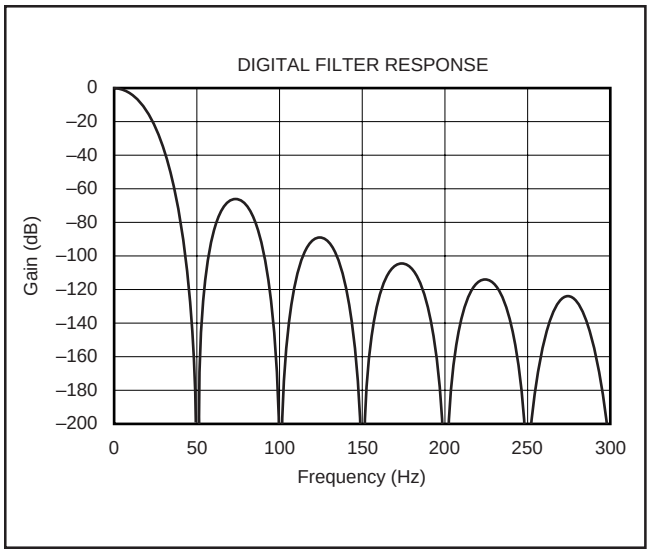


FIGURE 5. Digital Filter Response (50Hz).

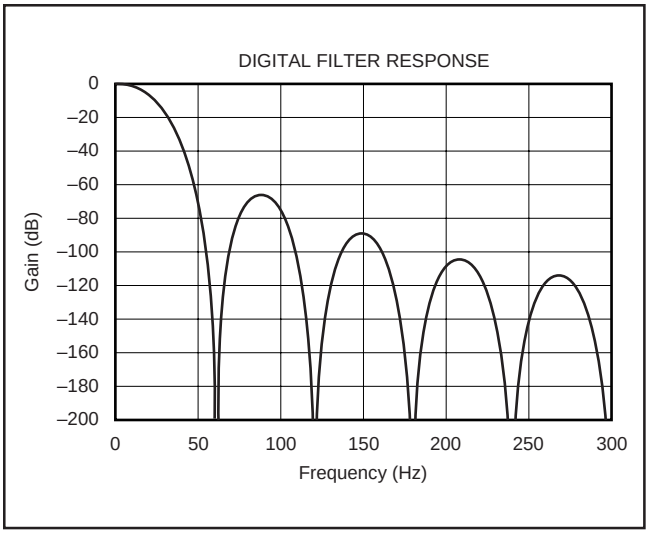


FIGURE 6. Digital Filter Response (60Hz).

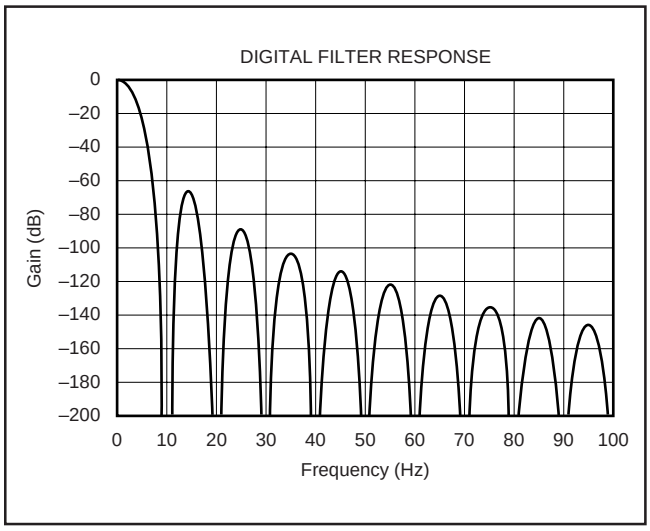


FIGURE 7. Digital Filter Response (10Hz).

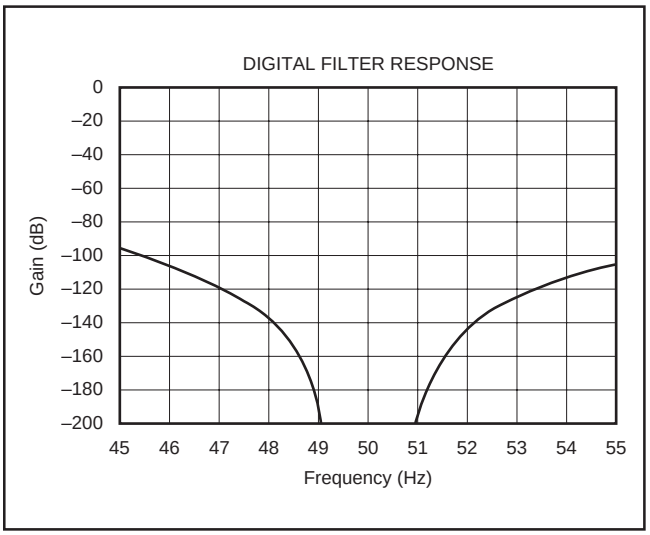


FIGURE 8. Expanded Digital Filter Response (50Hz with a 50Hz Data Output Rate).

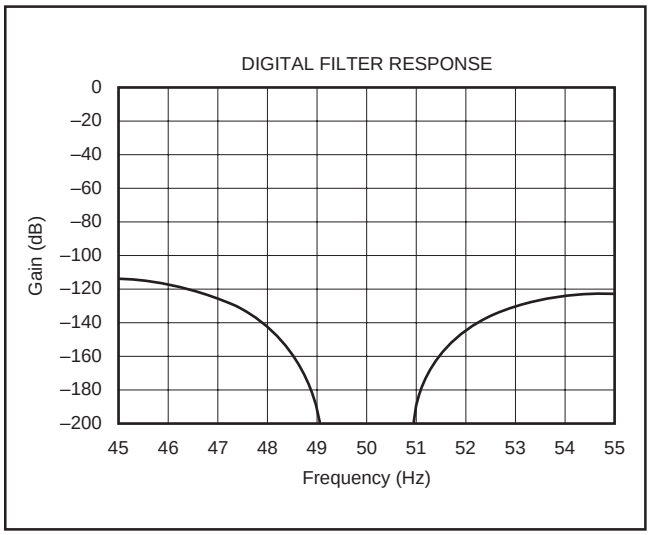


FIGURE 9. Expanded Digital Filter Response (50Hz with a 10Hz Data Output Rate).

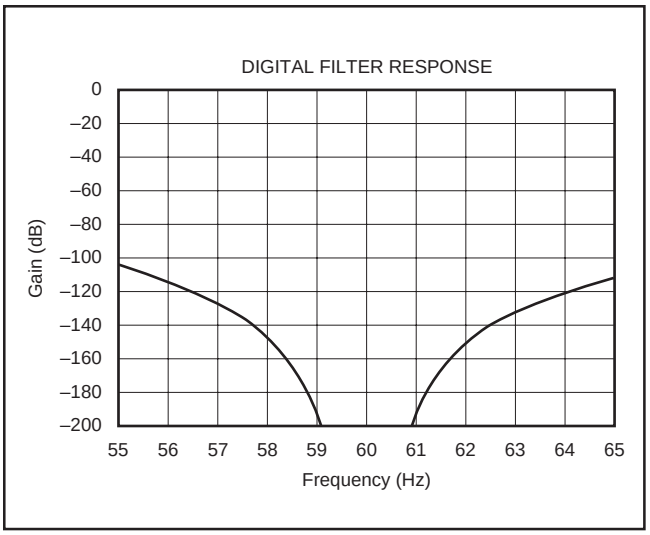


FIGURE 10. Expanded Digital Filter Response (60Hz with a 60Hz Data Output Rate).

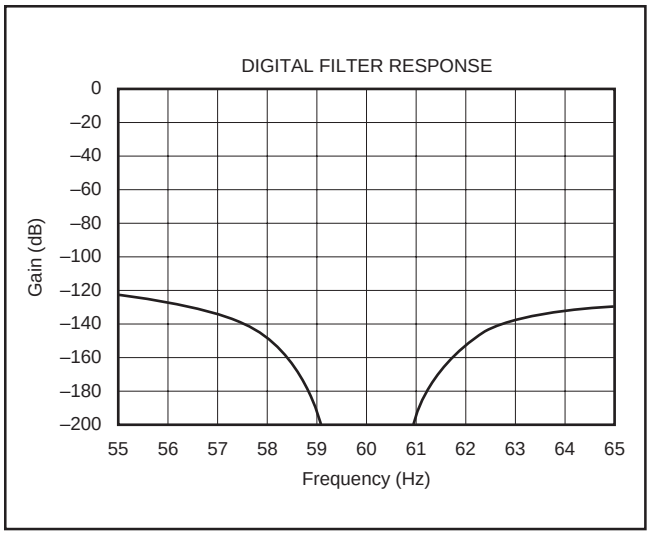


FIGURE 11. Expanded Digital Filter Response (60Hz with a 10Hz Data Output Rate).

frequency should be 19.200kHz, this will set the data-output rate to 50Hz (see Table II and Figure 5). For 60Hz rejection, the system CLK frequency should be 23.040kHz; this will set the data-output rate to 60Hz (see Table II and Figure 6). If both 50Hz and 60Hz rejection are required, then the system CLK should be 3.840kHz; this will set the data-output rate to 10Hz and reject both 50Hz and 60Hz (See Table II and Figure 7).

There is an additional benefit in using a lower data-output rate. It provides better rejection of signals in the frequency band of interest. For example, with a 50Hz data-output rate, a significant signal at 75Hz may alias back into the passband at 25Hz. This is due to the fact that rejection at 75Hz may only be 66dB in the stopband—frequencies higher than the first-notch frequency (see Figure 5). However, setting the data-output rate to 10Hz will provide 135dB rejection at 75Hz (see Figure 7). A similar benefit is gained at frequencies near the data-output rate (see Figures 8, 9, 10, and 11). For example, with a 50Hz data-output rate, rejection at 55Hz may only be 105dB (see Figure 8). However, with a 10Hz data-output rate, rejection at 55Hz will be 122dB (see Figure 9). If a slower data-output rate does not meet the system requirements, then the analog front end can be designed to provide the needed attenuation to prevent aliasing. Additionally, the data-output rate may be increased and additional digital filtering may be done in the processor or controller.

The digital filter is described by the following transfer function:

$$|H(f)| = \left| \frac{\sin\left(\frac{\pi \cdot f \cdot 64}{f_{MOD}}\right)}{64 \cdot \sin\left(\frac{\pi \cdot f}{f_{MOD}}\right)} \right|^5$$

or

$$H(z) = \left(\frac{1 - z^{-64}}{64 \cdot \left(1 - z^{-1}\right)} \right)^5$$

The digital filter requires five conversions to fully settle. The modulator has an oversampling ratio of 64; therefore, it requires 5 • 64, or 320 modulator results, or clocks, to fully settle. Since the modulator clock is derived from the system clock (CLK) (modulator clock = CLK ÷ 6), the number of system clocks required for the digital filter to fully settle is 5 • 64 • 6, or 1920 CLKs. This means that any significant step change at the analog input requires five full conversions to settle. However, if the step change at the analog input occurs asynchronously to the DOUT/$\overline{\text{DRDY}}$ pulse, six conversions are required to ensure full settling.

CONTROL LOGIC

The control logic is used for communications and control of the ADS1254.

Power-Up Sequence

Prior to power-up, all digital and analog-input pins must be LOW. During power-up, these signal inputs should never exceed $+AV_{DD}$ or $+DV_{DD}$.

Once the ADS1254 powers up, the DOUT/$\overline{DRDY}$ line will pulse LOW on the first conversion for which the data is valid from the analog input signal.

DOUT/$\overline{DRDY}$

The DOUT/$\overline{DRDY}$output signal alternates between two modes of operation. The first mode of operation is the Data Ready mode ($\overline{DRDY}$) to indicate that new data has been loaded into the data-output register and is ready to be read. The second mode of operation is the Data Output (DOUT) mode and is used to serially shift data out of the Data Output Register (DOR). The time domain partitioning of the $\overline{DRDY}$ and DOUT function as shown in Figure 12.

See Figure 13 for the basic timing of DOUT/$\overline{DRDY}$. During the time defined by t_2, t_3, and t_4, the DOUT/$\overline{DRDY}$ pin functions in $\overline{DRDY}$ mode. The state of the DOUT/$\overline{DRDY}$ pin would be HIGH prior to the internal transfer of new data to the DOR. The result of the A/D conversion would be written to the DOR from MSB to LSB in the time defined by t_1 (see Figures 12 and 13). The DOUT/$\overline{DRDY}$ line would then pulse LOW for the time defined by t_2, and then drive the line HIGH for the time defined by t_3 to indicate that new data was available to be read. At this point, the function of the DOUT/$\overline{DRDY}$ pin would change to DOUT mode. Data would be shifted out on the pin after t_7. If the MSB is high (because of a negative result) the DOUT/$\overline{DRDY}$ signal will stay HIGH after the end of time t_3. The device communicating with the ADS1254 can provide SCLKs to the ADS1254 after the time defined by t_6. The normal mode of reading data from the ADS1254 would be for the device reading the ADS1254 to latch the data on the rising edge of SCLK (since data is shifted out of the ADS1254 on the falling edge of SCLK). In order to retrieve valid data, the entire DOR must be read before the DOUT/$\overline{DRDY}$ pin reverts back to $\overline{DRDY}$ mode.

If SCLKs were not provided to the ADS1254 during the DOUT mode, the MSB of the DOR would be present on the DOUT/$\overline{DRDY}$ line until the beginning of the time defined by t_4. If an incomplete read of the ADS1254 took place while in DOUT mode (that is, fewer than 24 SCLKs were provided), the state of the last bit read would be present on the DOUT/$\overline{DRDY}$ line until the beginning of the time defined by t_4. If more than 24 SCLKs were provided during DOUT mode, the DOUT/$\overline{DRDY}$ line would stay LOW until the time defined by t_4.

The internal data pointer for shifting data out on DOUT/$\overline{DRDY}$ is reset on the falling edge of the time defined by t_1 and t_4. This ensures that the first bit of data shifted out of the ADS1254 after $\overline{DRDY}$ mode is always the MSB of new data.

SYNCHRONIZING MULTIPLE CONVERTERS

The normal state of SCLK is LOW; however, by holding SCLK HIGH, multiple ADS1254s can be synchronized. This is accomplished by holding SCLK HIGH for at least four, but less than twenty, consecutive DOUT/$\overline{DRDY}$ cycles (see Figure 14). After the ADS1254 circuitry detects that SCLK has been held HIGH for four consecutive DOUT/$\overline{DRDY}$ cycles, the DOUT/$\overline{DRDY}$ pin will pulse LOW for 3 CLK cycles and then be held HIGH, and the modulator will be held in a reset state. The modulator will be released from reset and synchronization will occur on the falling edge of SCLK. With multiple converters, the falling edge transition of SCLK must occur simultaneously on all devices. It is important to note that prior to synchronization, the DOUT/$\overline{DRDY}$ pulse of multiple ADS1254s in the system could have a difference in timing up to one $\overline{DRDY}$ period. Therefore, to ensure synchronization, the SCLK should be held HIGH for at least five $\overline{DRDY}$ cycles. The first DOUT/$\overline{DRDY}$ pulse after the falling edge of SCLK will occur at t_{14}. The first DOUT/$\overline{DRDY}$ pulse indicates valid data.

POWER-DOWN MODE

The normal state of SCLK is LOW, however, by holding SCLK HIGH, the ADS1254 will enter power-down mode. This is accomplished by holding SCLK HIGH for at least twenty consecutive DOUT/$\overline{DRDY}$ periods (see Figure 15). After the ADS1254 circuitry detects that SCLK has been held HIGH for four consecutive DOUT/$\overline{DRDY}$ cycles, the DOUT/$\overline{DRDY}$ pin will pulse LOW for 3 CLK cycles and then be held HIGH, and the modulator will be held in a reset state. If SCLK is held HIGH for an additional sixteen DOUT/$\overline{DRDY}$ periods, the ADS1254 will enter power-down mode. The part will be released from power-down mode on the falling edge of SCLK. It is important to note that the DOUT/$\overline{DRDY}$ pin will be held HIGH after four DOUT/$\overline{DRDY}$ cycles, but power-down mode will not be entered for an additional sixteen DOUT/$\overline{DRDY}$ periods. The first DOUT/$\overline{DRDY}$ pulse after the falling edge of SCLK will occur at t_{16} and will indicate valid data. Subsequent DOUT/$\overline{DRDY}$ pulses will occur normally.

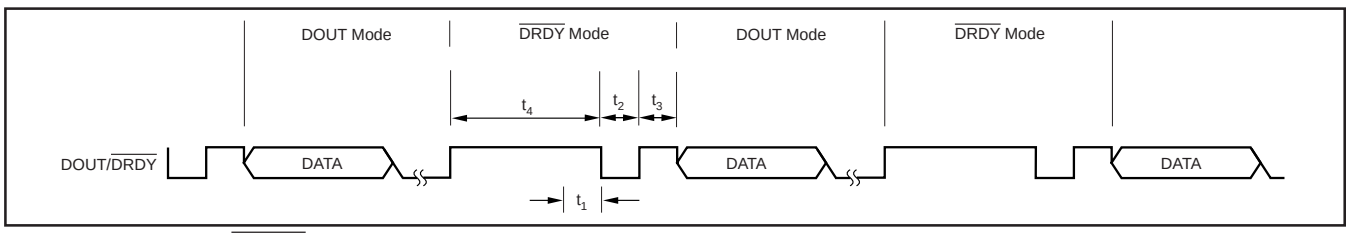


FIGURE 12. DOUT/$\overline{DRDY}$ Partitioning.

SERIAL INTERFACE

The ADS1254 includes a simple serial interface that can be connected to microcontrollers and digital signal processors in a variety of ways. Communications with the ADS1254 can commence on the first detection of the DOUT/$\overline{\text{DRDY}}$ pulse after power up.

It is important to note that the data from the ADS1254 is a 24-bit result transmitted MSB-first in Offset Two's Complement format, as shown in Table IV.

The data must be clocked out before the ADS1254 enters $\overline{\text{DRDY}}$ mode to ensure reception of valid data, as described in the DOUT/$\overline{\text{DRDY}}$ section of this data sheet.

ISOLATION

The serial interface of the ADS1254 provides for simple isolation methods. The CLK signal can be local to the ADS1254, which then only requires two signals (SCLK and DOUT/$\overline{\text{DRDY}}$) to be used for isolated data acquisition. The channel select signals (CHSEL0, CHSEL1) will also need to be isolated unless a counter is used to auto multiplex the channels.

DIFFERENTIAL VOLTAGE INPUT	DIGITAL OUTPUT (HEX)
+Full Scale	7FFFFFH
Zero	000000H
–Full Scale	800000H

TABLE IV. ADS1254 Data Format (Offset Two's Complement).

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{OSC}	CLK Period	125			ns
t_{DRDY}	Conversion Cycle		384 • t_{OSC}		ns
$\overline{\text{DRDY}}$ Mode	$\overline{\text{DRDY}}$ Mode		36 • t_{OSC}		ns
DOUT Mode	DOUT Mode		348 • t_{OSC}		ns
t_1	DOR Write Time		6 • t_{OSC}		ns
t_2	DOUT/$\overline{\text{DRDY}}$ LOW Time		6 • t_{OSC}		ns
t_3	DOUT/$\overline{\text{DRDY}}$ HIGH Time (Prior to Data Out)		6 • t_{OSC}		ns
t_4	DOUT/$\overline{\text{DRDY}}$ HIGH Time (Prior to Data Ready)		24 • t_{OSC}		ns
t_5	Rising Edge of CLK to Falling Edge of DOUT/$\overline{\text{DRDY}}$			60	ns
t_6	End of $\overline{\text{DRDY}}$ Mode to Rising Edge of First SCLK	30			ns
t_7	End of $\overline{\text{DRDY}}$ Mode to Data Valid (Propagation Delay)			60	ns
t_8	Falling Edge of SCLK to Data Valid (Hold Time)	5			ns
t_9	Falling Edge of SCLK to Next Data Out Valid (Propagation Delay)			60	ns
t_{10}	SCLK Setup Time for Synchronization or Power Down	30			ns
t_{11}	DOUT/$\overline{\text{DRDY}}$ Pulse for Synchronization or Power Down		3 • t_{OSC}		ns
t_{12}	Rising Edge of SCLK Until Start of Synchronization	1537 • CLK		7679 • CLK	ns
t_{13}	Synchronization Time	0.5 • CLK		6143.5 • CLK	ns
t_{14}	Falling Edge of CLK (After SCLK Goes Low) Until Start of $\overline{\text{DRDY}}$ Mode		2042.5 • CLK		ns
t_{15}	Rising Edge of SCLK Until Start of Power Down	7681 • CLK			ns
t_{16}	Falling Edge of CLK (After SCLK Goes Low) Until Start of $\overline{\text{DRDY}}$ Mode		2318.5 • t_{OSC}		ns
t_{17}	Falling Edge of Last DOUT/$\overline{\text{DRDY}}$ to Start of Power Down		6144.5 • t_{OSC}		ns
t_{18}	DOUT/$\overline{\text{DRDY}}$ High Time After Mux Change.		2043.5 • tosc		

NOTE: 30pF Load.

TABLE III. Digital Timing.

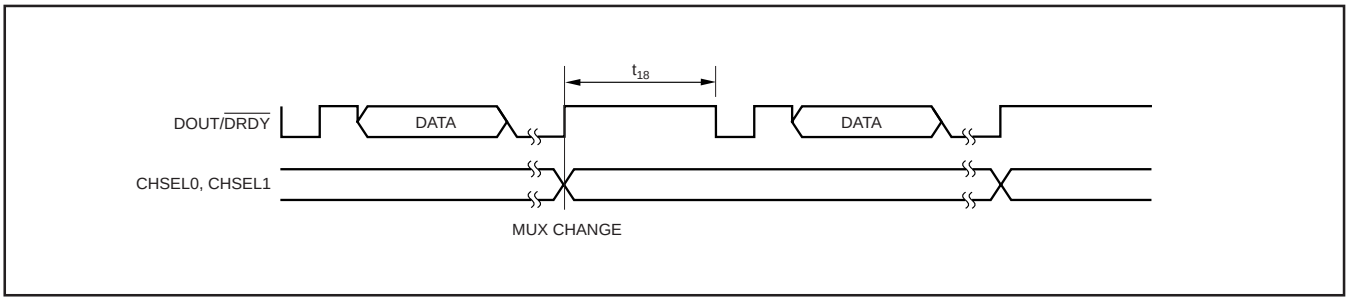


FIGURE 13. Multiplexer Operation.

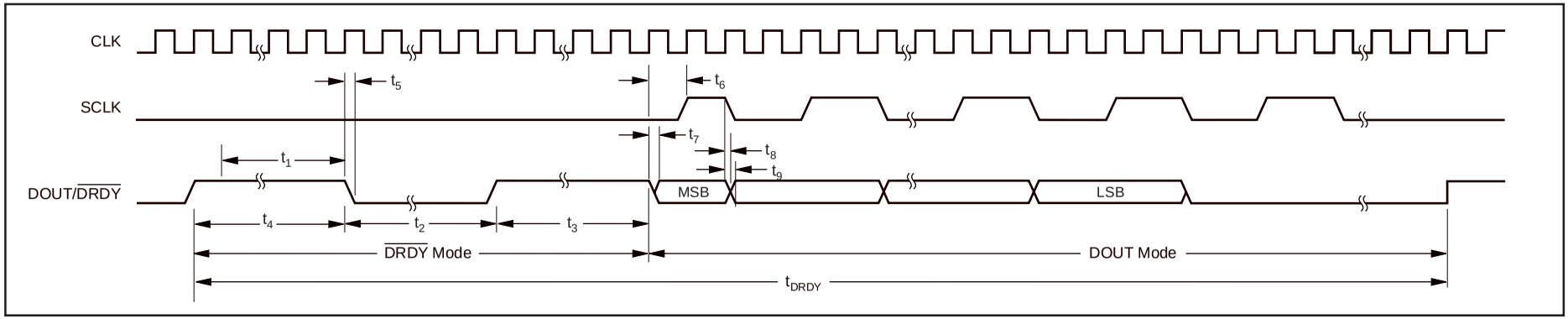


FIGURE 14. DOUT/$\overline{\text{DRDY}}$ Timing.

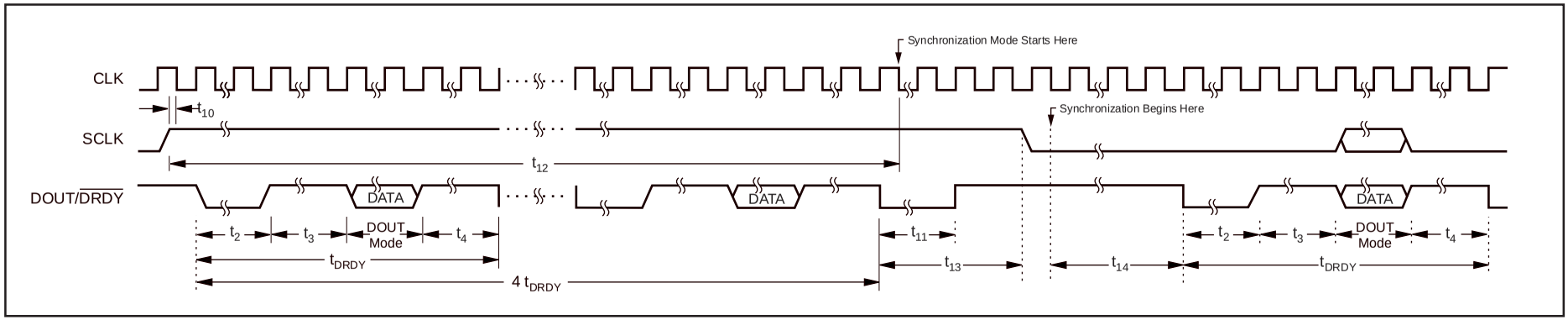


FIGURE 15. Synchronization Mode.

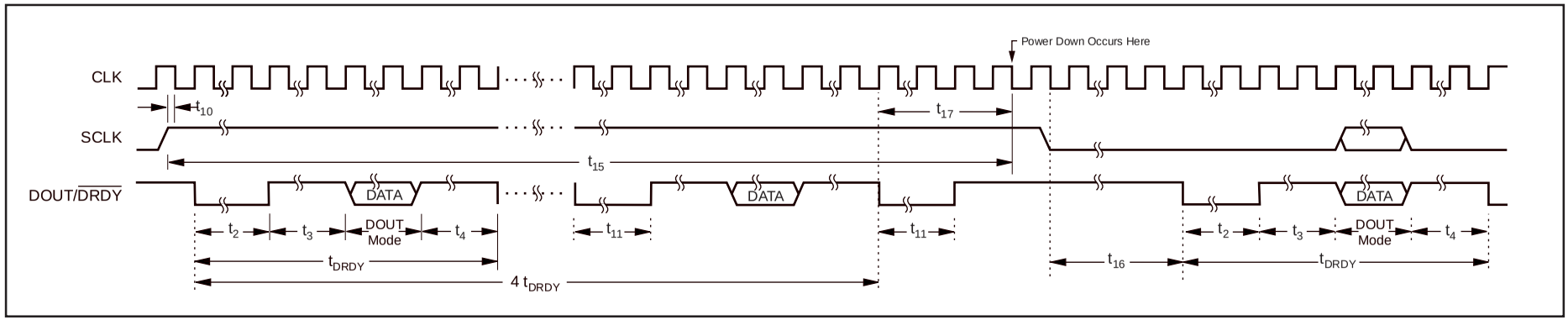


FIGURE 16. Power-Down Mode.

LAYOUT

POWER SUPPLY

The power supply should be well regulated and low noise. For designs requiring very high resolution from the ADS1254, power-supply rejection will be a concern. Avoid running digital lines under the device as they may couple noise onto the die. High-frequency noise can capacitively couple into the analog portion of the device and will alias back into the passband of the digital filter, affecting the conversion result. This clock noise will cause an offset error.

GROUNDING

The analog and digital sections of the system design should be carefully and cleanly partitioned. Each section should have its own ground plane with no overlap between them. AGND should be connected to the analog ground plane, as well as all other analog grounds. Do not join the analog and digital ground planes on the board, but instead connect the two with a moderate signal trace. For multiple converters, connect the two ground planes at one location as central to all of the converters as possible. In some cases, experimentation may be required to find the best point to connect the two planes together. The printed circuit board can be designed to provide different analog/digital ground connections via short jumpers. The initial prototype can be used to establish which connection works best.

DECOUPLING

Good decoupling practices should be used for the ADS1254 and for all components in the design. All decoupling capacitors, and specifically the 0.1µF ceramic capacitors, should be placed as close as possible to the pin being decoupled. A 1µF to 10µF capacitor, in parallel with a 0.1µF ceramic capacitor, should be used to decouple Supply to ground.

SYSTEM CONSIDERATIONS

The recommendations for power supplies and grounding will change depending on the requirements and specific design of the overall system. Achieving 24 bits of noise performance is a great deal more difficult than achieving 12 bits of noise performance. In general, a system can be broken up into four different stages:

- Analog Processing
- Analog Portion of the ADS1254
- Digital Portion of the ADS1254
- Digital Processing

For the simplest system consisting of minimal analog signal processing (basic filtering and gain), a microcontroller, and one clock source, one can achieve high resolution by powering all components by a common power supply. In addition, all components could share a common ground plane. Thus, there would be no distinctions between "analog" power and ground, and "digital" power and ground. The layout should still include a power plane, a ground plane, and careful decoupling. In a more extreme case, the design could include:

- Multiple ADS1254s
- Extensive Analog Signal Processing
- One or More Microcontrollers, Digital Signal Processors, or Microprocessors
- Many Different Clock Sources
- Interconnections to Various Other Systems

High resolution will be very difficult to achieve for this design. The approach would be to break the system into as many different parts as possible. For example, each ADS1254 may have its own "analog" processing front end.

DEFINITION OF TERMS

An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Analog-Input Differential Voltage—for an analog signal that is fully differential, the voltage range can be compared to that of an instrumentation amplifier. For example, if both analog inputs of the ADS1254 are at 2.048V, the differential voltage is 0V. If one analog input is at 0V and the other analog input is at 4.096V, then the differential voltage magnitude is 4.096V. This is the case regardless of which input is at 0V and which is at 4.096V. The digital-output result, however, is quite different. The analog-input differential voltage is given by the following equation:

$$+V_{IN} - (-V_{IN})$$

A positive digital output is produced whenever the analog-input differential voltage is positive, while a negative digital output is produced whenever the differential is negative. For example, a positive full-scale output is produced when the converter is configured with a 4.096V reference, and the analog-input differential is 4.096V. The negative full-scale output is produced when the differential voltage is –4.096V. In each case, the actual input voltages must remain within the –0.3V to $+AV_{DD}$ range.

Actual Analog-Input Voltage—the voltage at any one analog input relative to AGND.

Full-Scale Range (FSR)—as with most A/D Converters, the full-scale range of the ADS1254 is defined as the "input" that produces the positive full-scale digital output minus the "input" that produces the negative full-scale digital output. For example, when the converter is configured with a 4.096V reference, the differential full-scale range is:

[4.096V (positive full scale) – (–4.096V) (negative full scale)] = 8.192V

Least Significant Bit (LSB) Weight—this is the theoretical amount of voltage that the differential voltage at the analog input would have to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSB Weight} = \frac{\text{Full} - \text{Scale Range}}{2^N - 1} = \frac{2 \cdot V_{REF}}{2^N - 1}$$

where N is the number of bits in the digital output.

Conversion Cycle—as used here, a conversion cycle refers to the time period between DOUT/$\overline{\text{DRDY}}$ pulses.

Effective Resolution (ER)—of the ADS1254 in a particular configuration can be expressed in two different units: bits rms (referenced to output) and μVrms (referenced to input). Computed directly from the converter's output data, each is a statistical calculation based on a given number of results. Noise occurs randomly; the rms value represents a statistical measure that is one standard deviation. The ER in bits can be computed as follows:

$$\text{ER in bits rms} = \frac{20 \bullet \log\left(\frac{2 \bullet V_{REF}}{\text{Vrms noise}}\right)}{6.02}$$

The 2 • V_{REF} figure in each calculation represents the full-scale range of the ADS1254. This means that both units are absolute expressions of resolution—the performance in different configurations can be directly compared, regardless of the units.

f_{MOD}—frequency of the modulator and the frequency the input is sampled.

$$f_{MOD} = \frac{\text{CLK Frequency}}{6}$$

f_{DATA}—Data output rate.

$$f_{DATA} = \frac{f_{MOD}}{64} = \frac{\text{CLK Frequency}}{384}$$

Noise Reduction—for random noise, the ER can be improved with averaging. The result is the reduction in noise by the factor $\sqrt{N}$, where N is the number of averages, as shown in Table V. This can be used to achieve true 24-bit performance at a lower data rate. To achieve 24 bits of resolution, more than 24 bits must be accumulated. A 36-bit accumulator is required to achieve an ER of 24 bits. Table V uses V_{REF} = 4.096V, with the ADS1254 outputting data at 20kHz, a 4096 point average will take 204.8ms. The benefits of averaging will be degraded if the input signal drifts during that 200ms.

N (Number of Averages)	NOISE REDUCTION FACTOR	ER IN μVrms	ER IN BITS rms
1	1	14.6μV	19.1
2	1.414	10.3μV	19.6
4	2	7.3μV	20.1
8	2.82	5.16μV	20.6
16	4	3.65μV	21.1
32	5.66	2.58μV	21.6
64	8	1.83μV	22.1
128	11.3	1.29μV	22.6
256	16	0.91μV	23.1
512	22.6	0.65μV	23.6
1024	32	0.46μV	24.1
2048	45.25	0.32μV	24.6
4096	64	0.23μV	25.1

TABLE V. Averaging.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
6/06	B	11	DOUT/$\overline{\text{DRDY}}$	Text changes to DOUT/$\overline{\text{DRDY}}$ section.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1254E	ACTIVE	SSOP	DBQ	20	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1254E	Samples
ADS1254E/2K5	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1254E	Samples
ADS1254E/2K5G4	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1254E	Samples
ADS1254EG4	ACTIVE	SSOP	DBQ	20	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1254E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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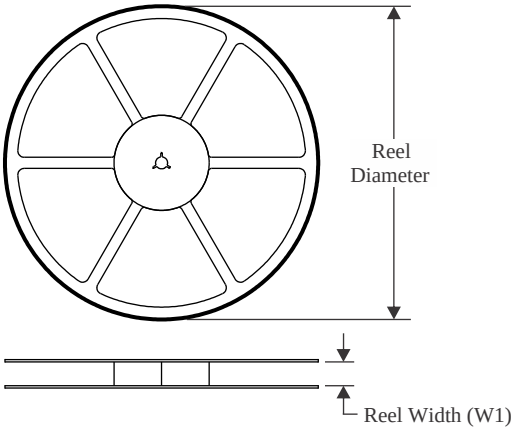
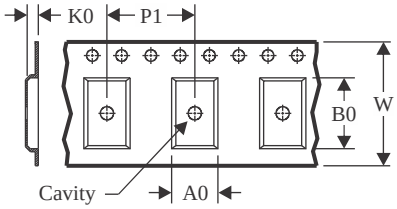
TAPE AND REEL INFORMATION

REEL DIMENSIONS

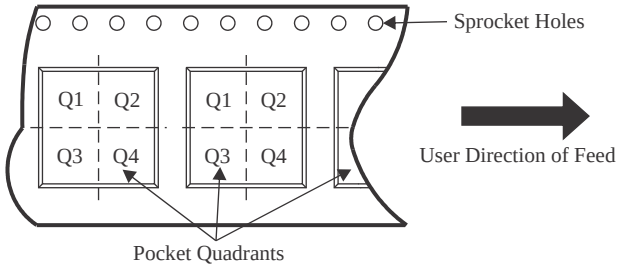


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

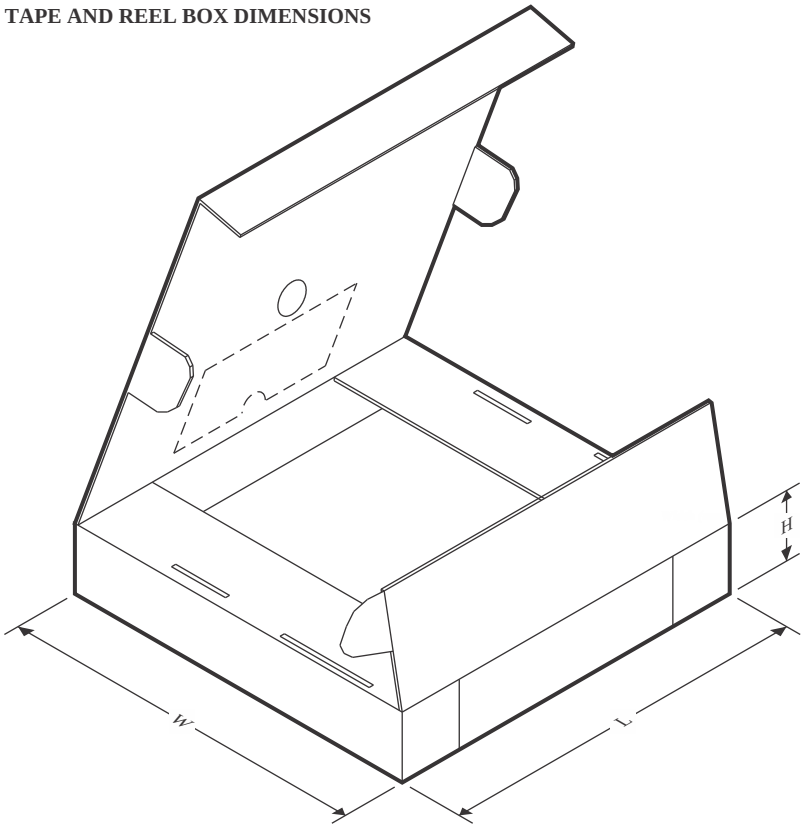
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1254E/2K5	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

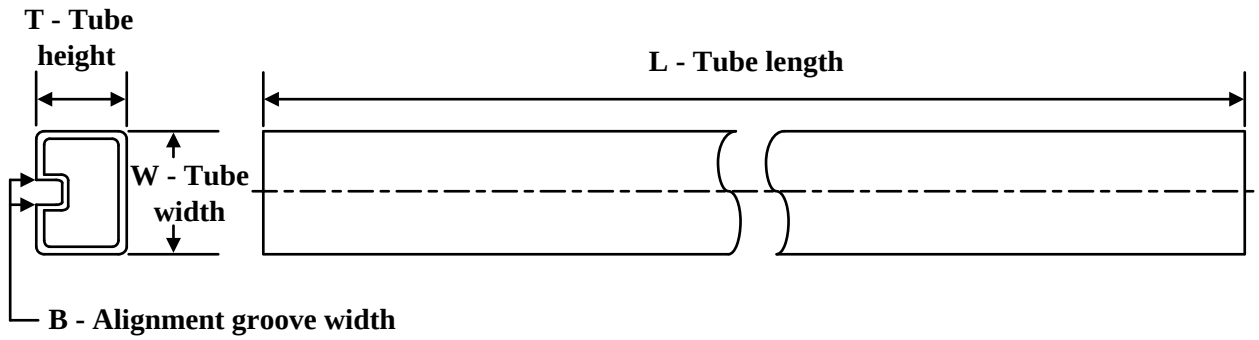
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1254E/2K5	SSOP	DBQ	20	2500	356.0	356.0	35.0

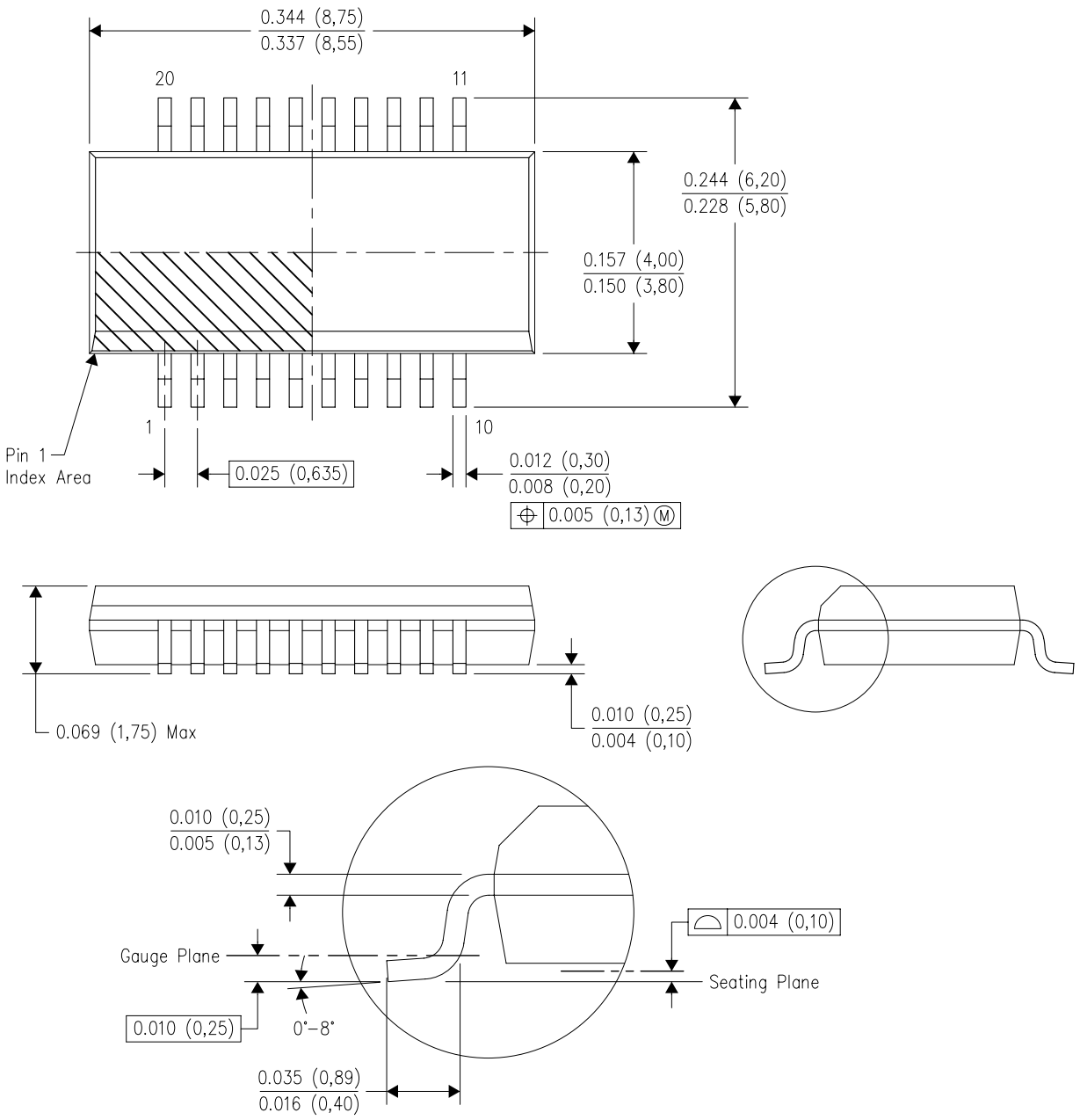
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS1254E	DBQ	SSOP	20	50	506.6	8	3940	4.32
ADS1254EG4	DBQ	SSOP	20	50	506.6	8	3940	4.32

DBQ (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AD.

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