WINSOURCE ELECTRONICS

THE DATASHEET OF

ADS1216Y

8-Channel, 24-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **24 BITS, NO MISSING CODES**
- **0.0015% INL**
- **22 BITS EFFECTIVE RESOLUTION (PGA = 1), 19 BITS (PGA = 128)**
- **PGA FROM 1 TO 128**
- **SINGLE-CYCLE SETTLING MODE**
- **PROGRAMMABLE DATA OUTPUT RATES: up to 1kHz**
- **ON-CHIP 1.25V/2.5V REFERENCE**
- **EXTERNAL DIFFERENTIAL REFERENCE: 0.1V to 2.5V**
- **ON-CHIP CALIBRATION**
- **SPI™-COMPATIBLE**
- **2.7V TO 5.25V**
- **< 1mW POWER CONSUMPTION**

APPLICATIONS

- **INDUSTRIAL PROCESS CONTROL**
- **LIQUID/GAS CHROMATOGRAPHY**
- **BLOOD ANALYSIS**
- **SMART TRANSMITTERS**
- **PORTABLE INSTRUMENTATION**
- **WEIGHT SCALES**
- **PRESSURE TRANSDUCERS**

DESCRIPTION

The ADS1216 is a precision, wide dynamic range, delta-sigma, Analog-to-Digital (A/D) converter with 24-bit resolution operating from 2.7V to 5.25V supplies. The delta-sigma A/D converter provides up to 24 bits of no-missing-code performance and an effective resolution of 22 bits.

The eight input channels are multiplexed. Internal buffering can be selected to provide a very high input impedance for direct connection to transducers or low-level voltage signals. Burnout current sources are provided that allow for the detection of an open or shorted sensor. An 8-bit Digital-to-Analog Converter (DAC) provides an offset correction with a range of 50% of the FSR (Full-Scale Range).

The PGA (Programmable Gain Amplifier) provides selectable gains of 1 to 128 with an effective resolution of 19 bits at a gain of 128. The A/D conversion is accomplished with a second-order delta-sigma modulator and programmable sinc filter. The reference input is differential and can be used for ratiometric cancellation. The onboard current DACs operate independently with the maximum current set by an external resistor.

The serial interface is SPI-compatible. Eight bits of digital I/O are also provided that can be used for input or output. The ADS1216 is designed for high-resolution measurement applications in smart transmitters, industrial process control, weight scales, chromatography, and portable instrumentation.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

	ADS1216	UNIT
AV_{DD} to AGND	–0.3 to +6	V
DV_{DD} to DGND	–0.3 to +6	V
Input Current	100, Momentary	mA
Input Current	10, Continuous	mA
A_{IN}	GND – 0.5 to AV_{DD} + 0.5	V
AV_{DD} to DV_{DD}	–6 to +6	V
AGND to DGND	–0.3 to +0.3	V
Digital Input Voltage to GND	–0.3 to DV_{DD} + 0.3	V
Digital Output Voltage to GND	–0.3 to DV_{DD} + 0.3	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	–40 to +85	°C
Storage Temperature Range	–60 to +100	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS: AV_{DD} = +5V

All specifications at T_{MIN} to T_{MAX}, AV_{DD} = +5V, DV_{DD} = +2.7V to +5.25V, f_{MOD} = 19.2kHz, PGA = 1, Buffer ON, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, and V_{REF} = +2.5V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1216			UNIT
		MIN	TYP	MAX	
ANALOG INPUT ($A_{IN}0$ – $A_{IN}7$, A_{INCOM})					
Analog input range	Buffer OFF	AGND – 0.1		AV_{DD} + 0.1	V
	Buffer ON	AGND + 0.05		AV_{DD} – 1.5	V
Full-scale input voltage range	(In+) – (In–); see Functional Block Diagram			$\pm V_{REF}$/PGA	V
Differential input impedance	Buffer OFF		5/PGA		MΩ
Input current	Buffer ON		0.5		nA
Bandwidth					
Fast-settling filter	–3dB		0.469 × f_{DATA}		Hz
$Sinc^2$ filter	–3dB		0.318 × f_{DATA}		Hz
$Sinc^3$ filter	–3dB		0.262 × f_{DATA}		Hz
Programmable gain amplifier	User-selectable gain ranges	1		128	
Input capacitance			9		pF
Input leakage current	Modulator OFF, T_A = +25°C		5		pA
Burnout current sources			2		µA
OFFSET DAC					
Offset DAC range			$\pm V_{REF}$ /(2 × PGA)		V
Offset DAC monotonicity		8			Bits
Offset DAC gain error			±10		%
Offset DAC gain error drift			1		ppm/°C
SYSTEM PERFORMANCE					
Resolution		24			Bits
No missing codes	$Sinc^3$ filter			24	Bits
Integral nonlinearity	End-point fit			±0.0015	% of FS
Offset error(1)			7.5		ppm of FS
Offset drift(1)			0.02		ppm of FS/°C
Gain error(1)			0.005		%
Gain error drift(1)			0.5		ppm/°C
Common-mode rejection	At DC	100			dB
	f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
	f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal-mode rejection	f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Output noise		See Typical Characteristics			
Power-supply rejection	At DC, dB = –20 log($\Delta V_{OUT}/\Delta V_{DD}$)(2)	80	95		dB
VOLTAGE REFERENCE INPUT					
Reference input range	REF IN+, REF IN–	AGND		AV_{DD}	V
V_{REF}	V_{REF} ≡ (REF IN+) – (REF IN–)	0.1	2.5	2.6	V
Common-mode rejection	at DC		120		dB
Common-mode rejection	f_{VREFCM} = 60Hz, f_{DATA} = 60Hz		120		dB
Bias current(3)	V_{REF} = 2.5V		1.3		µA

(1) Calibration can minimize these errors.
(2) Δ V_{OUT} is change in digital result.
(3) 12pF switched capacitor at f_{SAMP} clock frequency.

ELECTRICAL CHARACTERISTICS: AV_{DD} = +5V (continued)

All specifications at T_{MIN} to T_{MAX}, AV_{DD} = +5V, DV_{DD} = +2.7V to +5.25V, f_{MOD} = 19.2kHz, PGA = 1, Buffer ON, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, and V_{REF} = +2.5V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1216			UNIT
		MIN	TYP	MAX	
ON-CHIP VOLTAGE REFERENCE					
Output voltage	REF HI = 1	2.4	2.5	2.6	V
	REF HI = 0		1.25		V
Short-circuit current source			8		mA
Short-circuit current sink			50		µA
Short-circuit duration	Sink or source		Indefinite		
Drift			15		ppm/°C
Noise	V_{RCAP} = 0.1µF, BW = 0.1Hz to 100Hz		10		$µV_{PP}$
Output impedance	Sourcing 100µA		3		Ω
Startup time			50		µs
IDAC					
Full-scale output current	R_{DAC} = 150kΩ, range = 1		0.5		mA
	R_{DAC} = 150kΩ, range = 2		1		mA
	R_{DAC} = 150kΩ, range = 3		2		mA
	R_{DAC} = 15kΩ, range = 3		20		mA
Maximum short-circuit current duration	R_{DAC} = 10kΩ		Indefinite		
	R_{DAC} = 0kΩ			10	Minute
Monotonicity	R_{DAC} = 150kΩ	8			Bits
Compliance voltage		0		AV_{DD} – 1	V
Output impedance		See Typical Characteristics			
Power-supply rejection ratio	V_{OUT} = AV_{DD}/2		400		ppm/V
Absolute error	Individual IDAC		5		%
Absolute drift	Individual IDAC		75		ppm/°C
Mismatch error	Between IDACs, same range and code		0.25		%
Mismatch drift	Between IDACs, same range and code		15		ppm/°C
POWER-SUPPLY REQUIREMENTS					
Power-supply voltage	AV_{DD}	4.75		5.25	V
Analog current (I_{ADC} + I_{VREF} + IDAC)	$\overline{PDWN}$ = 0 or SLEEP		1		nA
ADC current (I_{ADC})	PGA = 1, buffer OFF		140	225	µA
	PGA = 128, buffer OFF		430	650	µA
	PGA = 1, buffer ON		180	275	µA
	PGA = 128, buffer ON		800	1250	µA
V_{REF} current (I_{VREF})			250	375	µA
IDAC current (IDAC)	Excludes load current		480	675	µA
Digital current	Normal mode, DV_{DD} = 5V		180	275	µA
	SLEEP mode, DV_{DD} = 5V		150		µA
	Read data continuous mode, DV_{DD} = 5V		230		µA
	$\overline{PDWN}$		1		nA
Power dissipation	PGA = 1, buffer OFF, REFEN = 0, IDACS OFF, DV_{DD} = 5V		1.6	2.5	mW
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

ELECTRICAL CHARACTERISTICS: AV_{DD} = +3V

All specifications at T_{MIN} to T_{MAX}, AV_{DD} = +3V, DV_{DD} = +2.7V to +5.25V, f_{MOD} = 19.2kHz, PGA = 1, Buffer ON, R_{DAC} = 75kΩ, f_{DATA} = 10Hz, and V_{REF} = +1.25V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1216			UNIT
		MIN	TYP	MAX	
ANALOG INPUT ($A_{IN}0$ – $A_{IN}7$, A_{INCOM})					
Analog input range	Buffer OFF	AGND – 0.1		AV_{DD} + 0.1	V
	Buffer ON	AGND + 0.05		AV_{DD} – 1.5	V
Full-scale input voltage range	(In+) – (In–); see Functional Block Diagram			$\pm V_{REF}$/PGA	V
Input impedance	Buffer OFF		5/PGA		MΩ
Input current	Buffer ON		0.5		nA
Bandwidth					
Fast-settling filter	–3dB		$0.469 \times f_{DATA}$		Hz
$Sinc^2$ filter	–3dB		$0.318 \times f_{DATA}$		Hz
$Sinc^3$ filter	–3dB		$0.262 \times f_{DATA}$		Hz
Programmable gain amplifier	User-selectable gain ranges	1		128	
Input capacitance			9		pF
Input leakage current	Modulator OFF, T_A = +25°C		5		pA
Burnout current sources			2		µA
OFFSET DAC					
Offset DAC range			$\pm V_{REF}/(2 \times PGA)$		V
Offset DAC monotonicity		8			Bits
Offset DAC gain error			±10		%
Offset DAC gain error drift			2		ppm/°C
SYSTEM PERFORMANCE					
Resolution		24			Bits
No missing codes	$Sinc^3$ filter			24	Bits
Integral nonlinearity	End-point fit			±0.0015	% of FS
Offset error(1)			15		ppm of FS
Offset drift(1)			0.04		ppm of FS/°C
Gain error(1)			0.010		%
Gain error drift(1)			1.0		ppm/°C
Common-mode rejection	At DC	100			dB
	f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
	f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal-mode rejection	f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Output noise		See Typical Characteristics			
Power-supply rejection	At DC, dB = $-20 \log(\Delta V_{OUT}/\Delta V_{DD})$(2)	75	90		dB
VOLTAGE REFERENCE INPUT					
Reference input range	REF IN+, REF IN–	0		AV_{DD}	V
V_{REF}	$V_{REF} \equiv$ (REF IN+) – (REF IN–)	0.1	1.25	1.3	V
Common-mode rejection	at DC		120		dB
Common-mode rejection	f_{VREFCM} = 60Hz, f_{DATA} = 60Hz		120		dB
Bias current(3)	V_{REF} = 1.25V		0.65		µA

(1) Calibration can minimize these errors.
(2) ΔV_{OUT} is change in digital result.
(3) 12pF switched capacitor at f_{SAMP} clock frequency.

ELECTRICAL CHARACTERISTICS: AV_{DD} = +3V (continued)

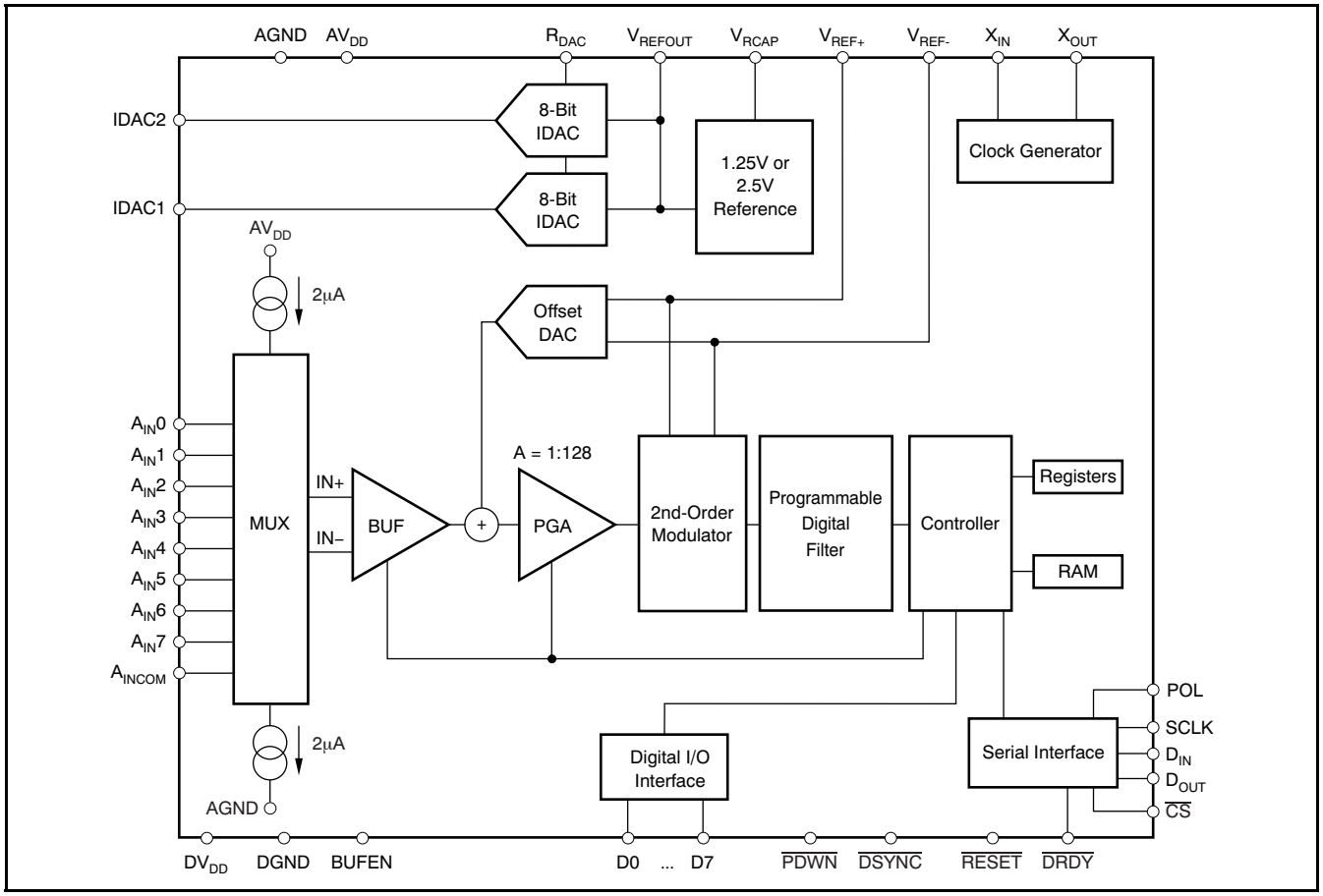
All specifications at T_{MIN} to T_{MAX}, AV_{DD} = +3V, DV_{DD} = +2.7V to +5.25V, f_{MOD} = 19.2kHz, PGA = 1, Buffer ON, R_{DAC} = 75kΩ, f_{DATA} = 10Hz, and V_{REF} = +1.25V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1216			UNIT
		MIN	TYP	MAX	
ON-CHIP VOLTAGE REFERENCE					
Output voltage	REF HI = 0	1.2	1.25	1.3	V
Short-circuit current source			3		mA
Short-circuit current sink			50		µA
Short-circuit duration	Sink or source		Indefinite		
Drift			15		ppm/°C
Noise	V_{RCAP} = 0.1µF, BW = 0.1Hz to 100Hz		10		$µV_{PP}$
Output impedance	Sourcing 100µA		3		Ω
Startup time			50		µs
IDAC					
Full-scale output current	R_{DAC} = 75kΩ, range = 1		0.5		mA
	R_{DAC} = 75kΩ, range = 2		1		mA
	R_{DAC} = 75kΩ, range = 3		2		mA
	R_{DAC} = 15kΩ, range = 3		20		mA
Maximum short-circuit current duration	R_{DAC} = 10kΩ		Indefinite		
	R_{DAC} = 0kΩ			10	Minute
Monotonicity	R_{DAC} = 75kΩ	8			Bits
Compliance voltage		0		AV_{DD} – 1	V
Output impedance		See Typical Characteristics			
Power-supply rejection ratio	V_{OUT} = AV_{DD}/2		600		ppm/V
Absolute error	Individual IDAC		5		%
Absolute drift	Individual IDAC		75		ppm/°C
Mismatch error	Between IDACs, same range and code		0.25		%
Mismatch drift	Between IDACs, same range and code		15		ppm/°C
POWER-SUPPLY REQUIREMENTS					
Power-supply voltage	AV_{DD}	2.7		3.3	V
Analog current (I_{ADC} + I_{VREF} + IDAC)	$\overline{PDWN}$ = 0 or SLEEP		1		nA
ADC current (I_{ADC})	PGA = 1, buffer OFF		120	200	µA
	PGA = 128, buffer OFF		370	600	µA
	PGA = 1, buffer ON		170	250	µA
	PGA = 128, buffer ON		750	1200	µA
V_{REF} current (I_{VREF})			250	375	µA
IDAC current (IDAC)	Excludes load current		480	675	µA
Digital current	Normal mode, DV_{DD} = 3V		90	200	µA
	SLEEP mode, DV_{DD} = 3V		75		µA
	Read data continuous mode, DV_{DD} = 3V		113		µA
	$\overline{PDWN}$ = 0		1		nA
Power dissipation	PGA = 1, buffer OFF, REFEN = 0, IDACS OFF, DV_{DD} = 3V		0.6	1.2	mW
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

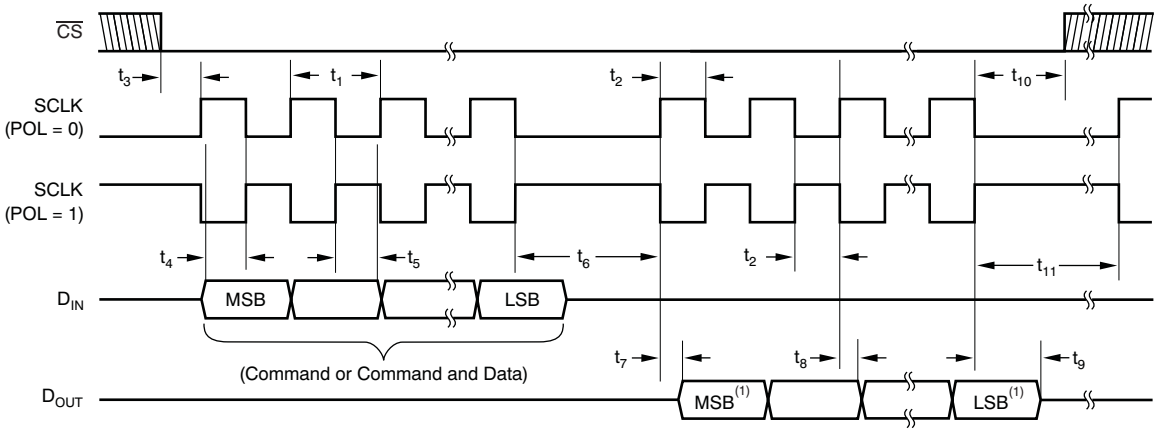
DIGITAL CHARACTERISTICS: T_{MIN} to T_{MAX}, DV_{DD} +2.7V to +5.25V

PARAMETER	CONDITIONS	ADS1216			UNIT
		MIN	TYP	MAX	
Digital input/output					
Logic family			CMOS		
Logic level: V_{IH}		$0.8 \times DV_{DD}$		DV_{DD}	V
Logic level: V_{IL}		DGND		$0.2 \times DV_{DD}$	V
Logic level: V_{OH}	I_{OH} = 1mA	DV_{DD} – 0.4			V
Logic level: V_{OL}	I_{OL} = 1mA	DGND		DGND + 0.4	V
Input leakage: I_{IH}	$V_I = DV_{DD}$			10	µA
Input leakage: I_{IL}	V_I = 0	–10			µA
Master clock rate: f_{OSC}		1		5	MHz
Master clock period: t_{OSC}	$1/f_{OSC}$	200		1000	ns

FUNCTIONAL BLOCK DIAGRAM

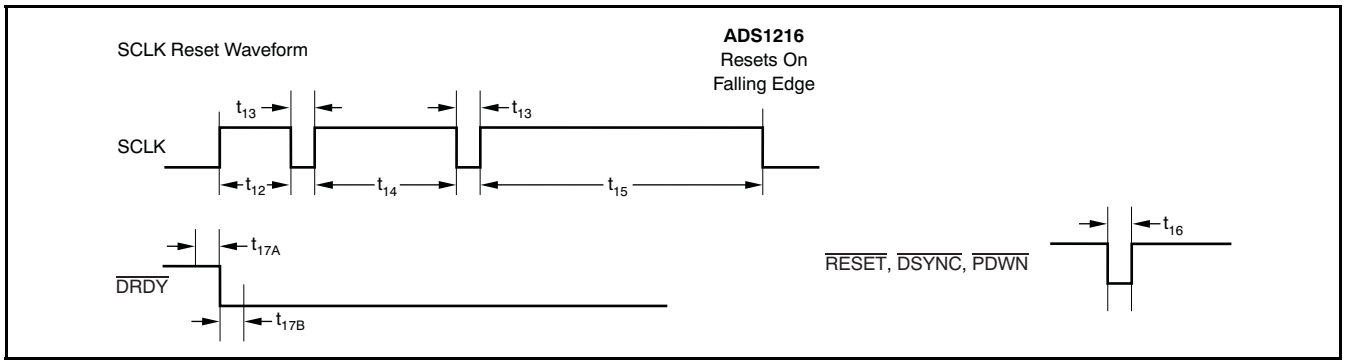


TIMING CHARACTERISTICS



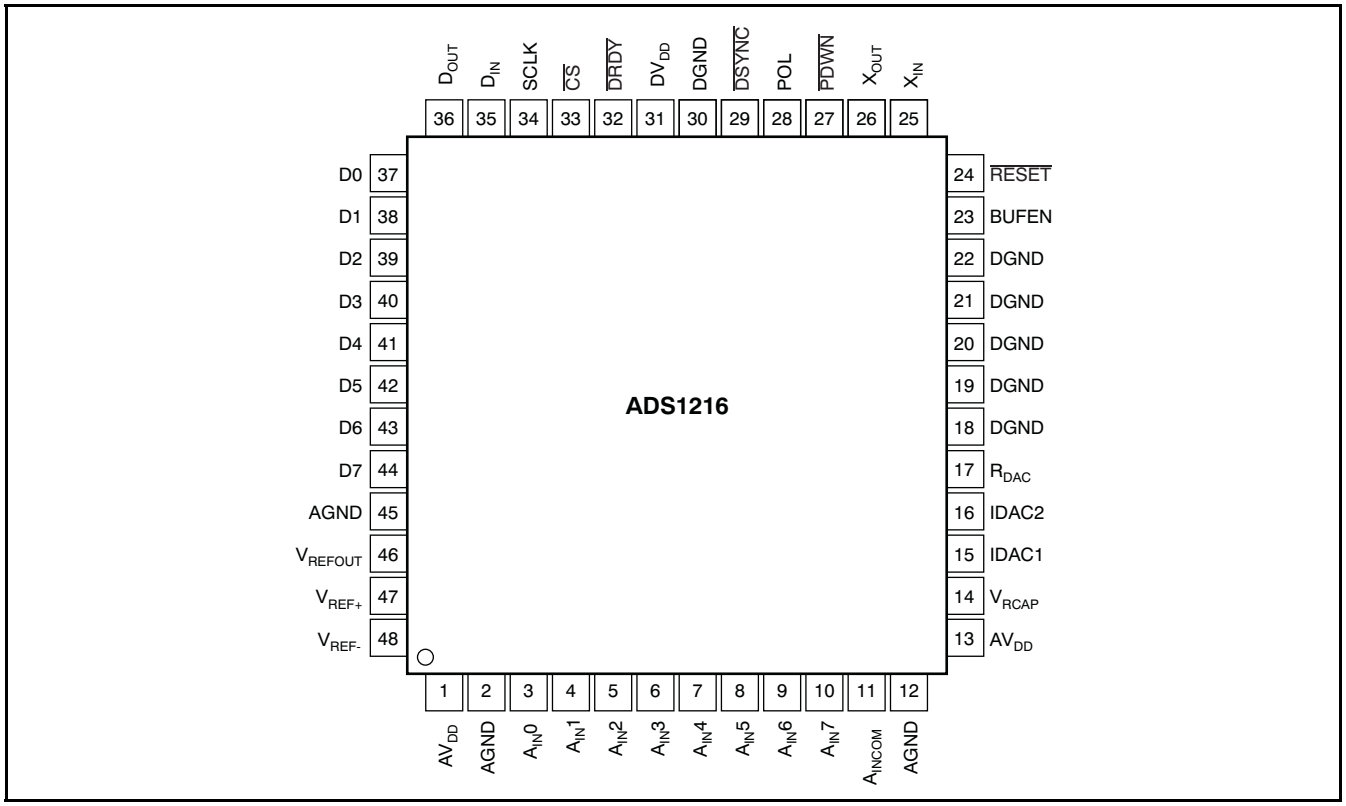
NOTE: (1) Bit Order = 0.

SPEC	DESCRIPTION	MIN	MAX	UNITS
t_1	SCLK period	4		t_{OSC} periods
			3	$\overline{DRDY}$ periods
t_2	SCLK pulse width, HIGH and LOW	200		ns
t_3	$\overline{CS}$ LOW to first SCLK edge; setup time	0		ns
t_4	D_{IN} valid to SCLK edge; setup time	50		ns
t_5	Valid D_{IN} to SCLK edge; hold time	50		ns
t_6	Delay between last SCLK edge for D_{IN} and first SCLK edge for D_{OUT}:			
	RDATA, RDATAC, RREG, WREG, RRAM, WRAM	50		t_{OSC} periods
	CSREG, CSRAMX, CSRAM	200		t_{OSC} periods
	CSARAM, CSARAMX	1100		t_{OSC} periods
t_7	SCLK edge to valid new D_{OUT}		50	ns
t_8	SCLK edge to D_{OUT}, hold time	0		ns
t_9	Last SCLK edge to D_{OUT} tri-state NOTE: D_{OUT} goes tri-state immediately when $\overline{CS}$ goes HIGH.	6	10	t_{OSC} periods
t_{10}	$\overline{CS}$ LOW time after final SCLK edge	16		t_{OSC} periods
t_{11}	Final SCLK edge of one op code until first edge SCLK of next command:			
	RREG, WREG, RRAM, WRAM, CSRAMX, CSARAMX, CSRAM, CSARAM, CSREG, SLEEP, RDATA, RDATAC, STOPC	4		t_{OSC} periods
	CREG, CRAM	220		t_{OSC} periods
	CREGA	1600		t_{OSC} periods
	SELFGCAL, SELFOCAL, SYSOCAL, SYSGCAL	7		$\overline{DRDY}$ periods
	SELFCAL	14		$\overline{DRDY}$ periods
	RESET (Command, SCLK or Pin), DSYNC	16		t_{OSC} periods



SPEC	DESCRIPTION	MIN	MAX	UNITS
t_{12}		300	500	t_{OSC} periods
t_{13}		5		t_{OSC} periods
t_{14}		550	750	t_{OSC} periods
t_{15}		1050	1250	t_{OSC} periods
t_{16}	Pulse width	4		t_{OSC} periods
t_{17A}	DOR data not valid during this update period	4		t_{OSC} periods
t_{17B}	DOR data not valid during this update period	12		t_{OSC} periods

DEVICE INFORMATION



DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS

PIN NUMBER	NAME	DESCRIPTION
1, 13	AV_{DD}	Analog power supply
2, 12, 45	AGND	Analog ground
3–10	$A_{IN}0–7$	Analog input 0–7
11	A_{INCOM}	Analog input common
14	V_{RCAP}	V_{REF} bypass capcitor
15	IDAC1	Current DAC1 output
16	IDAC2	Current DAC2 output
17	RDAC	Current DAC resistor
18–22, 30	DGND	Digital ground
23	BUFEN	Buffer enable
24	$\overline{\text{RESET}}$	Active LOW; resets the entire chip.
25	X_{IN}	Clock input
26	X_{OUT}	Clock output, used with crystal or resonator.
27	$\overline{\text{PDWN}}$	Active LOW; power down. The power-down function shuts down the analog and digital circuits.
28	POL	Serial clock polarity
29	$\overline{\text{DSYNC}}$	Active LOW; synchronization control
31	DV_{DD}	Digital power supply
32	$\overline{\text{DRDY}}$	Active LOW; data ready
33	$\overline{\text{CS}}$	Active LOW; chip select
34	SCLK	Serial clock, Schmitt trigger
35	D_{IN}	Serial data input, Schmitt trigger
36	D_{OUT}	Serial data output
37–44	D0–D7	Digital I/O 0–7
46	V_{REFOUT}	Voltage reference output
47	V_{REF+}	Positive differential reference input
48	$V_{REF–}$	Negative differential reference input

TYPICAL CHARACTERISTICS

At AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, and V_{REF} = +2.5V, unless otherwise specified.

EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO

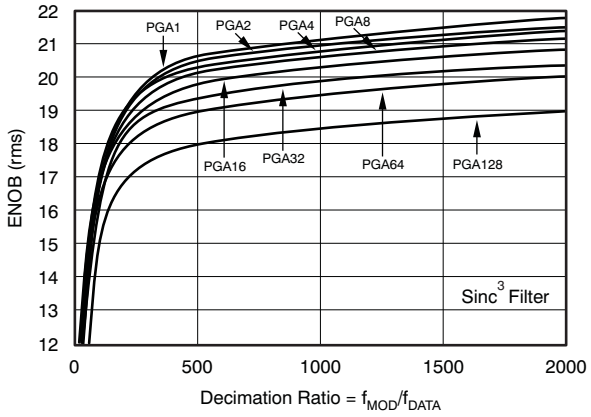


Figure 1.

EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO

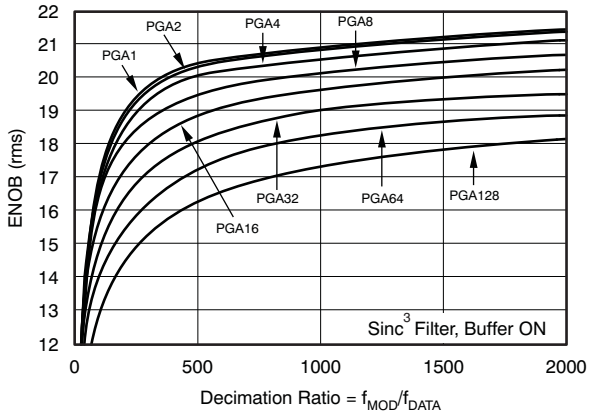


Figure 2.

EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO

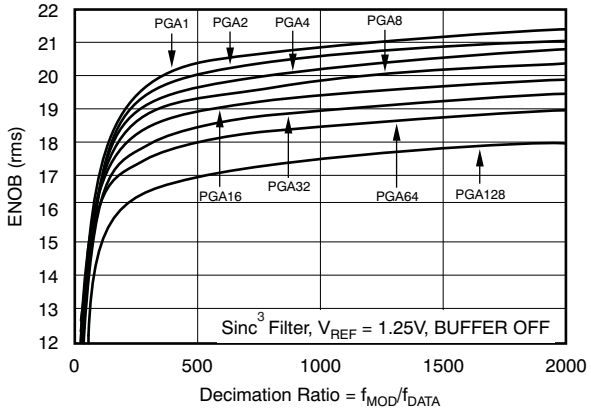


Figure 3.

EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO

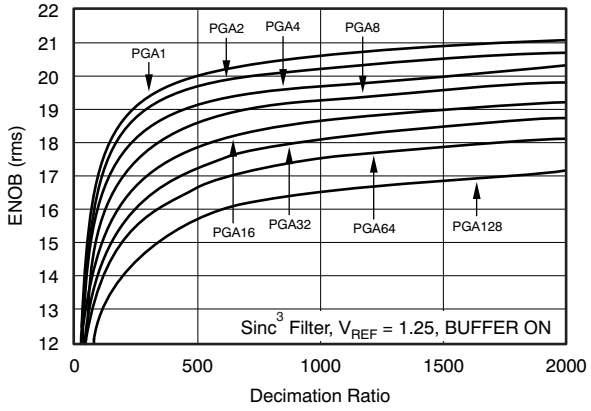


Figure 4.

EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO

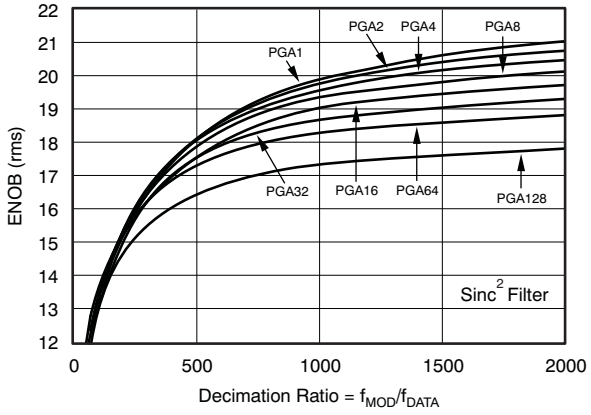


Figure 5.

FAST-SETTLING FILTER EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO

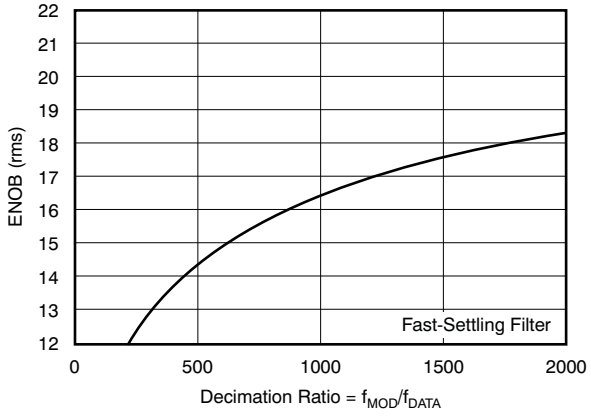


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, and V_{REF} = +2.5V, unless otherwise specified.

NOISE vs INPUT SIGNAL

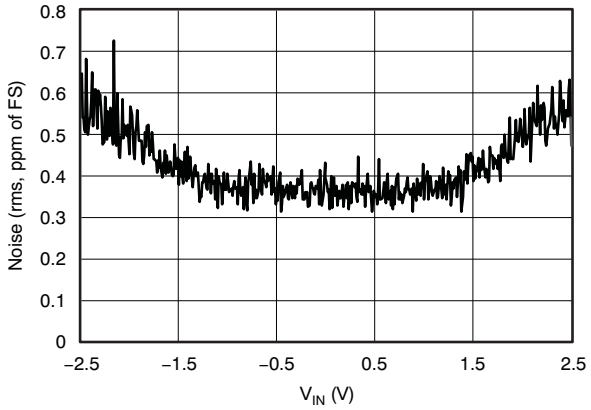


Figure 7.

CMRR vs FREQUENCY

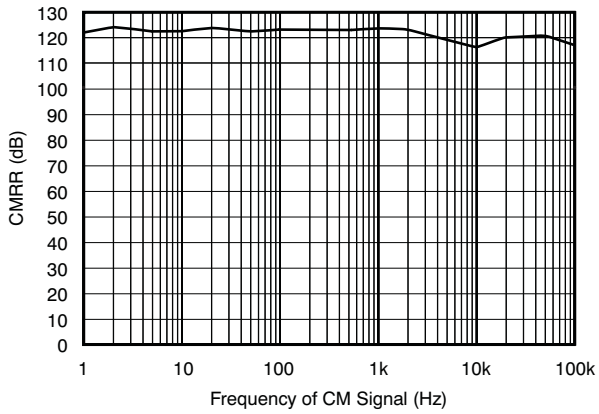


Figure 8.

PSRR vs FREQUENCY

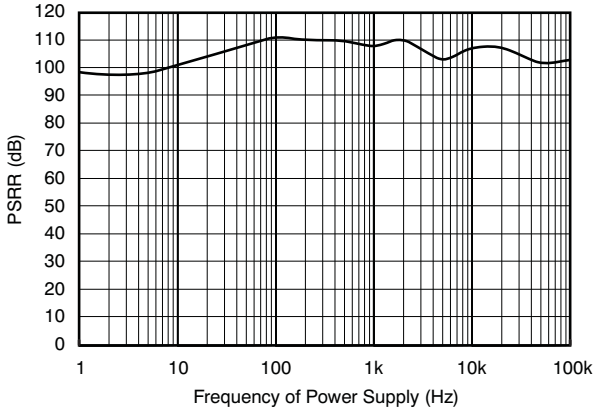


Figure 9.

OFFSET vs TEMPERATURE

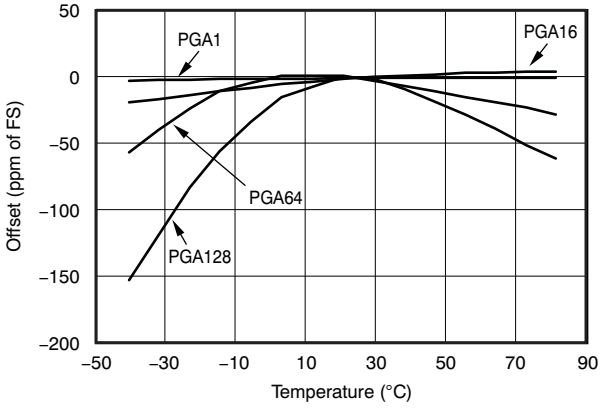


Figure 10.

GAIN vs TEMPERATURE

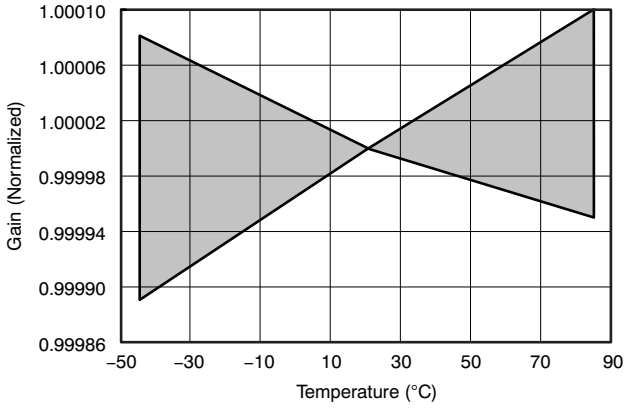


Figure 11.

INTEGRAL NONLINEARITY vs INPUT SIGNAL

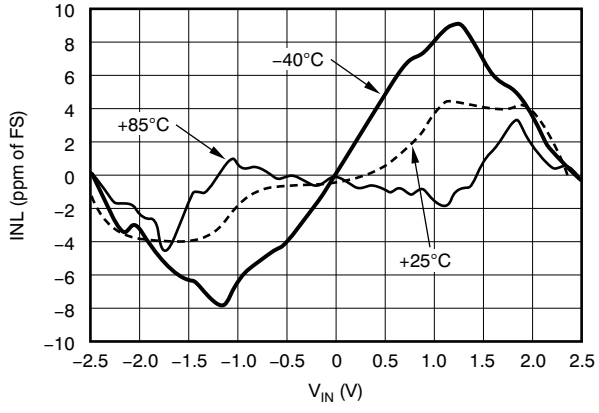


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, and V_{REF} = +2.5V, unless otherwise specified.

CURRENT vs TEMPERATURE

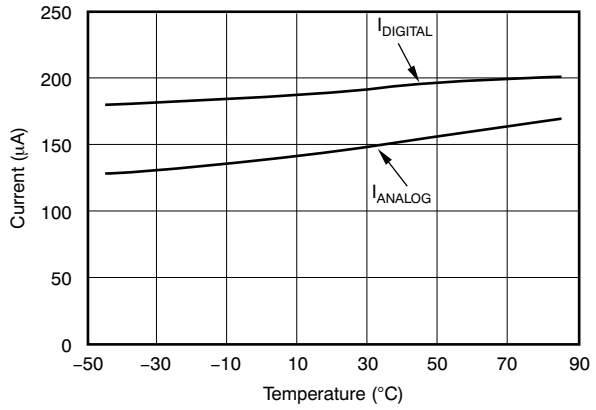


Figure 13.

ADC CURRENT vs PGA

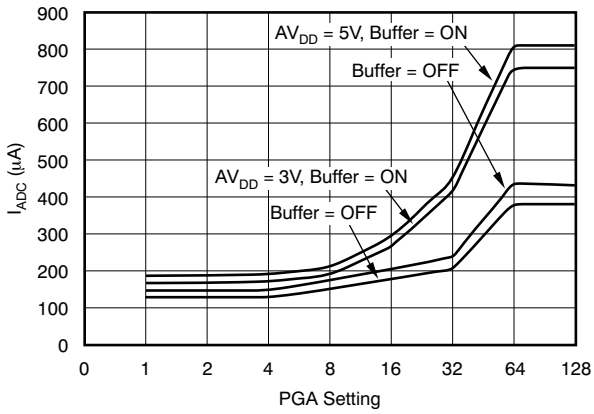


Figure 14.

DIGITAL CURRENT

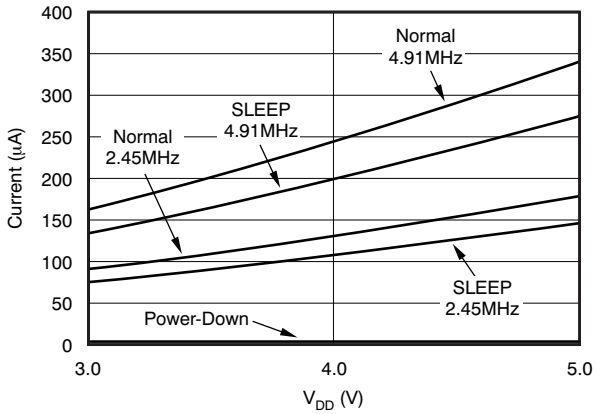


Figure 15.

HISTOGRAM OF OUTPUT DATA

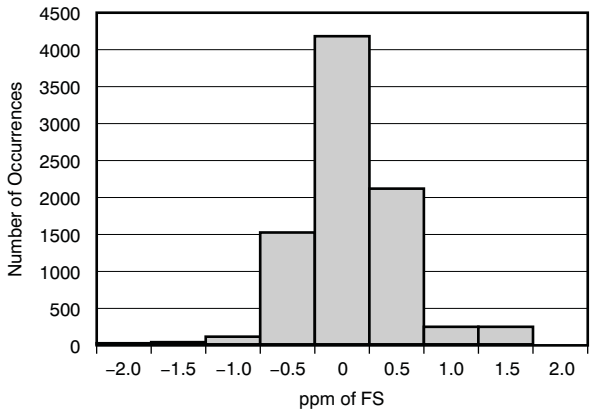


Figure 16.

V_{REFOUT} vs LOAD CURRENT

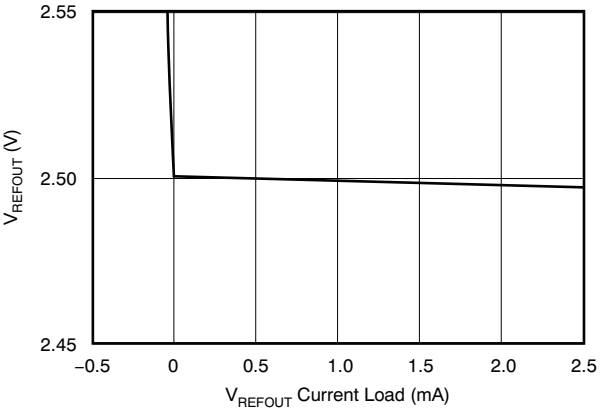


Figure 17.

OFFSET DAC – OFFSET vs TEMPERATURE

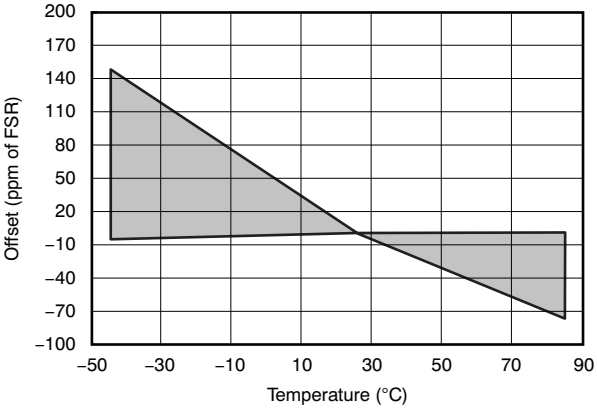


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, and V_{REF} = +2.5V, unless otherwise specified.

OFFSET DAC – GAIN vs TEMPERATURE

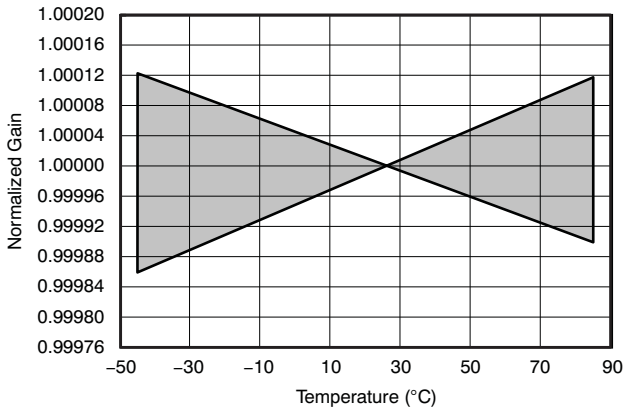


Figure 19.

IDAC R_{OUT} vs V_{OUT}

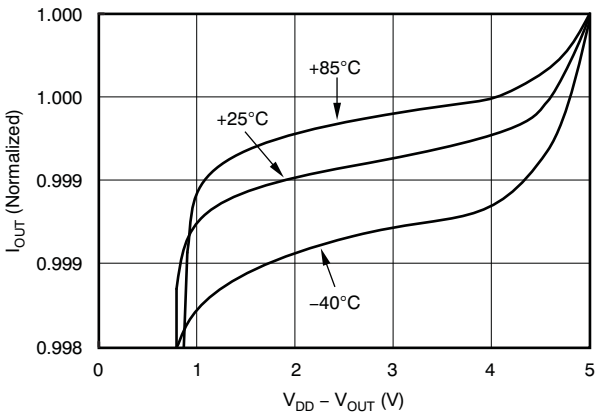


Figure 20.

IDAC NORMALIZED vs TEMPERATURE

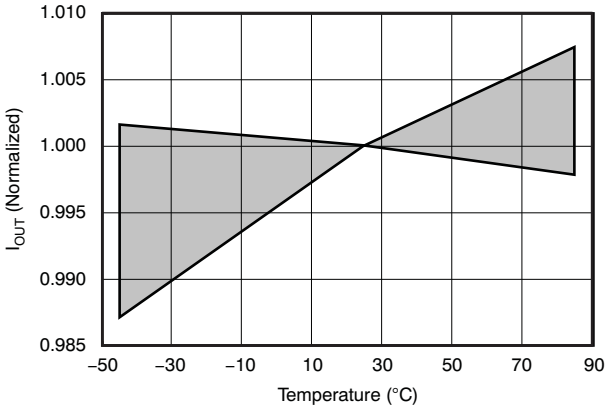


Figure 21.

IDAC MATCHING vs TEMPERATURE

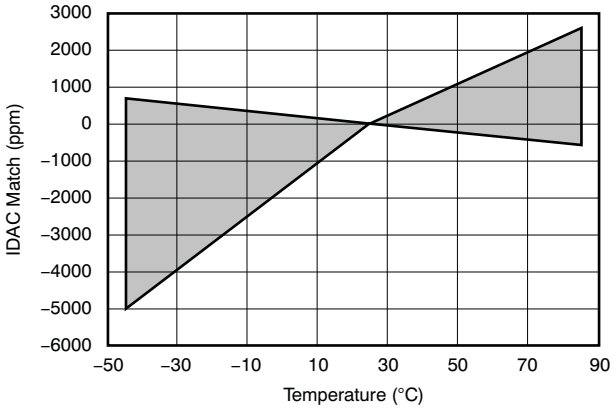


Figure 22.

IDAC DIFFERENTIAL NONLINEARITY
(Range = 1, R_{DAC} = 150kΩ, V_{REF} = 2.5V)

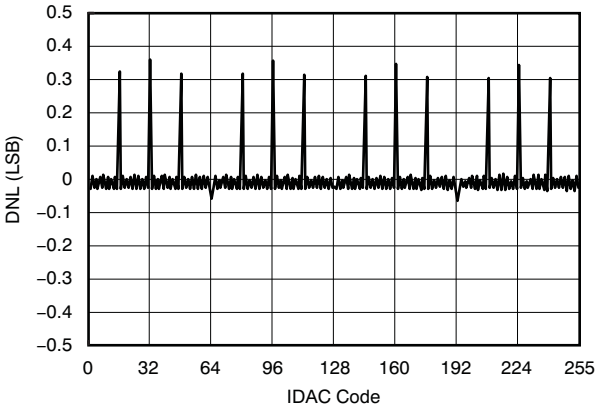


Figure 23.

IDAC INTEGRAL NONLINEARITY
(Range = 1, R_{DAC} = 150kΩ, V_{REF} = 2.5V)

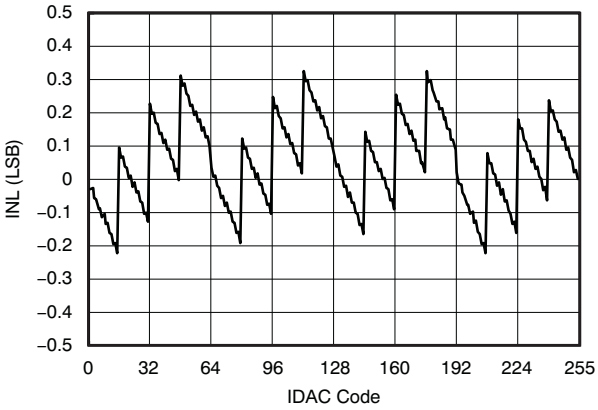


Figure 24.

OVERVIEW

INPUT MULTIPLEXER

The input multiplexer provides for any combination of differential inputs to be selected on any of the input channels, as shown in Figure 25. If channel 1 is selected as the positive differential input channel, any other channel can be selected as the negative differential input channel. With this method, it is possible to have up to eight fully-differential input channels.

In addition, current sources are supplied that will source or sink current to detect open or short circuits on the pins.

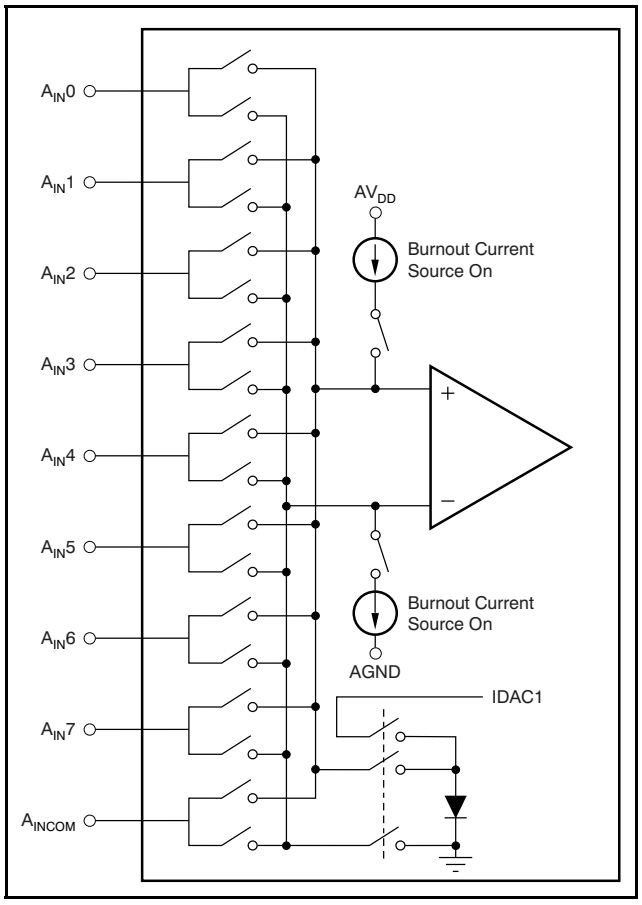


Figure 25. Input Multiplexer Configuration

TEMPERATURE SENSOR

An on-chip diode provides temperature sensing capability. When the configuration register for the input MUX is set to all 1s, the diode is connected to the input of the A/D converter. All other channels are open. The anode of the diode is connected to the positive input of the A/D converter, and the cathode of the diode is connected to the negative input of the A/D converter. The output of IDAC1 is connected to the anode to bias the diode and the cathode of the diode is also connected to ground to complete the circuit.

In this mode, the output of IDAC1 is also connected to the output pin, so some current may flow into an external load from IDAC1, rather than the diode. See Application Report *Measuring Temperature with the ADS1216, ADS1217, or ADS1216* (SBAA073), available for download at www.ti.com, for more information.

BURNOUT CURRENT SOURCES

When the Burnout bit is set in the ACR Configuration Register (see the Register Map section), two current sources are enabled. The current source on the positive input channel sources approximately 2µA of current. The current source on the negative input channel sinks approximately 2µA. This sinking allows for the detection of an open circuit (full-scale reading) or short circuit (0V differential reading) on the selected input differential pair.

INPUT BUFFER

The input impedance of the ADS1216 without the buffer is 5MΩ/PGA. With the buffer enabled, the input voltage range is reduced and the analog power-supply current is higher. The buffer is controlled by ANDing the state of the buffer pin with the state of the BUFFER bit in the ACR Register (see the Register Map section). See Application Report *Input Currents for High-Resolution ADCs* (SBAA080), available for download at www.ti.com, for more information.

IDAC1 AND IDAC2

The ADS1216 has two 8-bit current output DACs that can be controlled independently. The output current is set with R_{DAC}, the range select bits in the ACR register, and the 8-bit digital value in the IDAC register. The output current equals $V_{REF}/(8 \times R_{DAC})(2^{RANGE - 1})$(DAC CODE). With V_{REFOUT} = 2.5V and R_{DAC} = 150kΩ, the full-scale output can be selected to be 0.5, 1, or 2mA. The compliance voltage range is 0 to within 1V of AV_{DD}. When the internal voltage reference of the ADS1216 is used, it is the reference for the IDAC. An external reference may be used for the IDACs by disabling the internal reference and tying the external reference input to the V_{REFOUT} pin.

PROGRAMMABLE GAIN AMPLIFIER (PGA)

The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can improve the effective resolution of the A/D converter. For instance, with a PGA of 1 on a 5V full-scale range, the A/D converter can resolve to 1µV. With a PGA of 128 on a 40mV full-scale range, the A/D converter can resolve to 75nV.

PGA OFFSET DAC

The input to the PGA can be shifted by half the full-scale input range of the PGA by using the ODAC (Offset DAC) Register; see the Register Map section. The ODAC register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset. Using the ODAC does not reduce the performance of the A/D converter. See Application Report *The Offset DAC* (SBAA077), available for download at www.ti.com, for more information.

MODULATOR

The modulator is a single-loop, second-order system. The modulator runs at a clock speed (f_{MOD}) that is derived from the external clock (f_{OSC}), as shown in Table 1. The frequency division is determined by the SPEED bit in the Setup Register (see the Register Map section).

Table 1. Modulator Speed

SPEED BIT	f_{MOD}
0	$f_{OSC}/128$
1	$f_{OSC}/256$

VOLTAGE REFERENCE INPUT

The ADS1216 uses a differential voltage reference input. The input signal is measured against the differential voltage $V_{REF} \equiv (V_{REF+}) - (V_{REF-})$. For AV_{DD} = +5V, V_{REF} is typically +2.5V. For AV_{DD} = +3V, V_{REF} is typically +1.25V. As a result of the sampling nature of the modulator, the reference input current increases with higher modulator clock frequency (f_{MOD}) and higher PGA settings.

ON-CHIP VOLTAGE REFERENCE

A selectable voltage reference (1.25V or 2.5V) is available for supplying the voltage reference input. To use, connect V_{REF-} to AGND and V_{REF+} to V_{REFOUT}. The enabling and voltage selection are controlled through bits REF EN and REF HI in the Setup Register (see the Register Map section). The 2.5V reference requires AV_{DD} = +5V. When using the on-chip voltage reference, the V_{REFOUT} pin should be bypassed with a 0.1µF capacitor to AGND.

V_{RCAP} PIN

This pin provides a bypass cap for noise filtering on internal V_{REF} circuitry only. This pin is a sensitive pin; therefore place the capacitor as close as possible and avoid any resistive loading. The recommended capacitor is a 1000pF ceramic cap. If an external V_{REF} is used, this pin can be left unconnected.

CLOCK GENERATOR

The clock source for the ADS1216 can be provided from a crystal, oscillator, or external clock. When the clock source is a crystal, external capacitors must be provided to ensure startup and a stable clock frequency; this configuration is shown in Figure 26 and Table 2.

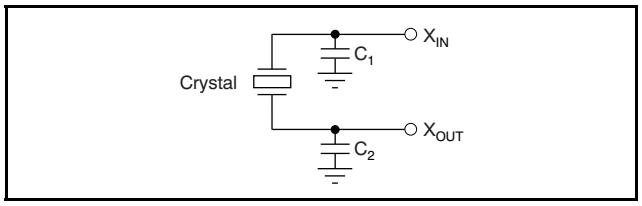


Figure 26. Crystal Connection

Table 2. Typical Clock Sources

CLOCK SOURCE	FREQUENCY	C_1	C_2	PART NUMBER
Crystal	2.4576	0–20pF	0–20pF	ECS, ECSD 2.45 – 32
Crystal	4.9152	0–20pF	0–20pF	ECS, ECSL 4.91
Crystal	4.9152	0–20pF	0–20pF	ECS, ECSD 4.91
Crystal	4.9152	0–20pF	0–20pF	CTS, MP 042 4M9182

CALIBRATION

The offset and gain errors in the ADS1216, or the complete system, can be reduced with calibration. Internal calibration of the ADS1216 is called self-calibration. Self-calibration is handled with three commands. One command does both offset and gain calibration. There is also a gain calibration command and an offset calibration command. Each calibration process takes seven t_{DATA} periods to complete. It takes 14 t_{DATA} periods to complete both an offset and gain calibration. Self-gain calibration is optimized for PGA gains less than 8. When using higher gains, system gain calibration is recommended.

For system calibration, the appropriate signal must be applied to the inputs. The system offset command requires a zero differential input signal. It then computes an offset that will nullify offset in the system. The system gain command requires a positive full-scale differential input signal. It then computes a value to nullify gain errors in the system. Each of these calibrations will take seven t_{DATA} periods to complete.

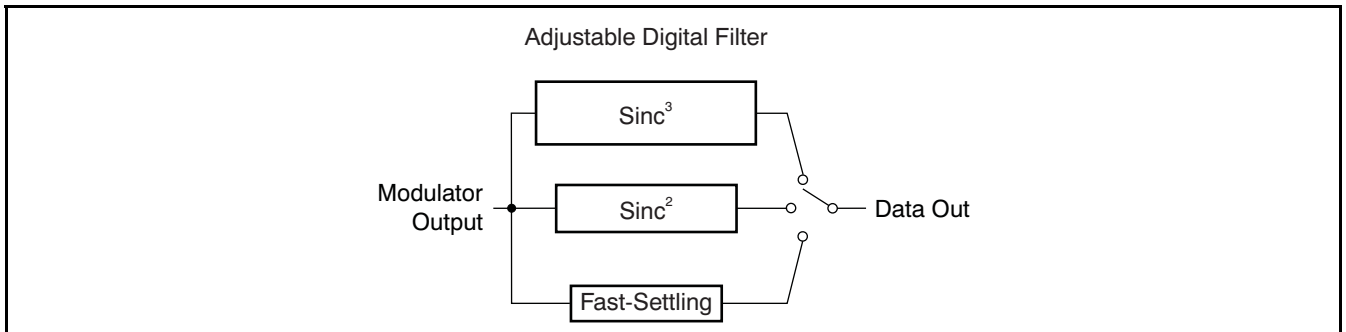
Calibration must be performed after power on, a change in decimation ratio, or a change of the PGA. For operation with a reference voltage greater than (AV_{DD} – 1.5V), the buffer must also be turned off during calibration.

At the completion of calibration, the $\overline{DRDY}$ signal goes low, which indicates the calibration is finished and valid data is available. See Application Report *Calibration Routine and Register Value Generation for the ADS121x Series* (SBAA099), available for download at www.ti.com, for more information.

DIGITAL FILTER

The Digital Filter can use either the Fast-Settling, $Sinc^2$, or $Sinc^3$ filter, as shown in Figure 27. In addition, the Auto mode changes the sinc filter after the input channel or PGA is changed. When switching to a new channel, it will use the Fast-Settling filter for the next two conversions, the first of which should be discarded. It will then use the $Sinc^2$ followed by the $Sinc^3$ filter. This architecture combines the low-noise advantage of the $Sinc^3$ filter with the quick response of the Fast-Settling time filter. See Figure 28 for the frequency response of each filter.

When using the Fast-Settling filter, select a decimation value set by the DEC0 and M/DEC1 registers that is evenly divisible by four for the best gain accuracy. For example, choose 260 rather than 261.



FILTER SETTLING TIME

FILTER	SETTLING TIME (Conversion Cycles)
$Sinc^3$	3(1)
$Sinc^2$	2(1)
Fast	1(1)

NOTE: (1) With Synchronized Channel Changes.

AUTO MODE FILTER SELECTION

CONVERSION CYCLE			
1	2	3	4
Discard	Fast	$Sinc^2$	$Sinc^3$

Figure 27. Filter Step Responses

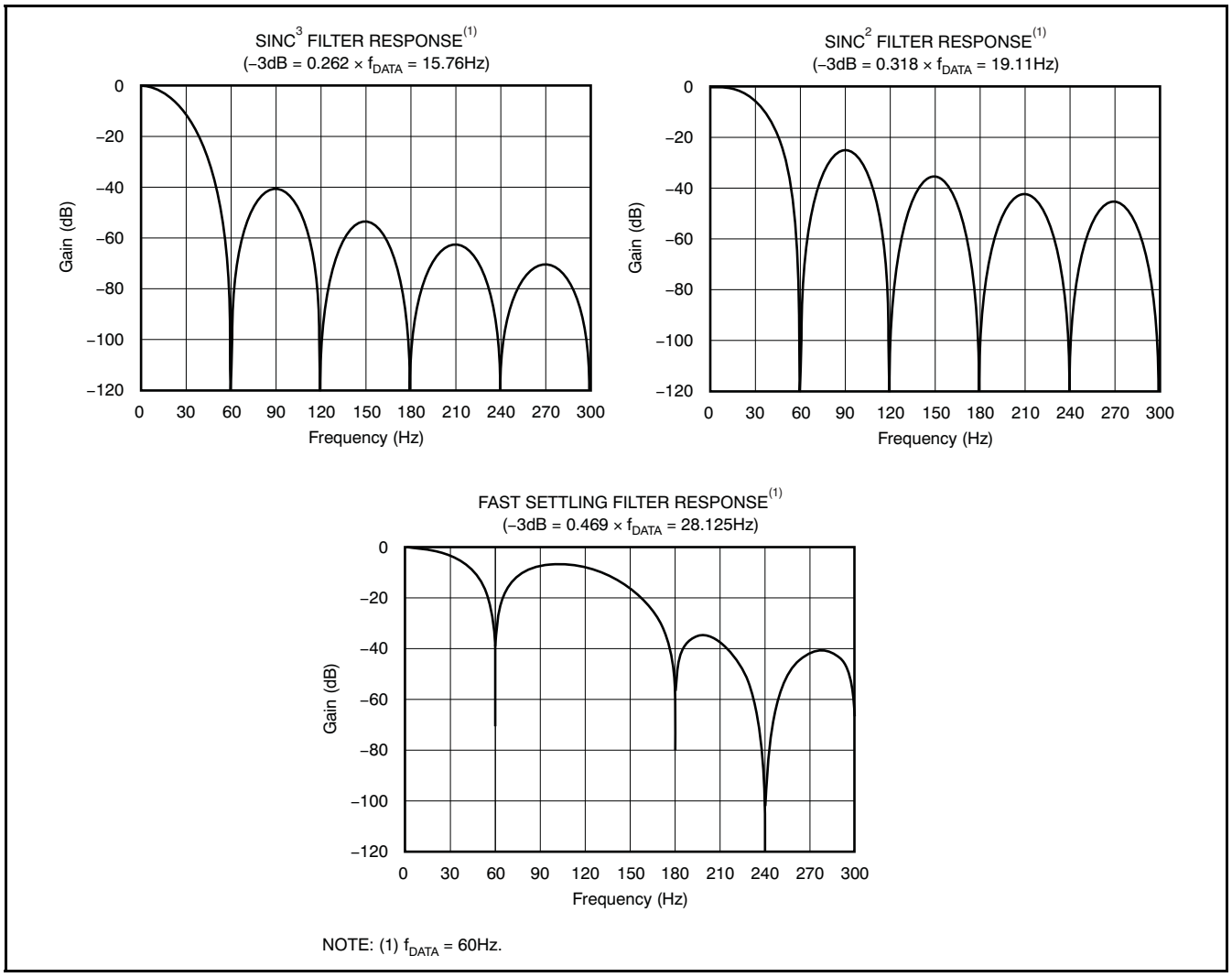


Figure 28. Filter Frequency Responses

DIGITAL I/O INTERFACE

The ADS1216 has eight pins dedicated for digital I/O. The default power-up condition for the digital I/O pins are as inputs. All of the digital I/O pins are individually configurable as inputs or outputs. They are configured through the DIR control register. The DIR register defines whether the pin is an input or output, and the DIO register defines the state of the digital output. When the digital I/O are configured as inputs, DIO is used to read the state of the pin. If the digital I/O are not used, either 1) configure as outputs; or 2) leave as inputs and tie to ground; this configuration prevents excess power dissipation.

SERIAL PERIPHERAL INTERFACE (SPI)

The SPI allows a controller to communicate synchronously with the ADS1216. The ADS1216 operates in slave-only mode.

Chip Select ($\overline{CS}$)

The chip select ($\overline{CS}$) input of the ADS1216 must be externally asserted before a master device can exchange data with the ADS1216. $\overline{CS}$ must be low for the duration of the transaction. $\overline{CS}$ can be tied low.

Serial Clock (SCLK)

SCLK, a Schmitt-Trigger input, clocks data transfer on the D_{IN} input and D_{OUT} output. When transferring data to or from the ADS1216, multiple bits of data may be transferred back-to-back with no delay in SCLKs or toggling of $\overline{CS}$. Make sure to avoid glitches on SCLK because they can cause extra shifting of the data.

Polarity (POL)

The serial clock polarity is specified by the POL input. When SCLK is active high, set POL high. When SCLK is active low, set POL low.

DATA READY

The $\overline{\text{DRDY}}$ output is used as a status signal to indicate when data is ready to be read from the ADS1216. $\overline{\text{DRDY}}$ goes low when new data is available. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated.

$\overline{\text{DSYNC}}$ OPERATION

$\overline{\text{DSYNC}}$ is used to provide for synchronization of the A/D conversion with an external event. Synchronization can be achieved either through the $\overline{\text{DSYNC}}$ pin or the DSYNC command. When the $\overline{\text{DSYNC}}$ pin is used, the filter counter is reset on the falling edge of $\overline{\text{DSYNC}}$. The modulator is held in reset until $\overline{\text{DSYNC}}$ is taken high. Synchronization occurs on the next rising edge of the system clock after $\overline{\text{DSYNC}}$ is taken high.

MEMORY

Two types of memory are used on the ADS1216: registers and RAM. 16 registers directly control the various functions (PGA, DAC value, Decimation Ratio, etc.) and can be directly read or written to. Collectively, the registers contain all the information needed to configure the part, such as data format, mux settings, calibration settings, decimation ratio, etc. Additional registers, such as conversion data, are accessed through dedicated instructions.

REGISTER BANK

The operation of the device is set up through individual registers. The set of the 16 registers required to configure the device is referred to as a Register Bank, as shown in Figure 29.

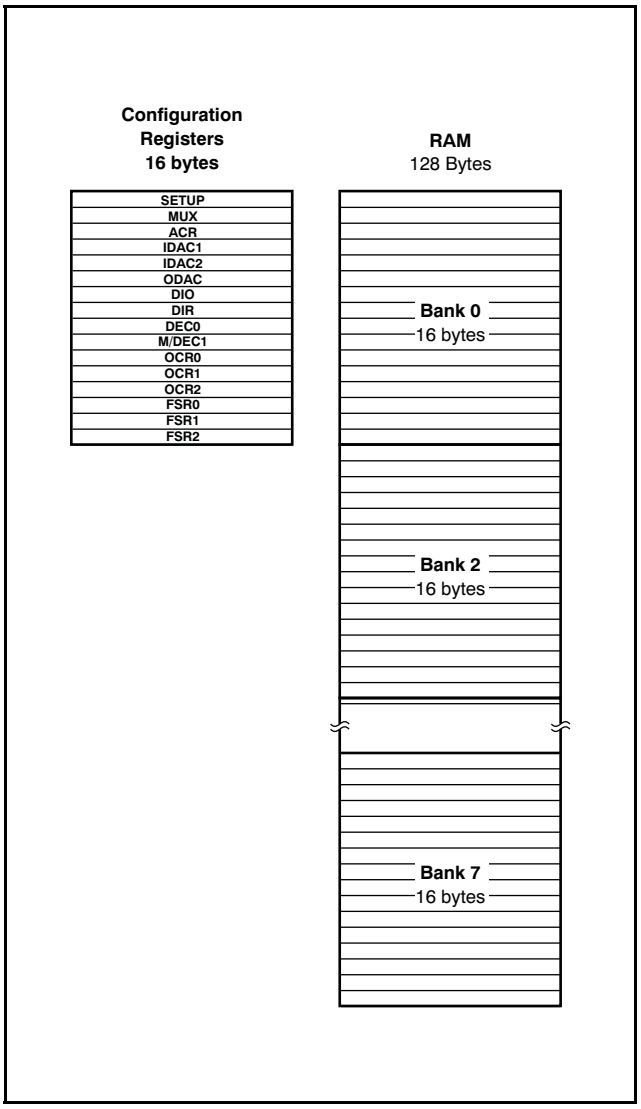


Figure 29. Memory Organization

RAM

Reads and Writes to Registers and RAM occur on a byte basis. However, copies between registers and RAM occur on a bank basis. The RAM is independent of the Registers; for example, the RAM can be used as general-purpose RAM.

The ADS1216 supports any combination of eight analog inputs. With this flexibility, the device can easily support eight unique configurations—one per input channel. In order to facilitate this type of usage, eight separate register banks are available. Therefore, each configuration could be written once and recalled as needed without having to serially retransmit all the configuration data. Checksum commands are also included, which can be used to verify the integrity of RAM.

The RAM provides eight *banks*, with a bank consisting of 16 bytes. The total size of the RAM is 128 bytes. Copies between the registers and RAM are performed on a bank basis. Also, the RAM can be directly read or written through the serial interface on power-up. The banks allow separate storage of settings for each input.

The RAM address space is linear; therefore, accessing RAM is done using an auto-incrementing pointer. Access to RAM in the entire memory map can be done consecutively without having to address each bank individually. For example, if you were currently accessing bank 0 at offset 0xF (the last location of bank 0), the next access would be bank 1 and offset 0x0. Any access after bank 7 and offset 0xF will wrap around to bank 0 and Offset 0x0.

Although the Register Bank memory is linear, the concept of addressing the device can also be thought of in terms of bank and offset addressing. Looking at linear and bank addressing syntax, we have the following comparison: in the linear memory map, the address 0x14 is equivalent to bank 1 and offset 0x4. Simply stated, the most significant four bits represent the bank, and the least significant four bits represent the offset. The offset is equivalent to the register address for that bank of memory.

REGISTER MAP

Table 3. Registers

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	**SETUP**	ID	ID	ID	SPEED	REF EN	REF HI	BUF EN	BIT ORDER
01h	**MUX**	PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0
02h	**ACR**	BOCS	IDAC2R1	IDAC2R0	IDAC1R1	IDAC1R0	PGA2	PGA1	PGA0
03h	**IDAC1**	IDAC1_7	IDAC1_6	IDAC1_5	IDAC1_4	IDAC1_3	IDAC1_2	IDAC1_1	IDAC1_0
04h	**IDAC2**	IDAC2_7	IDAC2_6	IDAC2_5	IDAC2_4	IDAC2_3	IDAC2_2	IDAC2_1	IDAC2_0
05h	**ODAC**	SIGN	OSET_6	OSET_5	OSET_4	OSET_3	OSET_2	OSET_1	OSET_0
06h	**DIO**	DIO_7	DIO_6	DIO_5	DIO_4	DIO_3	DIO_2	DIO_1	DIO_0
07h	**DIR**	DIR_7	DIR_6	DIR_5	DIR_4	DIR_3	DIR_2	DIR_1	DIR_0
08h	**DEC0**	DEC07	DEC06	DEC05	DEC04	DEC03	DEC02	DEC01	DEC00
09h	**M/DEC1**	$\overline{\text{DRDY}}$	U/$\overline{\text{B}}$	SMODE1	SMODE0	Reserved	DEC10	DEC9	DEC8
0Ah	**OCR0**	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
0Bh	**OCR1**	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
0Ch	**OCR2**	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
0Dh	**FSR0**	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
0Eh	**FSR1**	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
0Fh	**FSR2**	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

DETAILED REGISTER DEFINITIONS

SETUP (Address 00h) Setup Register

Reset value = iii01110.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ID	ID	ID	SPEED	REF EN	REF HI	BUF EN	BIT ORDER

bits 7-5 Factory programmed bits

bit 4 SPEED: modulator clock speed

0 : $f_{MOD} = f_{OSC}/128$
1 : $f_{MOD} = f_{OSC}/256$

bit 3 REF EN: Internal voltage reference enable
0 = Internal voltage reference disabled
1 = Internal voltage reference enabled

bit 2 REF HI: internal reference voltage select
0 = Internal reference voltage = 1.25V
1 = Internal reference voltage = 2.5V

bit 1 BUF EN: buffer enable
0 = Buffer disabled
1 = Buffer enabled

bit 0 BIT ORDER: set order bits are transmitted
0 = Most significant bit transmitted first
1 = Least significant bit transmitted first data is always shifted into the part most significant bit first. Data is always shifted out of the part most significant byte first. This configuration bit only controls the bit order within the byte of data that is shifted out.

MUX (Address 01h) Multiplexer Control Register

Reset value = 01h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0

bits 7-4 PSEL3: PSEL2: PSEL1: PSEL0: Positive channel select

0000 = $A_{IN}0$
0001 = $A_{IN}1$
0010 = $A_{IN}2$
0011 = $A_{IN}3$
0100 = $A_{IN}4$
0101 = $A_{IN}5$
0110 = $A_{IN}6$
0111 = $A_{IN}7$

1xxx = A_{INCOM} (except when all bits are 1s)
1111 = Temperature sensor diode

bits 3-0 NSEL3: NSEL2: NSEL1: NSEL0: Negative channel select

0000 = $A_{IN}0$
0001 = $A_{IN}1$
0010 = $A_{IN}2$
0011 = $A_{IN}3$
0100 = $A_{IN}4$
0101 = $A_{IN}5$
0110 = $A_{IN}6$
0111 = $A_{IN}7$

1xxx = A_{INCOM} (except when all bits are 1s)
1111 = Temperature sensor diode

ACR (Address 02h) Analog Control Register

Reset value = 00h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BOCS	IDAC2R1	IDAC2R0	IDAC1R1	IDAC1R0	PGA2	PGA1	PGA0

bit 7 BOCS: Burnout current source
0 = Disabled
1 = Enabled

$$\text{IDAC Current} = \left(\frac{V_{REF}}{8R_{DAC}}\right)\left(2^{RANGE-1}\right)(\text{DAC CODE})$$

bits 6-5 IDAC2R1: IDAC2R0: Full-scale range select for IDAC2

00 = Off
01 = Range 1
10 = Range 2
11 = Range 3

bits 4-3 IDAC1R1: IDAC1R0: Full-scale range select for IDAC1

00 = Off
01 = Range 1
10 = Range 2
11 = Range 3

bits 2-0 PGA2: PGA1: PGA0: Programmable gain amplifier gain selection

000 = 1
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

IDAC1 (Address 03h) Current DAC 1

Reset value = 00h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IDAC1_7	IDAC1_6	IDAC1_5	IDAC1_4	IDAC1_3	IDAC1_2	IDAC1_1	IDAC1_0

The DAC code bits set the output of DAC1 from 0 to full-scale. The value of the full-scale current is set by this byte, V_{REF}, R_{DAC}, and the DAC1 range bits in the ACR register.

IDAC2 (Address 04h) Current DAC 2

Reset value = 00h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IDAC2_7	IDAC2_6	IDAC2_5	IDAC2_4	IDAC2_3	IDAC2_2	IDAC2_1	IDAC2_0

The DAC code bits set the output of DAC2 from 0 to full-scale. The value of the full-scale current is set by this byte, V_{REF}, R_{DAC}, and the DAC2 range bits in the ACR register.

ODAC (Address 05h) Offset DAC Setting

Reset value = 00h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0

bit 7 Offset sign

0 = Positive
1 = Negative

bits 6-0

$$\text{Offset} = \frac{V_{REF}}{2\text{PGA}} \times \left(\frac{\text{Code}}{127}\right)$$

NOTE: The offset must be used after calibration or the calibration will nullify the effects.

DIO (Address 06h) Digital I/O

Reset value = 00h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

A value written to this register will appear on the digital I/O pins if the pin is configured as an output in the DIR register. Reading this register will return the value of the digital I/O pins.

DIR (Address 07h) Direction control for digital I/O

Reset value = FFh.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0

Each bit controls whether the Digital I/O pin is an output (= 0) or input (= 1). The default power-up state is as inputs.

DEC0 (Address 08h) Decimation Register (least significant 8 bits)

Reset value = 80h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DEC07	DEC06	DEC05	DEC04	DEC03	DEC02	DEC01	DEC00

The decimation value is defined with 11 bits for a range of 20 to 2047. This register is the least significant eight bits. The three most significant bits are contained in the M/DEC1 register.

M/DEC1 (Address 09h) Mode and Decimation Register

Reset value = 07h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$\overline{\text{DRDY}}$	U/$\overline{\text{B}}$	SMODE1	SMODE0	Reserved	DEC10	DEC09	DEC08

bit 7 $\overline{\text{DRDY}}$: Data ready (read-only)
This bit duplicates the state of the $\overline{\text{DRDY}}$ pin.

bit 6 U/$\overline{\text{B}}$: Data format
0 = Bipolar
1 = Unipolar

U/$\overline{\text{B}}$	ANALOG INPUT	DIGITAL OUTPUT
0	+FS Zero –FS	0x7FFFFF 0x000000 0x800000
1	+FS Zero –FS	0xFFFFFF 0x000000 0x000000

bits 5-4 SMODE1: SMODE0: Settling mode

00 = Auto
01 = Fast-Settling filter
10 = $Sinc^2$ filter
11 = $Sinc^3$ filter

bit 3 Reserved

This bit is not used in the ADS1216 and it is recommended that it be set to 0.

bits 2-0 DEC10: DEC09: DEC08: Most significant bits of the decimation value

OCR0 (Address 0Ah) Offset Calibration Coefficient (least significant byte)

Reset value = 00h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR1 (Address 0Bh) Offset Calibration Coefficient (middle byte)

Reset value = 00h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR2 (Address 0Ch) Offset Calibration Coefficient (most significant byte)

Reset value = 00h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

FSR0 (Address 0Dh) Full-Scale Register (least significant byte)

Reset value = 24h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR1 (Address 0Eh) Full-Scale Register (middle byte)

Reset value = 90h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

FSR2 (Address 0Fh) Full-Scale Register (most significant byte)

Reset value = 67h.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

COMMAND DEFINITIONS

The commands summarized in Table 4 control the operation of the ADS1216. All of the commands are stand-alone except for the register reads and writes (RREG, WREG) which require a second command byte plus data. Additional command and data bytes may be shifted in without delay after the first command byte. The ORDER bit in the STATUS register (see the Register map section) sets the order of the bits within the output data. $\overline{CS}$ must stay low during the entire command sequence.

Table 4. Command Definitions(1)

COMMAND	DESCRIPTION	1ST COMMAND BYTE	2ND COMMAND BYTE
WAKEUP	Completes SYNC and exits standby mode	0000 0000 (00h)	
RDATA	Read data	0000 0001 (01h)	
RDATAC	Read data continuously	0000 0011 (03h)	
SDATAC	Stop read data continuously	0000 1111 (0Fh)	
RREG	Read from REG *rrr*	0001 *rrrr* (1xh)	0000 *nnnn*
RRAM	Read from RAM bank *aaa*	0010 0*aaa* (2xh)	x*nnn nnnn* (number of bytes – 1)
CREG	Copy REG to RAM bank *aaa*	0100 0*aaa* (4xh)	
CREGA	Copy REG to all RAM banks	0100 1000 (48h)	
WREG	Write to REG *rrr*	0101 *rrrr* (5xh)	0000 *nnnn*
WRAM	Write to RAM bank *aaa*	0110 0*aaa* (6xh)	x*nnn nnnn* (number of bytes – 1)
CRAM	Copy RAM bank *aaa* to REG	1100 0*aaa* (Cxh)	
CSRAMX	Calculate RAM bank *aaa* checksum	1101 0*aaa* (Dxh)	
CSARAMX	Calculate all RAM banks checksum	1101 1000 (D8h)	
CSREG	Calculate REG checksum	1101 1111 (DFh)	
CSRAM	Calculate RAM bank *aaa* checksum	1110 0*aaa* (Exh)	
CSARAM	Calculate all RAM banks checksum	1110 1000 (E8h)	
SELFCAL	Offset and gain self-calibration	1111 0000 (F0h)	
SELFOCAL	Offset self-calibration	1111 0001 (F1h)	
SELFGCAL	Gain self-calibration	1111 0010 (F2h)	
SYSOCAL	System offset calibration	1111 0011 (F3h)	
SYSGCAL	System gain calibration	1111 0100 (F4h)	
DSYNC	Synchronize the A/D conversion	1111 1100 (FCh)	
SLEEP	Begin sleep mode	1111 1101 (FDh)	
RESET	Reset to power-up values	1111 1110 (FEh)	
WAKEUP	Completes SYNC and exits standby mode	1111 1111 (FFh)	

(1) n = number of registers to be read/written – 1. For example, to read/write three registers, set nnnn = 2 (0010). r = starting register address for read/write commands.

RDATA — Read Data

Description: Issue this command after $\overline{DRDY}$ goes low to read a single conversion result. After all 24 bits have been shifted out on D_{OUT}, $\overline{DRDY}$ goes high. It is not necessary to read back all 24 bits, but $\overline{DRDY}$ will then not return high until new data is being updated. See the Timing Characteristics for the required delay between the end of the RDATA command and the beginning of shifting data on D_{OUT}: t_6.

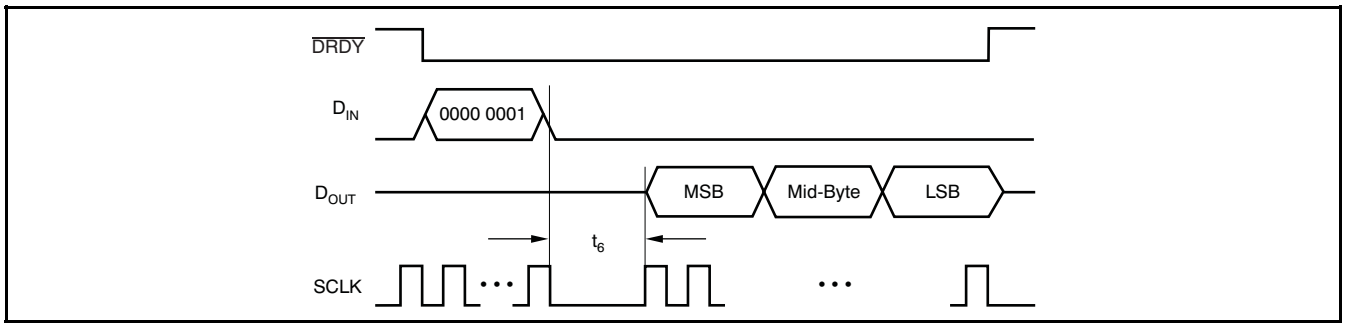


Figure 30. RDATA Command Sequence

RDATAC — Read Data Continuous

Description: Issue command after $\overline{DRDY}$ goes low to enter the Read Data Continuous mode. This mode enables the continuous output of new data on each $\overline{DRDY}$ without the need to issue subsequent read commands. After all 24 bits have been read, $\overline{DRDY}$ goes high. It is not necessary to read back all 24 bits, but $\overline{DRDY}$ will then not return high until new data is being updated. This mode may be terminated by the Stop Read Data Continuous command (STOPC). Because D_{IN} is constantly being monitored during the Read Data Continuous mode for the STOPC or RESET command, do not use this mode if D_{IN} and D_{OUT} are connected together. See the Timing Characteristics for the required delay between the end of the RDATAC command and the beginning of shifting data on D_{OUT}: t_6.

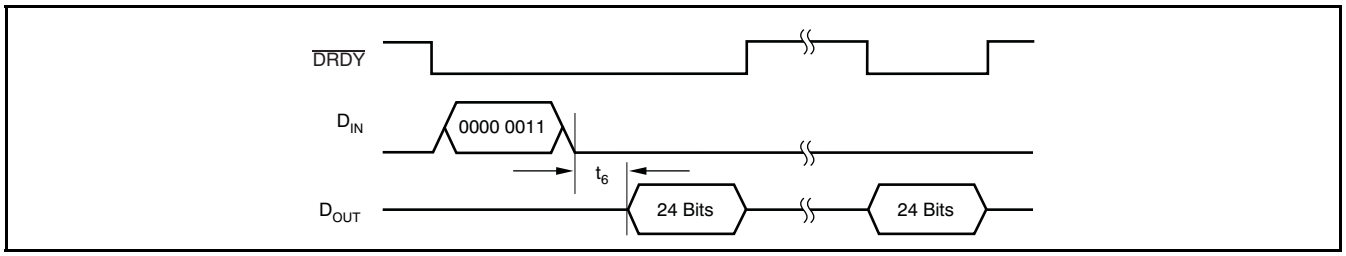


Figure 31. RDATAC Command Sequence

On the following $\overline{DRDY}$, shift out data by applying SCLKs. The Read Data Continuous mode terminates if input_data equals the STOPC or RESET command in any of the three bytes on D_{IN}.

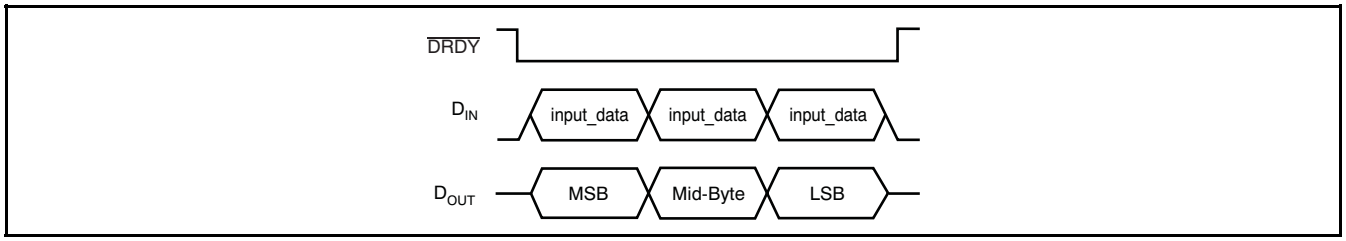


Figure 32. D_{IN} and D_{OUT} Command Sequence During Read Continuous mode

STOPC — Stop Read Data Continuous

Description: Ends the continuous data output mode; refer to RDATAC in the Command Definitions section. The command must be issued after $\overline{DRDY}$ goes low and completed before $\overline{DRDY}$ goes high.

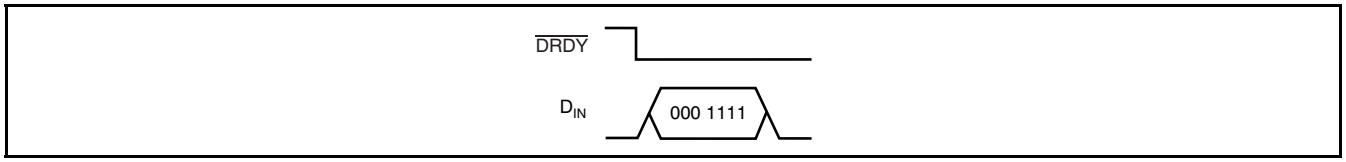


Figure 33. STOPC Command Sequence

RREG — Read from Registers

Description: Output the data from up to 16 registers starting with the register address specified as part of the command. The number of registers read will be one plus the second byte of the command. If the count exceeds the remaining registers, the addresses will wrap back to the beginning.

1st Command Byte: 0001 *rrrr* where *rrrr* is the address of the first register to read.

2nd Command Byte: 0000 *nnnn* where *nnnn* is the number of bytes to read – 1. See the Timing Characteristics for the required delay between the end of the RREG command and the beginning of shifting data on D_{OUT}: t_6.

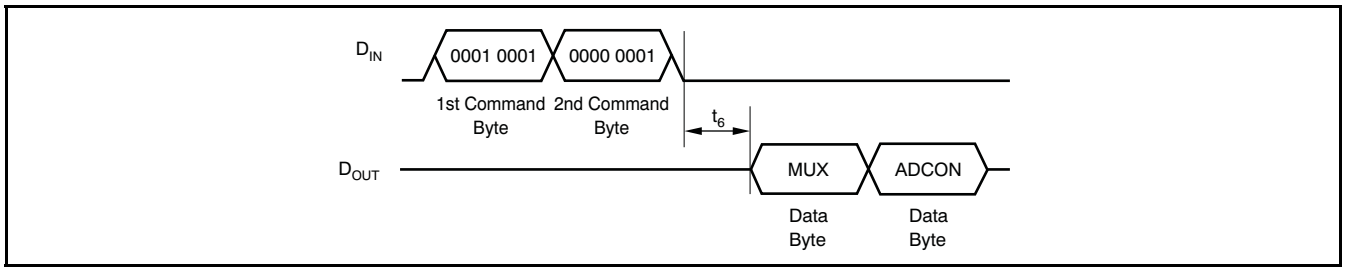


Figure 34. RREG Command Example: Read Two Registers Starting from Regiater 01h (multiplexer)

RRAM — Read from RAM

Description: This command allows for the direct reading of the RAM contents. All reads begin at the specified starting RAM bank. More than one bank can be read out in a single read operation. The reads will wrap around to the first bank if there is more data to be retrieved when the last bank is completely read. See the Timing Characteristics for the required delay between the end of the RRAM command and the beginning of shifting data on D_{OUT}: t_6.

1st Command Byte: 0010 0*aaa* where *aaa* is the starting RAM bank for the read.

2nd Command Byte: 0*nnn nnnn* where *nnn nnnn* is the number of bytes to be read – 1.

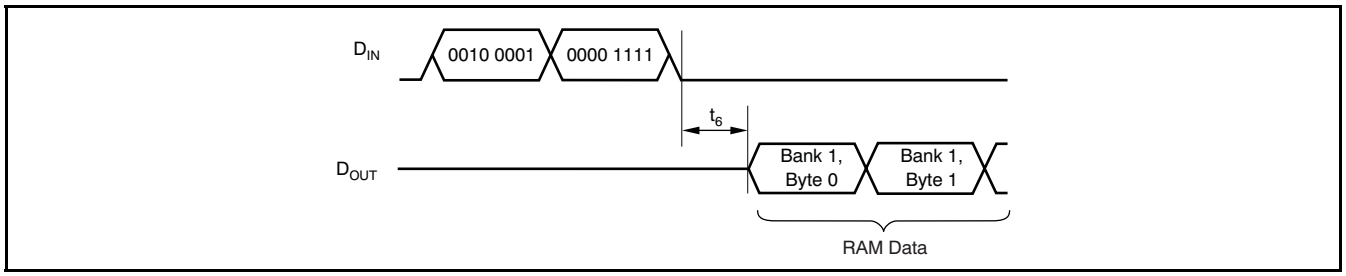


Figure 35. RRAM Command Example: Read 16 Bytes Starting from Bank 1

CREG **Copy Registers to RAM Bank**

Description: This command copies the registers to the selected RAM bank. Do not issue additional commands while the copy operation is underway.

1st Command byte: 0100 0*aaa* where *aaa* is the RAM bank that will be updated with a copy of the registers.

CREGA **Copy Registers to All RAM Banks**

Description: This command copies the registers to all RAM banks. Do not issue additional commands while the copy operation is underway.

WREG **Write to Register**

Description: Write to the registers starting with the register specified as part of the command. The number of registers that will be written is one plus the value of the second byte in the command.

1st Command Byte: 0101 *rrrr* where *rrrr* is the address to the first register to be written.

2nd Command Byte: 0000 *nnnn* where *nnnn* is the number of bytes to be written – 1.

Data Byte(s): data to be written to the registers.

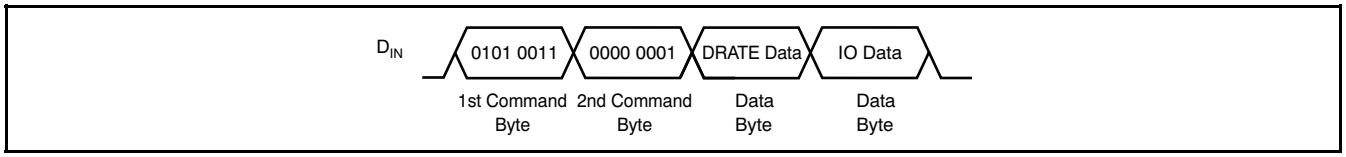


Figure 36. WREG Command Example: Write Two Registers Starting from 03h (DRATE)

WRAM **Write to RAM**

Description: This command allows for direct writing to the RAM. All writes begin at the specified starting RAM bank. More than one bank can be written in a single write operation. The writes will wrap around to the first bank if there is more data to be written when the last bank is completely written. See the Timing Characteristics for the required delay between the end of the RRAM command and the beginning of shifting data on D_{OUT}: t_6.

1st Command Byte: 0010 0*aaa* where *aaa* is the starting RAM bank for the write.

2nd Command Byte: 0*nnn nnnn* where *nnn nnnn* is the number of bytes to be written – 1.

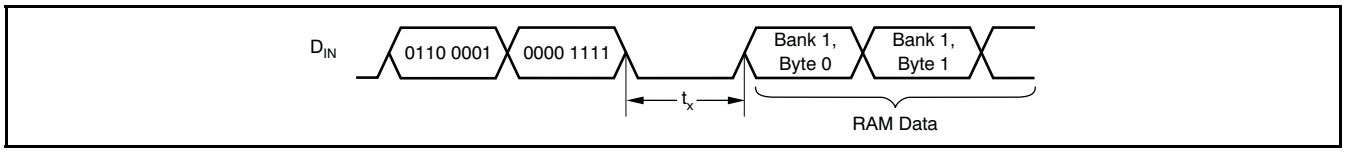


Figure 37. WRAM Command Example: Write 16 Bytes Starting at Bank 1

CRAM **Copy Selected RAM Bank to Registers**

Description: This command copies the selected RAM bank to the registers. This action will overwrite all previous register settings. Do not issue additional commands while this copy operation is underway.

1st Command Byte: 1100 0*aaa* where *aaa* is the selected RAM bank.

CSRAM — **Calculate Checksum for Selected RAM Bank**

Description: This command calculates the checksum for the selected RAM bank. The checksum is calculated as the sum of all the bytes in the registers with the carry ignored. Do not issue any additional commands while the checksum is being calculated.

CSRAMX — **Calculate Checksum for Selected RAM Bank, Ignoring Certain Bits**

Description: This command calculates the checksum of the selected RAM bank. The checksum is calculated as a sum of all the bytes in the RAM bank with the carry ignored. The ID, $\overline{DRDY}$, and DIO bits are masked and are not included in the checksum calculation. Do not issue any additional commands while the checksum is being calculated.

CSARAM — **Calculate Checksum for all RAM Banks**

Description: This command calculates the checksum for all RAM banks. The checksum is calculated as a sum of all the bytes in the RAM bank with the carry ignored. Do not issue any additional commands while the checksum is being calculated.

CSARAMX — **Calculate Checksum for all RAM Banks, Ignoring Certain Bits**

Description: This command calculates the checksum for all RAM banks. The checksum is calculated as a sum of all the bytes in the RAM bank with the carry ignored. The ID, $\overline{DRDY}$, and DIO bits are masked and are not included in the checksum calculation. Do not issue any additional commands while the checksum is being calculated.

CSREG — **Calculate Checksum for the Registers**

Description: This command calculates the checksum for the registers. The checksum is calculated as a sum of all the bytes in the registers with the carry ignored. The ID, $\overline{DRDY}$, and DIO bits are masked and are not included in the checksum calculation. Do not issue any additional commands while the checksum is being calculated.

See the Timing Characteristics for the required delay between the end of the checksum commands and the beginning of shifting data on D_{OUT}: t_6. Note that this time is dependent on the specific checksum command used.

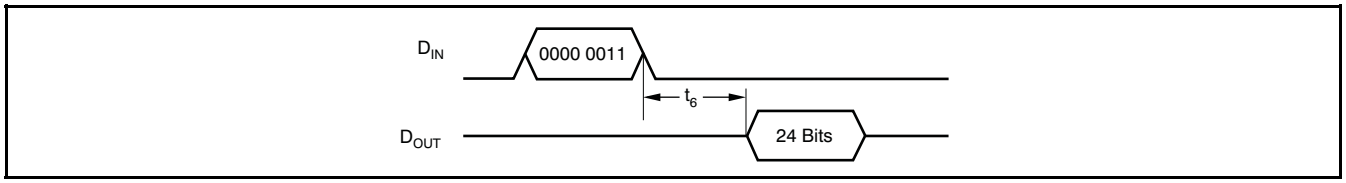


Figure 38. Checksum Command Sequence

SYSOCAL — **System Offset Calibration**

Description: Performs a system offset calibration. The Offset Calibration Register (OFC) is updated after this operation. $\overline{DRDY}$ goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until $\overline{DRDY}$ goes low indicating that the calibration is complete.

SYSGCAL — System Gain Calibration

Description: Performs a system gain calibration. The Full-Scale Calibration Register (FSC) is updated after this operation. $\overline{DRDY}$ goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until $\overline{DRDY}$ goes low indicating that the calibration is complete.

DSYNC — Synchronize the A/D Conversion

Description: This command synchronizes the A/D conversion. To use, first shift in the command. Then shift in the WAKEUP command. Synchronization occurs on the first CLKIN rising edge after the first SCLK used to shift in the WAKEUP command.

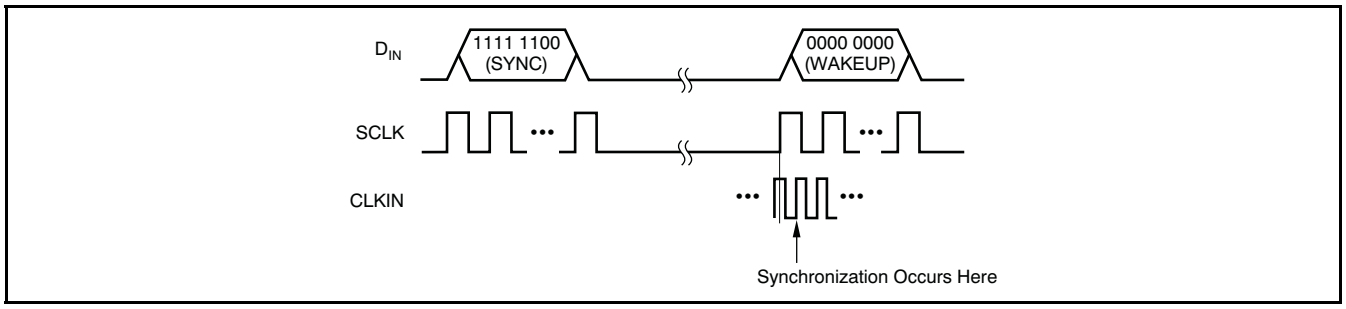


Figure 39. DSYNC Command Sequence

SLEEP — Sleep Mode

Description: This command puts the ADS1216 into a Sleep mode. After issuing the SLEEP command, make sure there is no more activity on SCLK while $\overline{CS}$ is low because this will interrupt Sleep mode. If $\overline{CS}$ is high, SCLK activity is allowed during Sleep mode. To exit Sleep mode, issue the WAKEUP command.

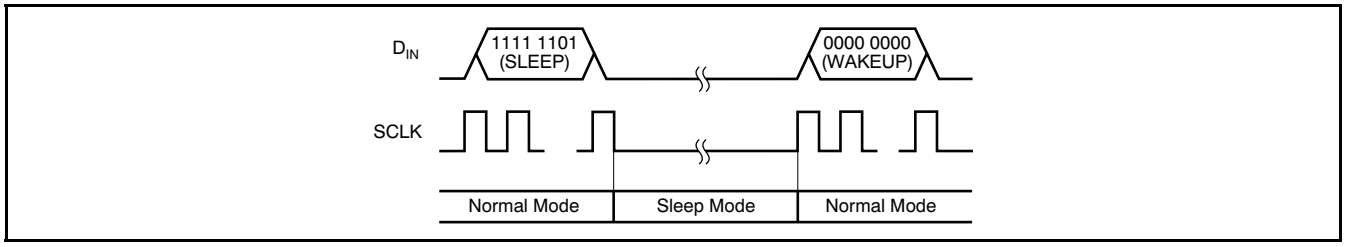


Figure 40. SLEEP Command Sequence

WAKEUP — Complete Synchronization or Exit Sleep Mode

Description: Used in conjunction with the SYNC and STANDBY commands. Two values (all zeros or all ones) are available for this command.

RESET — Reset Registers to Default Values

Description: Returns all registers to their default values. This command will also stop the Read Data Continuous mode. While in the Read Data Continuous mode, the RESET command must be issued after $\overline{DRDY}$ goes low and complete before $\overline{DRDY}$ returns high.

DEFINITIONS

Analog Input Voltage—the voltage at any one analog input relative to AGND.

Analog Input Differential Voltage—given by the following equation: $(A_{IN+}) - (A_{IN-})$. Thus, a positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative.

For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 1, the positive full-scale output is produced when the analog input differential is 2.5V. The negative full-scale output is produced when the differential is –2.5V. In each case, the actual input voltages must remain within the AGND to AV_{DD} range.

Conversion Cycle—the term *conversion cycle* usually refers to a discrete A/D conversion operation, such as that performed by a successive approximation converter. As used here, a conversion cycle refers to the t_{DATA} time period. However, each digital output is actually based on the modulator results from several t_{DATA} time periods.

FILTER SETTING	MODULATOR RESULTS
Fast Settling	1 t_{DATA} Time Period
$Sinc^2$	2 t_{DATA} Time Period
$Sinc^3$	3 t_{DATA} Time Period

Data Rate—the rate at which conversions are completed. See definition for f_{DATA}.

Decimation Ratio—defines the ratio between the output of the modulator and the output Data Rate. Valid values for the Decimation Ratio are from 20 to 2047. Larger Decimation Ratios will have lower noise.

Effective Resolution—the effective resolution of the ADS1216 in a particular configuration can be expressed in two different units: bits rms (referenced to output) and V_{RMS} (referenced to input). Computed directly from the converter output data, each is a statistical calculation. The conversion from one to the other is shown below.

Effective number of bits (ENOB) or *effective resolution* is commonly used to define the usable resolution of the A/D converter. It is calculated from empirical data taken directly from the device. It is typically determined by applying a fixed known signal source to the analog input and computing the standard deviation of the data sample set. The rms noise defines the $\pm\sigma$ interval about the sample mean.

The data from the A/D converter is output as codes, which then can be easily converted to other units, such as ppm or volts. The equations and table below show the relationship between bits or codes, ppm, and volts.

$$\text{ENOB} = \frac{-20\ \log(\text{ppm})}{6.02}$$

BITS rms	BIPOLAR V_{RMS}	UNIPOLAR V_{RMS}
	$\frac{\left(\frac{2V_{REF}}{PGA}\right)}{10\left(\frac{6.02ER}{20}\right)}$	$\frac{\left(\frac{V_{REF}}{PGA}\right)}{10\left(\frac{6.02ER}{20}\right)}$
24	298nV	149nV
22	1.19µV	597nV
20	4.77µV	2.39µV
18	19.1µV	9.55µV
16	76.4µV	38.2µV
14	505µV	152.7µV
12	1.22mV	610µV

f_{DATA}—the frequency of the digital output data produced by the ADS1216. f_{DATA} is also referred to as the data rate.

$$f_{DATA} = \left(\frac{f_{MOD}}{\text{Decimation Ratio}}\right) = \left(\frac{f_{OSC}}{\text{mfactor Decimation Ratio}}\right)$$

f_{MOD}—the frequency or speed at which the modulator of the ADS1216 is running. This rate depends on the SPEED bit as shown below:

SPEED BIT	f_{MOD}
0	$f_{OSC}/128$
1	$f_{OSC}/256$

f_{OSC}—the frequency of the crystal input signal at the X_{IN} input of the ADS1216.

f_{SAMP}—the frequency, or switching speed, of the input sampling capacitor. The value is given by one of the following equations:

PGA SETTING	SAMPLING FREQUENCY
1, 2, 4, 8	$f_{SAMP} = \frac{f_{OSC}}{\text{mfactor}}$
8	$f_{SAMP} = \frac{2f_{OSC}}{\text{mfactor}}$
16	$f_{SAMP} = \frac{8f_{OSC}}{\text{mfactor}}$
32	$f_{SAMP} = \frac{16f_{OSC}}{\text{mfactor}}$
64, 128	$f_{SAMP} = \frac{16f_{OSC}}{\text{mfactor}}$

Filter Selection—the ADS1216 uses a (sinx/x) filter or sinc filter. There are three different sinc filters that can be selected. A Fast-Settling filter will settle in one t_{DATA} cycle. The $Sinc^2$ filter will settle in two cycles and have lower noise. The $Sinc^3$ will achieve lowest noise and higher number of effective bits, but requires three cycles to settle. The ADS1216 will operate with any one of these filters, or it can operate in an auto mode, where it will first select the Fast-Settling filter after a new channel is selected for two readings and will then switch to $Sinc^2$ for one reading, followed by $Sinc^3$ from then on.

Full-Scale Range (FSR)—as with most A/D converters, the full-scale range of the ADS1216 is defined as the *input*, which produces the positive full-scale digital output minus the *input*, which produces the negative full-scale digital output. The full-scale range changes with gain setting; see Table 5.

For example, when the converter is configured with a 2.5V reference and is placed in a gain setting of 2, the full-scale range is: [1.25V (positive full-scale) – (–1.25V (negative full-scale))] = 2.5V.

Least Significant Bit (LSB) Weight—this is the theoretical amount of voltage that the differential voltage at the analog input would have to change in order to observe a change in the output data of one least significant bit. It is computed as shown in Equation 1:

$$\text{LSB Weight} = \frac{\text{Full–Scale Range}}{2^N} \quad (1)$$

where ***N*** is the number of bits in the digital output.

t_{DATA}—the inverse of f_{DATA}, or the period between each data output.

Table 5. Full-Scale Range vs PGA Setting

	5V SUPPLY ANALOG INPUT(1)			GENERAL EQUATIONS		
GAIN SETTING	FULL-SCALE RANGE	DIFFERENTIAL INPUT VOLTAGES(2)	PGA OFFSET RANGE	FULL-SCALE RANGE	DIFFERENTIAL INPUT VOLTAGES(2)	PGA SHIFT RANGE
1	5V	±2.5V	±1.25V	$\frac{2V_{REF}}{PGA}$	$\frac{\pm V_{REF}}{PGA}$	$\frac{\pm V_{REF}}{2PGA}$
2	2.5V	±1.25V	±0.625V			
4	1.25V	±0.625V	±312.5mV			
8	0.625V	±312.5mV	±156.25mV			
16	312.5mV	±156.25mV	±78.125mV			
34	156.25mV	±78.125mV	±39.0625mV			
64	78.125mV	±39.0625mV	±19.531mV			
128	39.0625mV	±19.531mV	±9.766mV			

(1) With a 2.5V reference.
(2) The ADS1216 allows common-mode voltage as long as the absolute input voltage on A_{IN+} or A_{IN-} does not go below AGND or above AV_{DD}.

Changes from C Revision (May 2006) to D Revision **Page**

- Added title for Table 1 16
- Changed *11 registers* to *16 registers* in Description text of RREG section in Command Definitions. 28

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1216Y/250	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1216Y	Samples
ADS1216Y/2K	ACTIVE	TQFP	PFB	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1216Y	Samples
ADS1216Y/2KG4	ACTIVE	TQFP	PFB	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1216Y	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

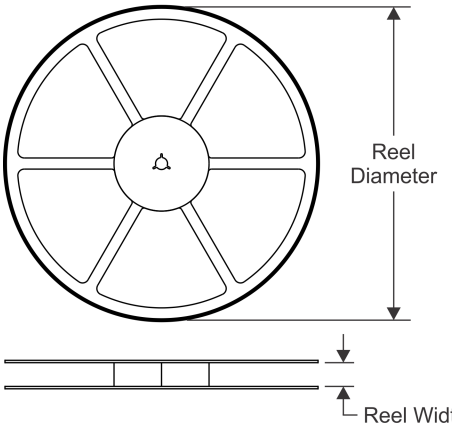
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

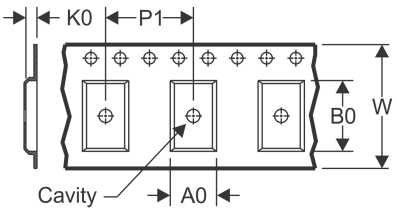
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

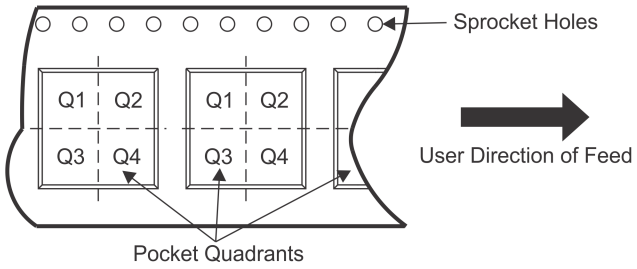


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

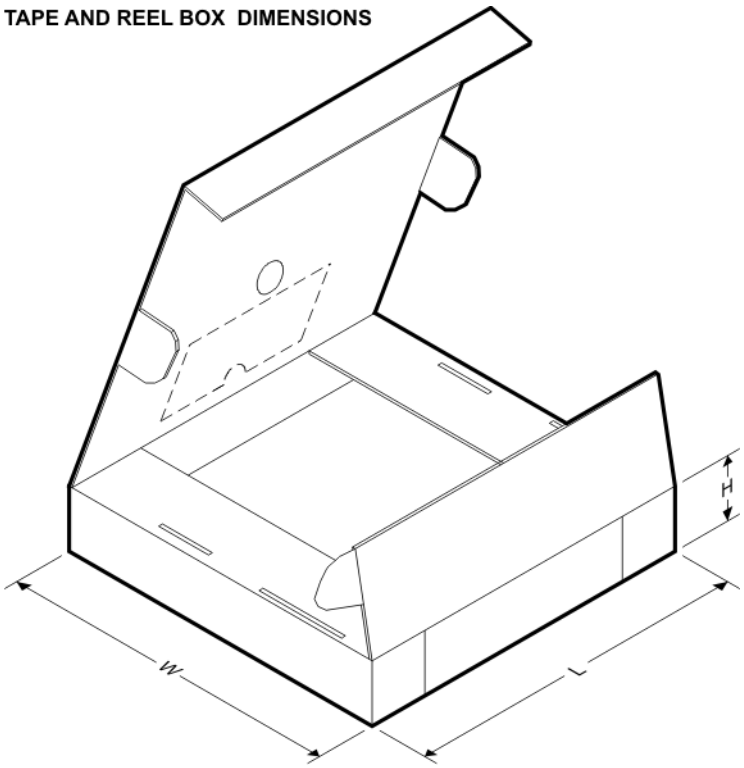
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1216Y/250	TQFP	PFB	48	250	180.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
ADS1216Y/2K	TQFP	PFB	48	2000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

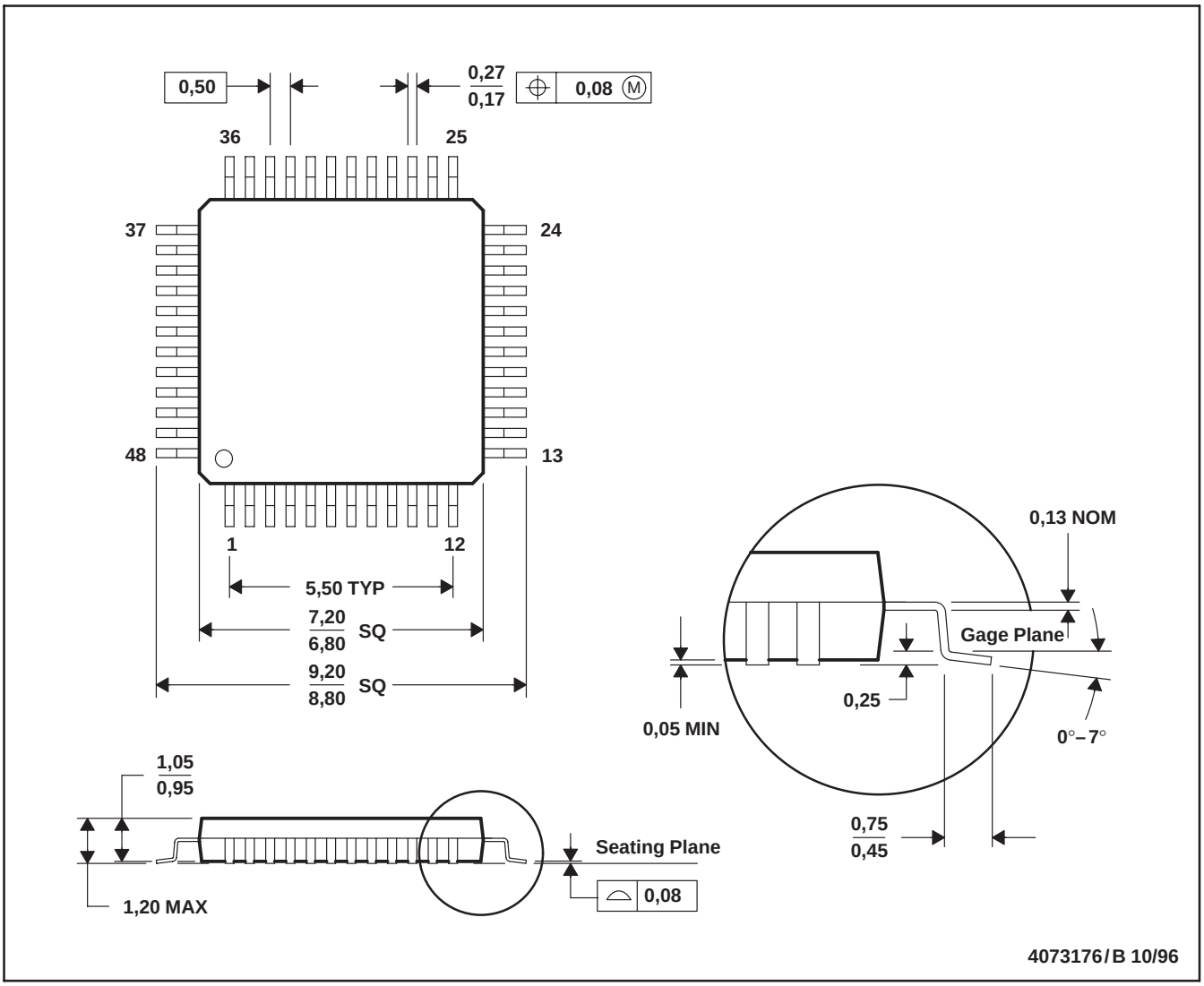


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1216Y/250	TQFP	PFB	48	250	213.0	191.0	55.0
ADS1216Y/2K	TQFP	PFB	48	2000	350.0	350.0	43.0

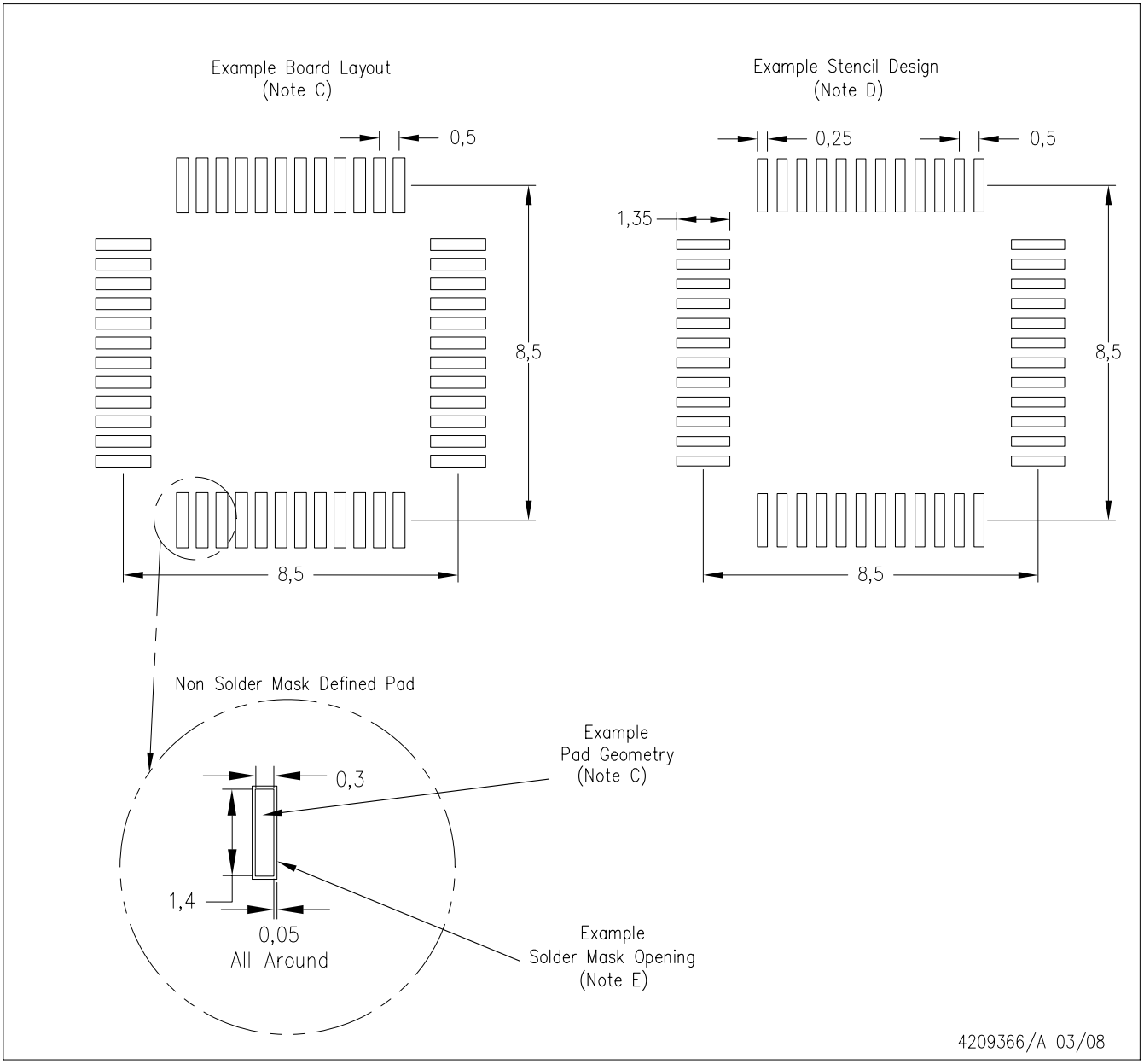
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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