



# THE DATASHEET OF STL8DN10LF3



## Automotive-grade dual N-channel 100 V, 25 mΩ typ., 7.8 A STripFET™ III Power MOSFET in a PowerFLAT™ 5x6 double island package

Datasheet — production data

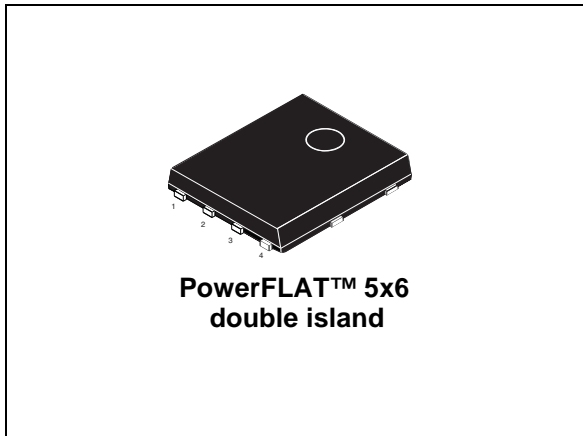
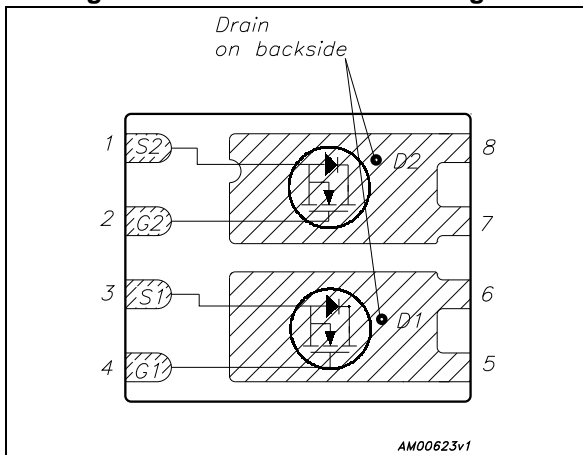


Figure 1. Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL8DN10LF3	100 V	35 mΩ	7.8 A

- Designed for automotive applications and AEC-Q101 qualified
- Logic level V<sub>GS(th)</sub>
- 175 °C junction temperature
- 100% avalanche rated
- Wettable flank package

### Applications

- Switching applications

### Description

This device is an N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1. Device summary

Order code	Marking	Packages <sup>(1)</sup>	Packaging
STL8DN10LF3	8DN10LF3	PowerFLAT™ 5x6 double island	Tape and reel

1. For wettable flank option, please contact ST sale offices

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1),(2)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	20	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	20	A
$I_D^{(4)}$	Drain current (continuous) at $T_{pcb} = 25^\circ\text{C}$	7.8	A
$I_D^{(4)}$	Drain current (continuous) at $T_{pcb}=100^\circ\text{C}$	5.5	A
$I_{DM}^{(3),(4)}$	Drain current (pulsed)	31.2	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	70	W
$P_{TOT}^{(4)}$	Total dissipation at $T_{pcb} = 25^\circ\text{C}$	4.3	W
$I_{AV}$	Not-repetitive avalanche current	7.8	A
$E_{AS}^{(5)}$	Single pulse avalanche energy	190	mJ
$T_J$	Operating junction temperature	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature		$^\circ\text{C}$

1. Specified by design. Not subject to production test.
2. Current is limited by bonding, with an  $R_{thJC} = 2.3^\circ\text{C/W}$  the chip is able to carry 32 A at  $25^\circ\text{C}$ .
3. Pulse width limited by safe operating area.
4. When mounted on FR-4 board of  $1\text{inch}^2$ , 2oz Cu,  $t < 10\text{ sec}$
5. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D = 8\text{ A}$ ,  $V_{DD} = 25\text{ V}$ , per channel, 100% tested.

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.1	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^\circ\text{C/W}$

1. When mounted on FR-4 board of  $1\text{inch}^2$ , 2oz Cu,  $t < 10\text{ sec}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 250\ \mu A$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 100\ V$			1	$\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\ V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu A$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ V$ , $I_D = 4\ A$		25	35	m $\Omega$
		$V_{GS} = 5\ V$ , $I_D = 4\ A$		40	50	m $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\ V$ , $f = 1\ MHz$ , $V_{GS} = 0$	-	970	-	pF
$C_{oss}$	Output capacitance		-	115	-	pF
$C_{rss}$	Reverse transfer capacitance		-	11.5	-	pF
$Q_g$	Total gate charge	$V_{DD} = 50\ V$ , $I_D = 7.8\ A$	-	20.5	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10\ V$	-	4	-	nC
$Q_{gd}$	Gate-drain charge	<a href="#">Figure 13</a>	-	5	-	nC
$R_G$	Intrinsic gate resistance	$f = 1\ MHz$ open drain	-	3.65	-	$\Omega$

**Table 6. Switching times**

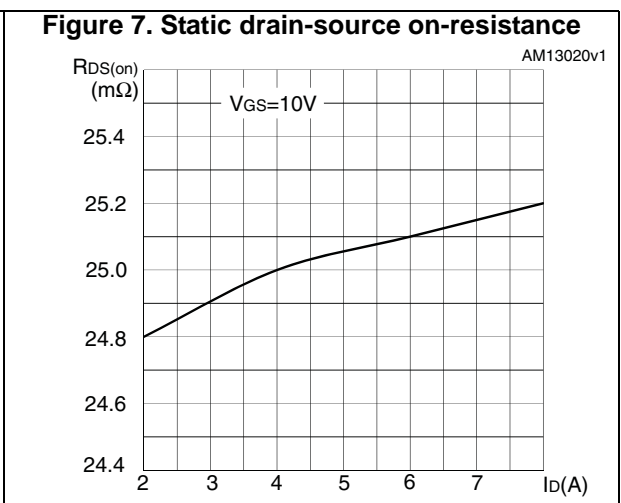
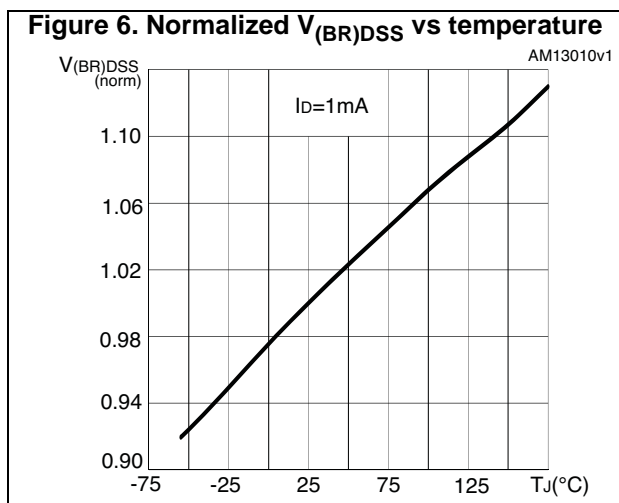
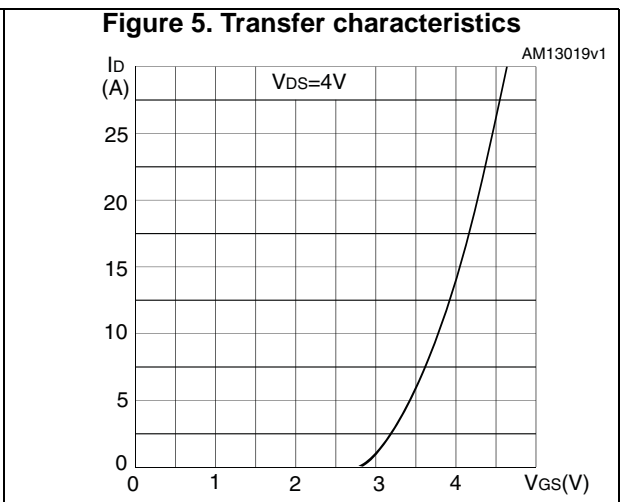
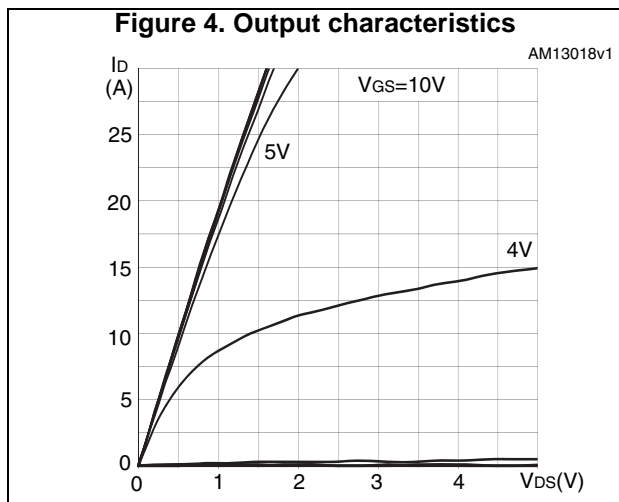
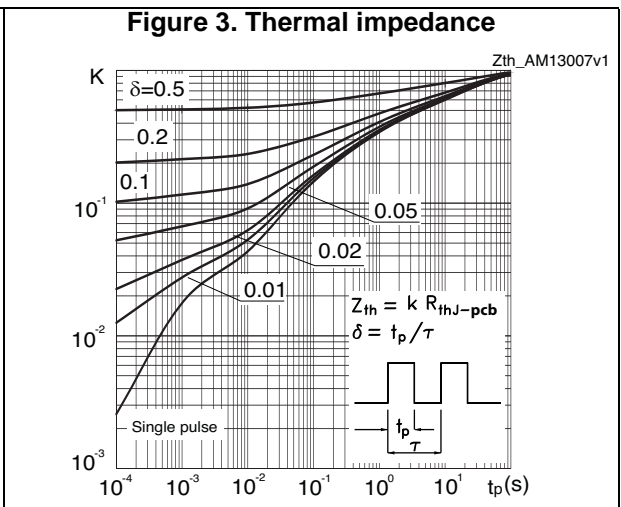
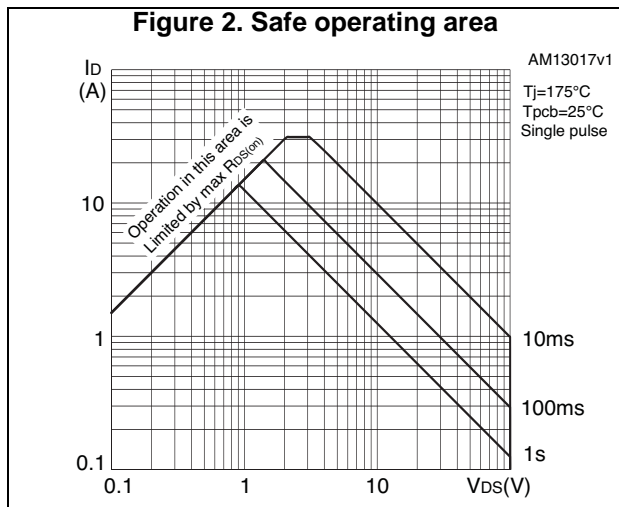
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ V$ , $I_D = 7.8\ A$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\ V$ <a href="#">Figure 14</a>	-	8.7	-	ns
$t_r$	Rise time		-	9.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	50.6	-	ns
$t_f$	Fall time		-	5.2	-	ns

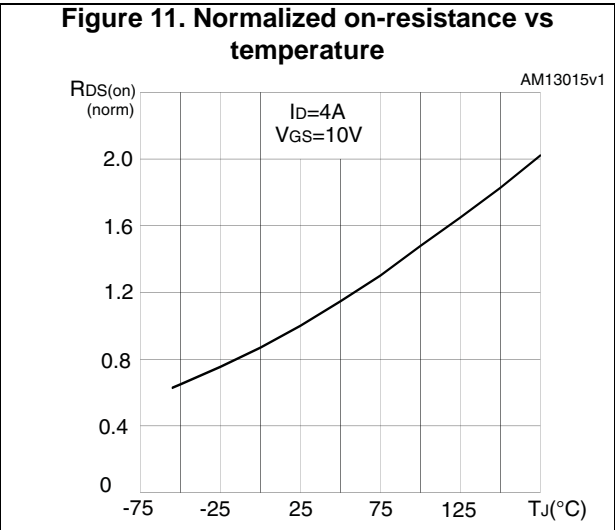
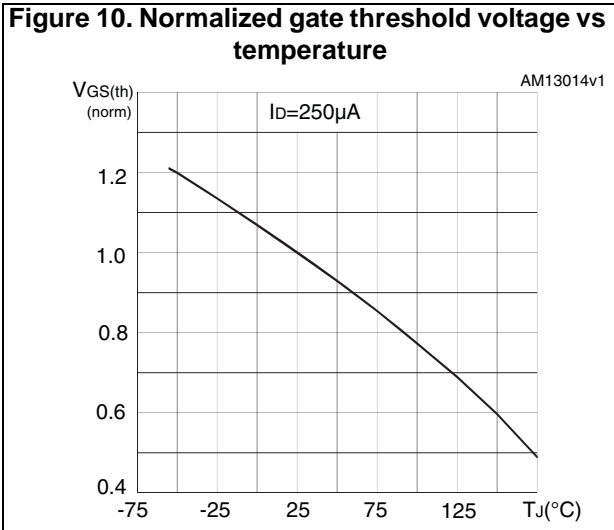
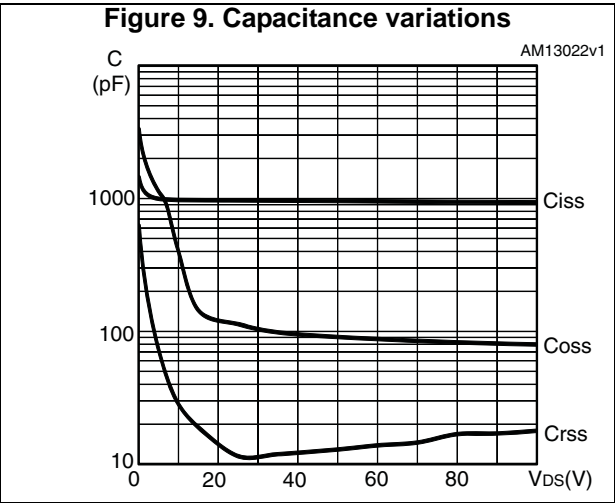
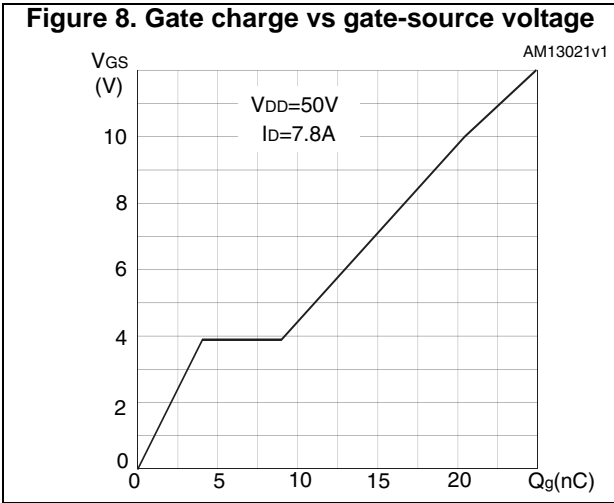
Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		7.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		31.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7.8 \text{ A}, V_{GS} = 0$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7.8 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 48 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$	-	42.5		ns
$Q_{rr}$	Reverse recovery charge		-	87		nC
$I_{RRM}$	Reverse recovery current		-	4.08		A

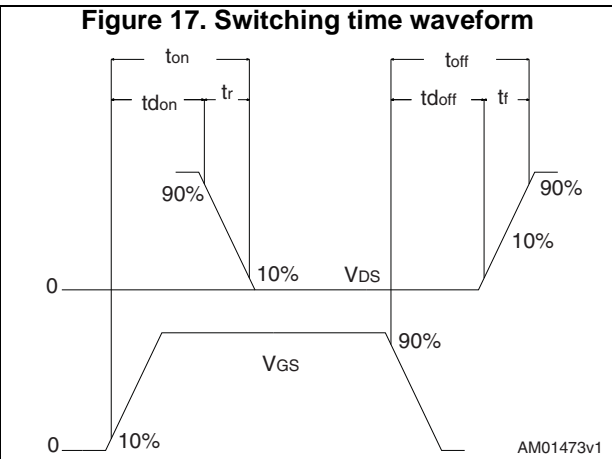
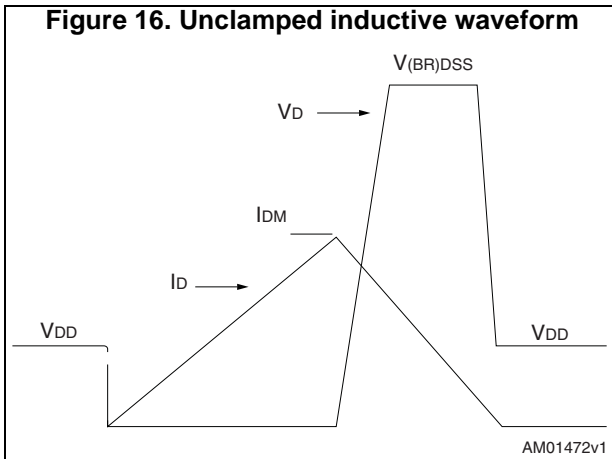
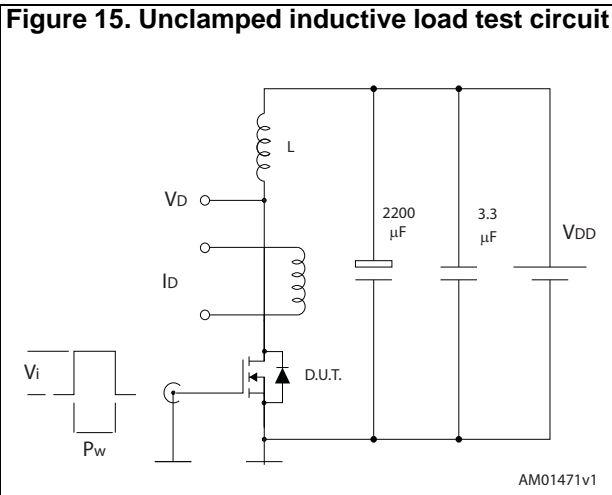
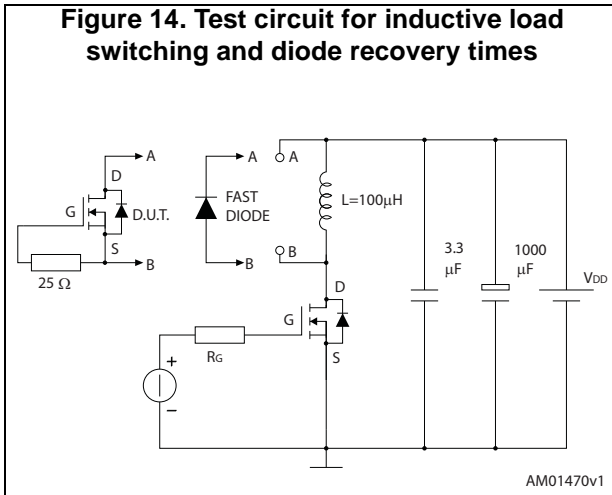
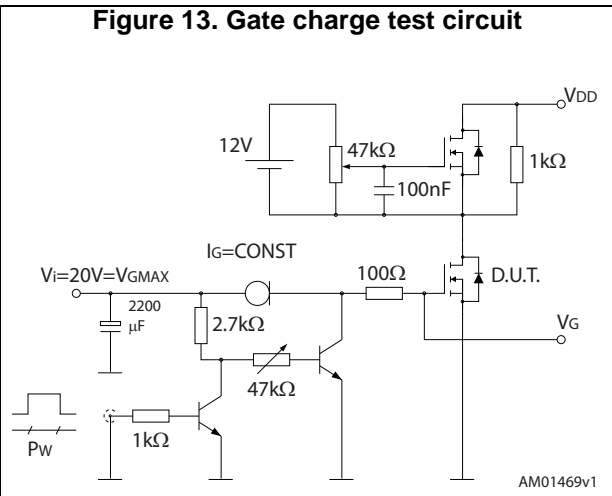
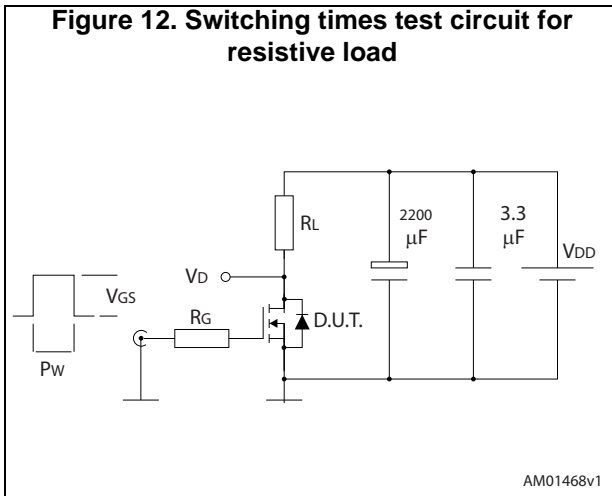
1. Pulse width limited by safe operating area
2. Pulsed: pulse duration= 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)





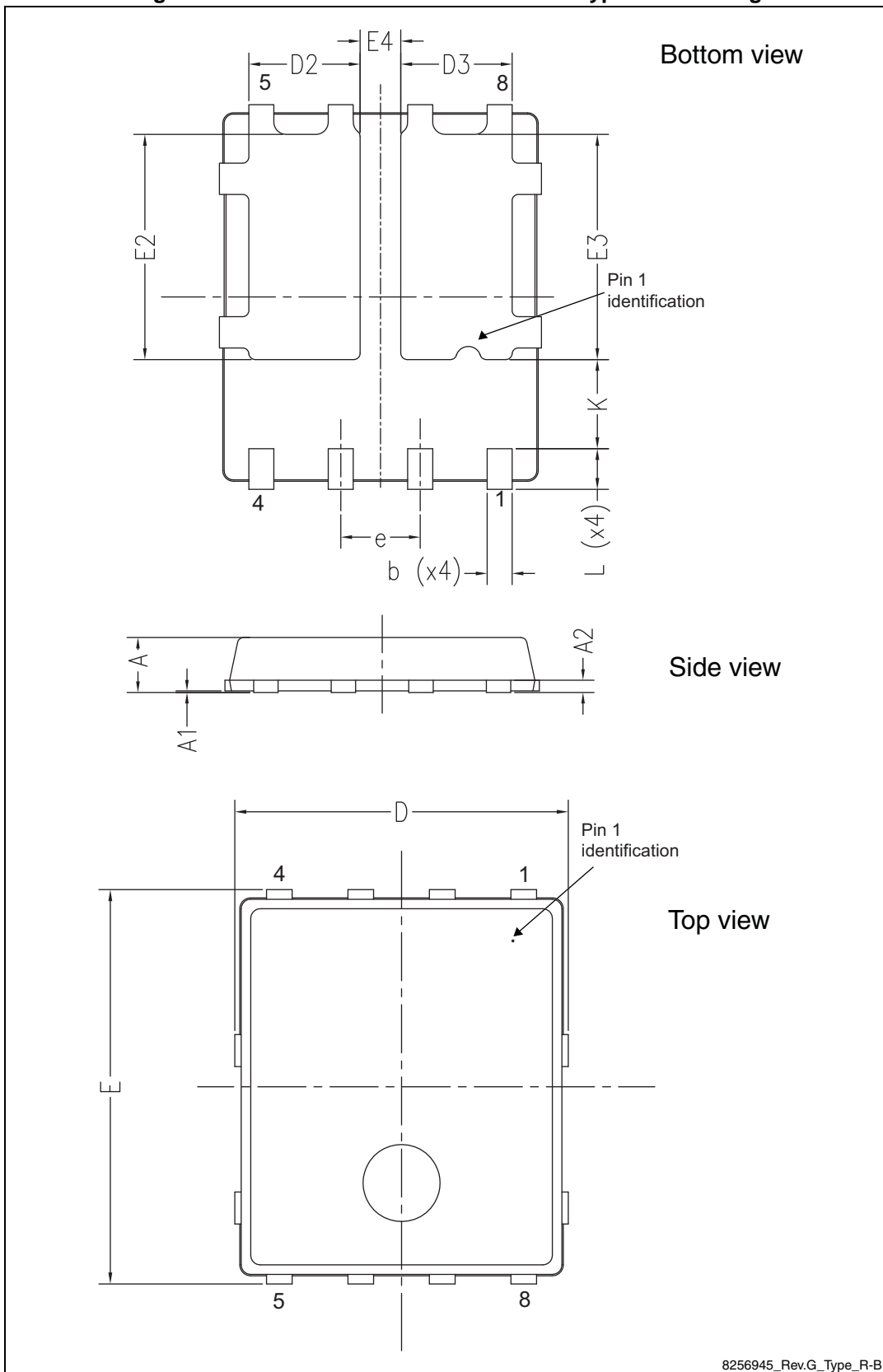
### 3 Test circuits



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 18. PowerFLAT™ 5x6 double island type R-B drawing



8256945\_Rev.G\_Type\_R-B

Table 8. PowerFLAT™ 5x6 double island type R-B mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 19. PowerFLAT 5x6 double island type WF drawing

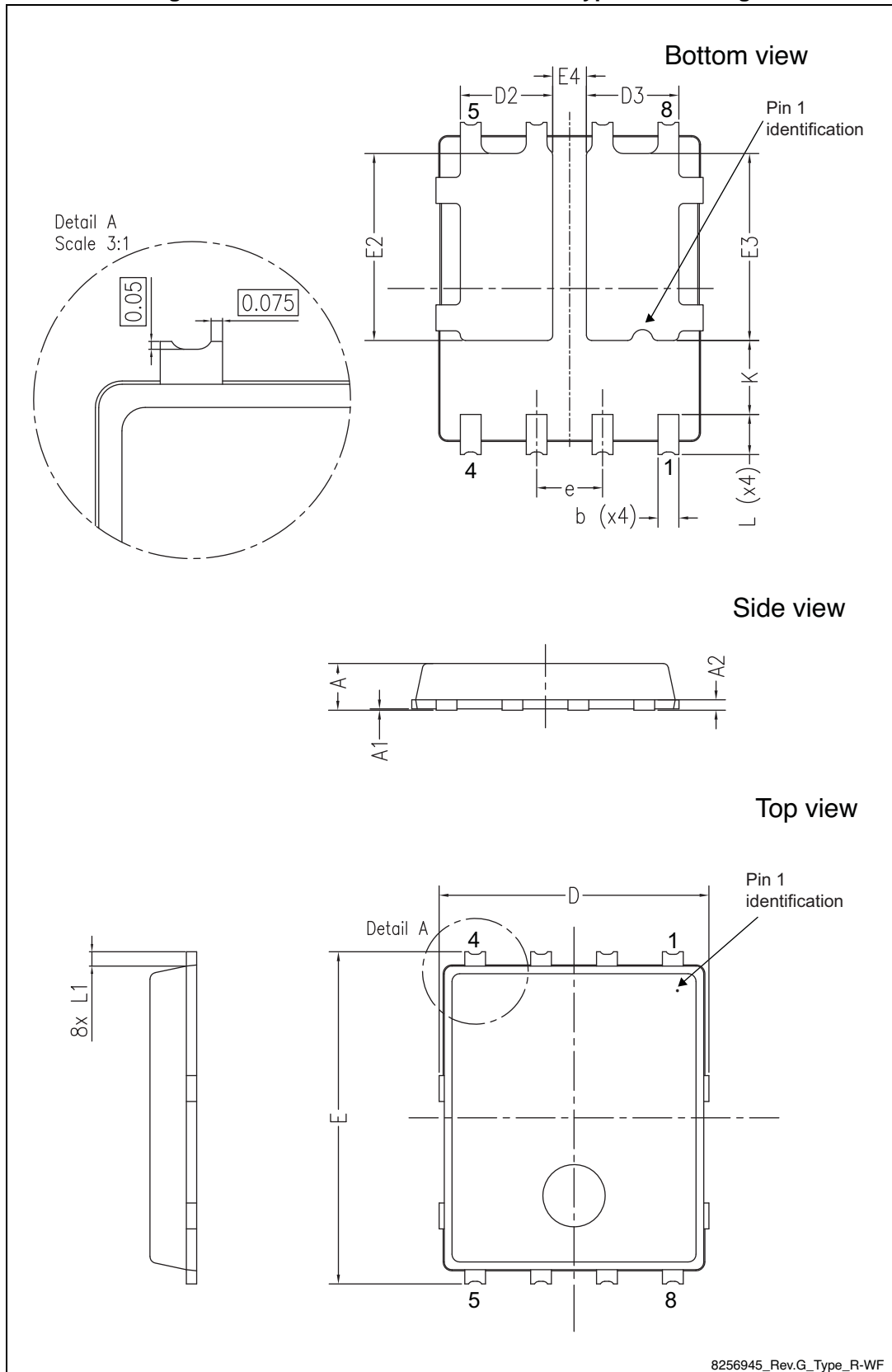
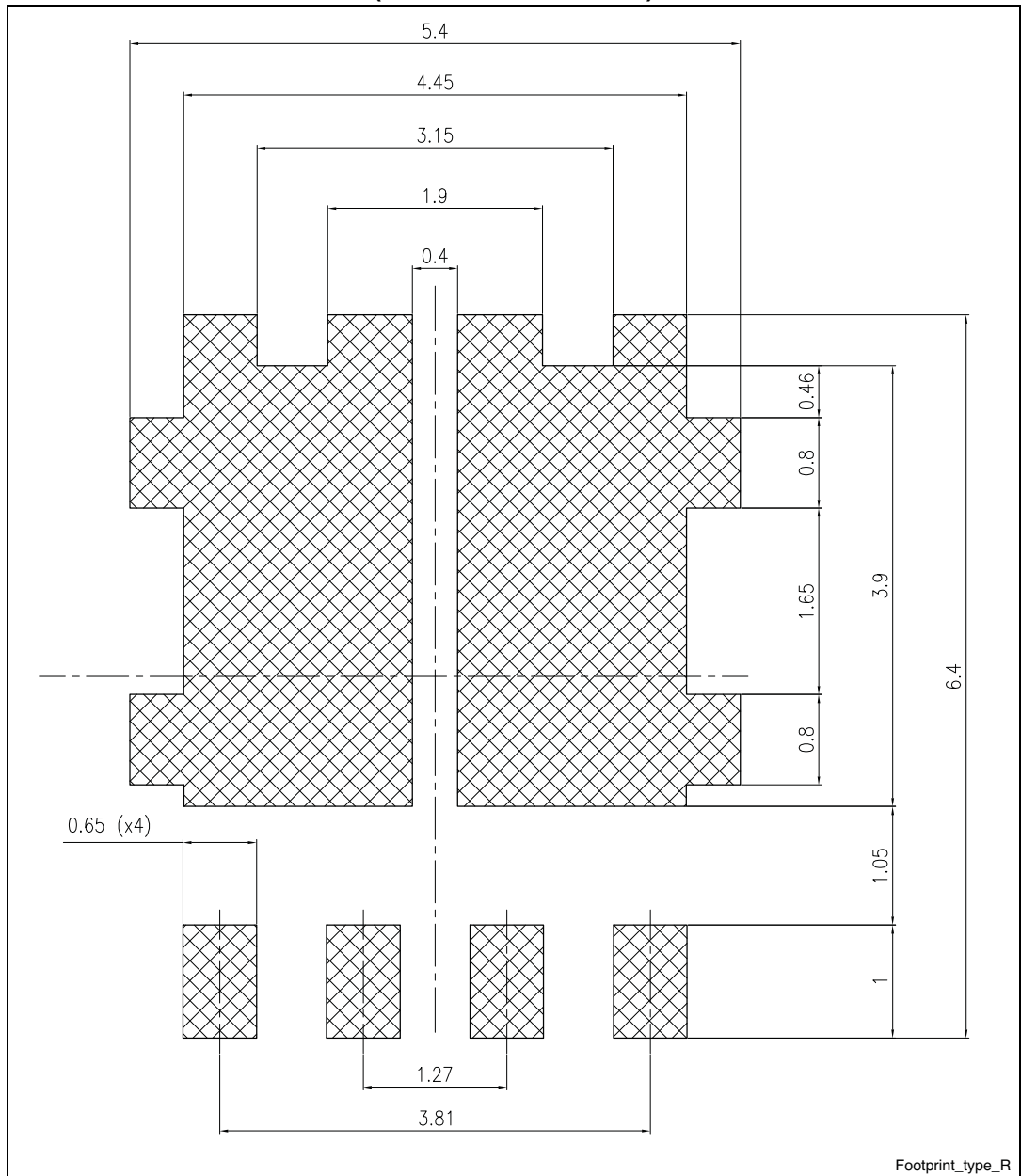


Table 9. PowerFLAT 5x6 double island type WF mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	6.20	6.40	6.60
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.70		0.90
L1		0.275	
K	1.275		1.575

Figure 20. PowerFLAT™ 5x6 double island type R drawing recommended footprint (dimensions are in mm)



# 5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 double island type R-B tape<sup>(a)</sup>

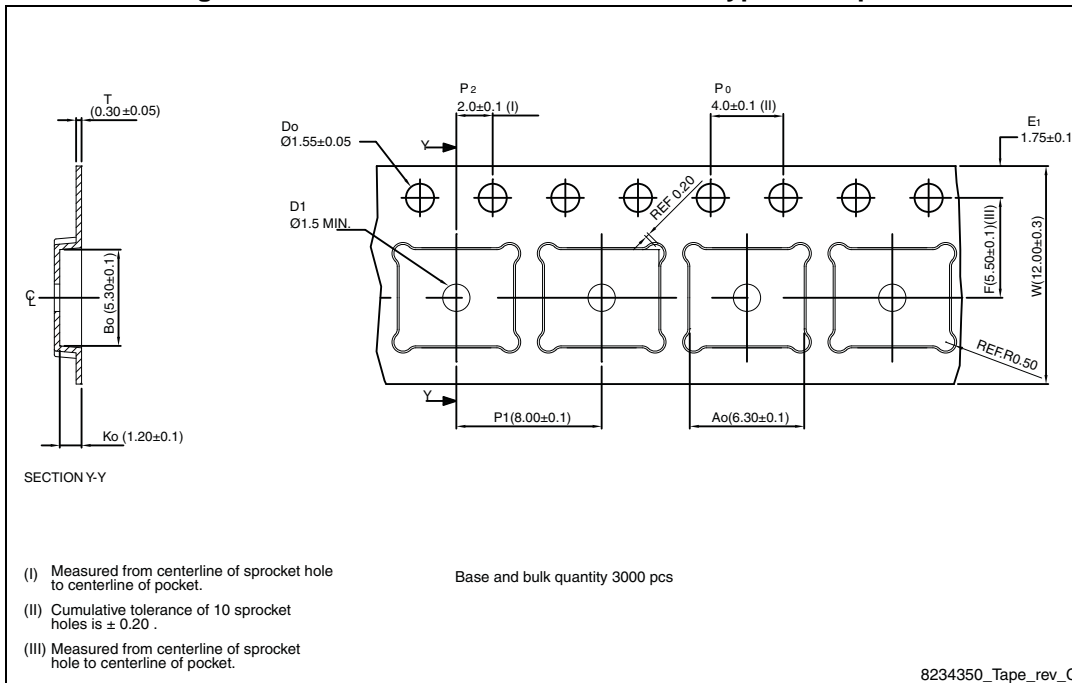
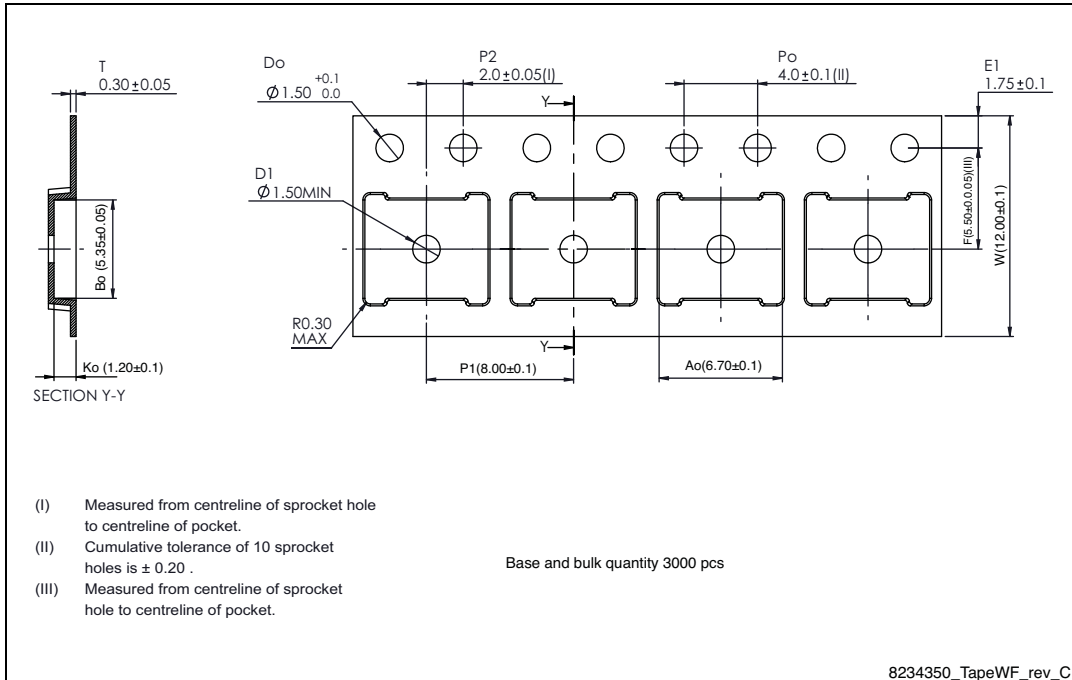


Figure 22. PowerFLAT 5x6 double island type WF tape<sup>(a)</sup>



a. All dimensions are in millimeters.



## 6 Revision history

**Table 10. Document revision history**

Date	Revision	Changes
28-Mar-2012	1	First release.
20-Jun-2012	2	Added <a href="#">Section 2.1: Electrical characteristics (curves)</a> . Updated <a href="#">Section 4: Package mechanical data</a> and title on the cover page.
26-Jun-2012	3	Updated <a href="#">Figure 9: Capacitance variations</a> . Document status promoted from preliminary to production data.
28-Oct-2013	4	<ul style="list-style-type: none"> <li>– Updated: <a href="#">Section 4: Package mechanical data</a> and <a href="#">Section 5: Packaging mechanical data</a></li> <li>– Updated title and features in cover page</li> <li>– Modified: <math>V_{GS(th)}</math> value in <a href="#">Table 4</a></li> <li>– Minor text changes</li> </ul>
20-Feb-2014	5	<ul style="list-style-type: none"> <li>– Added: <a href="#">Features</a> in cover page</li> <li>– Added: <a href="#">note 1</a> in <a href="#">Table 1</a></li> <li>– Added: <a href="#">Table 19</a> and <a href="#">Table 9</a></li> <li>– Added: <a href="#">Figure 22</a></li> <li>– Minor text changes</li> </ul>

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