THE DATASHEET OF

AD7924BRUZ

www.win-source.net 0086-755-83957316

4-Channel, 1 MSPS, 8-/10-/12-Bit ADCs with Sequencer in 16-Lead TSSOP

Data Sheet

AD7904/AD7914/AD7924

FEATURES

Fast throughput rate: 1 MSPS
Specified for AV_{DD} of 2.7 V to 5.25 V
Low power:
6 mW maximum at 1 MSPS with 3 V supplies
13.5 mW maximum at 1 MSPS with 5 V supplies
4 single-ended inputs with sequencer
Wide input bandwidth
AD7924, 70 dB SNR at 50 kHz input frequency
Flexible power/serial clock speed management
No pipeline delays
High speed serial interface: SPI/QSPI™/
MICROWIRE™/DSP compatible
Shutdown mode: 0.5 µA maximum
16-lead TSSOP package
Qualified for automotive applications

FUNCTIONAL BLOCK DIAGRAM

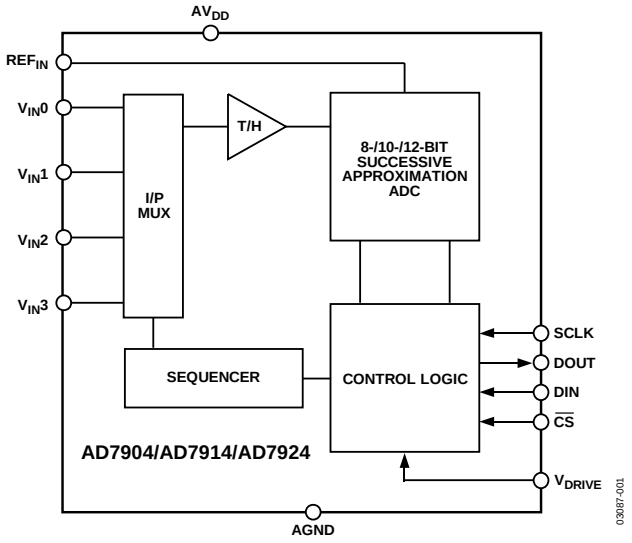

Figure 1.

GENERAL DESCRIPTION

The AD7904/AD7914/AD7924 are, respectively, 8-bit, 10-bit, and 12-bit, high speed, low power, 4-channel successive approximation ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1 MSPS. The parts contain a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 8 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock signal, allowing the device to easily interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and conversion is initiated at this point. There are no pipeline delays associated with the part.

The AD7904/AD7914/AD7924 use advanced design techniques to achieve very low power dissipation at maximum throughput rates. At maximum throughput rates, the AD7904/AD7914/AD7924 consume 2 mA maximum with 3 V supplies; with 5 V supplies, the current consumption is 2.7 mA maximum.

Through the configuration of the control register, the analog input range for the part can be selected as 0 V to REF_{IN} or 0 V to $2 \times REF_{IN}$, with either straight binary or twos complement output coding. The AD7904/AD7914/AD7924 each feature four single-ended analog inputs with a channel sequencer to allow a preprogrammed selection of channels to be converted sequentially.

The conversion time for the AD7904/AD7914/AD7924 is determined by the SCLK frequency, which is also used as the master clock to control the conversion.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption.
   The AD7904/AD7914/AD7924 offer throughput rates up to 1 MSPS. At the maximum throughput rate with 3 V supplies, the AD7904/AD7914/AD7924 dissipate only 6 mW of power maximum.
2. Four Single-Ended Inputs with Channel Sequencer.
   A consecutive sequence of channels can be selected, through which the ADC will cycle and convert on.
3. Single-Supply Operation with V_{DRIVE} Function.
   The AD7904/AD7914/AD7924 operate from a single 2.7 V to 5.25 V supply. The V_{DRIVE} function allows the serial interface to connect directly to 3 V or 5 V processor systems, independent of V_{DD}.
4. Flexible Power/Serial Clock Speed Management.
   The conversion rate is determined by the serial clock, allowing the conversion time to be reduced by increasing the serial clock speed. The parts also feature two shutdown modes to maximize power efficiency at lower throughput rates. Current consumption is 0.5 µA maximum when in full shutdown.
5. No Pipeline Delay.
   The parts feature a standard successive approximation ADC with accurate control of the sampling instant via the $\overline{CS}$ input and once-off conversion control.

Rev. C Document Feedback
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11/02—Revision 0: Initial Version

SPECIFICATIONS

AD7904 SPECIFICATIONS

AV_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK} = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz
Signal to (Noise + Distortion) (SINAD)[2]	49	dB min	B models
	48.5	dB min	W models
Signal-to-Noise Ratio (SNR)	49	dB min	B models
	48.5	dB min	W models
Total Harmonic Distortion (THD)[2]	−66	dB max	
Peak Harmonic or Spurious Noise (SFDR)	−64	dB max	
Intermodulation Distortion (IMD)			fa = 40.1 kHz, fb = 41.5 kHz
Second-Order Terms	−90	dB typ	
Third-Order Terms	−90	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation[2]	−85	dB typ	f_{IN} = 400 kHz
Full Power Bandwidth	8.2	MHz typ	@ 3 dB
	1.6	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	8	Bits	
Integral Nonlinearity (INL)[2]	±0.2	LSB max	
Differential Nonlinearity (DNL)[2]	±0.2	LSB max	Guaranteed no missed codes to 8 bits
0 V to REF_{IN} Input Range			Straight binary output coding
Offset Error[2]	±0.5	LSB max	
Offset Error Match[2]	±0.05	LSB max	
Gain Error[2]	±0.2	LSB max	
Gain Error Match[2]	±0.05	LSB max	
0 V to 2 × REF_{IN} Input Range			−REF_{IN} to +REF_{IN} biased about REF_{IN} with twos complement output coding
Positive Gain Error[2]	±0.2	LSB max	
Positive Gain Error Match[2]	±0.05	LSB max	
Zero Code Error[2]	±0.5	LSB max	
Zero Code Error Match[2]	±0.1	LSB max	
Negative Gain Error[2]	±0.2	LSB max	
Negative Gain Error Match[2]	±0.05	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to REF_{IN}	V	RANGE bit set to 1
	0 to 2 × REF_{IN}	V	RANGE bit set to 0, AV_{DD}/V_{DRIVE} = 4.75 V to 5.25 V
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage	2.5	V	±1% specified performance
DC Leakage Current	±1	µA max	
REF_{IN} Input Impedance	36	kΩ typ	f_{SAMPLE} = 1 MSPS
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 × V_{DRIVE}	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	pF max	

Parameter	B Version[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2	V min	I_{SOURCE} = 200 µA, AV_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (natural) binary		CODING bit set to 1
	Twos complement		CODING bit set to 0
CONVERSION RATE			
Conversion Time	800	ns max	16 SCLK cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time[2]	300	ns max	Sine wave input
	300	ns max	Full-scale step input
Throughput Rate	1	MSPS max	See the Serial Interface section
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/V max	
V_{DRIVE}	2.7/5.25	V min/V max	
I_{DD}[4]			Digital inputs = 0 V or V_{DRIVE}
Normal Mode (Static)	600	µA typ	AV_{DD} = 2.7 V to 5.25 V, SCLK on or off
Normal Mode (Operational)	2.7	mA max	AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
	2	mA max	AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz
Auto Shutdown Mode	960	µA typ	f_{SAMPLE} = 250 kSPS
	0.5	µA max	Static
Full Shutdown Mode	0.5	µA max	SCLK on or off (20 nA typ)
Power Dissipation[4]			
Normal Mode (Operational)	13.5	mW max	AV_{DD} = 5 V, f_{SCLK} = 20 MHz
	6	mW max	AV_{DD} = 3 V, f_{SCLK} = 20 MHz
Auto Shutdown Mode (Static)	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V
Full Shutdown Mode	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V

[1] Temperature range for B versions: −40°C to +85°C.
[2] See the Terminology section.
[3] Sample tested @ 25°C to ensure compliance.
[4] See the Power vs. Throughput Rate section.

AD7914 SPECIFICATIONS

AV_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK} = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz
Signal to (Noise + Distortion) (SINAD)[2]	61	dB min	B models
	60.5	dB min	W models
Signal-to-Noise Ratio (SNR)	61	dB min	B models
	60.5	dB min	W models
Total Harmonic Distortion (THD)[2]	−72	dB max	
Peak Harmonic or Spurious Noise (SFDR)	−74	dB max	
Intermodulation Distortion (IMD)			fa = 40.1 kHz, fb = 41.5 kHz
Second-Order Terms	−90	dB typ	
Third-Order Terms	−90	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation[2]	−85	dB typ	f_{IN} = 400 kHz
Full Power Bandwidth	8.2	MHz typ	@ 3 dB
	1.6	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity (INL)[2]	±0.5	LSB max	
Differential Nonlinearity (DNL)[2]	±0.5	LSB max	Guaranteed no missed codes to 10 bits
0 V to REF_{IN} Input Range			Straight binary output coding
Offset Error[2]	±2	LSB max	
Offset Error Match[2]	±0.2	LSB max	
Gain Error[2]	±0.5	LSB max	
Gain Error Match[2]	±0.2	LSB max	
0 V to 2 × REF_{IN} Input Range			−REF_{IN} to +REF_{IN} biased about REF_{IN} with twos complement output coding
Positive Gain Error[2]	±0.5	LSB max	
Positive Gain Error Match[2]	±0.2	LSB max	
Zero Code Error[2]	±2	LSB max	
Zero Code Error Match[2]	±0.2	LSB max	
Negative Gain Error[2]	±0.5	LSB max	
Negative Gain Error Match[2]	±0.2	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to REF_{IN}	V	RANGE bit set to 1
	0 to 2 × REF_{IN}	V	RANGE bit set to 0, AV_{DD}/V_{DRIVE} = 4.75 V to 5.25 V
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage	2.5	V	±1% specified performance
DC Leakage Current	±1	µA max	
REF_{IN} Input Impedance	36	kΩ typ	f_{SAMPLE} = 1 MSPS
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 × V_{DRIVE}	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	pF max	

Parameter	B Version[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2	V min	I_{SOURCE} = 200 µA, AV_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (natural) binary		CODING bit set to 1
	Twos complement		CODING bit set to 0
CONVERSION RATE			
Conversion Time	800	ns max	16 SCLK cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time[2]	300	ns max	Sine wave input
	300	ns max	Full-scale step input
Throughput Rate	1	MSPS max	See the Serial Interface section
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/V max	
V_{DRIVE}	2.7/5.25	V min/V max	
I_{DD}[4]			Digital inputs = 0 V or V_{DRIVE}
Normal Mode (Static)	600	µA typ	AV_{DD} = 2.7 V to 5.25 V, SCLK on or off
Normal Mode (Operational)	2.7	mA max	AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
	2	mA max	AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz
Auto Shutdown Mode	960	µA typ	f_{SAMPLE} = 250 kSPS
	0.5	µA max	Static
Full Shutdown Mode	0.5	µA max	SCLK on or off (20 nA typ)
Power Dissipation[4]			
Normal Mode (Operational)	13.5	mW max	AV_{DD} = 5 V, f_{SCLK} = 20 MHz
	6	mW max	AV_{DD} = 3 V, f_{SCLK} = 20 MHz
Auto Shutdown Mode (Static)	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V
Full Shutdown Mode	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V

[1] Temperature range for B versions: −40°C to +85°C.
[2] See the Terminology section.
[3] Sample tested @ 25°C to ensure compliance.
[4] See the Power vs. Throughput Rate section.

AD7924 SPECIFICATIONS

AV_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK} = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz
Signal to (Noise + Distortion) (SINAD)[2]	70	dB min	@ 5 V, B models
	69.5	dB min	@ 5 V, W models
	69	dB min	@ 3 V, typically 69.5 dB
Signal-to-Noise Ratio (SNR)	70	dB min	B models
	69.5	dB min	W models
Total Harmonic Distortion (THD)[2]	−77	dB max	@ 5 V, typically −84 dB
	−73	dB max	@ 3 V, typically −77 dB
Peak Harmonic or Spurious Noise (SFDR)	−78	dB max	@ 5 V, typically −86 dB
Intermodulation Distortion (IMD)			fa = 40.1 kHz, fb = 41.5 kHz
Second-Order Terms	−90	dB typ	
Third-Order Terms	−90	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation[2]	−85	dB typ	f_{IN} = 400 kHz
Full Power Bandwidth	8.2	MHz typ	@ 3 dB
	1.6	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity (INL)[2]	±1	LSB max	
Differential Nonlinearity (DNL)[2]	−0.9/+1.5	LSB max	Guaranteed no missed codes to 12 bits
0 V to REF_{IN} Input Range			Straight binary output coding
Offset Error[2]	±8	LSB max	Typically ±0.5 LSB
Offset Error Match[2]	±0.5	LSB max	
Gain Error[2]	±1.5	LSB max	
Gain Error Match[2]	±0.5	LSB max	
0 V to 2 × REF_{IN} Input Range			−REF_{IN} to +REF_{IN} biased about REF_{IN} with twos complement output coding
Positive Gain Error[2]	±1.5	LSB max	
Positive Gain Error Match[2]	±0.5	LSB max	
Zero Code Error[2]	±8	LSB max	Typically ±0.8 LSB
Zero Code Error Match[2]	±0.5	LSB max	
Negative Gain Error[2]	±1	LSB max	
Negative Gain Error Match[2]	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to REF_{IN}	V	RANGE bit set to 1
	0 to 2 × REF_{IN}	V	RANGE bit set to 0, AV_{DD}/V_{DRIVE} = 4.75 V to 5.25 V
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage	2.5	V	±1% specified performance
DC Leakage Current	±1	µA max	
REF_{IN} Input Impedance	36	kΩ typ	f_{SAMPLE} = 1 MSPS
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 × V_{DRIVE}	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	pF max	

Parameter	B Version[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2	V min	I_{SOURCE} = 200 µA, AV_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (natural) binary		CODING bit set to 1
	Twos complement		CODING bit set to 0
CONVERSION RATE			
Conversion Time	800	ns max	16 SCLK cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time[2]	300	ns max	Sine wave input
	300	ns max	Full-scale step input
Throughput Rate	1	MSPS max	See the Serial Interface section
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/V max	
V_{DRIVE}	2.7/5.25	V min/V max	
I_{DD}[4]			Digital inputs = 0 V or V_{DRIVE}
Normal Mode (Static)	600	µA typ	AV_{DD} = 2.7 V to 5.25 V, SCLK on or off
Normal Mode (Operational)	2.7	mA max	AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
	2	mA max	AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz
Auto Shutdown Mode	960	µA typ	f_{SAMPLE} = 250 kSPS
	0.5	µA max	Static
Full Shutdown Mode	0.5	µA max	SCLK on or off (20 nA typ)
Power Dissipation[4]			
Normal Mode (Operational)	13.5	mW max	AV_{DD} = 5 V, f_{SCLK} = 20 MHz
	6	mW max	AV_{DD} = 3 V, f_{SCLK} = 20 MHz
Auto Shutdown Mode (Static)	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V
Full Shutdown Mode	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V

[1] Temperature range for B versions: −40°C to +85°C.
[2] See the Terminology section.
[3] Sample tested @ 25°C to ensure compliance.
[4] See the Power vs. Throughput Rate section.

TIMING SPECIFICATIONS

AV_{DD} = 2.7 V to 5.25 V, $V_{DRIVE} \le AV_{DD}$, REF_{IN} = 2.5 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 4.

	Limit at T_{MIN}, T_{MAX}			
Parameter[1]	**AV_{DD} = 3 V**	**AV_{DD} = 5 V**	**Unit**	**Description**
f_{SCLK}[2]	10	10	kHz min	
	20	20	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}	16 × t_{SCLK}		
t_{QUIET}	50	50	ns min	Minimum quiet time required between the $\overline{CS}$ rising edge and the start of the next conversion
t_2	10	10	ns min	$\overline{CS}$ to SCLK setup time
t_3[3]	35	30	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled
t_4[3]	40	40	ns max	Data access time after SCLK falling edge
t_5	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK high pulse width
t_7	10	10	ns min	SCLK to DOUT valid hold time
t_8[4]	15/45	15/35	ns min/ns max	SCLK falling edge to DOUT high impedance
t_9	10	10	ns min	DIN setup time prior to SCLK falling edge
t_{10}	5	5	ns min	DIN hold time after SCLK falling edge
t_{11}	20	20	ns min	16th SCLK falling edge to $\overline{CS}$ high
t_{12}	1	1	µs max	Power-up time from full shutdown/auto shutdown modes

[1] Sample tested @ 25°C to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of AV_{DD}) and timed from a voltage level of 1.6 V (see Figure 2). The 3 V operating range spans from 2.7 V to 3.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.4 V or 0.7 × V_{DRIVE}.
[4] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

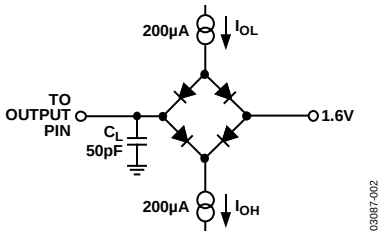

Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to AGND	−0.3 V to +7 V
Digital Output Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
REF_{IN} to AGND	−0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (B Version)	−40°C to +85°C
Automotive (W Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	150.4°C/W (TSSOP)
θ_{JC} Thermal Impedance	27.6°C/W (TSSOP)
Lead Temperature, Soldering	
Vapor Phase (60 secs)	215°C
Infrared (15 secs)	220°C
ESD	1.5 kV

[1] Transient currents of up to 100 mA will not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

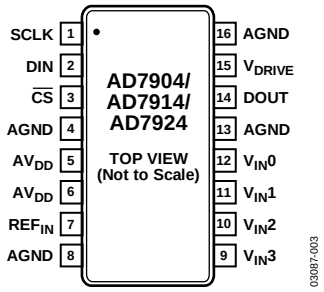

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	SCLK	Serial Clock, Logic Input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7904/AD7914/AD7924 conversion process.
2	DIN	Data In, Logic Input. Data to be written to the control register of the AD7904/AD7914/AD7924 is provided on this input and is clocked into the register on the falling edge of SCLK (see the Control Register section).
3	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7904/AD7914/AD7924 and frames the serial data transfer.
4, 8, 13, 16	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7904/AD7914/AD7924. All analog input signals and any external reference signal should be referred to this AGND voltage. All AGND pins should be connected together.
5, 6	AV_{DD}	Analog Power Supply Input. The AV_{DD} range for the AD7904/AD7914/AD7924 is from 2.7 V to 5.25 V. For the 0 V to 2 × REF_{IN} range, AV_{DD} should be from 4.75 V to 5.25 V.
7	REF_{IN}	Reference Input for the AD7904/AD7914/AD7924. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V ± 1% for specified performance.
9, 10, 11, 12	$V_{IN}3$, $V_{IN}2$, $V_{IN}1$, $V_{IN}0$	Analog Input 0 through Analog Input 3. The four single-ended analog input channels are multiplexed into the on-chip track-and-hold. The analog input channel to be converted is selected using the address bits ADD1 and ADD0 of the control register. The address bits, in conjunction with the SEQ1 and SEQ0 bits, allow the sequencer to be programmed. The input range for all input channels can extend from 0 V to REF_{IN} or from 0 V to 2 × REF_{IN} as selected via the RANGE bit in the control register. Any unused input channels should be connected to AGND to avoid noise pickup.
14	DOUT	Data Out, Logic Output. The conversion result from the AD7904/AD7914/AD7924 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7904 consists of two leading zeros, two address bits indicating which channel the conversion result corresponds to, followed by the eight bits of conversion data, followed by four trailing zeros, provided MSB first. The data stream from the AD7914 consists of two leading zeros, two address bits indicating which channel the conversion result corresponds to, followed by the 10 bits of conversion data, followed by two trailing zeros, provided MSB first. The data stream from the AD7924 consists of two leading zeros, two address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data, provided MSB first. The output coding can be selected as straight binary or twos complement via the CODING bit in the control register.
15	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines the voltage at which the serial interface of the AD7904/AD7914/AD7924 operates.

TYPICAL PERFORMANCE CHARACTERISTICS

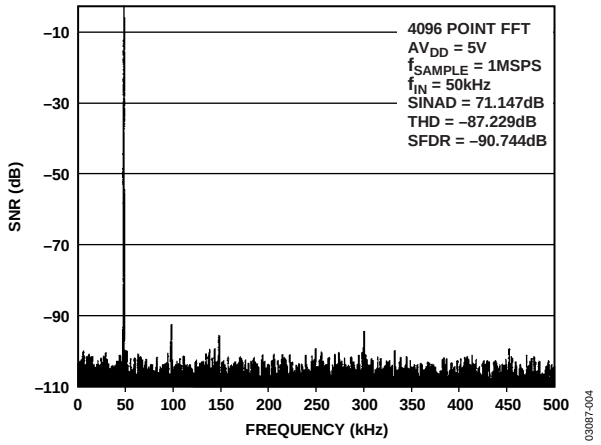

Figure 4. AD7924 Dynamic Performance at 1 MSPS

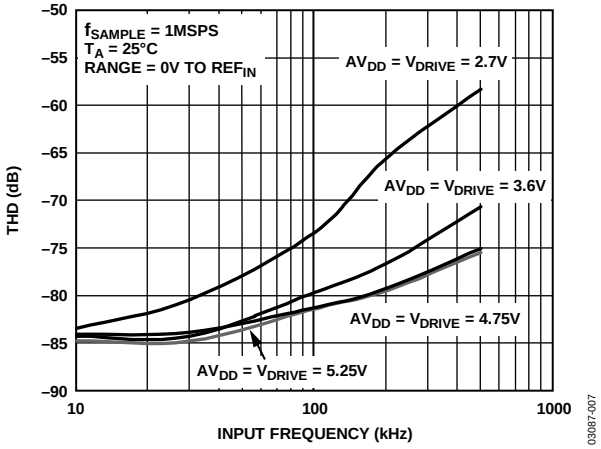

Figure 7. AD7924 THD vs. Analog Input Frequency for Various Supply Voltages at 1 MSPS

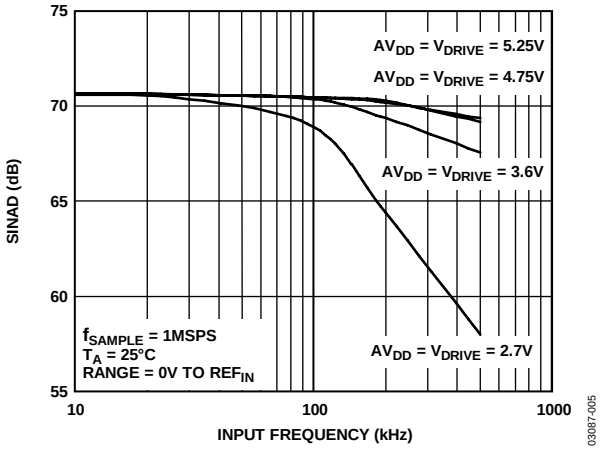

Figure 5. AD7924 SINAD vs. Analog Input Frequency for Various Supply Voltages at 1 MSPS, SCLK = 20 MHz

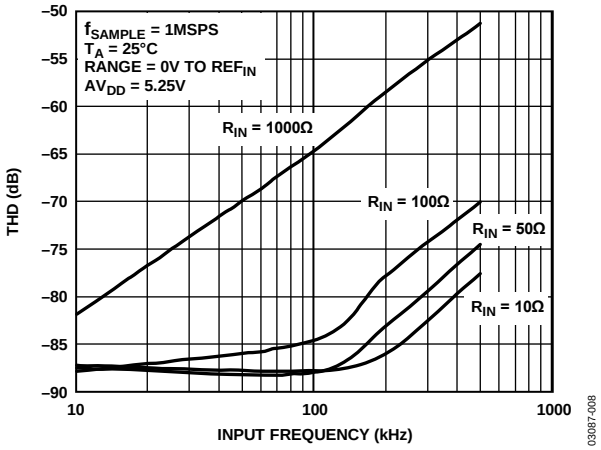

Figure 8. AD7924 THD vs. Analog Input Frequency for Various Source Impedances

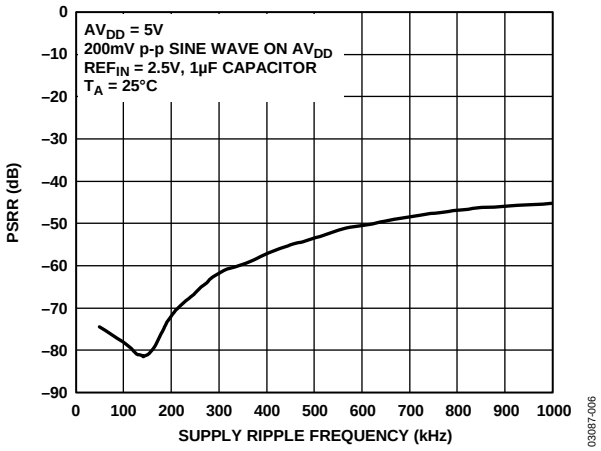

Figure 6. AD7924 PSRR vs. Supply Ripple Frequency (No Decoupling)

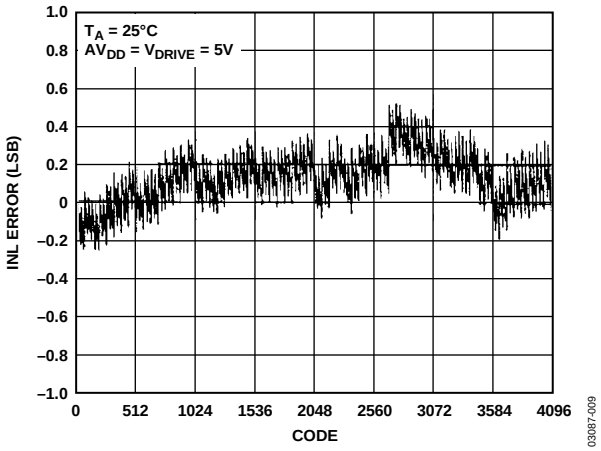

Figure 9. AD7924 Typical INL

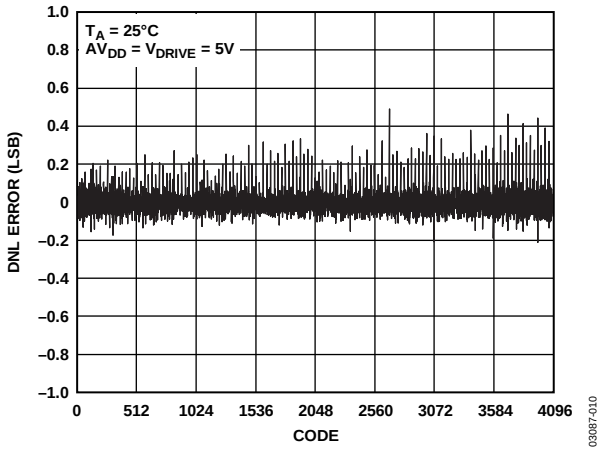

Figure 10. AD7924 Typical DNL

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
Offset error is the deviation of the first code transition (00 … 000 to 00 … 001) from the ideal, that is, AGND + 1 LSB.

Offset Error Match
Offset error match is the difference in offset error between any two channels.

Gain Error
Gain error is the deviation of the last code transition (111 … 110 to 111 … 111) from the ideal, that is, REF_{IN} − 1 LSB, after the offset error has been adjusted out.

Gain Error Match
Gain error match is the difference in gain error between any two channels.

Zero Code Error
Zero code error is the deviation of the midscale transition (all 0s to all 1s) from the ideal V_{IN} voltage, that is, REF_{IN} − 1 LSB. It applies when using the twos complement output coding option with the 2 × REF_{IN} input range (−REF_{IN} to +REF_{IN} biased about the REF_{IN} point).

Zero Code Error Match
Zero code error match is the difference in zero code error between any two channels.

Positive Gain Error
Positive gain error is the deviation of the last code transition (011 … 110 to 011 … 111) from the ideal, that is, +REF_{IN} − 1 LSB, after the zero code error is adjusted out. It applies when using the twos complement output coding option with the 2 × REF_{IN} input range (−REF_{IN} to +REF_{IN} biased about the REF_{IN} point).

Positive Gain Error Match
Positive gain error match is the difference in positive gain error between any two channels.

Negative Gain Error
Negative gain error is the deviation of the first code transition (100 … 000 to 100 … 001) from the ideal, that is, −REF_{IN} + 1 LSB, after the zero code error is adjusted out. It applies when using the twos complement output coding option with the 2 × REF_{IN} input range (−REF_{IN} to +REF_{IN} biased about the REF_{IN} point).

Negative Gain Error Match
Negative gain error match is the difference in negative gain error between any two channels.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 400 kHz sine wave signal to all three nonselected input channels and determining how much that signal is attenuated in the selected channel with a 50 kHz signal. The figure is given worst case across all four channels for the AD7904/AD7914/AD7924.

Power Supply Rejection (PSR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value (see Figure 6).

Power Supply Rejection Ratio (PSRR)

PSRR is the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200 mV p-p sine wave applied to the ADC AV_{DD} supply of frequency f_S.

$$PSRR(\text{dB}) = 10 \log(Pf/Pfs)$$

where:
Pf is the power at frequency f in the ADC output.
Pf_S is the power at frequency f_S coupled onto the ADC AV_{DD} supply.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of a conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of a conversion.

Signal to (Noise + Distortion) (SINAD) Ratio
SINAD is the measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f_S/2), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical SINAD ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\ to\ (Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

Thus, for a 12-bit converter, SINAD is 74 dB, for a 10-bit converter, it is 62 dB, and for an 8-bit converter, it is 50 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7904/AD7914/AD7924, it is defined as

$$THD(\text{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

CONTROL REGISTER

The control register of the AD7904/AD7914/AD7924 is a 12-bit, write-only register. Data is loaded from the DIN pin of the AD7904/AD7914/AD7924 on the falling edge of SCLK. The data is transferred on the DIN line at the same time that the conversion result is read from the part. The data transferred on the DIN line corresponds to the AD7904/AD7914/AD7924 configuration for the next conversion. This requires 16 serial clocks for every data transfer. Only the information provided on the first 12 falling clock edges (after the $\overline{CS}$ falling edge) is loaded to the control register. MSB denotes the first bit in the data stream. The bit functions are outlined in Table 8.

Table 7. Channel Selection

ADD1	ADD0	Analog Input Channel
0	0	$V_{IN}0$
0	1	$V_{IN}1$
1	0	$V_{IN}2$
1	1	$V_{IN}3$

Table 8. Control Register Bit Functions

MSB											LSB
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WRITE	SEQ1	DONTC	DONTC	ADD1	ADD0	PM1	PM0	SEQ0	DONTC	RANGE	CODING

Bit	Mnemonic	Description
11	WRITE	The value written to this bit determines whether the following 11 bits will be loaded to the control register. If this bit is set to 1, the following 11 bits will be written to the control register; if this bit is set to 0, the remaining 11 bits are not loaded to the control register, which remains unchanged.
10	SEQ1	The SEQ1 bit is used in conjunction with the SEQ0 bit to control the use of the sequencer function (see Table 10).
[9:8]	DONTC	Don't care bits.
[7:6]	ADD1, ADD0	The two address bits are loaded at the end of the present conversion sequence and select which analog input channel is to be converted in the next serial transfer, or they may select the final channel in a consecutive sequence as described in Table 10. The selected input channel is decoded as shown in Table 7. The address bits corresponding to the conversion result are also output on DOUT prior to the 12 bits of data (see the Serial Interface section). The next channel to be converted on will be selected by the mux on the 14th SCLK falling edge.
[5:4]	PM1, PM0	The two power management bits decode the mode of operation of the AD7904/AD7914/AD7924 as described in Table 9.
3	SEQ0	The SEQ0 bit is used in conjunction with the SEQ1 bit to control the use of the sequencer function (see Table 10).
2	DONTC	Don't care bit.
1	RANGE	This bit selects the analog input range to be used on the AD7904/AD7914/AD7924. If it is set to 0, the analog input range will extend from 0 V to 2 × REF_{IN}. If it is set to 1, the analog input range will extend from 0 V to REF_{IN} (for the next conversion). For the 0 V to 2 × REF_{IN} input range, V_{DD} = 4.75 V to 5.25 V.
0	CODING	This bit selects the type of output coding that the AD7904/AD7914/AD7924 will use for the conversion result. If this bit is set to 0, the output coding for the part will be twos complement. If this bit is set to 1, the output coding from the part will be straight binary (for the next conversion).

Table 9. Power Mode Selection

PM1	PM0	Mode	Description
1	1	Normal operation	In normal operation mode, the AD7904/AD7914/AD7924 remain in full power mode regardless of the status of any of the logic inputs. This mode allows the fastest possible throughput rate from the AD7904/AD7914/AD7924.
1	0	Full shutdown	In full shutdown mode, the AD7904/AD7914/AD7924 are in full shutdown with all circuitry on the device powering down. The AD7904/AD7914/AD7924 retain the information in the control register while in full shutdown. The part remains in full shutdown until these bits are changed.
0	1	Auto shutdown	In auto shutdown mode, the AD7904/AD7914/AD7924 automatically enter full shutdown mode at the end of each conversion when the control register is updated. Wake-up time from full shutdown is 1 µs; the user should ensure that 1 µs has elapsed before attempting to perform a valid conversion on the part in this mode.
0	0	Invalid	Invalid selection. This configuration is not allowed.

SEQUENCER OPERATION

The SEQ1 and SEQ0 bits in the control register allow the user to select a mode of operation for the sequencer function. Table 10 outlines the three modes of operation of the sequencer.

Figure 11 shows the traditional operation of a multichannel ADC, where each serial transfer selects the next channel for conversion. In this mode of operation, the sequencer function is not used.

Figure 12 shows how to program the AD7904/AD7914/AD7924 to continuously convert on a sequence of consecutive channels from Channel 0 to a selected final channel. To exit this mode of operation and revert to the traditional mode of operation of a multichannel ADC (as shown in Figure 11), ensure that the WRITE bit = 1 and SEQ1 = SEQ0 = 0 on the next serial transfer.

Table 10. Sequence Selection

SEQ1	SEQ0	Sequencer Function	Description
0	X	Not used	The sequencer function is not used. The analog input channel selected for each individual conversion is determined by the contents of the channel address bits, ADD1 and ADD0, in each previous write operation. This mode of operation reflects the traditional operation of a multichannel ADC, without using the sequencer function, where each write to the AD7904/AD7914/AD7924 selects the next channel for conversion (see Figure 11).
1	0	Used (not interrupted upon completion)	The sequencer function is not interrupted upon completion of the write operation. This configuration allows other bits in the control register to be altered between conversions while in a sequence without terminating the cycle.
1	1	Continuous conversions	This configuration is used in conjunction with the channel address bits, ADD1 and ADD0, to program continuous conversions on a consecutive sequence of channels from Channel 0 to a selected final channel that is specified by the channel address bits in the control register (see Figure 12).

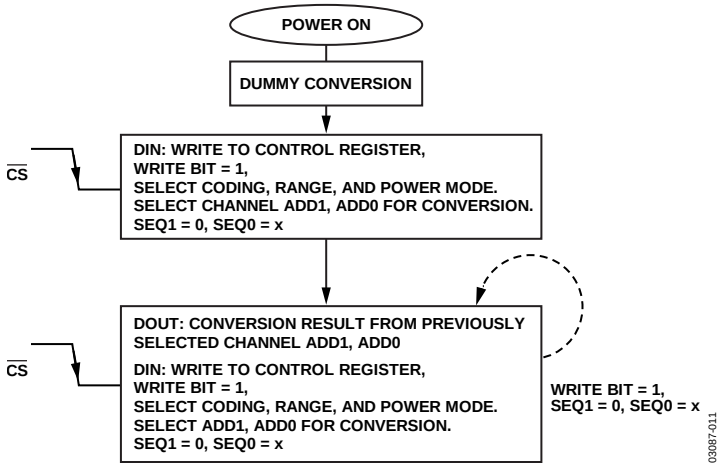

Figure 11. SEQ1 Bit = 0, SEQ0 Bit = x Flowchart

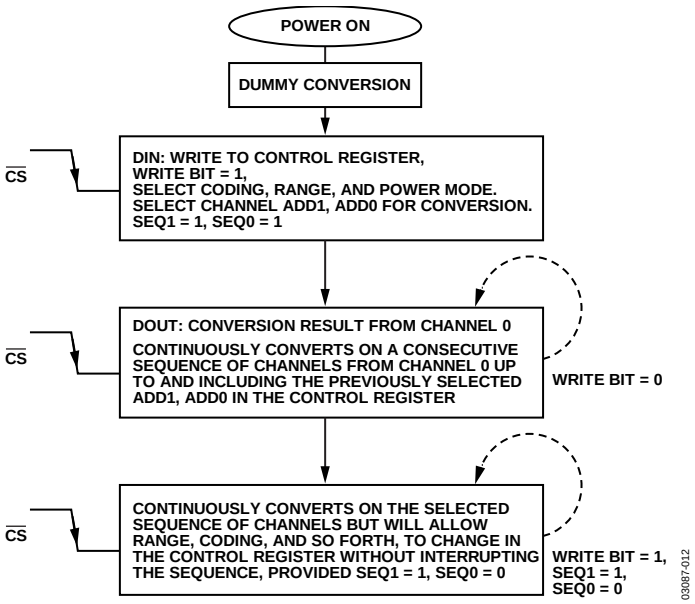

Figure 12. SEQ1 Bit = 1, SEQ0 Bit = 1 Flowchart

CIRCUIT INFORMATION

The AD7904/AD7914/AD7924 are, respectively, 8-bit, 10-bit, and 12-bit, high speed, 4-channel, single-supply ADCs. The parts can be operated from a 2.7 V to 5.25 V supply. When operated from either a 5 V or 3 V supply, the AD7904/AD7914/AD7924 are capable of throughput rates of 1 MSPS when provided with a 20 MHz clock.

The AD7904/AD7914/AD7924 provide the user with an on-chip track-and-hold ADC and serial interface housed in a 16-lead TSSOP package. The AD7904/AD7914/AD7924 each have four single-ended input channels with a channel sequencer, allowing the user to select a channel sequence through which the ADC can cycle with each consecutive $\overline{CS}$ falling edge. The serial clock input accesses data from the part, controls the transfer of data written to the ADC, and provides the clock source for the successive approximation ADC. The analog input range for the AD7904/AD7914/AD7924 is 0 V to REF_{IN} or 0 V to 2 × REF_{IN}, depending on the status of Bit 1 in the control register. For the 0 V to 2 × REF_{IN} range, the part must be operated from a 4.75 V to 5.25 V supply.

The AD7904/AD7914/AD7924 provide flexible power management options to allow the user to achieve the best power performance for a given throughput rate. These options are selected by programming the power management bits, PM1 and PM0, in the control register.

CONVERTER OPERATION

The AD7904/AD7914/AD7924 are 8-, 10-, and 12-bit SAR ADCs, respectively, based around a capacitive DAC. The AD7904/AD7914/AD7924 can convert analog input signals in the range of 0 V to REF_{IN} or 0 V to 2 × REF_{IN}. Figure 13 and Figure 14 show simplified schematics of the ADC. The AD7904/AD7914/AD7924 include control logic, the SAR ADC, and a capacitive DAC, which are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 13 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on the selected V_{IN} channel.

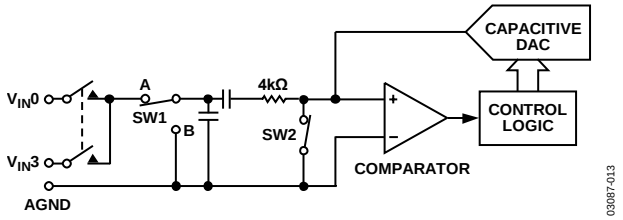

Figure 13. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 14), SW2 opens and SW1 moves to position B, causing the comparator to become unbalanced. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 16 and Figure 17 show the ADC transfer functions.

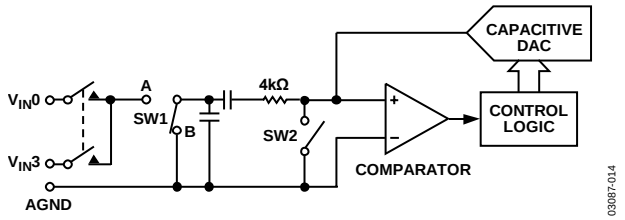

Figure 14. ADC Conversion Phase

Analog Input

Figure 15 shows an equivalent circuit of the analog input structure of the AD7904/AD7914/AD7924. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200 mV. This will cause these diodes to become forward-biased and start conducting current into the substrate. The maximum current that these diodes can conduct without causing irreversible damage to the part is 10 mA.

Capacitor C1 in Figure 15 is typically about 4 pF and can primarily be attributed to pin capacitance. The resistor, R1, is a lumped component made up of the on resistance of a track-and-hold switch and the on resistance of the input multiplexer. The total resistance is typically about 400 Ω. Capacitor C2 is the ADC sampling capacitor and has a capacitance of 30 pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended by use of a low-pass RC filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases, and performance will degrade (see Figure 8).

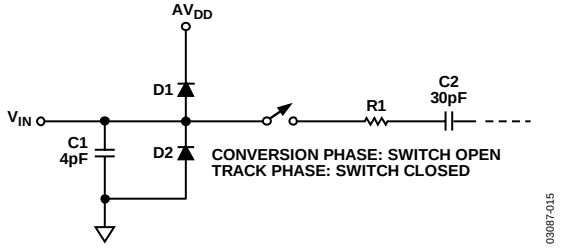

Figure 15. Equivalent Analog Input Circuit

ADC TRANSFER FUNCTION

The output coding of the AD7904/AD7914/AD7924 is either straight binary or twos complement, depending on the status of the LSB in the control register. The designed code transitions occur at successive LSB values (that is, 1 LSB, 2 LSBs, and so on). For the 0 V to REF_{IN} input range, the LSB size is $REF_{IN}/256$ for the AD7904, $REF_{IN}/1024$ for the AD7914, and $REF_{IN}/4096$ for the AD7924. For the 0 V to 2 × REF_{IN} input range, the LSB size is 2 × $REF_{IN}/256$ for the AD7904, 2 × $REF_{IN}/1024$ for the AD7914, and 2 × $REF_{IN}/4096$ for the AD7924. The ideal transfer characteristic for the AD7904/AD7914/AD7924 when straight binary coding is selected is shown in Figure 16; the ideal transfer characteristic for the AD7904/AD7914/AD7924 when twos complement coding is selected is shown in Figure 17.

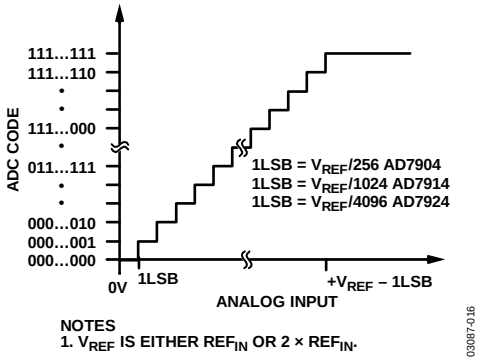

Figure 16. Straight Binary Transfer Characteristic

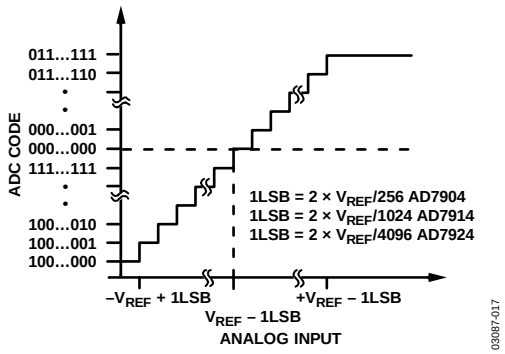

Figure 17. Twos Complement Transfer Characteristic with 0 V to 2 × REF_{IN} Input Range

Handling Bipolar Input Signals

Figure 18 shows how the combination of the 0 V to 2 × REF_{IN} input range and the twos complement output coding scheme is particularly useful for handling bipolar input signals. If the bipolar input signal is biased about REF_{IN} and twos complement output coding is selected, REF_{IN} becomes the zero code point, $-REF_{IN}$ is negative full scale, and $+REF_{IN}$ becomes positive full scale, with a dynamic range of 2 × REF_{IN}.

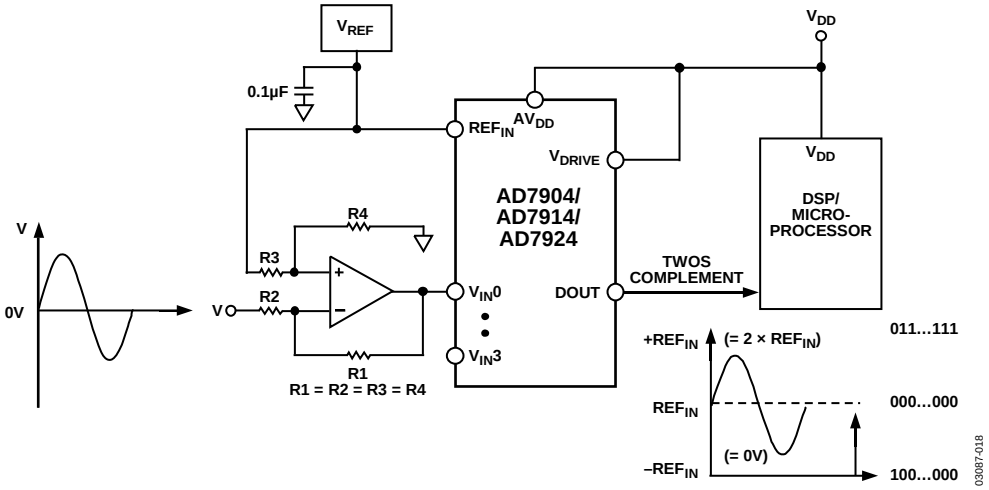

Figure 18. Handling Bipolar Signals

TYPICAL CONNECTION DIAGRAM

Figure 19 shows a typical connection diagram for the AD7904/AD7914/AD7924. In this setup, the AGND pin is connected to the analog ground plane of the system. In Figure 19, the REF_{IN} pin is connected to a decoupled 2.5 V supply from a reference source, the AD780, to provide an analog input range of 0 V to 2.5 V (if the RANGE bit is set to 1) or 0 V to 5 V (if the RANGE bit is set to 0).

Although the AD7904/AD7914/AD7924 are connected to a V_{DD} of 5 V, the serial interface is connected to a 3 V microprocessor. The V_{DRIVE} pin of the AD7904/AD7914/AD7924 is connected to the same 3 V supply as the microprocessor to allow a 3 V logic interface (see the Digital Inputs section). The conversion result is output in a 16-bit word. This 16-bit data stream consists of two leading zeros, two address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data for the AD7924 (10 bits of data for the AD7914 and 8 bits of data for the AD7904, each followed by two and four trailing zeros, respectively). For applications where power consumption is of concern, the power-down modes should be used between conversions or bursts of several conversions to improve power performance (see the Modes of Operation section).

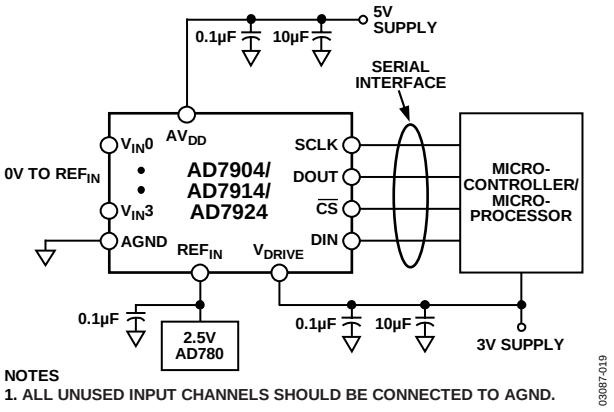

Figure 19. Typical Connection Diagram

Analog Input Selection

Any one of four analog input channels can be selected for conversion by programming the multiplexer with the address bits ADD1 and ADD0 in the control register. The channel configurations are shown in Table 7.

The AD7904/AD7914/AD7924 can also be configured to automatically cycle through a number of selected channels. The sequencer feature is accessed via the SEQ1 and SEQ0 bits in the control register (see Table 10). The AD7904/AD7914/AD7924 can be programmed to continuously convert on a number of consecutive channels in ascending order from Channel 0 to a selected final channel as determined by the channel address bits, ADD1 and ADD0. This is possible if the SEQ1 and SEQ0 bits are set to 11. The next serial transfer will then act on the sequence programmed by executing a conversion on Channel 0. The next serial transfer will result in a conversion on Channel 1, and so on, until the channel selected via the address bits, ADD1 and ADD0, is reached.

It is not necessary to write to the control register again after a sequence operation has been initiated. To ensure that the control register is not accidently overwritten or the sequence operation interrupted, the WRITE bit must be set to 0 or the DIN line must be tied low. If the control register is written to at any time during the sequence, the SEQ1 and SEQ0 bits must be set to 10 to avoid interrupting the automatic conversion sequence. This pattern continues until the AD7904/AD7914/AD7924 are written to and the SEQ1 and SEQ0 bits are configured with a bit combination other than 10, resulting in the termination of the sequence. If the sequence is uninterrupted (WRITE bit = 0, or WRITE bit = 1 and SEQ1 and SEQ0 bits are set to 10), then upon completion of the sequence, the AD7904/AD7914/AD7924 sequencer returns to Channel 0 and restarts the sequence.

Regardless of the channel selection method used, the 16-bit word output from the AD7924 during each conversion always contains two leading zeros, two channel address bits that the conversion result corresponds to, followed by the 12-bit conversion result; the AD7914 outputs two leading zeros, two channel address bits that the conversion result corresponds to, followed by the 10-bit conversion result and two trailing zeros; the AD7904 outputs two leading zeros, two channel address bits that the conversion result corresponds to, followed by the 8-bit conversion result and four trailing zeros (see the Serial Interface section).

Digital Inputs

The digital inputs applied to the AD7904/AD7914/AD7924 can go to 7 V and are not restricted by the AV_{DD} + 0.3 V limit on the analog inputs.

Because the SCLK, DIN, and $\overline{CS}$ inputs are not restricted by the AV_{DD} + 0.3 V limit, power supply sequencing issues are avoided. If $\overline{CS}$, DIN, or SCLK is applied before AV_{DD}, there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V is applied prior to AV_{DD}.

V_{DRIVE}

The AD7904/AD7914/AD7924 also include the V_{DRIVE} feature. V_{DRIVE} controls the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7904/AD7914/AD7924 are operated with a V_{DD} of 5 V, the V_{DRIVE} pin can be powered from a 3 V supply. The AD7904/AD7914/AD7924 have better dynamic performance with a V_{DD} of 5 V while still being able to interface to 3 V processors. Care should be taken to ensure that V_{DRIVE} does not exceed AV_{DD} by more than 0.3 V (see the Absolute Maximum Ratings section).

Reference

An external reference source should be used to supply the 2.5 V reference to the AD7904/AD7914/AD7924. Errors in the reference source result in gain errors in the AD7904/AD7914/AD7924 transfer function and add to the specified full-scale errors of the part. A capacitor of at least 0.1 µF should be placed on the REF_{IN} pin. Suitable reference sources for the AD7904/AD7914/AD7924 include the AD780, REF193, and AD1582.

If 2.5 V is applied to the REF_{IN} pin, the analog input range can be either 0 V to 2.5 V or 0 V to 5 V, depending on the setting of the RANGE bit in the control register.

MODES OF OPERATION

The AD7904/AD7914/AD7924 have three modes of operation. These modes are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements. The mode of operation of the AD7904/AD7914/AD7924 is controlled by the power management bits, PM1 and PM0, in the control register (see Table 9). When power supplies are first applied to the AD7904/AD7914/AD7924, care should be taken to ensure that the part is placed in the required mode of operation (see the Powering Up the AD7904/AD7914/AD7924 section).

NORMAL MODE (PM1 = PM0 = 1)

Normal mode is intended for the fastest throughput rate performance. Because the AD7904/AD7914/AD7924 remain fully powered up at all times, the user does not need to worry about power-up times. Figure 20 shows the general diagram of the operation of the AD7904/AD7914/AD7924 in this mode.

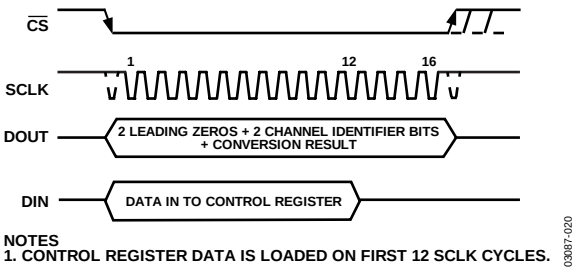

Figure 20. Normal Mode Operation

The conversion is initiated on the falling edge of $\overline{CS}$; the track-and-hold enters hold mode as described in the Serial Interface section. The data presented to the AD7904/AD7914/AD7924 on the DIN line during the first 12 clock cycles of the data transfer is loaded into the control register (provided that the WRITE bit is set to 1). In normal mode, the part remains fully powered up at the end of the conversion as long as the PM1 and PM0 bits are set to 1 in the write transfer during that same conversion. To ensure continued operation in normal mode, PM1 and PM0 must both be set to 1 on every data transfer, assuming that a write operation is taking place. If the WRITE bit is set to 0, the power management bits are left unchanged, and the part remains in normal mode.

Sixteen serial clock cycles are required to complete the conversion and to access the conversion result. The track-and-hold returns to track mode on the 14th SCLK falling edge. $\overline{CS}$ may then idle high until the next conversion or it may idle low until some time prior to the next conversion (effectively idling $\overline{CS}$ low).

When a data transfer is complete (DOUT has returned to three-state), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

FULL SHUTDOWN MODE (PM1 = 1, PM0 = 0)

In full shutdown mode, all internal circuitry on the AD7904/AD7914/AD7924 is powered down. The part retains information in the control register during full shutdown. The AD7904/AD7914/AD7924 remain in full shutdown until the power management bits in the control register, PM1 and PM0, are changed.

If a write to the control register occurs while the part is in full shutdown, and the power management bits are changed to PM0 = PM1 = 1 (that is, normal mode), the part will begin to power up on the $\overline{CS}$ rising edge. The track-and-hold, which was in hold mode while the part was in full shutdown, returns to track mode on the 14th SCLK falling edge.

To ensure that the part is fully powered up, $t_{POWER-UP}$ (t_{12}) should have elapsed before the next $\overline{CS}$ falling edge. Figure 21 shows the general diagram for this sequence.

AUTO SHUTDOWN MODE (PM1 = 0, PM0 = 1)

In auto shutdown mode, the AD7904/AD7914/AD7924 automatically enter shutdown at the end of each conversion when the control register is updated. When the part is in auto shutdown, the track-and-hold is in hold mode. Figure 22 shows the general diagram of the operation of the AD7904/AD7914/AD7924 in this mode.

In auto shutdown mode, all internal circuitry on the AD7904/AD7914/AD7924 is powered down. The part retains information in the control register during auto shutdown. The AD7904/AD7914/AD7924 remain in shutdown until the next $\overline{CS}$ falling edge that it receives. On this $\overline{CS}$ falling edge, the track-and-hold, which was in hold mode while the part was in shutdown, returns to track mode. Wake-up time from auto shutdown is 1 μs maximum, and the user should ensure that 1 μs has elapsed before attempting a valid conversion.

When running the AD7904/AD7914/AD7924 with a 20 MHz clock, one 16 SCLK dummy cycle should be sufficient to ensure that the part is fully powered up. During this dummy cycle, the contents of the control register should remain unchanged; therefore, the WRITE bit should be set to 0 on the DIN line. This dummy cycle effectively halves the throughput rate of the part, with every other conversion result being valid. In auto shutdown mode, the power consumption of the part is greatly reduced because the part enters shutdown at the end of each conversion. When the control register is programmed to move into auto shutdown mode, it does so at the end of the conversion. The user can move the ADC in and out of the low power state by controlling the $\overline{CS}$ signal.

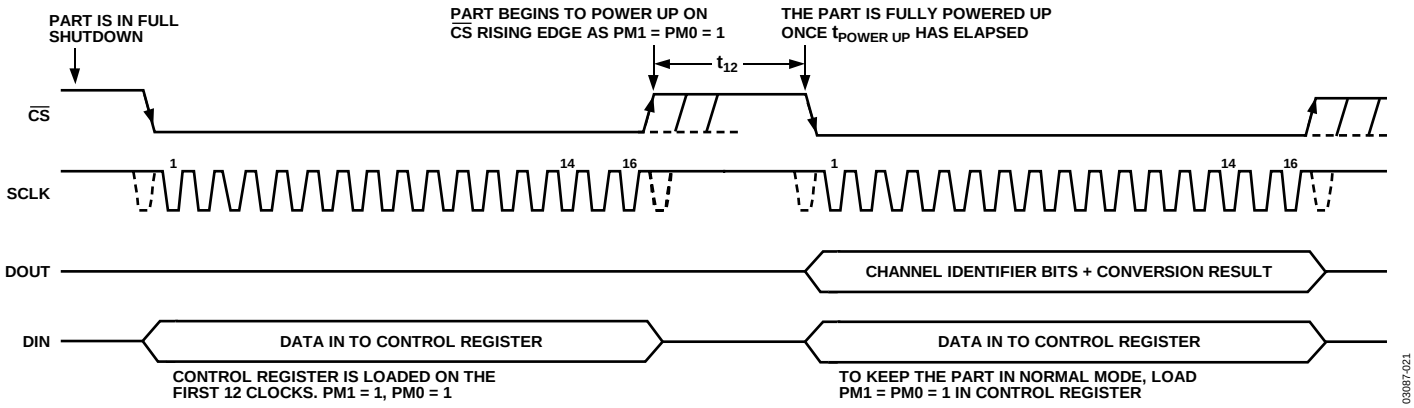

Figure 21. Full Shutdown Mode Operation

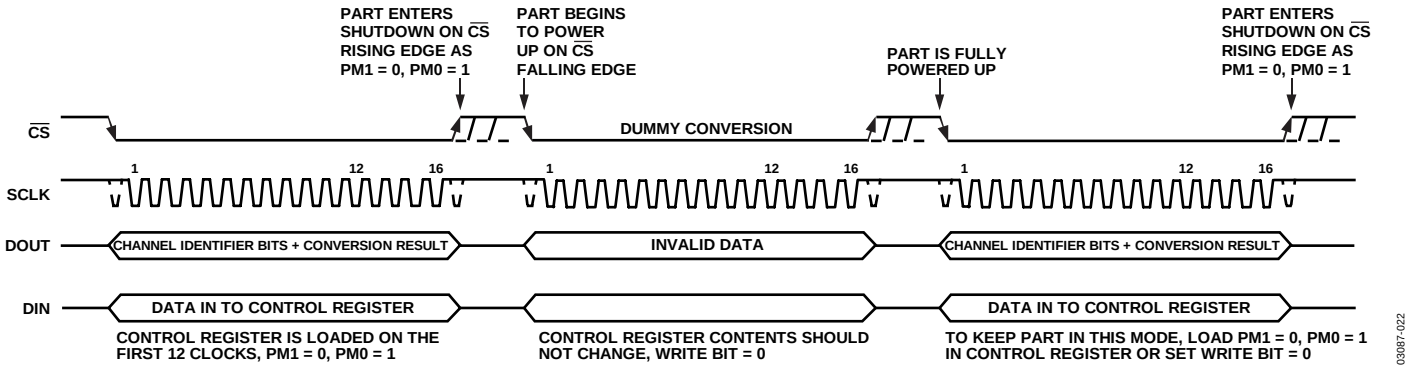

Figure 22. Auto Shutdown Mode Operation

POWERING UP THE AD7904/AD7914/AD7924

When supplies are first applied to the AD7904/AD7914/AD7924, the ADC may power up in any of the operating modes of the part. To ensure that the part is placed into the required operating mode, the user should perform a dummy cycle operation as shown in Figure 23, Figure 24, and Figure 25.

The dummy conversion operation must be performed to place the part into the desired mode of operation. To ensure that the part is in normal mode, this dummy cycle operation can be performed with the DIN line tied high, that is, the PM1 and PM0 bits are set to 11 (depending on other required settings in the control register). However, the minimum power-up time of 1 μs must be allowed from the rising edge of $\overline{CS}$, where the control register is updated, before attempting the first valid conversion. This power-up time allows for the possibility that the part was initially powered up in shutdown mode.

If the desired mode of operation is full shutdown, one dummy cycle is required after supplies are applied. In this dummy cycle, the user simply sets the power management bits, PM1 and PM0, to 10 and, upon the rising edge of $\overline{CS}$ at the end of that serial transfer, the part enters full shutdown mode.

If the desired mode of operation after supplies are applied is auto shutdown mode, two dummy cycles are required: the first dummy cycle with DIN tied high, and the second to set the power management bits, PM1 and PM0, to 01. On the second $\overline{CS}$ rising edge after the supplies are applied, the control register contains the correct information and the part enters auto shutdown mode as programmed. If power consumption is of critical concern, then in the first dummy cycle, the user can set PM1 and PM0 to 10, that is, full shutdown mode, and then place the part into auto shutdown mode in the second dummy cycle. For illustration purposes, Figure 25 is shown with DIN tied high on the first dummy cycle in this case.

Figure 23, Figure 24, and Figure 25 show the required dummy cycles after supplies are applied for normal mode, full shutdown mode, and auto shutdown mode, respectively.

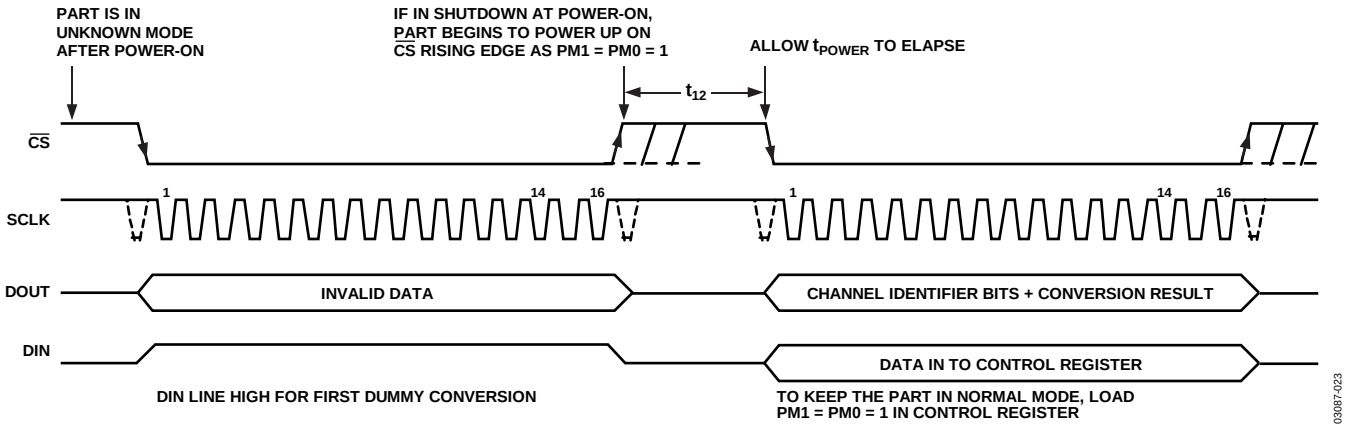

Figure 23. Placing the AD7904/AD7914/AD7924 into Normal Mode After Supplies Are First Applied

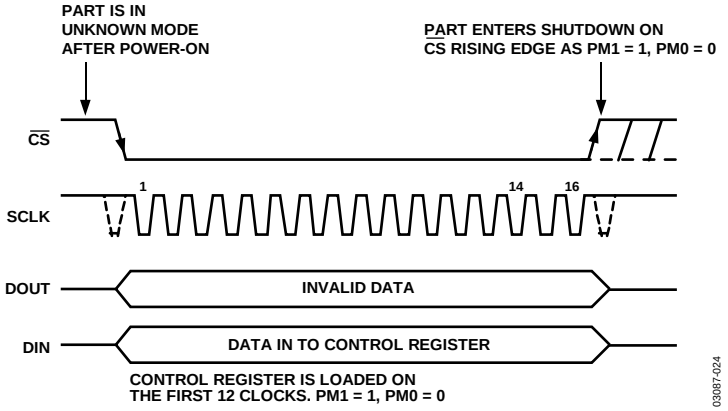

Figure 24. Placing the AD7904/AD7914/AD7924 into Full Shutdown Mode After Supplies Are First Applied

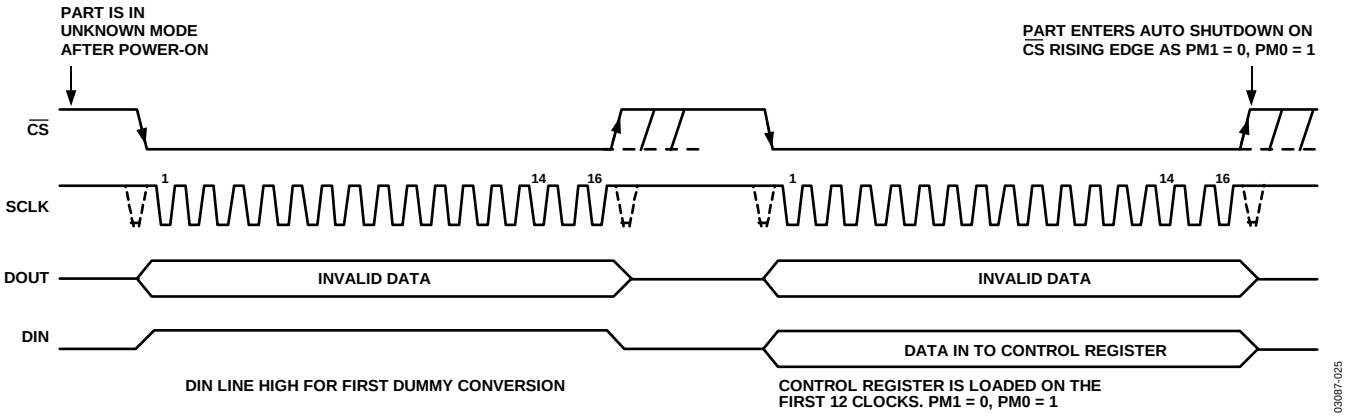

Figure 25. Placing the AD7904/AD7914/AD7924 into Auto Shutdown Mode After Supplies Are First Applied

POWER vs. THROUGHPUT RATE

By operating the AD7904/AD7914/AD7924 in auto shutdown mode, the average power consumption of the ADC decreases at lower throughput rates. Figure 26 shows how, as the throughput rate is reduced, the part remains in its shutdown state longer, and the average power consumption over time drops accordingly.

For example, if the AD7924 is operated in continuous sampling mode with a throughput rate of 100 kSPS and an SCLK of 20 MHz (AV_{DD} = 5 V), and the device is placed into auto shutdown mode (PM1 = 0 and PM0 = 1), the power consumption is calculated as described in this section.

The maximum power dissipation during normal operation is 13.5 mW (AV_{DD} = 5 V). If the power-up time from auto shutdown is one dummy cycle, that is, 1 µs, and the remaining conversion time is another cycle, that is, 1 µs, then the AD7924 can be said to dissipate 13.5 mW for 2 µs during each conversion cycle. For the remainder of the conversion cycle, 8 µs, the part remains in shutdown. The AD7924 can be said to dissipate 2.5 µW for the remaining 8 µs of the conversion cycle. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each cycle is ((2/10) × 13.5 mW) + ((8/10) × 2.5 µW) = 2.702 mW.

Figure 26 shows the maximum power vs. throughput rate when using the auto shutdown mode with 5 V and 3 V supplies.

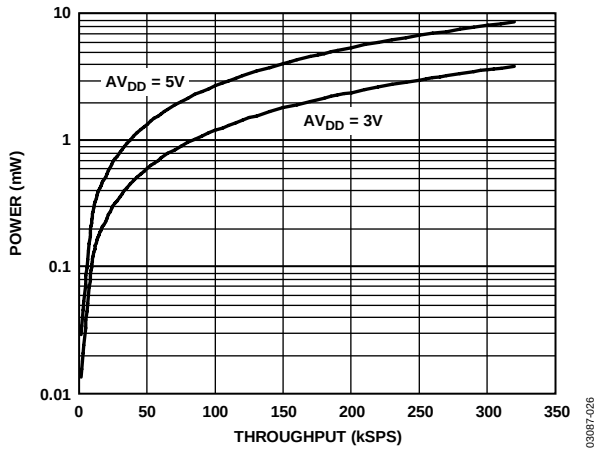

Figure 26. AD7924 Power vs. Throughput Rate

SERIAL INTERFACE

Figure 27, Figure 28, and Figure 29 show the detailed timing diagrams for serial interfacing to the AD7904, AD7914, and AD7924, respectively. The serial clock provides the conversion clock and controls the transfer of information to and from the AD7904/AD7914/AD7924 during each conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode and takes the bus out of three-state; the analog input is sampled at this point. The conversion is also initiated at this point and requires 16 SCLK cycles to complete. The track-and-hold returns to track mode on the 14th SCLK falling edge, as shown by Point B in Figure 27, Figure 28, and Figure 29. On the 16th SCLK falling edge, the DOUT line returns to three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion is terminated, the DOUT line returns to three-state, and the control register is not updated; otherwise, DOUT returns to three-state on the 16th SCLK falling edge, as shown in Figure 27, Figure 28, and Figure 29.

Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7904/AD7914/AD7924. For the AD7904/AD7914/AD7924, the 8/10/12 bits of data are preceded by two leading zeros and the two channel address bits, ADD1 and ADD0, which identify the channel that the result corresponds to. $\overline{CS}$ going low clocks out the first leading zero to be read in by the microcontroller or DSP on the first falling edge of SCLK. The first falling edge of SCLK also clocks out the second leading zero to be read in by the microcontroller or DSP on the second SCLK falling edge, and so on. The two address bits and the 8/10/12 data bits are then clocked out by subsequent SCLK falling edges beginning with the first address bit, ADD1; thus, the second falling clock edge on the serial clock has the second leading zero provided and also clocks out the address bit ADD1. The final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge.

The writing of information to the control register takes place on the first 12 falling edges of SCLK in a data transfer, assuming that the MSB (the WRITE bit) has been set to 1.

The AD7904 outputs two leading zeros, two channel address bits that the conversion result corresponds to, followed by the 8-bit conversion result and four trailing zeros. The AD7914 outputs two leading zeros, two channel address bits that the conversion result corresponds to, followed by the 10-bit conversion result and two trailing zeros. The 16-bit word read from the AD7924 always contains two leading zeros, two channel address bits that the conversion result corresponds to, followed by the 12-bit conversion result.

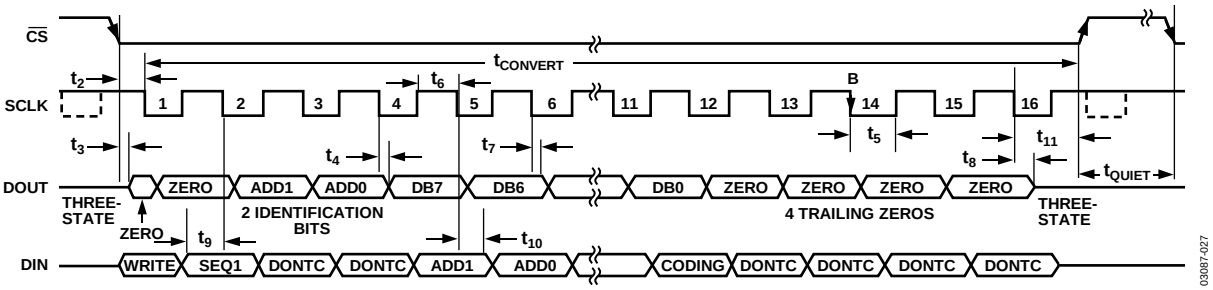

Figure 27. AD7904 Serial Interface Timing Diagram

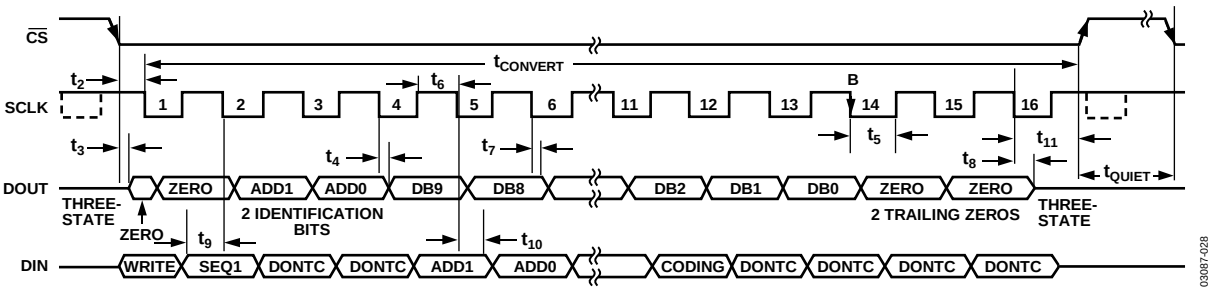

Figure 28. AD7914 Serial Interface Timing Diagram

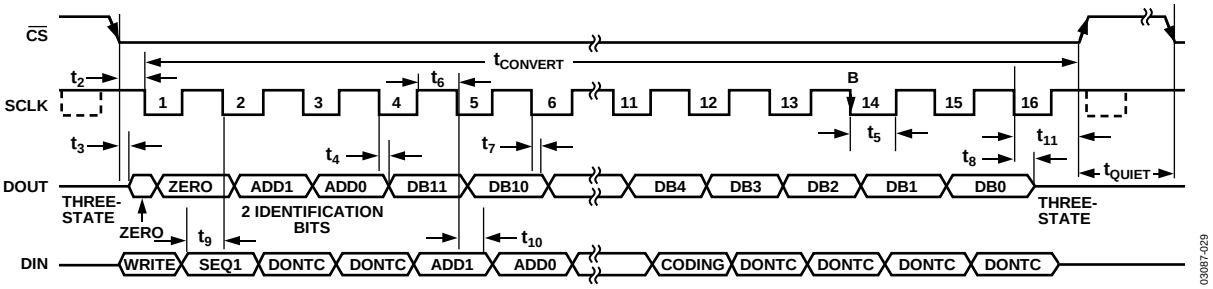

Figure 29. AD7924 Serial Interface Timing Diagram

APPLICATIONS INFORMATION

MICROPROCESSOR INTERFACING

The serial interface of the AD7904/AD7914/AD7924 allows the part to be directly connected to a range of different microprocessors. This section explains how to interface the AD7904/AD7914/AD7924 to some of the more common microcontroller and DSP serial interface protocols.

AD7904/AD7914/AD7924 to TMS320C541

The serial interface of the TMS320C541 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices such as the AD7904/AD7914/AD7924. The $\overline{CS}$ input allows easy interfacing between the TMS320C541 and the AD7904/AD7914/AD7924 without any glue logic required. The serial port of the TMS320C541 is set up to operate in burst mode with internal CLKX0 (TX serial clock on Serial Port 0) and FSX0 (TX frame sync from Serial Port 0). The serial port control (SPC) register must have the following setup: FO = 0, FSM = 1, MCM = 1, and TXM = 1. The connection diagram is shown in Figure 30. Note that for signal processing applications, it is imperative that the frame synchronization signal from the TMS320C541 provide equidistant sampling. The V_{DRIVE} pin of the AD7904/AD7914/AD7924 takes the same supply voltage as the TMS320C541. This allows the ADC to operate at a higher voltage than the serial interface, that is, the TMS320C541, if necessary.

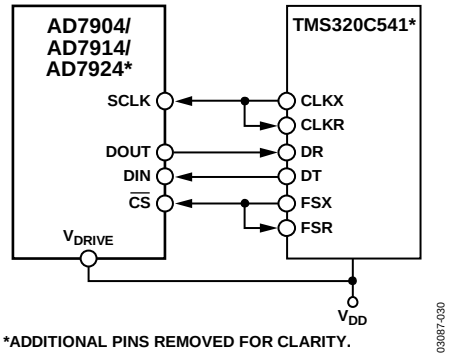

Figure 30. Interfacing to the TMS320C541

AD7904/AD7914/AD7924 to ADSP-218x

The ADSP-218x family of DSPs interfaces directly to the AD7904/AD7914/AD7924 without any glue logic required. The V_{DRIVE} pin of the AD7904/AD7914/AD7924 takes the same supply voltage as the ADSP-218x. This allows the ADC to operate at a higher voltage than the serial interface, that is, the ADSP-218x, if necessary.

The SPORT0 control register of the ADSP-218x should be set up as follows:

TFSW = RFSW = 1, alternate framing
INVRFS = INVTFS = 1, active low frame signal
DTYPE = 00, right justify data
SLEN = 1111, 16-bit data-words
ISCLK = 1, internal serial clock
TFSR = RFSR = 1, frame every word
IRFS = 0
ITFS = 1

The connection diagram is shown in Figure 31. The ADSP-218x has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in alternate framing mode and the SPORT0 control register is set up as described. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$ and, as with all signal processing applications, equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC, and under certain conditions equidistant sampling may not be achieved.

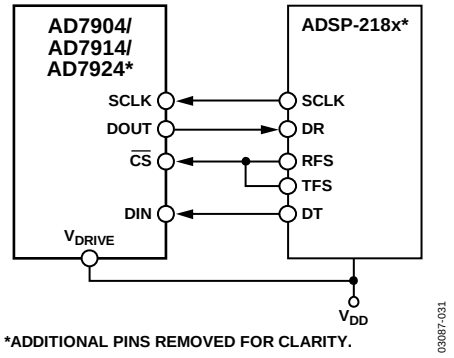

Figure 31. Interfacing to the ADSP-218x

The timer register, for example, is loaded with a value that provides an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and thus the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given (that is, AX0 = TX0), the state of the SCLK is checked. The DSP waits until SCLK goes high, low, and high again before transmission starts. If the timer and SCLK values are chosen in such a way that the instruction to transmit occurs on or near the rising edge of SCLK, the data may be transmitted or it may wait until the next clock edge.

For example, if the ADSP-2189 has a 20 MHz crystal so that its master clock frequency is 40 MHz, then the master cycle time is 25 ns. If the SCLKDIV register is loaded with the value 3, then an SCLK of 5 MHz is obtained and eight master clock periods elapse for every one SCLK period.

Depending on the throughput rate selected, if the timer register is loaded with a value such as 803 (803 + 1 = 804), then 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This setup results in nonequidistant sampling because the transmit instruction occurs on an SCLK edge. If the number of SCLKs between interrupts is a whole integer value N, equidistant sampling is implemented by the DSP.

AD7904/AD7914/AD7924 to DSP563xx

The connection diagram in Figure 32 shows how the AD7904/AD7914/AD7924 can be connected to the ESSI (synchronous serial interface) of the DSP563xx family of DSPs from Motorola. Each ESSI (two on board) is operated in synchronous mode (SYN bit in CRB = 1) with internally generated 1-bit clock period frame sync for both Tx and Rx (bits FSL1 = 0 and FSL0 = 0 in CRB). Normal operation of the ESSI is selected by setting MOD = 0 in the CRB. Set the word length to 16 by setting bits WL1 = 1 and WL0 = 0 in CRA. The FSP bit in the CRB should be set to 1 so that the frame sync is negative. Note that for signal processing applications, it is imperative that the frame synchronization signal from the DSP563xx provide equidistant sampling.

In the example shown in Figure 32, the serial clock is taken from the ESSI so the SCK0 pin must be set as an output (SCKD = 1). The V_{DRIVE} pin of the AD7904/AD7914/AD7924 takes the same supply voltage as the DSP563xx. This allows the ADC to operate at a higher voltage than the serial interface, that is, the DSP563xx, if necessary.

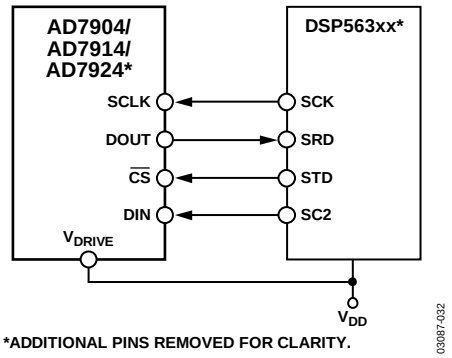

Figure 32. Interfacing to the DSP563xx

GROUNDING AND LAYOUT

The AD7904/AD7914/AD7924 have very good immunity to noise on the power supplies (see Figure 6). However, care should be taken with regard to grounding and layout.

The PCB that houses the AD7904/AD7914/AD7924 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes because it provides the best shielding. All four AGND pins of the AD7904/AD7914/AD7924 should be sunk in the AGND plane. Digital and analog ground planes should be joined at only one place. If the AD7904/AD7914/AD7924 are in a system where multiple devices require an AGND-to-DGND connection, the connection should still be made at one point only: a star ground point established as close as possible to the AD7904/AD7914/AD7924.

Avoid running digital lines under the device because these lines couple noise onto the die. The analog ground plane should be allowed to run under the AD7904/AD7914/AD7924 to avoid noise coupling. The power supply lines to the AD7904/AD7914/AD7924 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other to reduce the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 μF tantalum capacitors in parallel with 0.1 μF capacitors to AGND. To achieve the best performance from these decoupling components, place them as close as possible to the device, ideally right up against the device. The 0.1 μF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface-mount types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

OUTLINE DIMENSIONS

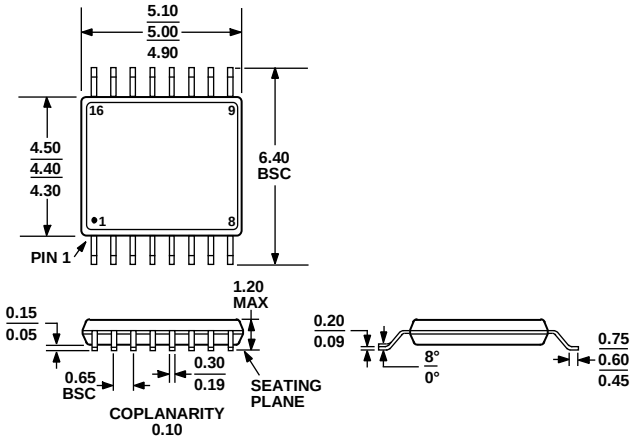

Figure 33. 16-Lead Thin Shrink Small Outline Package (TSSOP)
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Notes	Temperature Range	Linearity Error (LSB)[3]	Package Option	Package Description
AD7904BRU		−40°C to +85°C	±0.2	RU-16	16-Lead TSSOP
AD7904BRU-REEL		−40°C to +85°C	±0.2	RU-16	16-Lead TSSOP
AD7904BRUZ		−40°C to +85°C	±0.2	RU-16	16-Lead TSSOP
AD7904BRUZ-REEL		−40°C to +85°C	±0.2	RU-16	16-Lead TSSOP
AD7904BRUZ-REEL7		−40°C to +85°C	±0.2	RU-16	16-Lead TSSOP
AD7904WYRUZ-REEL7		−40°C to +125°C	±0.2	RU-16	16-Lead TSSOP
AD7914BRU-REEL		−40°C to +85°C	±0.5	RU-16	16-Lead TSSOP
AD7914BRUZ		−40°C to +85°C	±0.5	RU-16	16-Lead TSSOP
AD7914BRUZ-REEL7		−40°C to +85°C	±0.5	RU-16	16-Lead TSSOP
AD7914WYRUZ-REEL7		−40°C to +125°C	±0.5	RU-16	16-Lead TSSOP
AD7924BRU		−40°C to +85°C	±1	RU-16	16-Lead TSSOP
AD7924BRU-REEL7		−40°C to +85°C	±1	RU-16	16-Lead TSSOP
AD7924BRUZ		−40°C to +85°C	±1	RU-16	16-Lead TSSOP
AD7924BRUZ-REEL		−40°C to +85°C	±1	RU-16	16-Lead TSSOP
AD7924BRUZ-REEL7		−40°C to +85°C	±1	RU-16	16-Lead TSSOP
AD7924WYRUZ-REEL7		−40°C to +125°C	±1	RU-16	16-Lead TSSOP

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] Linearity error refers to integral linearity error.

AUTOMOTIVE PRODUCTS

The AD7904W/AD7914W/AD7924W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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