THE DATASHEET OF

ADP3808JCPZ-RL

High Efficiency Switch Mode Li-Ion Battery Charger

ADP3808

FEATURES

Selectable 3-cell or 4-cell operation
Adjustable 4.0 V to 4.5 V per cell
High end-of-charge voltage accuracy
±0.4% @ 25°C
±0.6% @ 5°C to 55°C
±0.8% @ 0°C to 100°C
Programmable charge current, including trickle charge
Bootstrapped synchronous drive for external N-channel MOSFETs
Programmable oscillator frequency

APPLICATIONS

Portable computers
Portable equipment

GENERAL DESCRIPTION

The ADP3808 is a complete Li-Ion battery charging controller for 3- or 4-cell battery packs. The device combines accurate final battery charge voltage control with constant current control to simplify the implementation of constant-current, constant-voltage (CCCV) chargers.

The final battery charge voltage is programmable between 4.0 V to 4.5 V per cell, allowing the charging of various cell types. The charge current is programmable over a wide range from trickle charging to full charging. The system current sense amplifier includes an ac adapter detection output to signal that the adapter is connected. The bootstrapped synchronous driver controls two N-channel MOSFET transistors for high efficiency charging at a low system cost.

The ADP3808 is specified over the extended commercial temperature range of 0°C to 100°C and is available in a 24-lead LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

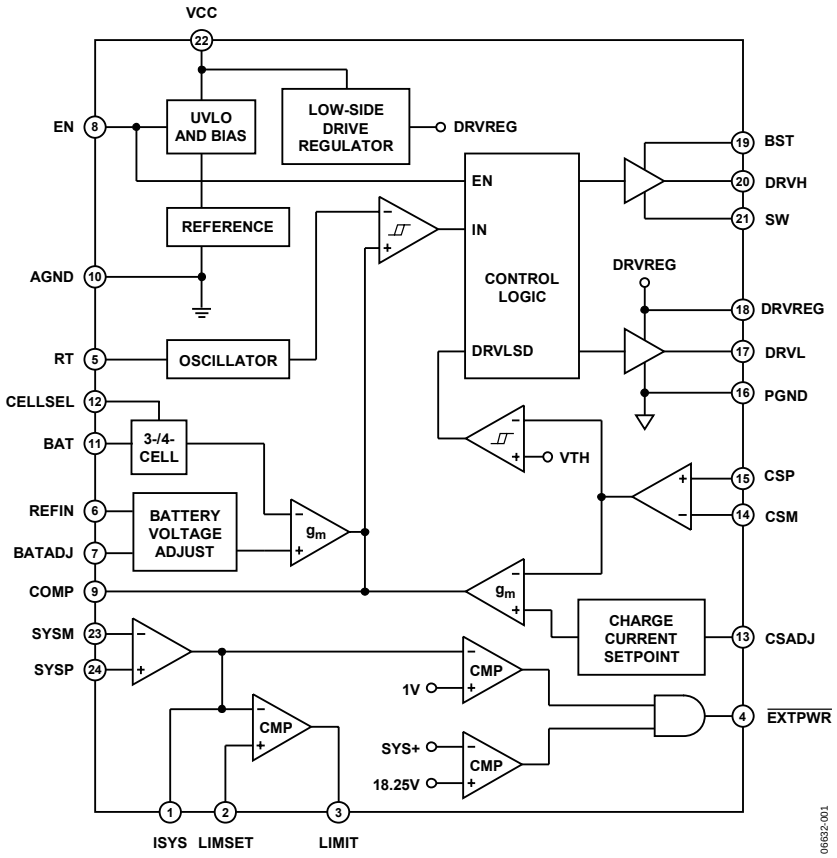

Figure 1.

Rev. 0

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REVISION HISTORY

6/07—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 20 V, EN = 5 V, REFIN = 3 V, T_A = 0°C to 100°C, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BATTERY VOLTAGE SENSING						
Accuracy	ΔV_{BAT}	T_A = 25°C, 13 V ≤ V_{CC} ≤ 21 V, BATADJ = 0 V or BATADJ = REFIN	−0.4		+0.4	%
		5°C ≤ T_A ≤ 55°C, 13 V ≤ V_{CC} ≤ 21 V, BATADJ = 0 V or BATADJ = REFIN	−0.6		+0.6	%
		13 V ≤ V_{CC} ≤ 21 V, BATADJ = 0 V or BATADJ = REFIN	−0.8		+0.8	%
Input Resistance	R_{BAT}			170		kΩ
Shutdown Leakage Current	$I_{BAT(SD)}$	EN = 0 V		0.2	1.0	µA
Overvoltage Threshold	$V_{BAT(OV)}$		120	135		%
Overvoltage Response Time	$t_{BAT(OV)}$	$V_{BAT(OV)}$ to COMP < 1 V		1		µs
BATTERY VOLTAGE ADJUST						
BATADJ Input Range	V_{BATADJ}		0		REFIN	
REFIN Input Range	V_{REFIN}		2.0		3.5	V
3-Cell Voltage Low	V_{BAT}	BATADJ = 0 V, CELLSEL = 3.3 V		12.0		V
3-Cell Voltage High	V_{BAT}	BATADJ = REFIN, CELLSEL = 3.3 V		13.5		V
4-Cell Voltage Low	V_{BAT}	BATADJ = 0 V, CELLSEL = 0 V		16.0		V
4-Cell Voltage High	V_{BAT}	BATADJ = REFIN, CELLSEL = 0 V		18.0		V
BATTERY CURRENT SENSE AMPLIFIER						
Accuracy[2]		CSADJ = REFIN, 3.9 V ≤ $V_{CS(CM)}$ ≤ 21 V	−8		+8	%
		CSADJ = 0.2 × REFIN, 3.9 V ≤ $V_{CS(CM)}$ ≤ 21 V	−20		+30	%
Input Common Mode Range	$V_{CM(CS)}$		0		V_{CC}	V
Input Bias Current—Operating	$I_{B(CSP)}$			40		µA
Input Bias Current—Shutdown	$I_{B(CSP,SD)}$	EN = 0 V		0.1	1	µA
Input Bias Current—CSM	$I_{B(CSM)}$			0.1	2	µA
Gain	$A_{V(CS)}$			31.25		V/V
CSADJ Bias Current	$I_{B(CSADJ)}$			1	2	µA
Overcurrent Threshold[2]	$V_{CS(OC)}$		90	100	110	mV
Overcurrent Response Time	t_{DC}	V_{OC} > 130 mV to COMP < 1 V		1		µs
DRVL Shutdown Threshold	$V_{CS(DRVLSD)}$			32		mV
SYSTEM CURRENT SENSE AMPLIFIER						
Input Common Mode Range	$V_{CM(SYS)}$	SYSP and SYSM to AGND	10		22	V
Input Bias Current, SYSP	$I_{B(SYSP)}$	$V_{SYS(CM)}$ = 19 V		300	400	µA
Input Bias Current, SYSM	$I_{B(SYSM)}$	$V_{SYS(CM)}$ = 19 V		0.1	1	µA
Voltage Gain		$V_{ISYS}/(V_{SYSP} - V_{SYSM})$	49.5	50	51.5	V/V
ISYS Output Current		V_{ISYS} = 2.5 V		5		µA
LIMIT Threshold	$V_{TH(LIMIT)}$	SYSP to SYSM, LIMSET = 2.5 V	48	53	58	mV
LIMSET Input Range	V_{LIMSET}		0		3.5	V
LIMIT Output Voltage Low	$V_{OL(LIMIT)}$	I_{LIMIT} = −100 µA		30	75	mV
LIMIT Propagation Delay Time	$t_{pdl(LIMIT)}$	(SYSP) – (SYSM) rising > 55 mV to LIMIT going low		1		µs
$\overline{\text{EXTPWR}}$ Current Threshold	$V_{TH(\overline{EXTPWR})}$	SYSP to SYSM	17.5	22.5	27.5	mV
$\overline{\text{EXTPWR}}$ Voltage Threshold	$V_{TH(\overline{EXTPWR})}$	SYSP to AGND	18.0	18.25	18.5	V
$\overline{\text{EXTPWR}}$ Output Voltage Low	$V_{TH(\overline{EXTPWR})}$	$I_{\overline{EXTPWR}}$ = −100 µA		5	50	mV
$\overline{\text{EXTPWR}}$ Propagation Delay Time	$t_{dpl(\overline{EXTPWR})}$	SYSP Rising > 18.5 V to $\overline{\text{EXTPWR}}$ going low		1		µs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OSCILLATOR						
Maximum Frequency	f_{OSC}			1		MHz
Frequency Variation	Δf_{OSC}	RT = 150 kΩ	250	290	340	kHz
RT Output Voltage	V_{RT}		1.9	2	2.1	V
Zero Duty Cycle Threshold		Measured at COMP		1		V
Maximum Duty Cycle Threshold		Measured at COMP		2		V
LOGIC INPUTS (EN, CELLSEL)						
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.8	V
Input Current	I_{IN}	Inputs = 0 V or 5 V	−1		+1	µA
HIGH-SIDE DRIVER						
Output Resistance, Sourcing Current		BST to SW = 5 V		3	8	Ω
Output Resistance, Sinking Current		BST to SW = 5 V		3	8	Ω
Output Resistance, Unbiased		BST to SW = 0 V		10		kΩ
Transition Time	t_{rDRVH}, t_{fDRVH}	BST to SW = 5 V, C_{LOAD} = 1 nF		20	40	ns
Propagation Delay Time	$t_{pdhDRVH}$	BST to SW = 5 V, C_{LOAD} = 1 nF	25	60	85	ns
LOW-SIDE DRIVER						
Output Resistance, Sourcing Current				3.8	8	Ω
Output Resistance, Sinking Current				1.5	8	Ω
Output Resistance, Unbiased		VCC = PGND		10		kΩ
Transition Time	t_{rDRVL}, t_{fDRVL}	C_{LOAD} = 1 nF		20	40	ns
Propagation Delay Time[3]	$t_{pdhDRVL}$	C_{LOAD} = 1 nF		15	35	ns
Timeout Delay[4]		SW = 5 V	150	300		ns
		SW = PGND	150	300		ns
SUPPLY V_{CC}						
Supply Voltage Range	V_{CC}		10		22	V
Supply Current						
Normal Mode	I_{VCC}	EN = 5 V		9.8	12	mA
Shutdown Mode	$I_{VCC(SD)}$	EN = 0 V		5	10	µA
Undervoltage Lockout Threshold	V_{UVLO}	V_{CC} rising	9	9.5	10	V
Undervoltage Lockout Hysteresis				600		mV
DRV Regulator Output Voltage	V_{DRVREG}	C_L = 100 nF	5.0	5.25	5.5	V
DRV Regulator Output Current	I_{DRVREG}		10			mA

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC) methods.
[2] Measured between CSP and CSM. ($V_{CSP} - V_{CSM}$) = 96 mV × CSADJ/REFIN.
[3] For propagation delays, t_{pdh} refers to the specified signal going high, and t_{pdl} refers to it going low.
[4] The turn-on of DRVL is initiated after DRVH turns off by either SW crossing a ~1 V threshold or by expiration of the timeout delay.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	−0.3 V to +25 V
PGND	−0.3 V to +0.3 V
BST	−0.3 V to +30 V
BST to SW	−0.3 V to +6 V
SW	−4 V to +25 V
DRVH	SW − 0.3 V to BST + 0.3 V
DRVL	PGND − 0.3 V to DRVREG + 0.3 V
SYSP, SYSM to AGND	−25 V to +25 V
BAT, CSP, CSM to AGND	−0.3 V to V_{CC} + 0.3 V
SYSP to SYSM	−5 V to +5 V
CSP to CSM	−5 V to +5 V
All Other Inputs and Outputs	−0.3 V to +6 V
θ_{JA}	
2-Layer Board	125°C/W
4-Layer Board	83°C/W
Operating Ambient Temperature Range	0°C to 100°C
Junction Temperature Range	0°C to 150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

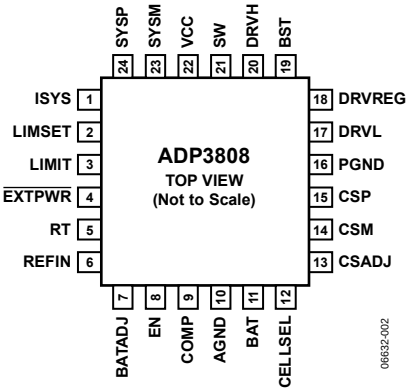

Figure 2. LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	ISYS	Output for System Current Sense Amplifier.
2	LIMSET	System Current Limit Set Point Input.
3	LIMIT	System Current Limit Output. This is an open-drain pin and requires a pull-up resistor to a maximum of 6 V.
4	$\overline{\text{EXTPWR}}$	External Adapter Sense Open-Drain Output. This pin pulls low when the ac adapter voltage is present. A pull-up resistor is required to a maximum of 6 V.
5	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and AGND sets the oscillator frequency of the device.
6	REFIN	Reference Input for BATADJ and CSADJ.
7	BATADJ	Battery Voltage Adjust Input. This pin uses an analog voltage referenced to REFIN to program voltage from 4.0 V to 4.5 V per cell.
8	EN	Charger Enable Input. Pulling this pin to AGND disables the DRVH and DRVL outputs and puts the circuitry powered by V_{CC} into a low power state. The system amplifier and $\overline{\text{EXTPWR}}$ are still active.
9	COMP	Output of Error Amplifiers and Compensation Point.
10	AGND	Analog Ground. Reference point for the battery sense and all analog functions.
11	BAT	Battery Sense Input.
12	CELLSEL	Battery Cell Selection Input. Pulling this pin high selects 3-cell operation; pulling it low selects 4-cell operation.
13	CSADJ	Charge Current Programming Input. This pin uses an analog voltage referenced to REFIN to program the battery charge current. ($V_{CSP} - V_{CSM}$) = 96 mV x CSADJ/REFIN.
14	CSM	Negative Current Sense Input. This pin connects to the battery side of the battery current sense resistor.
15	CSP	Positive Current Sense Input. This pin connects to the inductor side of the battery current sense resistor.
16	PGND	Power Ground. This pin should closely connect to the source of the lower MOSFET.
17	DRVL	Synchronous Rectifier Drive. Output drive for the lower MOSFET.
18	DRVREG	Driver Supply Output. A bypass capacitor should be connected from this pin to PGND to provide filtering for the low-side supply.
19	BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between the BST and SW pins holds this bootstrapped voltage for the high-side MOSFET as it is switched.
20	DRVH	Main Switch Drive. Output drive for the upper MOSFET.
21	SW	Switch Node Input. This pin is connected to the buck-switching node, close to the source of the upper MOSFET, and is the floating return for the upper MOSFET drive signal.
22	VCC	Input Supply. This pin does not power the SYS amplifier section.
23	SYSM	Negative System Current Sense Input. This pin connects to the battery side of the system current sense resistor.
24	SYSP	Positive System Current Sense Input. This pin connects to the adapter side of the system current sense resistor. This pin also provides power to the system amplifier section.
25	Paddle	This pin should be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

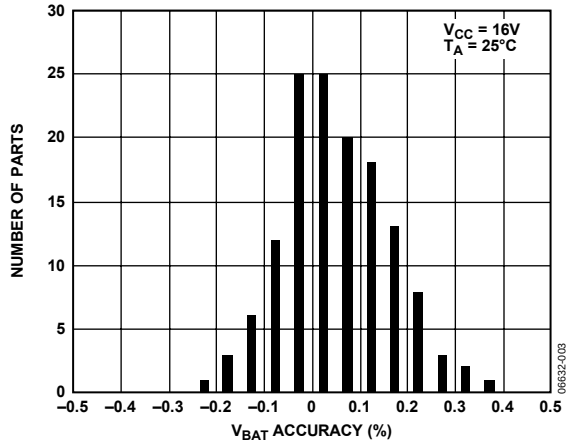

Figure 3. V_{BAT} Accuracy Distribution

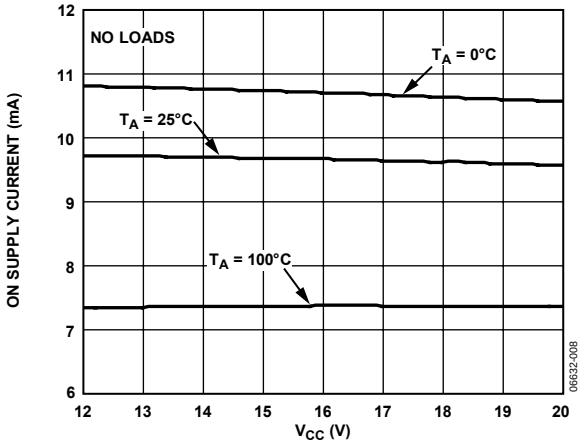

Figure 6. On Supply Current vs. V_{CC}

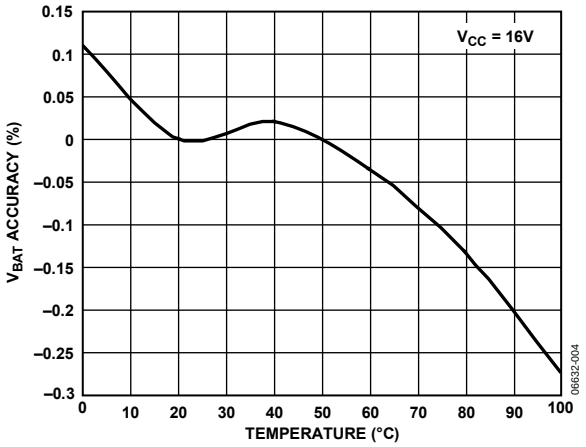

Figure 4. V_{BAT} Accuracy vs. Temperature

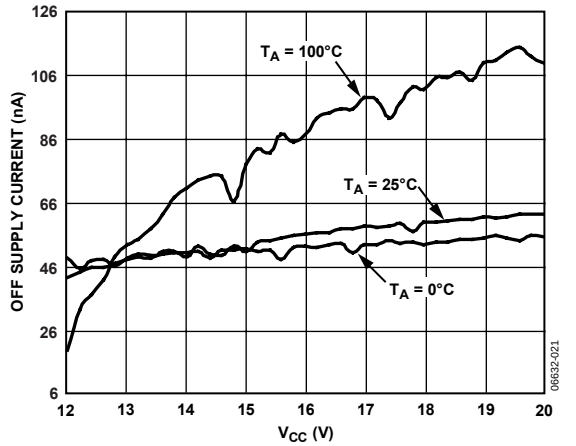

Figure 7. Off Supply Current vs. V_{CC}

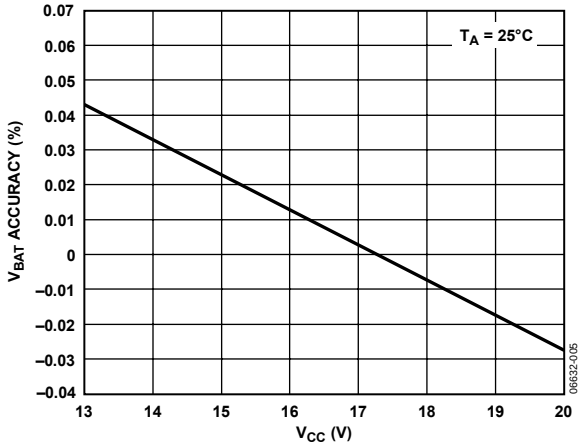

Figure 5. V_{BAT} Accuracy vs. V_{CC}

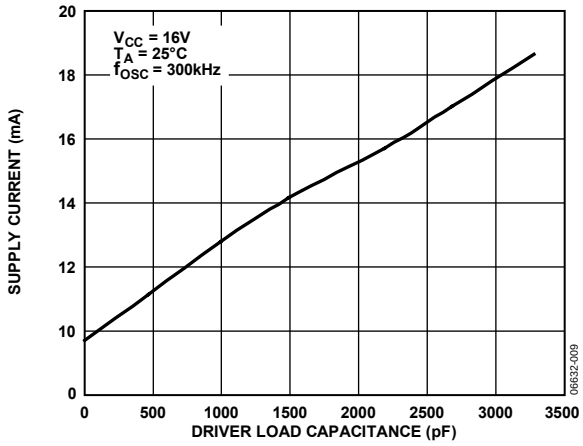

Figure 8. Supply Current vs. Driver Load Capacitance

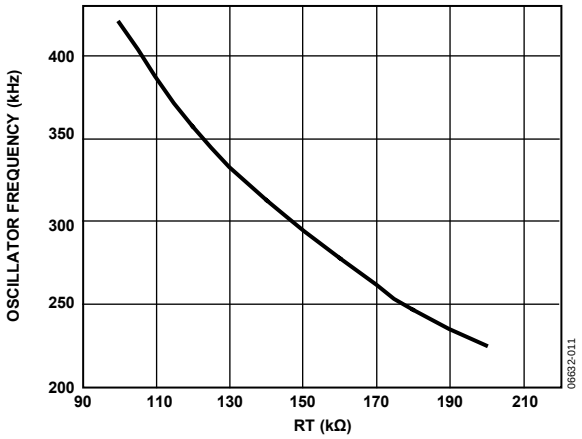

Figure 9. Oscillator Frequency vs. RT

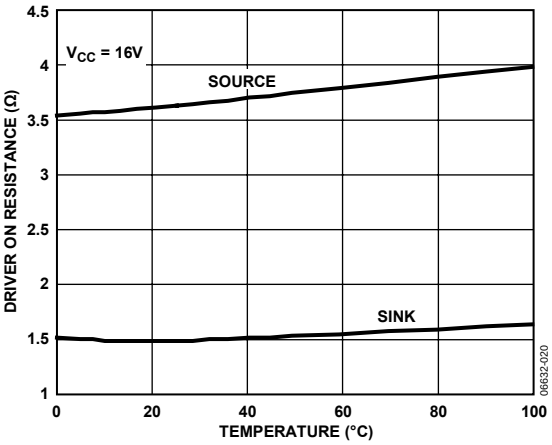

Figure 12. DRVL On Resistance vs. Temperature

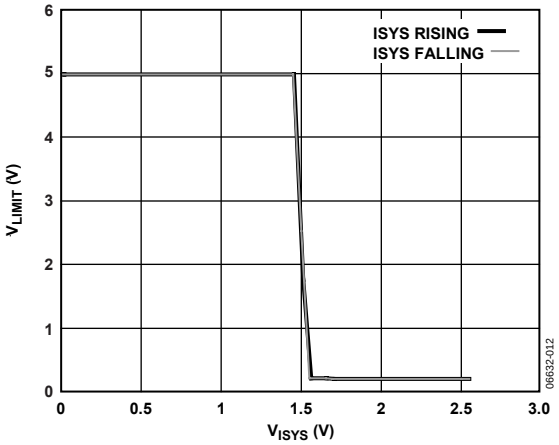

Figure 10. V_{LIMIT} vs. V_{ISYS}

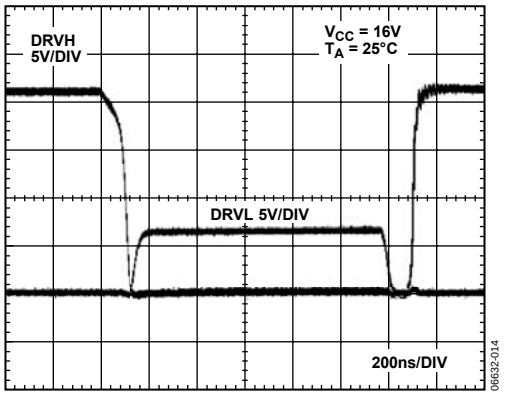

Figure 13. Driver Waveforms

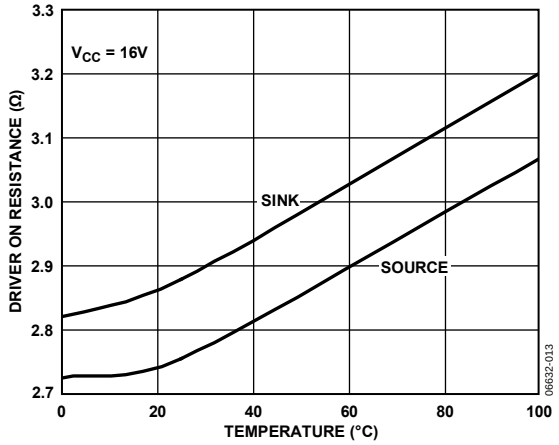

Figure 11. DRVH On Resistance vs. Temperature

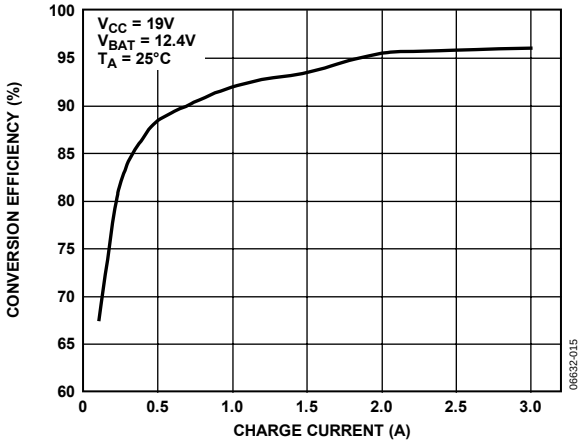

Figure 14. Conversion Efficiency vs. Charge Current

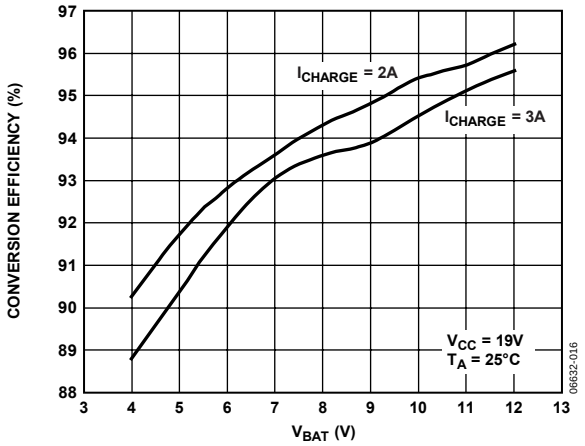

Figure 15. Conversion Efficiency vs. Battery Voltage

THEORY OF OPERATION

The ADP3808 combines a bootstrapped synchronous switching driver with programmable current control and accurate final battery voltage control in a constant-current, constant-voltage (CCCV) Li-Ion battery charger. High accuracy voltage control is needed to safely charge Li-Ion batteries, which are typically specified at 4.2 V ± 1% per cell. For a typical notebook computer battery pack, three or four cells are in series, giving a total voltage of 12.6 V or 16.8 V. The ADP3808 allows the final battery voltage to be programmed. The programmable range is 4.0 V to 4.5 V per cell. The total number of cells to be charged can be set to either 3 or 4 via a control pin.

Another requirement for safely charging Li-Ion batteries is accurate control of the charge current. The actual charge current depends on the number of cells in parallel within the battery pack. Typically, this is in the range of 2 A to 3 A. The ADP3808 provides flexibility in programming the charge current over a wide range. An external resistor is used to sense the charge current. The charge current can be set by programming the sense resistor voltage drop. The voltage drop can be set to a maximum of 96 mV. This programmability allows the current to be changed during charging. For example, the charge current can be reduced for trickle charging.

The synchronous driver provides high efficiency when charging at high currents. Efficiency is important mainly to reduce the amount of heat generated in the charger, but also to stay within the power limits of the ac adapter. With the addition of a bootstrapped high-side driver, the ADP3808 drives two external power NMOS transistors for a simple, lower cost power stage.

The ADP3808 also provides an uncommitted current sense amplifier. This amplifier provides an analog output pin for monitoring the current through an external sense resistor. The amplifier can be used anywhere in the system that high-side current sensing is needed. The sense amplifier output is compared to a programmable voltage limit. If the limit is exceeded, the LIMIT pin is asserted. The system sense amplifier is also used to detect the presence of an ac adaptor. If the adaptor is detected, the ADP3808 asserts a logic pin to signal the detection.

SETTING THE CHARGE CURRENT

The charge current is measured across an external sense resistor, R_{CS}, between the CSP and CSM pins. The input common-mode range is from ground to V_{CC}, allowing current control in short-circuit and low dropout conditions. The voltage between CSP and CSM is programmed by a ratio of the voltages at CSADJ and REFIN according to Equation 1.

$$V_{CSP} - V_{CSM} = 96\ \text{mV} \frac{CSADJ}{REFIN} \quad (1)$$

For example, using a 20 mΩ sense resistor gives a range from 150 mA with CSADJ = REFIN/32 to 4.8 A maximum when CSADJ = REFIN.

The power dissipation in R_{CS} should be kept below 500 mW. Components R4 and C13 provide high frequency filtering for the current sense signal.

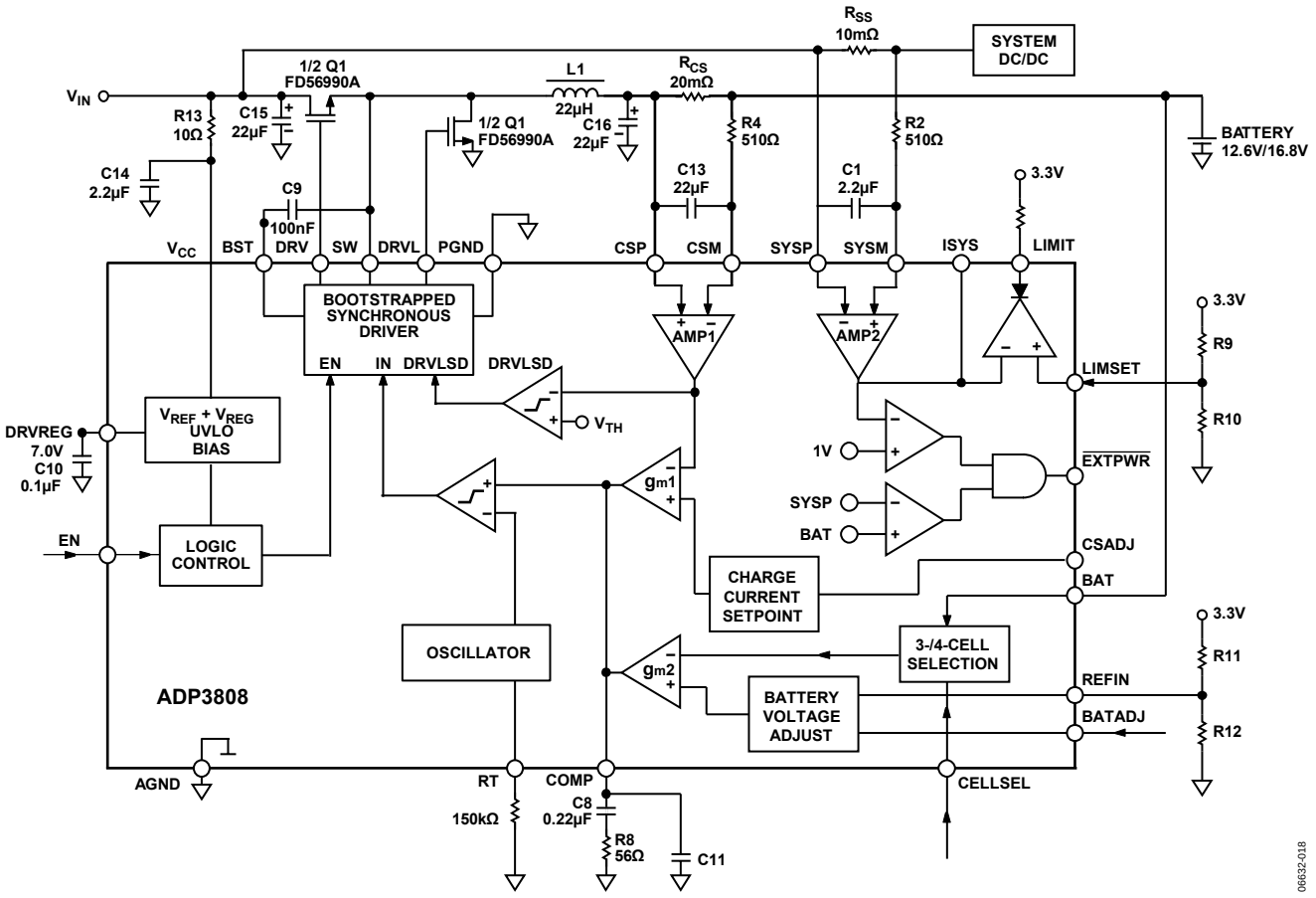

Figure 16. Typical Application Circuit

FINAL BATTERY VOLTAGE CONTROL

As the battery approaches its final voltage, the ADP3808 switches from CC mode to CV mode. The change is achieved by the common output node of g_m1 and g_m2. Only one of the two outputs controls the voltage at the COMP pin. Both amplifiers can only pull down on COMP, such that when either amplifier has a positive differential input voltage, its output is not active. For example, when the battery voltage, V_{BAT}, is low, g_m2 does not control VCOMP. When the battery voltage reaches the desired final voltage, g_m2 takes control of the loop, and the charge current is reduced.

Amplifier g_m2 compares the battery voltage to a programmable level set by pins BATADJ and REFIN. The target battery voltage is dependent on the state of the CELLSEL pin as CELLSEL sets the number of cells to be charged. Pulling CELLSEL high sets the ADP3808 to charge three cells. When CELLSEL is tied to ground, four cells are selected. CELLSEL has a 2 µA pull-up current as a fail-safe to select three cells when it is left open.

The final battery voltage is programmable from 4.0 V to 4.5 V per cell. The programming voltage is applied to the BATADJ pin and is ratioed to the REFIN pin. The battery voltage V_{BAT} is set according to Equation 2 and Equation 3.

For CELLSEL > 2 V:

$$V_{BAT} = 12\text{ V} + 1.5\text{ V}\frac{BATADJ}{REFIN} \quad (2)$$

For CELLSEL < 0.8 V:

$$V_{BAT} = 16\text{ V} + 2\text{ V}\frac{BATADJ}{REFIN} \quad (3)$$

OSCILLATOR AND PWM

The oscillator generates a triangle waveform between 1 V and 2 V, which is compared to the voltage at the COMP pin, setting the duty cycle of the driver stage. When V_{COMP} is below 1.0 V, the duty cycle is zero. Above 2.0 V, the duty cycle reaches its maximum. The oscillator frequency is set by the external resistor at the RT pin, R_{OSC}, and is given by Equation 4.

$$f_{OSC} = \frac{41 \times 10^9}{R_{OSC}} \quad (4)$$

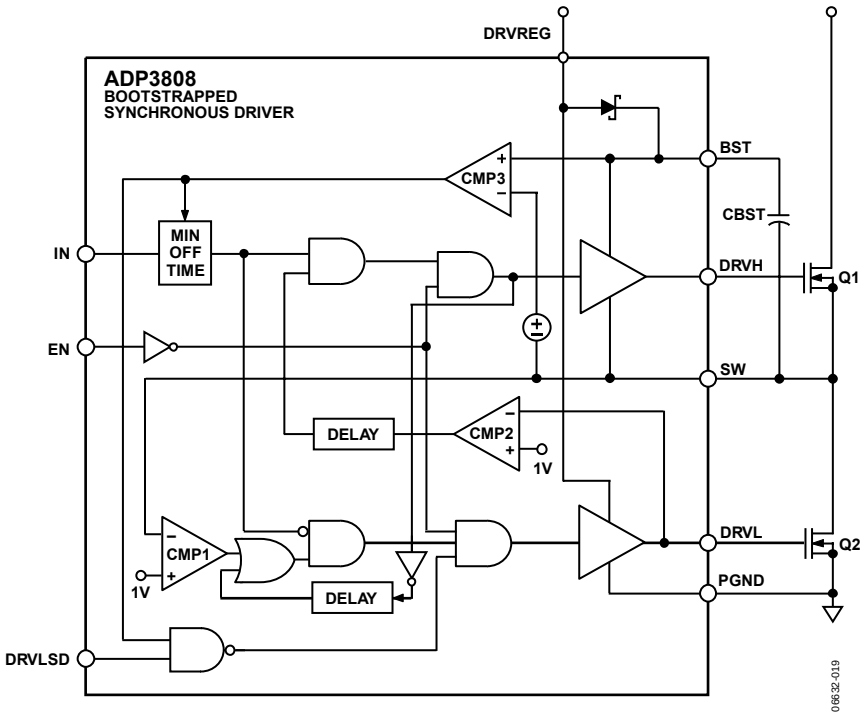

Figure 17. Bootstrapped Synchronous Driver

5.25 V BOOTSTRAP REGULATOR

The driver stage is powered by the internal 5.25 V bootstrap regulator, which is available at the DRVREG pin. Because the switching currents are supplied by this regulator, decoupling must be added. A 0.1 µF capacitor should be placed close to the ADP3808, with the ground side connected close to the power ground pin, PGND. This supply is not recommended for use externally due to high switching noise.

BOOTSTRAPPED SYNCHRONOUS DRIVER

The PWM comparator controls the state of the synchronous driver shown in Figure 17. A high output from the PWM comparator forces DRVH on and DRVL off. The drivers have an on resistance of less than 4 Ω for fast rise and fall times when driving external MOSFETs. Furthermore, the bootstrapped drive allows an external NMOS transistor for the main switch instead of a PMOS. A boost capacitor of 0.1 µF must be added externally between BST and SW.

The DRVL pin switches between DRVREG and PGND. The 5.25 V output of DRVREG drives the external NMOS with high V_{GS} to lower the on resistance. PGND should be connected close to the source pin of the external synchronous NMOS. When DRVL is high, this turns on the lower NMOS and pulls the SW node to ground. At this point, the boost capacitor is charged up through the internal boost diode. When the PWM switches high, DRVL is turned off and DRVH turns on. DRVH switches between BST and SW. When DRVH is on, the SW pin is pulled up to the input supply (typically 16 V), and BST rises above this voltage by approximately 4.75 V.

Overlap protection is included in the driver to ensure that both external MOSFETs are not on at the same time. When DRVH turns off the upper MOSFET, the SW node goes low due to the inductor current. The ADP3808 monitors the SW voltage, and DRVL goes high to turn on the lower MOSFET when SW goes below 1 V. When DRVL turns off, an internal timer adds a delay of 50 ns before turning DRVH on.

When the charge current is low, the DRVLSD comparator signals the driver to turn off the low-side MOSFET and DRVL is held low. The DRVLSD threshold is set to 0.8 V corresponding to a 32 mV differential between the CS pins.

The driver stage monitors the voltage across the BST capacitor with CMP3. When this voltage is less than 4 V, CMP3 forces a minimum off time of 200 ns. This ensures that the BST capacitor is charged even during DRVLSD. However, because a minimum off time is only forced when needed, the maximum duty cycle is greater than 99%.

SYSTEM CURRENT SENSE

An uncommitted differential amplifier is provided for additional high-side current sensing. This amplifier, AMP2, has a fixed gain of 50 V/V from the SYSP and SYSM pins to the analog output at ISYS. ISYS has a 100 µA source capability to drive an external load. The common-mode range of the input pins is from 10 V to 22 V. This amplifier is the only part of the ADP3808 that remains active during shutdown. The power to this block is derived from the bias current on the SYSP and SYSM pins.

LIMIT

The LIMIT pin is an open-drain output that signals when the voltage at ISYS exceeds the voltage at LIMSET. The internal comparator produces the function shown in Figure 10. This is a graph of V_{LIMIT} vs. V_{ISYS} where LIMSET is set to 1.5 V. The LIMIT pin should be pulled up to a maximum of 6 V through a resistor. When ISYS is below LIMSET, the LIMIT pin has high output impedance. The open-drain output is capable of sinking 700 μA when the threshold is exceeded. This comparator is turned off during shutdown to conserve power.

AC ADAPTOR DETECTION

The $\overline{\text{EXTPWR}}$ pin on the ADP3808 is an open-drain active low output used to signal that an ac adaptor is connected. If the ISYS voltage level is greater than 1 V or the SYSP sense pin voltage is greater then 18.25 V, the $\overline{\text{EXTPWR}}$ pin is driven low. A pull-up resistor must be connected when this function is required. The maximum pull-up voltage is 6 V.

EN

A high impedance CMOS logic input is provided to turn off the ADP3808. When the voltage on EN is less than 0.8 V, the ADP3808 is placed in low power shutdown. With the exception of the system current sense amplifier, AMP2, all other circuitry is turned off. The reference and regulators are pulled to ground during shutdown and all switching is stopped. During this state, the supply current is less than 5 A. In addition, the BAT, CSP, CSM, and SW pins go to high impedance to minimize current drain from the battery.

UVLO

Undervoltage lock-out, UVLO, is included in the ADP3808 to ensure proper startup. As V_{CC} rises above 1 V, the regulator tracks V_{CC} until it reaches its final voltage. However, the rest of the circuitry is held off by the UVLO comparator. The UVLO comparator monitors the regulator to ensure that it is above 5 V before turning on the main charger circuitry. This occurs when V_{CC} reaches 9.5 V. Monitoring the regulator outputs makes sure that the charger circuitry and driver stage have sufficient voltage to operate normally. The UVLO comparator includes 600 mV of hysteresis to prevent oscillations near the threshold.

LOOP FEED FORWARD

As the startup sequence discussion shows, the response time at COMP is slowed by the large compensation capacitor. To speed up the response, two comparators can quickly feed forward around the normal control loop and pull the COMP node down to limit any overshoot in either short-circuit or overvoltage conditions. The overvoltage comparator has a trip point set to 35% higher than the final battery voltage. The overcurrent comparator threshold is set to 100 mV across the CS pins. When these comparators are tripped, a normal soft start sequence is initiated. The overvoltage comparator is valuable when the battery is removed during charging. In this case, the current in the inductor causes the output voltage to spike up, and the comparator limits the maximum voltage. Neither of these comparators affects the loop under normal charging conditions.

APPLICATION INFORMATION

DESIGN PROCEDURE

Refer to Figure 16, the typical application circuit, for the following description. The design follows that of a buck converter. With Li-Ion cells it is important to have a regulator with accurate output voltage control.

BATTERY VOLTAGE SETTINGS

Inductor Selection

Usually the inductor is chosen based on the assumption that the inductor ripple current is ±15% of the maximum output dc current at maximum input voltage. As long as the inductor used has a value close to this, the system should work fine. The final choice affects the trade-offs between cost, size, and efficiency. For example, the lower the inductance, the size is smaller but ripple current is higher. This situation, if taken too far, leads to higher ac losses in the core and the windings. Conversely, a higher inductance results in lower ripple current and smaller output filter capacitors, but the transient response will be slower. With these considerations, the required inductance can be calculated using Equation 6.

$$L1 = \frac{V_{IN,MAX} - V_{BAT}}{\Delta I} \times D_{MIN} \times T_S \quad (6)$$

where the maximum input voltage $V_{IN, MAX}$ is used with the minimum duty ratio D_{MIN}. The duty ratio is defined as the ratio of the output voltage to the input voltage, V_{BAT}/V_{IN}. The ripple current is calculated using Equation 7.

$$\Delta I = 0.3 \times I_{BAT, MAX} \quad (7)$$

The maximum peak-to-peak ripple is 30%, that is 0.3, and maximum battery current, $I_{BAT, MAX}$, is used.

For example, with $V_{IN, MAX}$ = 19 V, V_{BAT} = 12.6 V, $I_{BAT, MAX}$ = 3A, and T_S = 4 µs, the value of L1 is calculated as 18.9 µH. Choosing the closest standard value gives L1 = 22 µH.

Output Capacitor Selection

An output capacitor is needed in the charger circuit to absorb the switching frequency ripple current and smooth the output voltage. The rms value of the output ripple current is given by

$$I_{rms} = \frac{V_{IN,MAX}}{fL1\sqrt{12}} D\left(1 - D\right) \quad (8)$$

The maximum value occurs when the duty cycle is 0.5. Thus,

$$I_{rms\_MAX} = 0.072 \frac{V_{IN, MAX}}{fL1} \quad (9)$$

For an input voltage of 19 V and a 22 µH inductance, the maximum rms current is 0.26 A. A typical 10 µF or 22 µF ceramic capacitor is a good choice to absorb this current.

Input Capacitor Ripple

As is the case with a normal buck converter, the pulse current at the input has a high rms component. Therefore, because the input capacitor has to absorb this current ripple, it must have an appropriate rms current rating. The maximum input rms current is given by

$$I_{rms} = \frac{P_{BAT}}{\eta \times D\ V_{IN}} \times \frac{\sqrt{D(1-D)}}{D} \quad (10)$$

where η is the estimated converter efficiency (approximately 90%, 0.9) and P_{BAT} is the maximum battery power consumed.

This is a worst-case calculation and, depending on total charge time, the calculated number could be relaxed. Consult the capacitor manufacturer for further technical information.

Decoupling the VCC Pin

It is a good idea to use an RC filter (R13 and C14) from the input voltage to the IC both to filter out switching noise and to supply bypass to the chip. During layout, this capacitor should be placed as close to the IC as possible. Values between 0.1 µF and 2.2 µF are recommended.

Current Sense Filtering

During normal circuit operation, the current sense signals can have high frequency transients that need filtering to ensure proper operation. In the case of the CSP and CSM inputs, Resistor R4 is set to 510 Ω and the filter capacitor C13 is 22 nF. For the system current sense filter on SYSP, SYSM, R2 is set to 510 Ω, C1 is 2.2 µF, and C2 is 470 nF.

MOSFET Selection

One of the features of the ADP3808 is that it allows use of a high-side NMOS switch instead of a more costly PMOS device. The converter also uses synchronous rectification for optimal efficiency. To use a high-side NMOS, an internal bootstrap regulator automatically generates a 5.25 V supply across C9.

Maximum output current determines the $R_{DS(ON)}$ requirement for the two power MOSFETs. When the ADP3808 is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the load current. The power dissipation for each MOSFET is given by

Upper MOSFET:

$$P_{DISS} = R_{DS(ON)} \times (I_{BAT} \times \sqrt{D})^2 + V_{IN} \times I_{BAT} \times \sqrt{D} \times T_{SW} \times f \quad (11)$$

Lower MOSFET:

$$P_{DISS} = R_{DS(ON)} \times (I_{BAT} \times \sqrt{D})^2 + V_{IN} \times (I_{BAT} \times \sqrt{1-D})^2 \times t_{SW} \times f \quad (12)$$

where f is the switching frequency and t_{SW} is the switch transition time, usually 10 ns.

The first term accounts for conduction losses while the second term estimates switching losses. Using these equations and the manufacturer's data sheets, the proper device can be selected.

OUTLINE DIMENSIONS

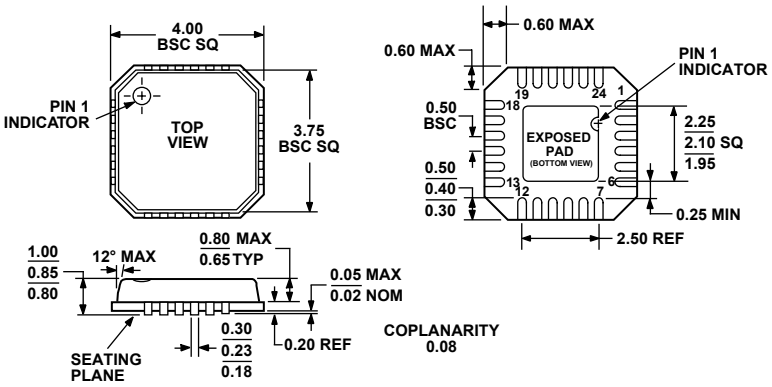

Figure 20. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADP3808JCPZ[1]	0°C to 100°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-1	
ADP3808JCPZ-RL[1]	0°C to 100°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-1	5000

[1] Z = RoHS Compliant Part.

NOTES

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View ADP3808JCPZ-RL on WIN SOURCE
- ON Semiconductor Information

Optimize Your Supply Chain with WIN SOURCE Solutions

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- Alternative Solution
- Excess Inventory Management