



**THE DATASHEET OF
AD7533KNZ**



FEATURES

Low cost 10-bit DAC
Low cost AD7520 replacement
Linearity: ½ LSB, 1 LSB, or 2 LSB
Low power dissipation
Full 4-quadrant multiplying DAC
CMOS/TTL direct interface
Latch free (protection Schottky not required)
Endpoint linearity

APPLICATIONS

Digitally controlled attenuators
Programmable gain amplifiers
Function generation
Linear automatic gain controls

GENERAL DESCRIPTION

The AD7533 is a low cost, 10-bit, 4-quadrant multiplying DAC manufactured using an advanced thin-film-on-monolithic-CMOS wafer fabrication process.

Pin and function equivalent to the AD7520 industry standard, the AD7533 is recommended as a lower cost alternative for old AD7520 sockets or new 10-bit DAC designs.

AD7533 application flexibility is demonstrated by its ability to interface to TTL or CMOS, operate on 5 V to 15 V power, and provide proper binary scaling for reference inputs of either positive or negative polarity.

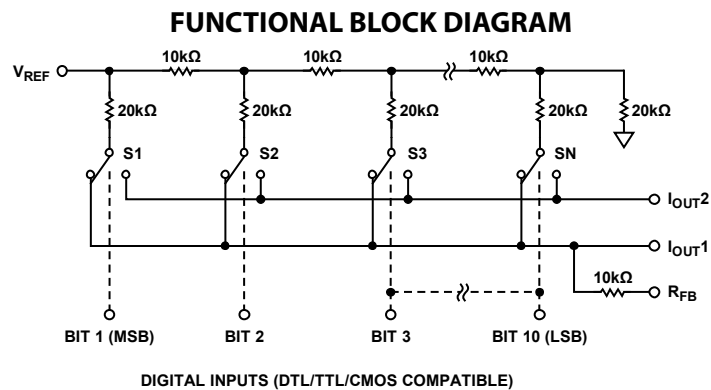


Figure 1.

Rev. C

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TABLE OF CONTENTS

Features 1
 Applications 1
 General Description 1
 Functional Block Diagram 1
 Revision History 2
 Specifications 3
 Absolute Maximum Ratings 4
 ESD Caution 4
 Terminology 5
 Pin Configurations and Function Descriptions 6

Circuit Description 7
 General Circuit Information 7
 Equivalent Circuit Analysis 7
 Operation 8
 Unipolar Binary Code 8
 Bipolar (Offset Binary) Code 8
 Applications 9
 Outline Dimensions 10
 Ordering Guide 12

REVISION HISTORY

3/07—Rev. B to Rev. C

Changes to Table 1 3
 Changes to Table 2 4
 Changes to Figure 13, Figure 14, and Figure 17 9
 Updated Outline Dimensions 10
 Changes to Ordering Guide 12

3/04—Rev. 0 to Rev. A

Changes to Specifications 2
 Changes to Absolute Maximum Ratings 3
 Changes to Ordering Guide 3
 Updated Outline Dimensions 7

1/06—Rev. A to Rev. B

Updated Format Universal
 Changes to Absolute Maximum Ratings 4
 Added Pin Configurations
 and Function Descriptions Section 6
 Updated Outline Dimensions 10
 Changes to Ordering Guide 12

SPECIFICATIONS

$V_{DD} = 15\text{ V}$, $V_{OUT1} = V_{OUT2} = 0\text{ V}$, $V_{REF} = 10\text{ V}$, unless otherwise noted.

Table 1.

Parameter	$T_A = 25^\circ\text{C}$	$T_A = \text{Operating Range}$	Test Conditions
STATIC ACCURACY			
Resolution	10 Bits	10 Bits	
Relative Accuracy ¹			
AD7533JN, AD7533AQ, AD7533SQ, AD7533JP	$\pm 0.2\%$ FSR maximum	$\pm 0.2\%$ FSR maximum	
AD7533KN, AD7533BQ, AD7533KP, AD7533TE	$\pm 0.1\%$ FSR maximum	$\pm 0.1\%$ FSR maximum	
AD7533LN, AD7533CQ, AD7533UQ	$\pm 0.05\%$ FSR maximum	$\pm 0.05\%$ FSR maximum	
DNL	± 1 LSB maximum	± 1 LSB maximum	
Gain Error ^{2, 3}	$\pm 1\%$ FS maximum	$\pm 1\%$ FS maximum	Digital input = V_{INH}
Supply Rejection ⁴			
$\Delta\text{Gain}/\Delta V_{DD}$	0.001%/ % maximum	0.001%/ % maximum	Digital inputs = V_{INH} , $V_{DD} = 14\text{ V}$ to 17 V
Output Leakage Current			
I_{OUT1}	$\pm 5\text{ nA}$ maximum	$\pm 200\text{ nA}$ maximum	Digital inputs = V_{INL} , $V_{REF} = \pm 10\text{ V}$
I_{OUT2}	$\pm 5\text{ nA}$ maximum	$\pm 200\text{ nA}$ maximum	Digital inputs = V_{INH} , $V_{REF} = \pm 10\text{ V}$
DYNAMIC ACCURACY			
Output Current Settling Time	600 ns maximum ⁴	800 ns ⁵	To 0.05% FSR; $R_{LOAD} = 100\ \Omega$, digital inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error	$\pm 0.05\%$ FSR maximum ⁵	$\pm 0.1\%$ FSR maximum ⁵	Digital inputs = V_{INL} , $V_{REF} = \pm 10\text{ V}$, 100 kHz sine wave
Propagation Delay	100 ns typical	100 ns typical	
Glitch Impulse	100 nV-s typical	100 nV-s typical	
REFERENCE INPUT			
Input Resistance (V_{REF})	5 k Ω min, 20 k Ω maximum	5 k Ω min, 20 k Ω maximum ⁶	11 k Ω nominal
ANALOG OUTPUTS			
Output Capacitance			
C_{IOUT1}	50 pF maximum ⁵	100 pF maximum ⁵	Digital inputs = V_{INH}
C_{IOUT2}	20 pF maximum ⁵	35 pF maximum ⁵	
C_{IOUT1}	30 pF maximum ⁵	35 pF maximum ⁵	
C_{IOUT2}	50 pF maximum ⁵	100 pF maximum ⁵	Digital inputs = V_{INL}
DIGITAL INPUTS			
Input High Voltage (V_{INH})	2.4 V minimum	2.4 V minimum	
Input Low Voltage (V_{INL})	0.8 V maximum	0.8 V maximum	
Input Leakage Current (I_{IN})	$\pm 1\ \mu\text{A}$ maximum	$\pm 1\ \mu\text{A}$ maximum	$V_{IN} = 0\text{ V}$ and V_{DD}
Input Capacitance (C_{IN})	8 pF maximum ⁵	8 pF maximum ⁵	
POWER REQUIREMENTS			
V_{DD}	15 V \pm 10%	15 V \pm 10%	Rated accuracy
V_{DD} Ranges ⁵	5 V to 16 V	5 V to 16 V	Functionality with degraded performance
I_{DD}	2 mA maximum	2 mA maximum	Digital inputs = V_{INL} or V_{INH} D
	25 μA maximum	50 μA maximum	Digital inputs over V_{IN}

¹ FSR = full-scale range.

² Full scale (FS) = V_{REF} .

³ Maximum gain change from $T_A = 25^\circ\text{C}$ to T_{MIN} or T_{MAX} is $\pm 0.1\%$ FSR.

⁴ AC parameter, sample tested to ensure specification compliance.

⁵ Guaranteed, not tested.

⁶ Absolute temperature coefficient is approximately $-300\text{ ppm}/^\circ\text{C}$.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to GND	-0.3 V, +17 V
R_{FB} to GND	± 25 V
V_{REF} to GND	± 25 V
Digital Input Voltage Range	-0.3 V to $V_{DD} + 0.3$ V
I_{OUT1} , I_{OUT2} to GND	-0.3 V to V_{DD}
Power Dissipation (Any Package)	
To 75°C	450 mW
Derates above 75°C by	6 mW/°C
Operating Temperature Range	
Plastic (JN, JP, KN, KP, LN Versions)	-40°C to +85°C
Hermetic (AQ, BQ, CQ Versions)	-40°C to +85°C
Hermetic (SQ, TE, UQ Versions)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TERMINOLOGY

Relative Accuracy

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % of full-scale range or (sub) multiples of 1 LSB.

Resolution

Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n}) (V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}] (V_{REF})$. Resolution in no way implies linearity.

Settling Time

Time required for the output function of the DAC to settle to within $\frac{1}{2}$ LSB for a given digital input stimulus, that is, 0 to full scale.

Gain Error

Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error is adjusted out and is expressed in LSBs. Gain error is adjustable to zero with an external potentiometer.

Feedthrough Error

Error caused by capacitive coupling from V_{REF} to output with all switches off.

Output Capacitance

Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

Output Leakage Current

Current that appears on I_{OUT1} terminal with all digital inputs low or on I_{OUT2} terminal when all inputs are high.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

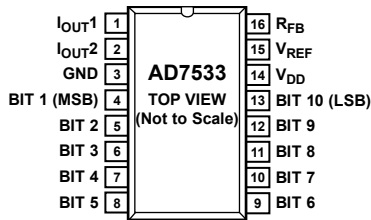


Figure 2. 16-Lead PDIP Pin Configuration

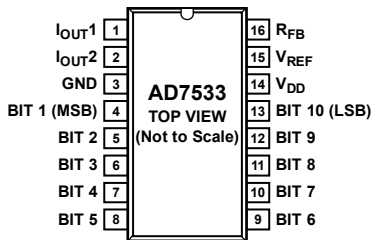


Figure 3. 16-Lead SOIC Pin Configuration

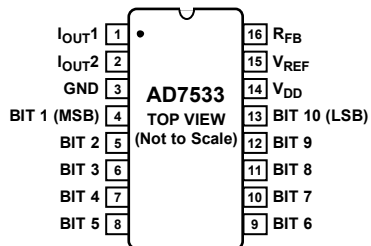


Figure 4. 16-Lead CERDIP Pin Configuration

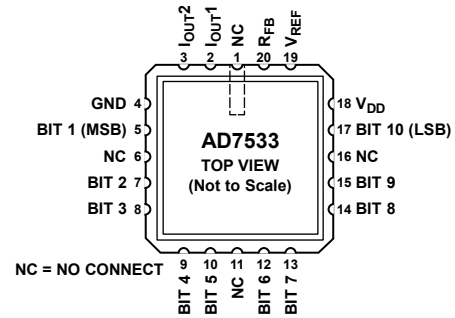


Figure 5. 20-Terminal LCC Pin Configuration

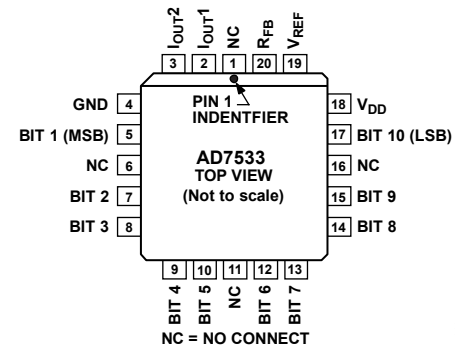


Figure 6. 20-Lead PLCC Pin Configuration

Table 3. Pin Function Descriptions

Pin Number		Mnemonic	Description
16-Lead PDIP, SOIC, CERDIP	20-Lead LCC, PLCC		
1	2	I _{OUT1}	DAC Current Output.
2	3	I _{OUT2}	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	4	GND	Ground.
4 to 13	5, 7 to 10, 12 to 15, 17	BIT 1 to BIT 10	MSB to LSB.
14	18	V _{DD}	Positive Power Supply Input. These parts can be operated from a supply of 5 V to 16 V.
15	19	V _{REF}	DAC Reference Voltage Input Terminal.
16	20	R _{FB}	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting R _{FB} to external amplifier output.
NA	1, 6, 11, 16	NC	No Connect.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7533 is a 10-bit multiplying DAC that consists of a highly stable thin-film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 7. An inverted R-2R ladder structure is used, that is, the binary weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

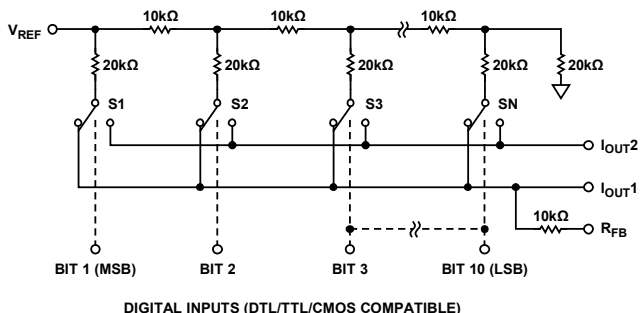


Figure 7. Functional Diagram

One of the CMOS current switches is shown in Figure 8. The geometries of Device 1, Device 2, and Device 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (Device 4, Device 5, Device 6, and Device 7), which in turn drive the two output N channels. The on resistances of the switches are binary sealed so that the voltage drop across each switch is the same. For example, Switch 1 in Figure 8 is designed for an on resistance of 20 Ω, Switch 2 for 40 Ω, and so on. For a 10 V reference input, the current through Switch 1 is 0.5 mA, the current through Switch 2 is 0.25 mA, and so on, thus maintaining a constant 10 mV drop across each switch. It is essential that each switch voltage drop be equal if the binary weighted current division property of the ladder is to be maintained.

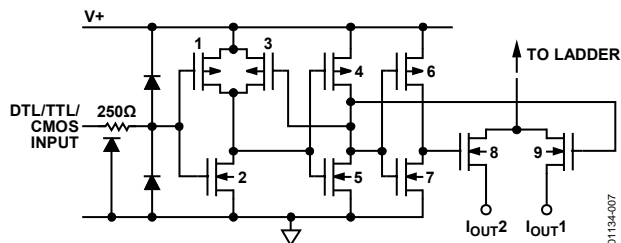


Figure 8. CMOS Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and digital inputs low are shown in Figure 9 and Figure 10. In Figure 9 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source I_{LEAKAGE} is composed of surface and junction leakages to the substrate, while the I/1024 current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The on capacitance of the output N channel switch is 100 pF, as shown on the I_{OUT2} terminal. The off switch capacitance is 35 pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 10, is similar to Figure 9; however, the on switches are now on Terminal I_{OUT1}. Therefore, there is the 100 pF at that terminal.

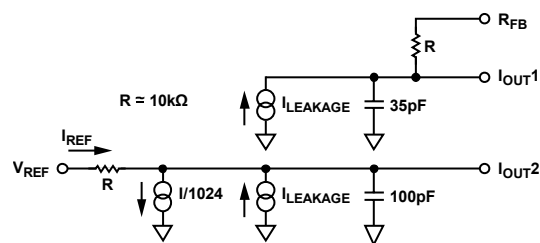


Figure 9. Equivalent Circuit—All Digital Inputs Low

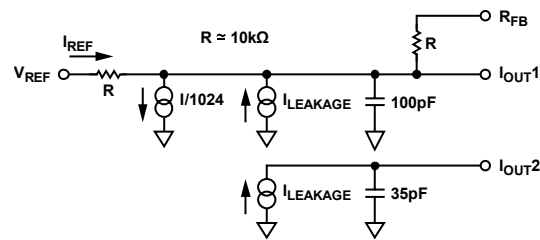


Figure 10. Equivalent Circuit—All Digital Inputs High

AD7533

OPERATION

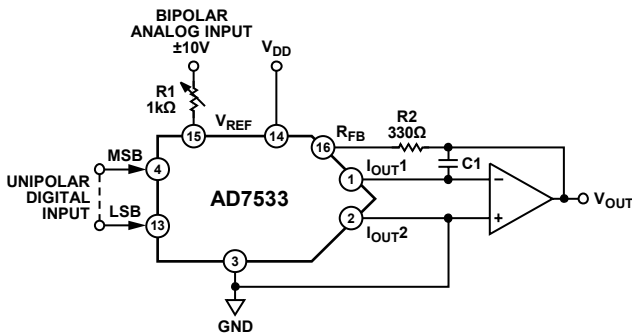
UNIPOLAR BINARY CODE

Table 4. Unipolar Binary Operation
(2-Quadrant Multiplication)

Digital Input		Analog Output (V_{OUT} as shown in Figure 11)
MSB	LSB	
1	1111111111	$-V_{REF} \left(\frac{1023}{1024} \right)$
1	000000001	$-V_{REF} \left(\frac{513}{1024} \right)$
1	000000000	$-V_{REF} \left(\frac{512}{1024} \right) = \left(\frac{V_{REF}}{2} \right)$
0	1111111111	$-V_{REF} \left(\frac{511}{1024} \right)$
0	000000001	$-V_{REF} \left(\frac{1}{1024} \right)$
0	000000000	$-V_{REF} \left(\frac{0}{1024} \right) = 0$

Nominal LSB magnitude for the circuit of Figure 11 is given by

$$LSB = V_{REF} \left(\frac{1}{1024} \right)$$



NOTES

1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. C1 PHASE COMPENSATION (5pF TO 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

Figure 11. Unipolar Binary Operation (2-Quadrant Multiplication)

01134-010

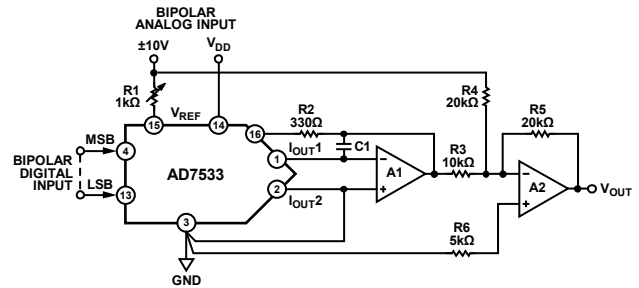
BIPOLAR (OFFSET BINARY) CODE

Table 5. Unipolar Binary Operation
(4-Quadrant Multiplication)

Digital Input		Analog Output (V_{OUT} as shown in Figure 12)
MSB	LSB	
1	1111111111	$+V_{REF} \left(\frac{511}{512} \right)$
1	000000001	$+V_{REF} \left(\frac{1}{512} \right)$
1	000000000	0
0	1111111111	$-V_{REF} \left(\frac{1}{512} \right)$
0	000000001	$-V_{REF} \left(\frac{511}{512} \right)$
0	000000000	$-V_{REF} \left(\frac{512}{512} \right)$

Nominal LSB magnitude for the circuit of Figure 12 is given by

$$LSB = V_{REF} \left(\frac{1}{512} \right)$$



NOTES

1. R3, R4, AND R5 SELECTED FOR MATCHING AND TRACKING.
2. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. C1 PHASE COMPENSATION (5pF TO 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIERS.

Figure 12. Bipolar Operation (4-Quadrant Multiplication)

01134-011

APPLICATIONS

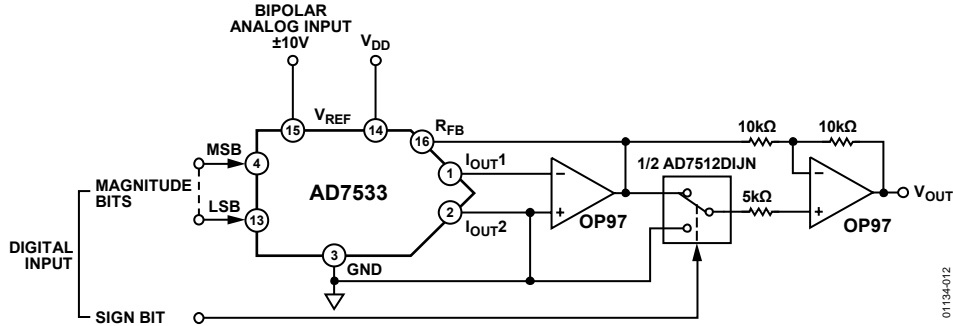


Figure 13. 10-Bit and Sign Multiplying DAC

01134-012

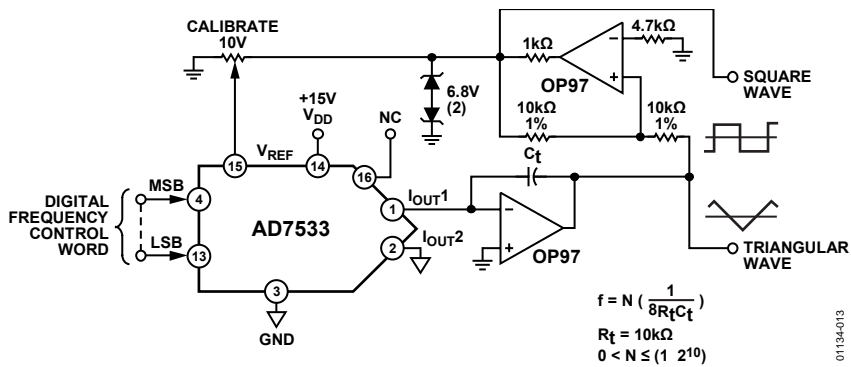


Figure 14. Programmable Function Generator

01134-013

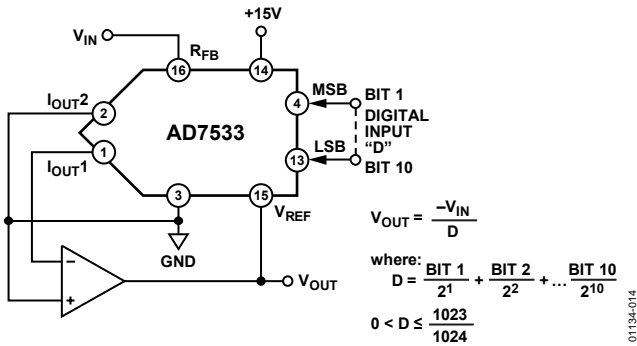


Figure 15. Divider (Digitally Controlled Gain)

01134-014

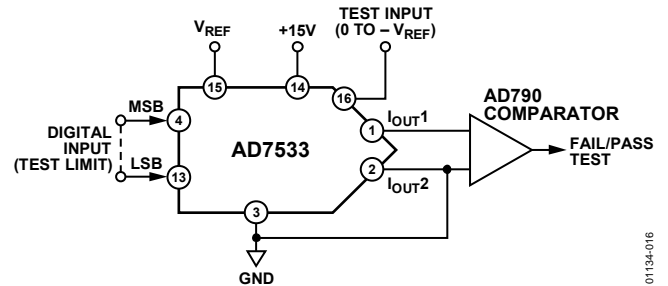


Figure 17. Digitally Programmable Limit Detector

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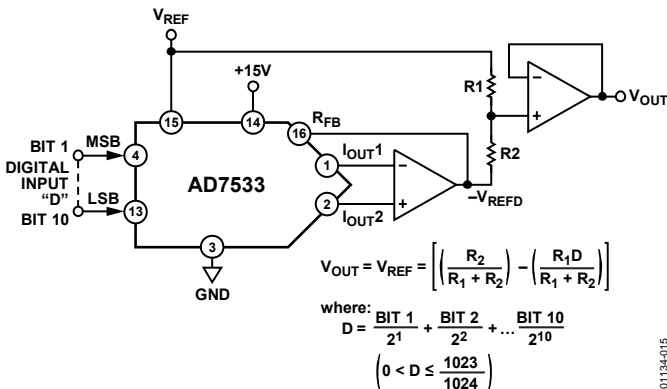
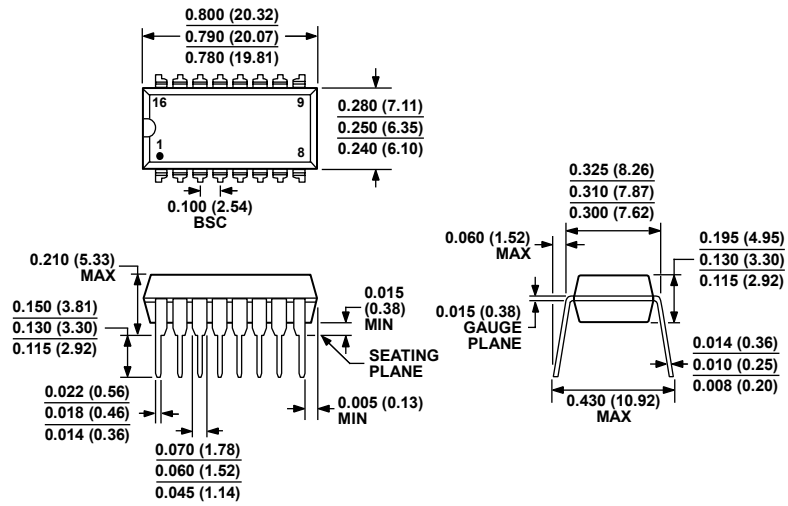


Figure 16. Modified Scale Factor and Offset

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OUTLINE DIMENSIONS

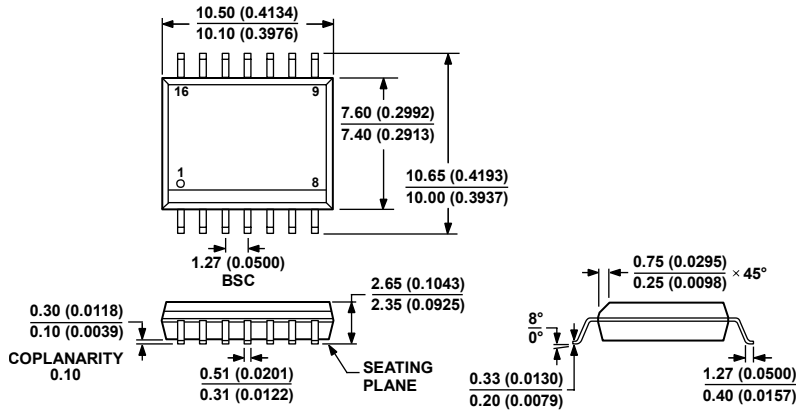


COMPLIANT TO JEDEC STANDARDS MS-001-AB
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
 CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 18. 16-Lead Plastic Dual In-Line Package [PDIP]
 (N-16)

Dimensions shown in inches and (millimeters)

073106-B

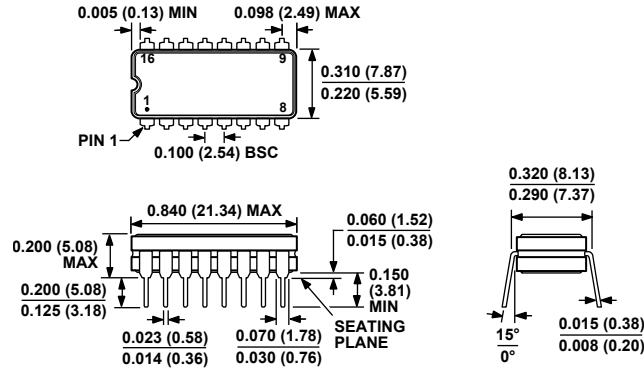


COMPLIANT TO JEDEC STANDARDS MS-013-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 19. 16-Lead Standard Small Outline Package [SOIC_W]
 Wide Body (RW-16)

Dimensions shown in millimeters and (inches)

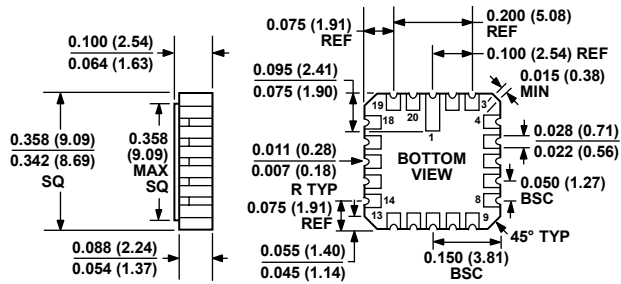
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CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 20. 16-Lead Ceramic Dual In-Line Package [CERDIP] (Q-16)

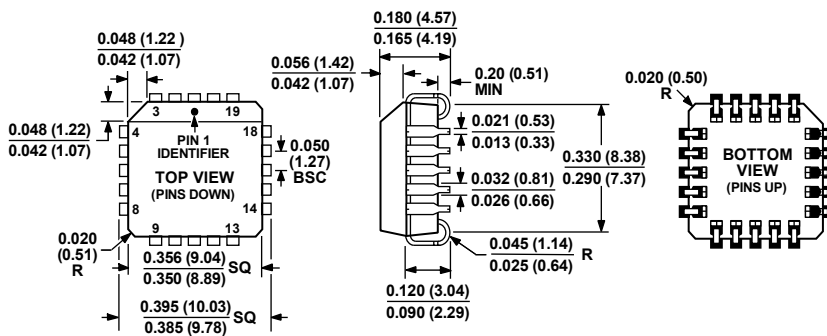
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 21. 20-Terminal Ceramic Leadless Chip Carrier [LCC] (E-20-1)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-047-AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 22. 20-Lead Plastic Leaded Chip Carrier [PLCC] (P-20)

Dimensions shown in inches and (millimeters)

AD7533

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Nonlinearity (% FSR max)
AD7533ACHIPS			DIE	
AD7533JN	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	±0.2
AD7533JNZ ¹	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	±0.2
AD7533KN	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	±0.1
AD7533KNZ ¹	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	±0.1
AD7533LN	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	±0.05
AD7533LNZ ¹	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	±0.05
AD7533JP	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.2
AD7533JP-REEL	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.2
AD7533JPZ ¹	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.2
AD7533JPZ-REEL ¹	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.2
AD7533KP	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.1
AD7533KP-REEL	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.1
AD7533KPZ ¹	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.1
AD7533KPZ-REEL ¹	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.1
AD7533KR	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	±0.1
AD7533KR-REEL	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	±0.1
AD7533KRZ ¹	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	±0.1
AD7533KRZ-REEL ¹	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	±0.1
AD7533AQ	−40°C to +85°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	±0.2
AD7533BQ	−40°C to +85°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	±0.1
AD7533CQ	−40°C to +85°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	±0.05
AD7533SQ	−55°C to +125°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	±0.2
AD7533UQ	−55°C to +125°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	±0.05
AD7533UQ/883B	−55°C to +125°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	±0.05
AD7533TE/883B	−55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier [LCC]	E-20-1	±0.1

¹Z = RoHS compliant part.

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-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management