# THE DATASHEET OF

# SN65HVD231QDRQ1

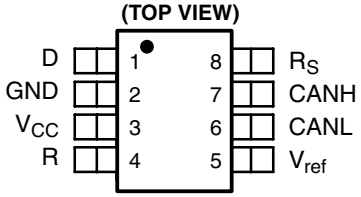
SGLS398A – APRIL 2002 – REVISED APRIL 2008

# 3.3-V CAN TRANSCEIVERS

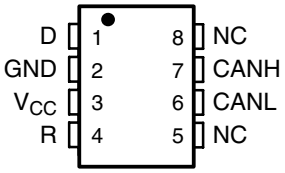
## FEATURES

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Operates With a 3.3-V Supply
- Low Power Replacement for the PCA82C250 Footprint
- Bus/Pin ESD Protection Exceeds 15-kV HBM
- Controlled Driver Output Transition Times for Improved Signal Quality on the SN65HVD230Q and SN65HVD231Q
- Unpowered Node Does Not Disturb the Bus
- Compatible With the Requirements of the ISO 11898 Standard
- Low-Current SN65HVD230Q Standby Mode 370 μA Typical
- Low-Current SN65HVD231Q Sleep Mode 0.1 μA Typical
- Designed for Signaling Rates‡ Up To 1 Megabit/Second (Mbps)
- Thermal Shutdown Protection
- Open-Circuit Fail-Safe Design

**SN65HVD230QD**
**SN65HVD231QD**
**(TOP VIEW)**



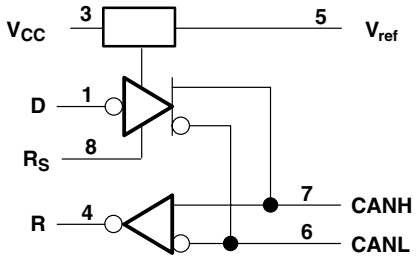

**SN65HVD232QD**
**(TOP VIEW)**



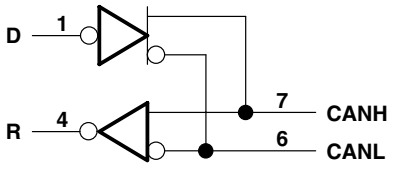

NC – No internal connection

## logic diagram (positive logic)

**SN65HVD230Q, SN65HVD231Q**
**Logic Diagram (Positive Logic)**




**SN65HVD232Q**
**Logic Diagram (Positive Logic)**






‡ The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

## DESCRIPTION

The SN65HVD230Q, SN65HVD231Q, and SN65HVD232Q controller area network (CAN) transceivers are designed for use with the Texas Instruments TMS320Lx240x 3.3-V DSPs with CAN controllers, or with equivalent devices. They are intended for use in applications employing the CAN serial communication physical layer in accordance with the ISO 11898 standard. Each CAN transceiver is designed to provide differential transmit capability to the bus and differential receive capability to a CAN controller at speeds up to 1 Mbps.

Designed for operation in especially-harsh environments, these devices feature cross-wire protection, loss-of-ground and overvoltage protection, overtemperature protection, as well as wide common-mode range.

The transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial, building automation, and automotive applications. It operates over a –2-V to 7-V common-mode range on the bus, and it can withstand common-mode transients of ±25 V.

On the SN65HVD230Q and SN65HVD231Q, $R_S$ (pin 8) provides three different modes of operation: high-speed, slope control, and low-power modes. The high-speed mode of operation is selected by connecting pin 8 to ground, allowing the transmitter output transistors to switch on and off as fast as possible with no limitation on the rise and fall slopes. The rise and fall slopes can be adjusted by connecting a resistor to ground at pin 8, since the slope is proportional to the pin's output current. This slope control is implemented with external resistor values of 10 kΩ, to achieve a 15-V/μs slew rate, to 100 kΩ, to achieve a 2-V/μs slew rate.

The circuit of the SN65HVD230Q enters a low-current standby mode during which the driver is switched off and the receiver remains active if a high logic level is applied to $R_S$ (pin 8). The DSP controller reverses this low-current standby mode when a dominant state (bus differential voltage > 900 mV typical) occurs on the bus.

The unique difference between the SN65HVD230Q and the SN65HVD231Q is that both the driver and the receiver are switched off in the SN65HVD231Q when a high logic level is applied to $R_S$ (pin 8) and remain in this sleep mode until the circuit is reactivated by a low logic level on $R_S$.

The $V_{ref}$ (pin 5 on the SN65HVD230Q and SN65HVD231Q) is available as a $V_{CC}/2$ voltage reference.

The SN65HVD232Q is a basic CAN transceiver with no added options; pins 5 and 8 are NC, no connection.

**AVAILABLE OPTIONS**[†‡]

| FUNCTION NUMBER | LOW POWER MODE | INTEGRATED SLOPE CONTROL | Vref PIN |
|---|---|---|---|
| ’230 | 370-μA standby mode | Yes | Yes |
| ’231 | 10-μA sleep mode | Yes | Yes |
| ’232 | No standby or sleep mode | No | No |

| PART NUMBER | Q100 | $T_A$ | MARKED AS: |
|---|---|---|---|
| SN65HVD230QD | No | –40°C to 125°C | HV230Q |
| SN65HVD231QD | No | | HV231Q |
| SN65HVD232QD | No | | HV232Q |
| SN65HVD230QDQ1 | Yes | –40°C to 125°C | 230Q1 |
| SN65HVD231QDQ1 | Yes | | 231Q1 |
| SN65HVD232QDQ1 | Yes | | 232Q1 |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

The D package is available taped and reeled. Add the suffix R to device type (e.g., SN65HVD230QDRQ1).

## Function Tables

**DRIVER (SN65HVD230Q, SN65HVD231Q)**

| INPUT D | $R_S$ | OUTPUTS | | BUS STATE |
|---|---|---|---|---|
| | | CANH | CANL | |
| L | $V_{(Rs)} < 1.2$ V | H | L | Dominant |
| H | | Z | Z | Recessive |
| Open | X | Z | Z | Recessive |
| X | $V_{(Rs)} > 0.75\ V_{CC}$ | Z | Z | Recessive |

H = high level; L = low level; X = irrelevant; ? = indeterminate

**DRIVER (SN65HVD232Q)**

| INPUT D | OUTPUTS | | BUS STATE |
|---|---|---|---|
| | CANH | CANL | |
| L | H | L | Dominant |
| H | Z | Z | Recessive |
| Open | Z | Z | Recessive |

H = high level; L = low level

**RECEIVER (SN65HVD230Q)**

| DIFFERENTIAL INPUTS | $R_S$ | OUTPUT R |
|---|---|---|
| $V_{ID} \geq 0.9$ V | X | L |
| $0.5\ V < V_{ID} < 0.9$ V | X | ? |
| $V_{ID} \leq 0.5$ V | X | H |
| Open | X | H |

H = high level; L = low level; X = irrelevant; ? = indeterminate

**RECEIVER (SN65HVD231Q)**

| DIFFERENTIAL INPUTS | $R_S$ | OUTPUT R |
|---|---|---|
| $V_{ID} \geq 0.9$ V | $V_{(Rs)} < 1.2$ V | L |
| $0.5\ V < V_{ID} < 0.9$ V | | ? |
| $V_{ID} \leq 0.5$ V | | H |
| X | $V_{(Rs)} > 0.75\ V_{CC}$ | H |
| X | $1.2\ V < V_{(Rs)} < 0.75\ V_{CC}$ | ? |
| Open | X | H |

H = high level; L = low level; X = irrelevant; ? = indeterminate

**RECEIVER (SN65HVD232Q)**

| DIFFERENTIAL INPUTS | OUTPUT R |
|---|---|
| $V_{ID} \geq 0.9$ V | L |
| $0.5\ V < V_{ID} < 0.9$ V | ? |
| $V_{ID} \leq 0.5$ V | H |
| Open | H |

H = high level; L = low level; X = irrelevant; ? = indeterminate

## Function Tables (Continued)

**TRANSCEIVER MODES (SN65HVD230Q, SN65HVD231Q)**

| $V_{(Rs)}$ | OPERATING MODE |
|---|---|
| $V_{(RS)} > 0.75\ V_{CC}$ | Standby |
| 10 kΩ to 100 kΩ to ground | Slope control |
| $V_{(RS)} < 1$ V | High speed (no slope control) |

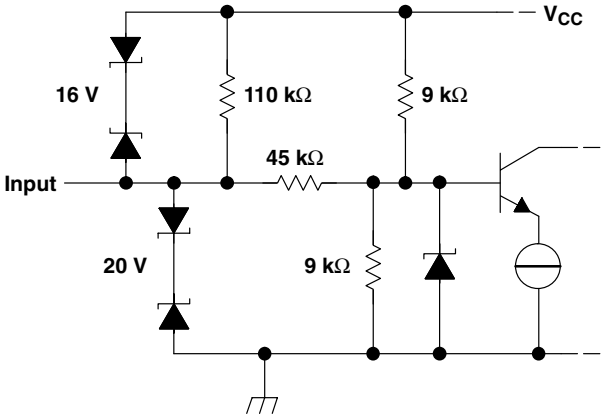
## Terminal Functions

| SN65HVD230Q, SN65HVD231Q | | |
|---|---|---|
| TERMINAL NAME | TERMINAL NO. | DESCRIPTION |
| CANL | 6 | Low bus output |
| CANH | 7 | High bus output |
| D | 1 | Driver input |
| GND | 2 | Ground |
| R | 4 | Receiver output |
| $R_S$ | 8 | Standby/slope control |
| $V_{CC}$ | 3 | Supply voltage |
| $V_{ref}$ | 5 | Reference output |

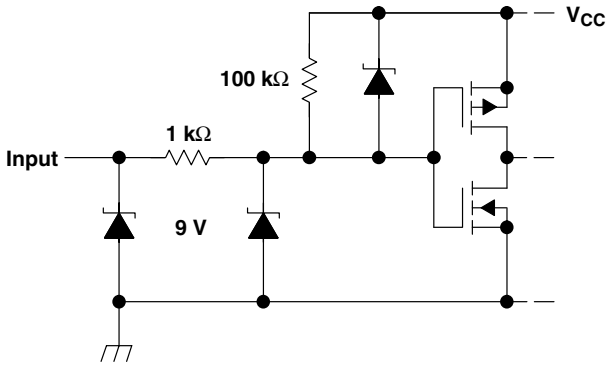
| SN65HVD232Q | | |
|---|---|---|
| TERMINAL NAME | TERMINAL NO. | DESCRIPTION |
| CANL | 6 | Low bus output |
| CANH | 7 | High bus output |
| D | 1 | Driver input |
| GND | 2 | Ground |
| NC | 5, 8 | No connection |
| R | 4 | Receiver output |
| $V_{CC}$ | 3 | Supply voltage |

## equivalent input and output schematic diagrams

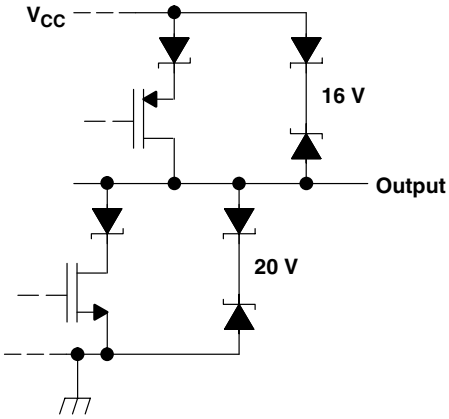
**CANH and CANL Inputs**



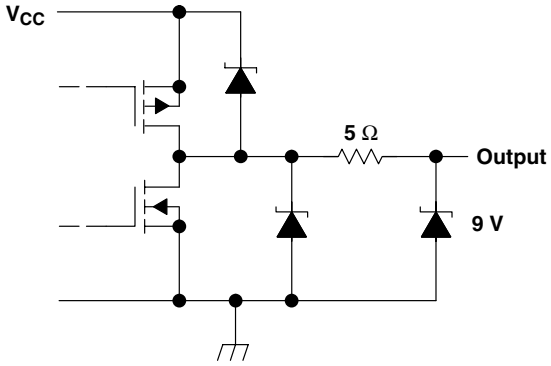

**D Input**




**CANH and CANL Outputs**




**R Output**



### absolute maximum ratings over operating free-air temperature (see Note 1) (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.3 V to 6 V
Voltage range at any bus terminal (CANH or CANL) . . . . . −7 V to 16 V
Voltage input range, transient pulse, CANH and CANL, through 100 Ω (see Figure 7) . . . . . −25 V to 25 V
Input voltage range, $V_I$ (D or R) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Electrostatic discharge: Human body model (see Note 2) CANH, CANL and GND . . . . . 15 kV
All pins . . . . . 2.5 kV
Charged-device model (see Note 3) All pins . . . . . 4 kV
Continuous total power dissipation . . . . . See Dissipation Rating table
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with JEDEC Standard 22, Test Method A114-A.
3. Tested in accordance with JEDEC Standard 22, Test Method C101.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR‡ ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|---|
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW | 145 mW |

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

### recommended operating conditions

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 3 | | 3.6 | V |
| Voltage at any bus terminal (common mode) $V_{IC}$ | | −2§ | | 7 | V |
| Voltage at any bus terminal (separately) $V_I$ | | −2.5 | | 7.5 | V |
| High-level input voltage, $V_{IH}$ | D, R | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | D, R | | | 0.8 | V |
| Differential input voltage, $V_{ID}$ (see Figure 5) | | −6 | | 6 | V |
| $V_{(RS)}$ | | 0 | | $V_{CC}$ | V |
| $V_{(RS)}$ for standby or sleep | | 0.75 $V_{CC}$ | | $V_{CC}$ | V |
| Rs wave-shaping resistance | | 0 | | 100 | kΩ |
| High-level output current, $I_{OH}$ | Driver | −40 | | | mA |
| | Receiver | −8 | | | |
| Low-level output current, $I_{OL}$ | Driver | | | 48 | mA |
| | Receiver | | | 8 | |
| Operating free-air temperature, $T_A$ | | −40 | | 125 | °C |

§ The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## driver electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Bus output voltage | Dominant | | $V_I$ = 0 V, See Figure 1 and Figure 3 | | CANH | 2.45 | | $V_{CC}$ | V |
| | | | | | | CANL | 0.5 | | 1.25 | |
| $V_{OL}$ | | Recessive | | $V_I$ = 3 V, See Figure 1 and Figure 3 | | CANH | | 2.3 | | |
| | | | | | | CANL | | 2.3 | | |
| $V_{OD(D)}$ | Differential output voltage | Dominant | | $V_I$ = 0 V, | See Figure 1 | | 1.5 | 2 | 3 | V |
| | | | | $V_I$ = 0 V, | See Figure 2 | | 1.2 | 2 | 3 | |
| $V_{OD(R)}$ | | Recessive | | $V_I$ = 3 V, | See Figure 1 | | −120 | 0 | 12 | mV |
| | | | | $V_I$ = 3 V, | No load | | −0.5 | −0.2 | 0.05 | V |
| $I_{IH}$ | High-level input current | | | $V_I$ = 2 V | | | −30 | | | μA |
| $I_{IL}$ | Low-level input current | | | $V_I$ = 0.8 V | | | −30 | | | μA |
| $I_{OS}$ | Short-circuit output current | | | $V_{CANH}$ = −2 V | | | −250 | | 250 | mA |
| | | | | $V_{CANL}$ = 7 V | | | −250 | | 250 | |
| $C_o$ | Output capacitance | | | See receiver | | | | | | |
| $I_{CC}$ | Supply current | Standby | SN65HVD230Q | $V_{(RS)}$ = $V_{CC}$ | | | | 370 | 600 | μA |
| | | Sleep | SN65HVD231Q | | | | | 0.1 | | |
| | | All devices | Dominant | $V_I$ = 0 V, | No load | Dominant | | 10 | 17 | mA |
| | | | Recessive | $V_I$ = $V_{CC}$, | No load | Recessive | | 10 | 17 | |

† All typical values are at 25°C and with a 3.3-V supply.

## driver switching characteristics at $T_A$ = 25°C (unless otherwise noted)

### SN65HVD230Q and SN65HVD231Q

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $V_{(RS)}$ = 0 V | $C_L$ = 50 pF, See Figure 4 | | 35 | 85 | ns |
| | | $R_S$ with 10 kΩ to ground | | | 70 | 125 | |
| | | $R_S$ with 100 kΩ to ground | | | 500 | 870 | |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | $V_{(RS)}$ = 0 V | | | 70 | 120 | ns |
| | | $R_S$ with 10 kΩ to ground | | | 130 | 180 | |
| | | $R_S$ with 100 kΩ to ground | | | 870 | 1200 | |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{P(HL)} - t_{P(LH)} \rvert$) | $V_{(RS)}$ = 0 V | | | 35 | | ns |
| | | $R_S$ with 10 kΩ to ground | | | 60 | | |
| | | $R_S$ with 100 kΩ to ground | | | 370 | | |
| $t_r$ | Differential output signal rise time | $V_{(RS)}$ = 0 V | | 25 | 50 | 100 | ns |
| $t_f$ | Differential output signal fall time | | | 40 | 55 | 80 | ns |
| $t_r$ | Differential output signal rise time | $R_S$ with 10 kΩ to ground | | 80 | 120 | 160 | ns |
| $t_f$ | Differential output signal fall time | | | 80 | 125 | 150 | ns |
| $t_r$ | Differential output signal rise time | $R_S$ with 100 kΩ to ground | | 600 | 800 | 1200 | ns |
| $t_f$ | Differential output signal fall time | | | 600 | 825 | 1000 | ns |

## driver switching characteristics at $T_A$ = 25°C (unless otherwise noted)

### SN65HVD232Q

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 50 pF, See Figure 4 | | 35 | 85 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 70 | 120 | ns |
| $t_{sk(p)}$ | Pulse skew ($\|t_{P(HL)} - t_{P(LH)}\|$) | | | 35 | | ns |
| $t_r$ | Differential output signal rise time | | 25 | 50 | 100 | ns |
| $t_f$ | Differential output signal fall time | | 40 | 55 | 80 | ns |

## receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | See Table 1 | | | 750 | 900 | mV |
| $V_{IT-}$ | Negative-going input threshold voltage | | | 500 | 650 | | mV |
| $V_{hys}$ | Hysteresis voltage ($V_{IT+} - V_{IT-}$) | | | | 100 | | |
| $V_{OH}$ | High-level output voltage | $-6\ V \le V_{ID} \le 500$ mV, $I_O$ = –8 mA, See Figure 5 | | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | 900 mV ≤ $V_{ID}$ ≤ 6 V, $I_O$ = 8 mA, See Figure 5 | | | | 0.4 | |
| $I_I$ | Bus input current | $V_{IH}$ = 7 V | Other input at 0 V, D = 3 V | 100 | | 250 | µA |
| | | $V_{IH}$ = 7 V, $V_{CC}$ = 0 V | | 100 | | 350 | |
| | | $V_{IH}$ = –2 V | | –200 | | –30 | µA |
| | | $V_{IH}$ = –2 V, $V_{CC}$ = 0 V | | –100 | | –20 | |
| $C_i$ | CANH, CANL input capacitance | Pin-to-ground, $V_I$ = 0.4 sin(4E6πt) + 0.5 V | $V_{(D)}$ = 3 V, | | 32 | | pF |
| $C_{diff}$ | Differential input capacitance | Pin-to-pin, $V_I$ = 0.4 sin(4E6πt) + 0.5 V | $V_{(D)}$ = 3 V, | | 16 | | pF |
| $R_{diff}$ | Differential input resistance | Pin-to-pin, $V_{(D)}$ = 3 V | | 40 | 70 | 100 | kΩ |
| $R_T$ | CANH, CANL input resistance | | | 20 | 35 | 50 | kΩ |
| $I_{CC}$ | Supply current | See driver | | | | | |

† All typical values are at 25°C and with a 3.3-V supply.

## receiver switching characteristics at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | | See Figure 6 | | 35 | 50 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 35 | 50 | ns |
| $t_{sk(p)}$ | Pulse skew ($\|t_{P(HL)} - t_{P(LH)}\|$) | | | | | 10 | ns |
| $t_r$ | Output signal rise time | | See Figure 6 | | 1.5 | | ns |
| $t_f$ | Output signal fall time | | | | 1.5 | | ns |
| $t_{(loop)}$ | Total loop delay, driver input to receiver output | $V_{(RS)}$ = 0 V | | | 70 | 135 | ns |
| $t_{(loop)}$ | Total loop delay, driver input to receiver output | $R_S$ with 10 kΩ to ground | | | 105 | 175 | |
| $t_{(loop)}$ | Total loop delay, driver input to receiver output | $R_S$ with 100 kΩ to ground | | | 535 | 920 | |

**device control-pin characteristics over recommended operating conditions (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(WAKE)}$ | SN65HVD230Q wake-up time from standby mode with $R_S$ | See Figure 8 | | 0.55 | 1.5 | µS |
| | SN65HVD231Q wake-up time from sleep mode with $R_S$ | | | | 3 | µS |
| $V_{ref}$ | Reference output voltage | $-5\ \mu A < I_{(Vref)} < 5\ \mu A$ | 0.45 $V_{CC}$ | | 0.55 $V_{CC}$ | V |
| | | $-50\ \mu A < I_{(Vref)} < 50\ \mu A$ | 0.4 $V_{CC}$ | | 0.6 $V_{CC}$ | |
| $I_{(RS)}$ | Input current for high-speed | $V_{(RS)} < 1$ V | −450 | | 0 | µA |

† All typical values are at 25°C and with a 3.3 V supply.

## PARAMETER MEASUREMENT INFORMATION

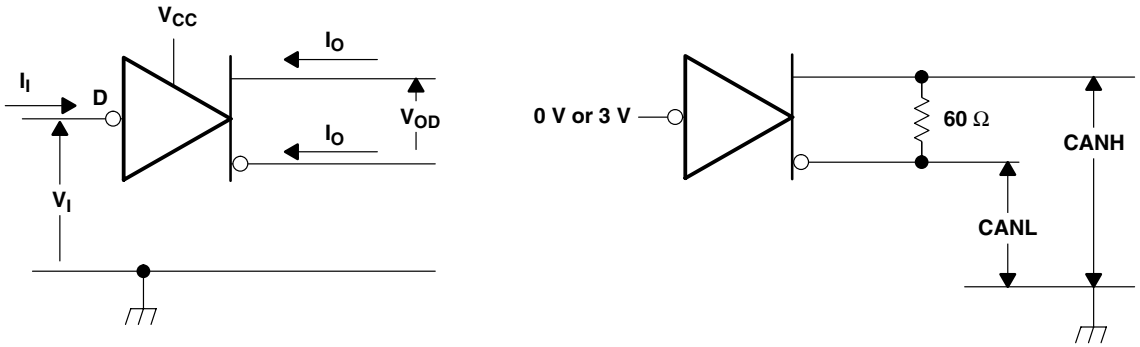



**Figure 1. Driver Voltage and Current Definitions**

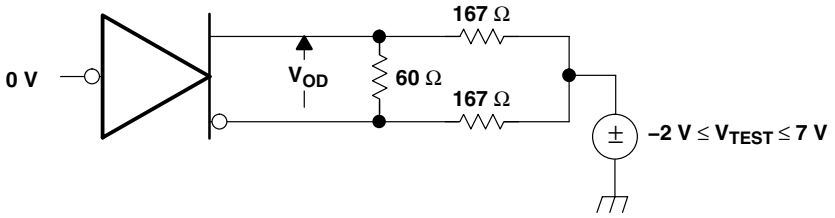



**Figure 2. Driver $V_{OD}$**

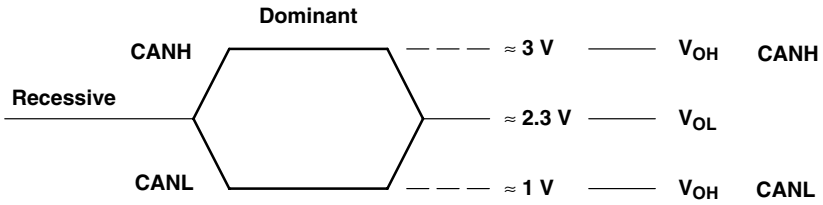
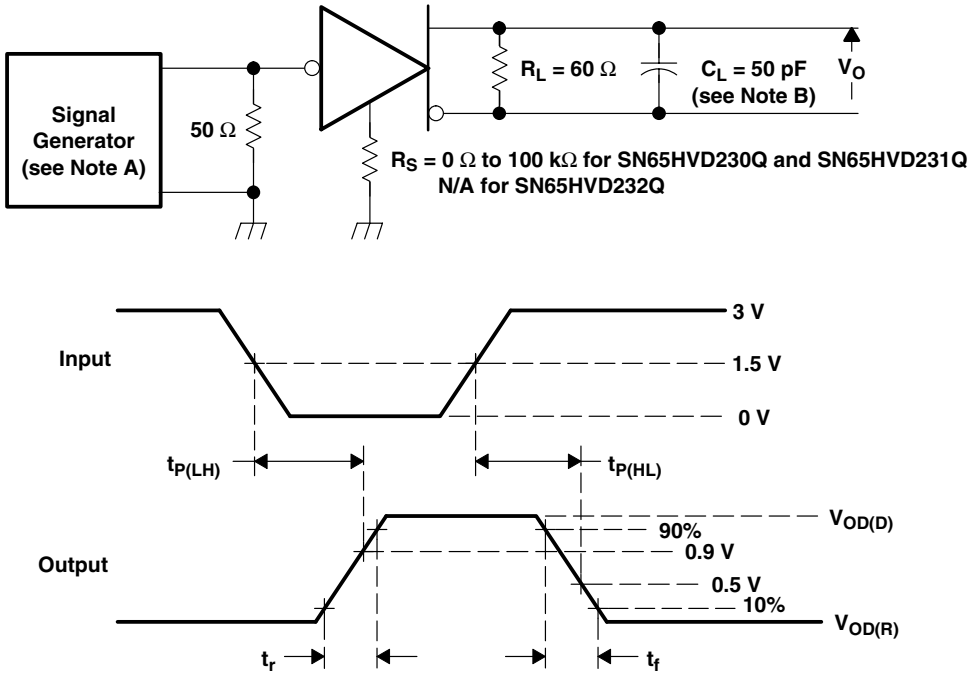



**Figure 3. Driver Output Voltage Definitions**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_o$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 4. Driver Test Circuit and Voltage Waveforms**

$$V_{IC} = \frac{V_{CANH} + V_{CANL}}{2}$$

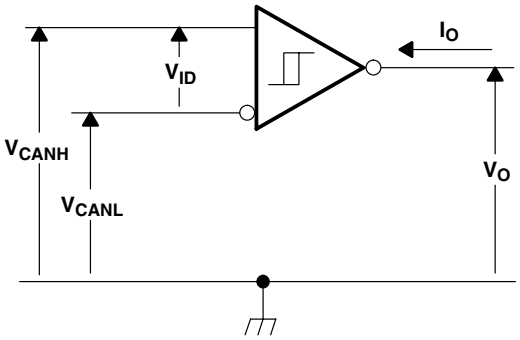
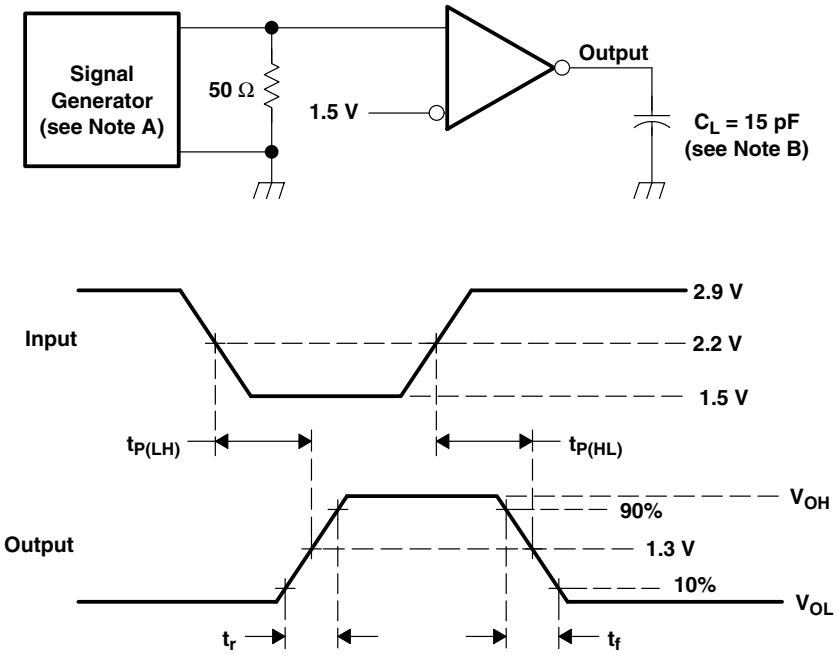



**Figure 5. Receiver Voltage and Current Definitions**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, Zo = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 6. Receiver Test Circuit and Voltage Waveforms**

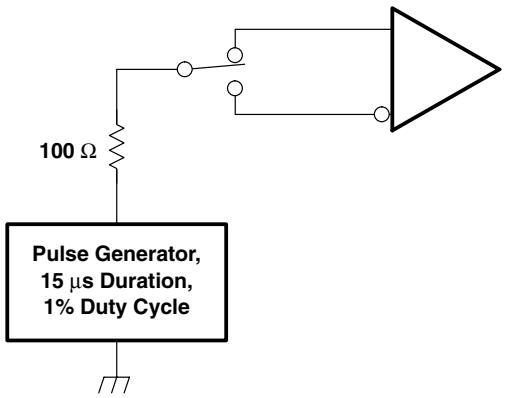



**Figure 7. Overvoltage Protection**

## PARAMETER MEASUREMENT INFORMATION

**Table 1. Receiver Characteristics Over Common Mode With V(RS) at 1.2 V**

| $V_{IC}$ | $V_{ID}$ | $V_{CANH}$ | $V_{CANL}$ | R OUTPUT | |
|---|---|---|---|---|---|
| –2 V | 900 mV | –1.55 V | –2.45 V | L | $V_{OL}$ |
| 7 V | 900 mV | 8.45 V | 6.55 V | L | |
| 1 V | 6 V | 4 V | –2 V | L | |
| 4 V | 6 V | 7 V | 1 V | L | |
| –2 V | 500 mV | –1.75 V | –2.25 V | H | $V_{OH}$ |
| 7 V | 500 mV | 7.25 V | 6.75 V | H | |
| 1 V | –6 V | –2 V | 4 V | H | |
| 4 V | –6 V | 1 V | 7 V | H | |
| X | X | Open | Open | H | |

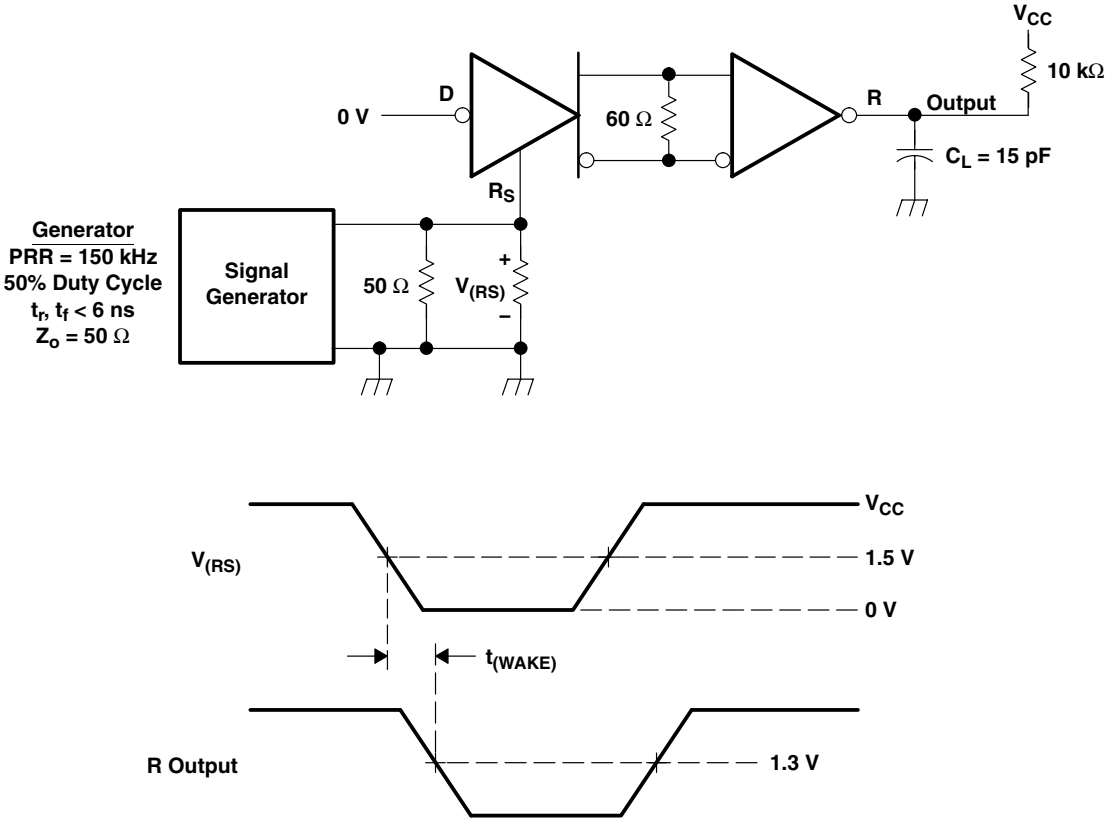



**Figure 8. $t_{(WAKE)}$ Test Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS

SUPPLY CURRENT (RMS)
vs
FREQUENCY

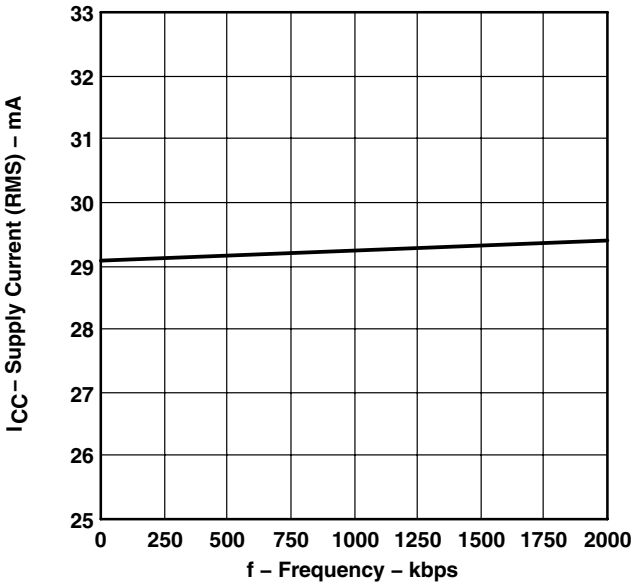



Figure 9

LOGIC INPUT CURRENT (D PIN)
vs
INPUT VOLTAGE

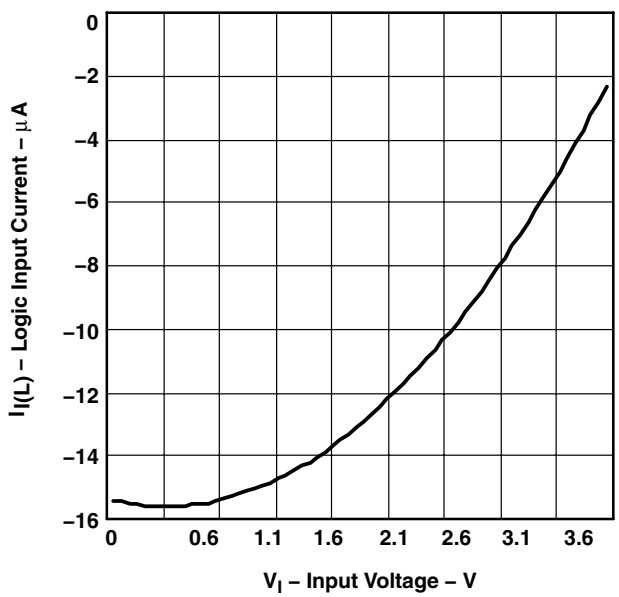



Figure 10

BUS INPUT CURRENT
vs
BUS INPUT VOLTAGE

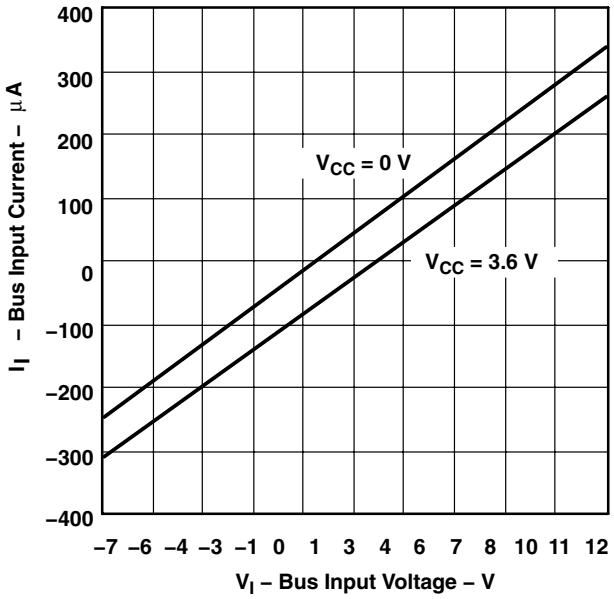



Figure 11

DRIVER LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

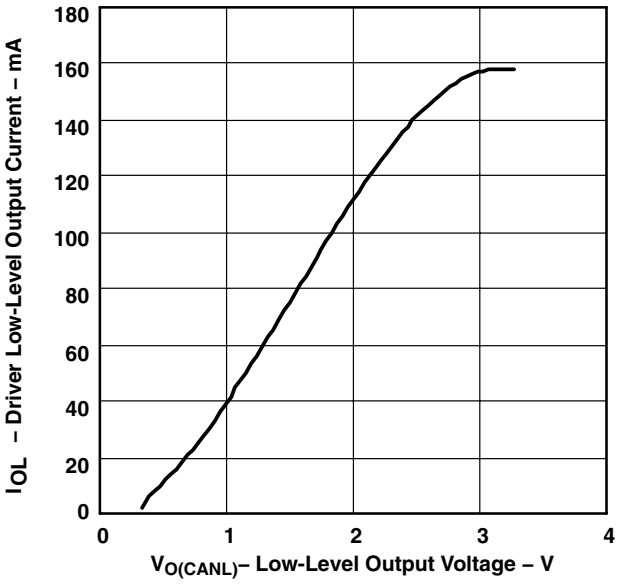



Figure 12

## TYPICAL CHARACTERISTICS

**DRIVER HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE**

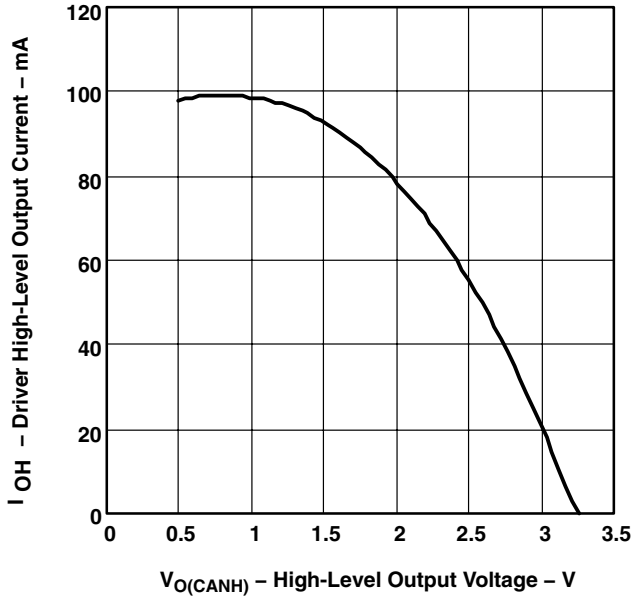



**Figure 13**

**DOMINANT VOLTAGE ($V_{OD}$) vs FREE-AIR TEMPERATURE**

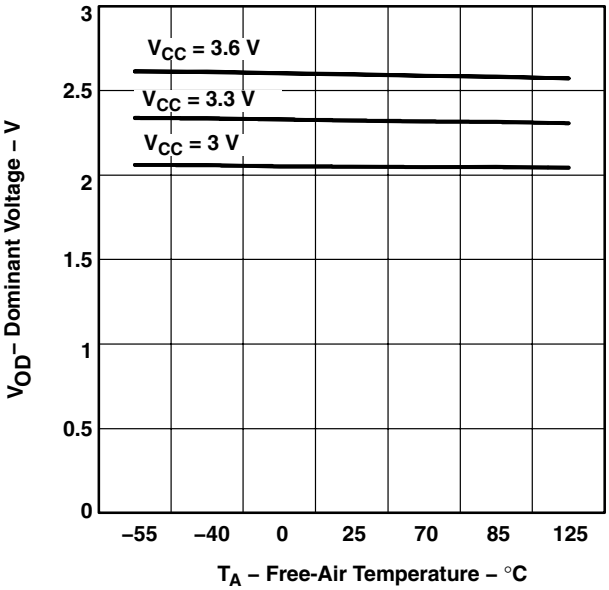



**Figure 14**

**RECEIVER LOW-TO-HIGH PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE**

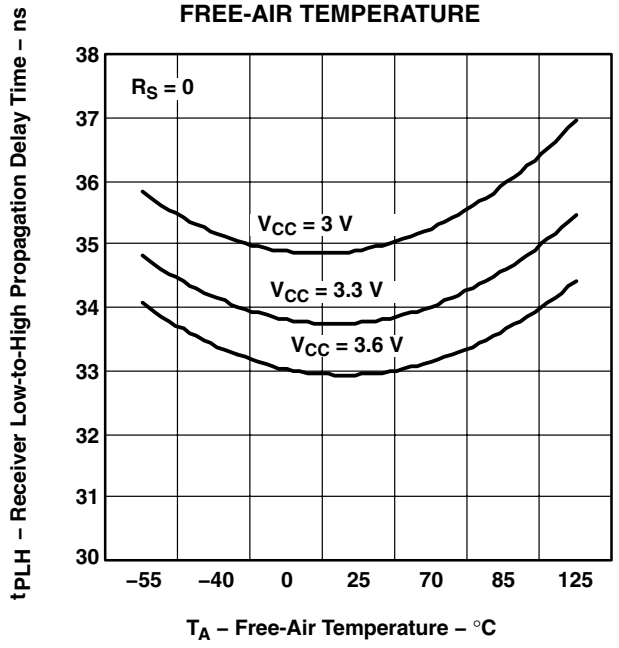



**Figure 15**

**RECEIVER HIGH-TO-LOW PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE**

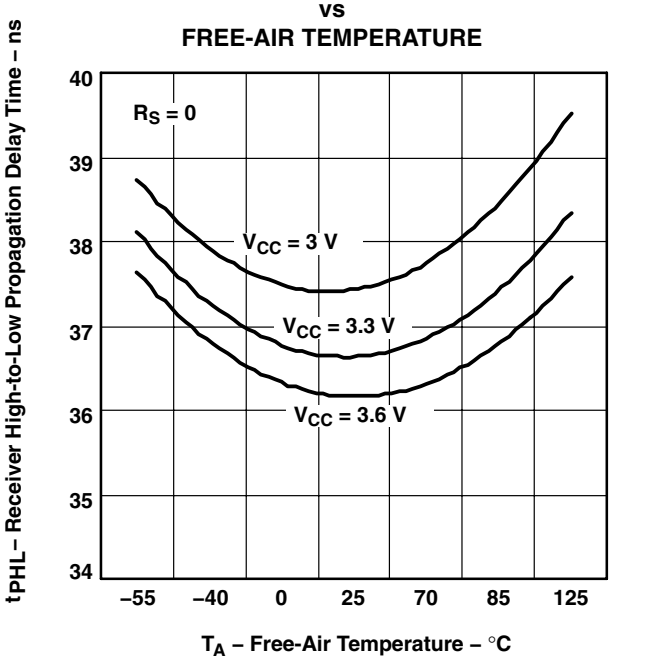



**Figure 16**

## TYPICAL CHARACTERISTICS

**DRIVER LOW-TO-HIGH PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE**

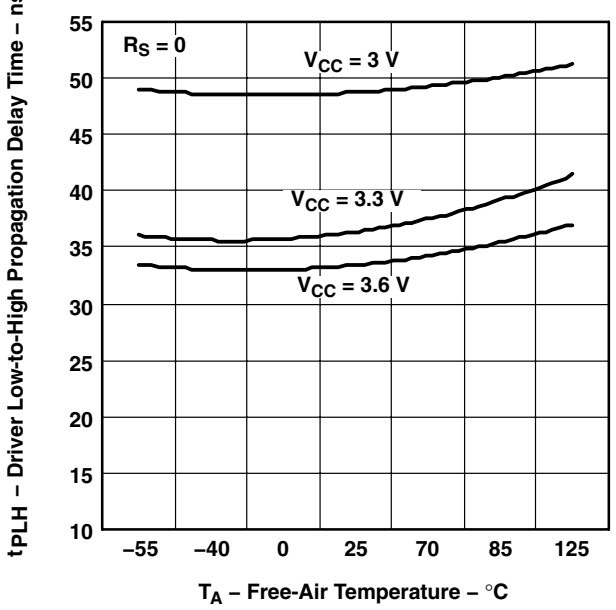



**Figure 17**

**DRIVER HIGH-TO-LOW PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE**

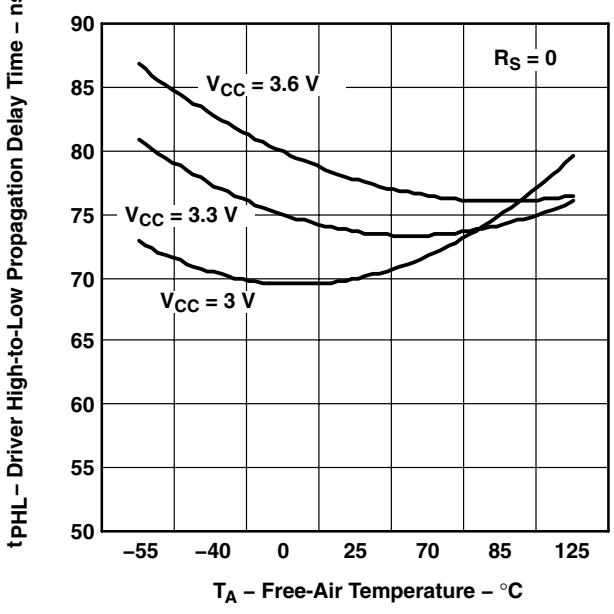



**Figure 18**

**DRIVER LOW-TO-HIGH PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE**

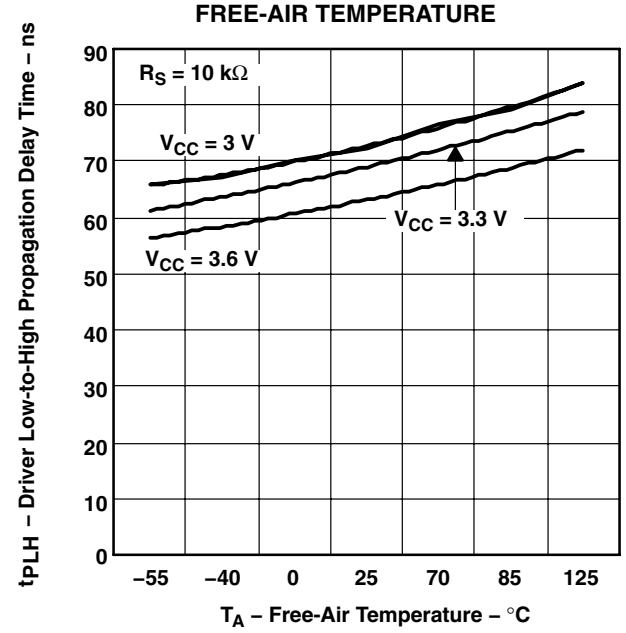



**Figure 19**

**DRIVER HIGH-TO-LOW PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE**

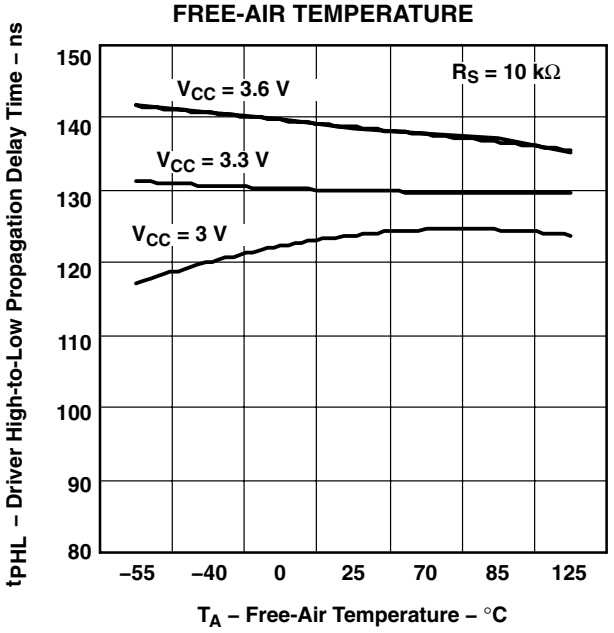



**Figure 20**

## TYPICAL CHARACTERISTICS

**DRIVER LOW-TO-HIGH PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE**

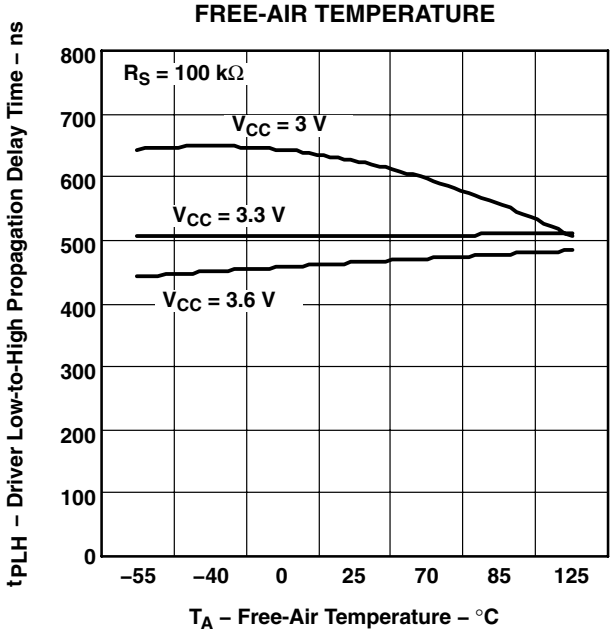



Figure 21

**DRIVER HIGH-TO-LOW PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE**

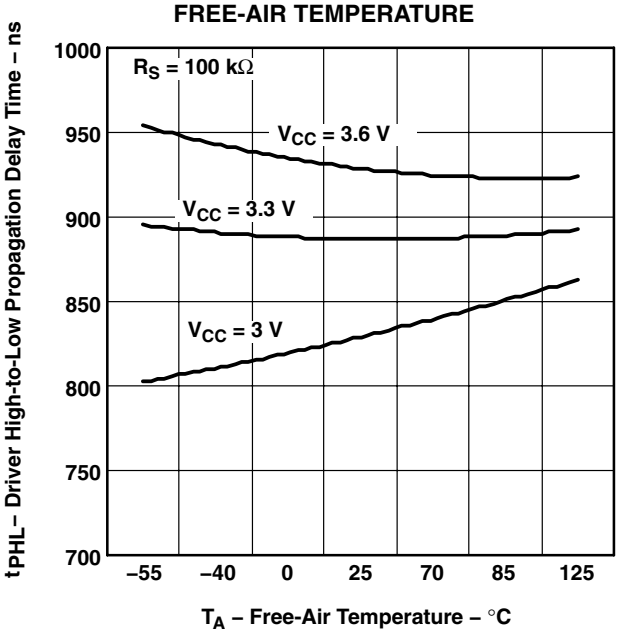



Figure 22

**DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE**

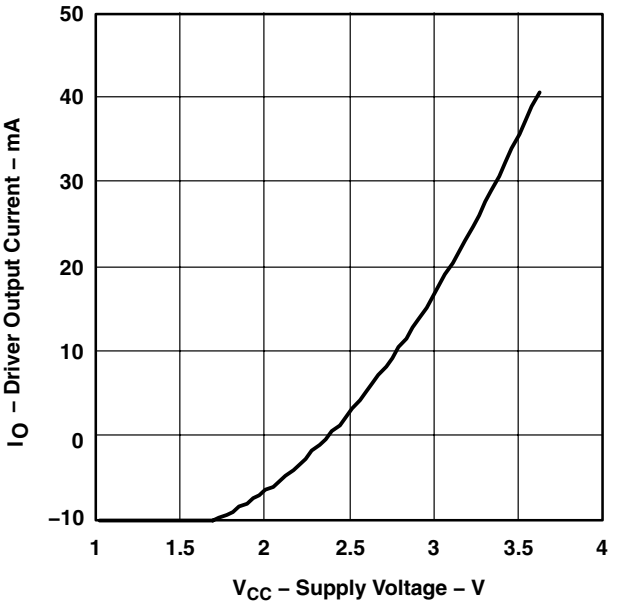



Figure 23

**DIFFERENTIAL DRIVER OUTPUT FALL TIME vs Source Resistance ($R_S$)**

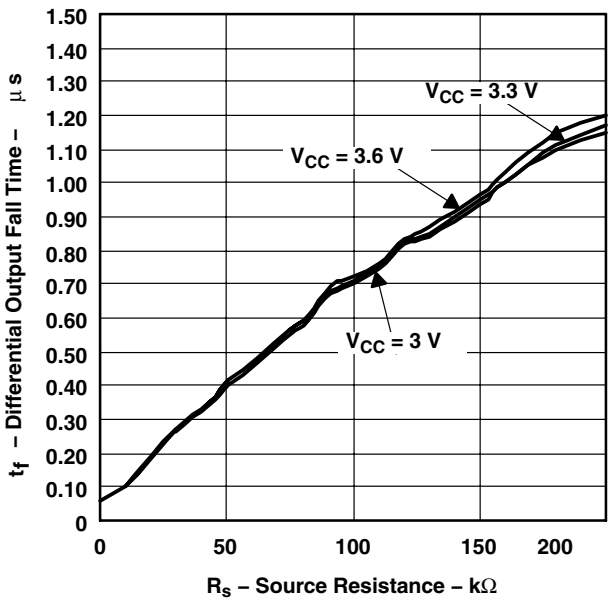



Figure 24

## TYPICAL CHARACTERISTICS

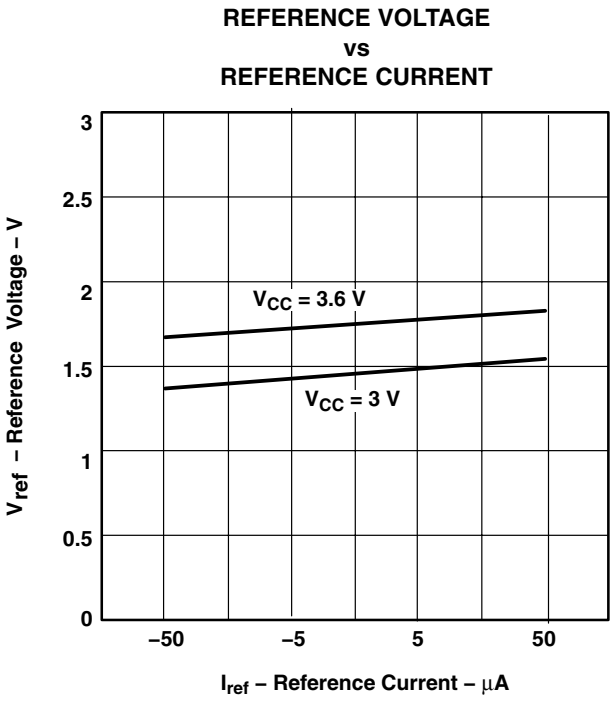



**Figure 25**

## APPLICATION INFORMATION

This application provides information concerning the implementation of the physical medium attachment layer in a CAN network according to the ISO 11898 standard. It presents a typical application circuit and test results, as well as discussions on slope control, total loop delay, and interoperability in 5-V systems.

### introduction

ISO 11898 is the international standard for high-speed serial communication using the controller area network (CAN) bus protocol. It supports multimaster operation, real-time control, programmable data rates up to 1 Mbps, and powerful redundant error checking procedures that provide reliable data transmission. It is suited for networking *intelligent* devices as well as sensors and actuators within the rugged electrical environment of a machine chassis or factory floor. The SN65HVD230Q family of 3.3-V CAN transceivers implement the lowest layers of the ISO/OSI reference model. This is the interface with the physical signaling output of the CAN controller of the Texas Instruments TMS320Lx240x 3.3-V DSPs, as illustrated in Figure 26.

## APPLICATION INFORMATION

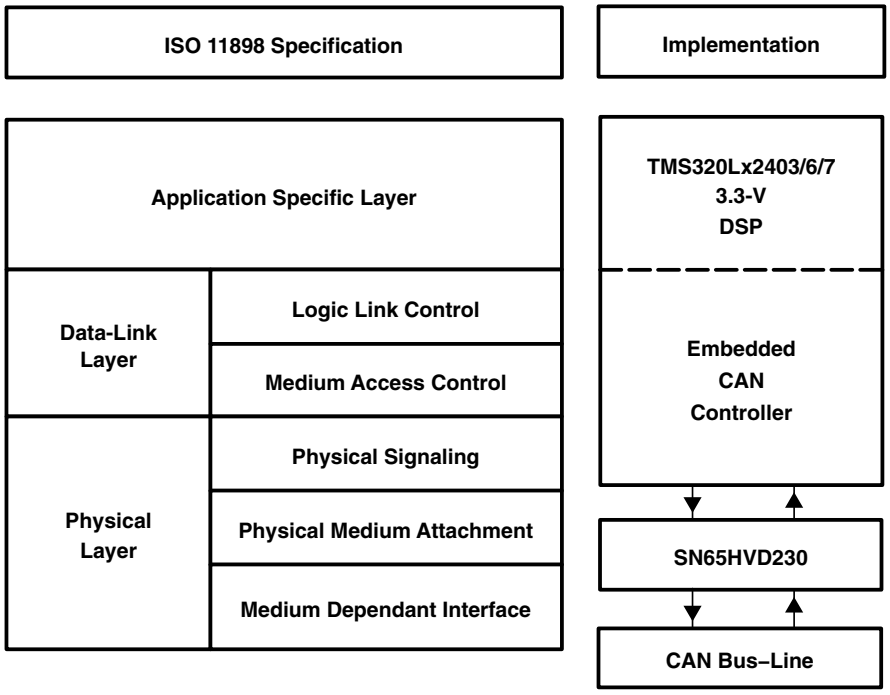



**Figure 26. The Layered ISO 11898 Standard Architecture**

The SN65HVD230Q family of CAN transceivers are compatible with the ISO 11898 standard; this ensures interoperability with other standard-compliant products.

### application of the SN65HVD230Q

Figure 27 illustrates a typical application of the SN65HVD230Q family. The output of a DSP's CAN controller is connected to the serial driver input, pin D, and receiver serial output, pin R, of the transceiver. The transceiver is then attached to the differential bus lines at pins CANH and CANL. Typically, the bus is a twisted pair of wires with a characteristic impedance of 120 Ω, in the standard half-duplex multipoint topology of Figure 28. Each end of the bus is terminated with 120-Ω resistors in compliance with the standard to minimize signal reflections on the bus.

## APPLICATION INFORMATION

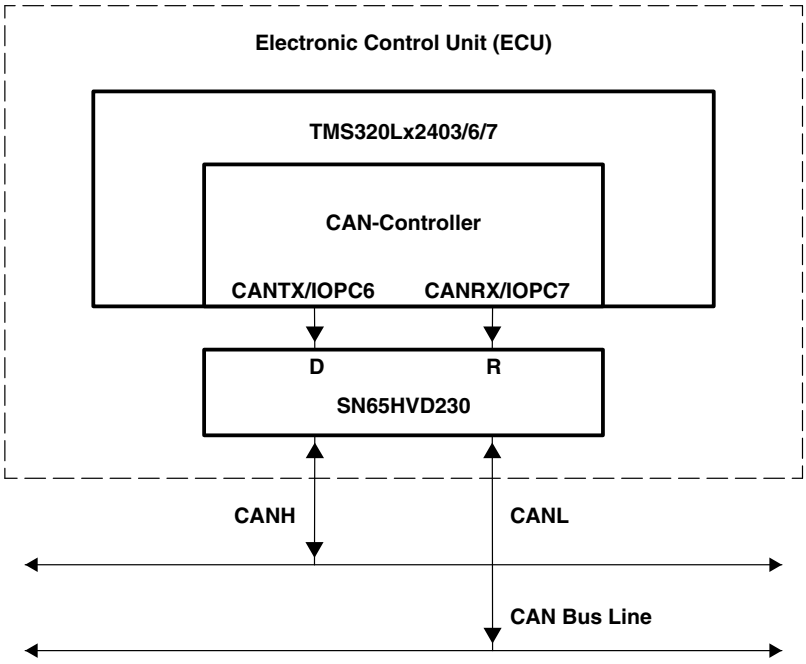



**Figure 27. Details of a Typical CAN Node**

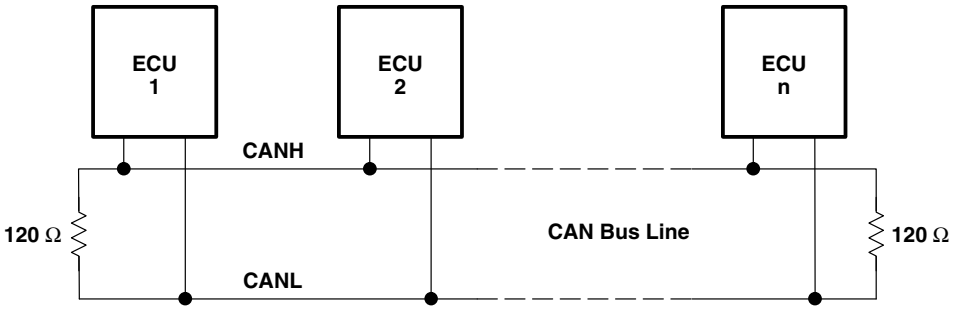



**Figure 28. Typical CAN Network**

The SN65HVD230Q/231Q/232Q 3.3-V CAN transceivers provide the interface between the 3.3-V TMS320Lx2403/6/7 CAN DSPs and the differential bus line, and are designed to transmit data at signaling rates up to 1 Mbps as defined by the ISO 11898 standard.

### features of the SN65HVD230Q, SN65HVD231Q, and SN65HVD232Q

The SN65HVD230Q/231Q/232Q are pin-compatible (but not functionally identical) with one another and, depending upon the application, may be used with identical circuit boards.

These transceivers feature 3.3-V operation and standard compatibility with signaling rates up to 1 Mbps, and also offer 16-kV HBM ESD protection on the bus pins, thermal shutdown protection, bus fault protection, and open-circuit receiver failsafe. The failsafe design of the receiver assures a logic high at the receiver output if the bus wires become open circuited. If a high ambient operating environment temperature or excessive output current result in thermal shutdown, the bus pins become high impedance, while the D and R pins default to a logic high.

## APPLICATION INFORMATION

### features of the SN65HVD230Q, SN65HVD231Q, and SN65HVD232Q (continued)

The bus pins are also maintained in a high-impedance state during low $V_{CC}$ conditions to ensure glitch-free power-up and power-down bus protection for hot-plugging applications. This high-impedance condition also means that an unpowered node will not disturb the bus. Transceivers without this feature usually have a very low output impedance. This results in a high current demand when the transceiver is unpowered, a condition that could affect the entire bus.

### operating modes

$R_S$ (pin 8) of the SN65HVD230Q and SN65HVD231Q provides for three different modes of operation: high-speed mode, slope-control mode, and low-power standby mode.

#### high-speed mode

The high-speed mode can be selected by applying a logic low to Rs (pin 8). The high-speed mode of operation is commonly employed in industrial applications. High-speed allows the output to switch as fast as possible with no internal limitation on the output rise and fall slopes. The only limitations of the high-speed operation are cable length and radiated emission concerns, each of which is addressed by the slope control mode of operation.

If the low-power standby mode is to be employed in the circuit, direct connection to a DSP output pin can be used to switch between a logic-low level (< 1 V) for high speed mode operation, and the logic-high level (> 0.75 $V_{CC}$) for standby mode operation. Figure 29 shows a typical DSP connection, and Figure 30 shows the SN65HVD230Q driver output signal in high-speed mode on the CAN bus.


**Figure 29. $R_S$ (Pin 8) Connection to a TMS320LF2406/07 for High-Speed or Standby Mode Operation**

## APPLICATION INFORMATION

### high-speed mode (continued)

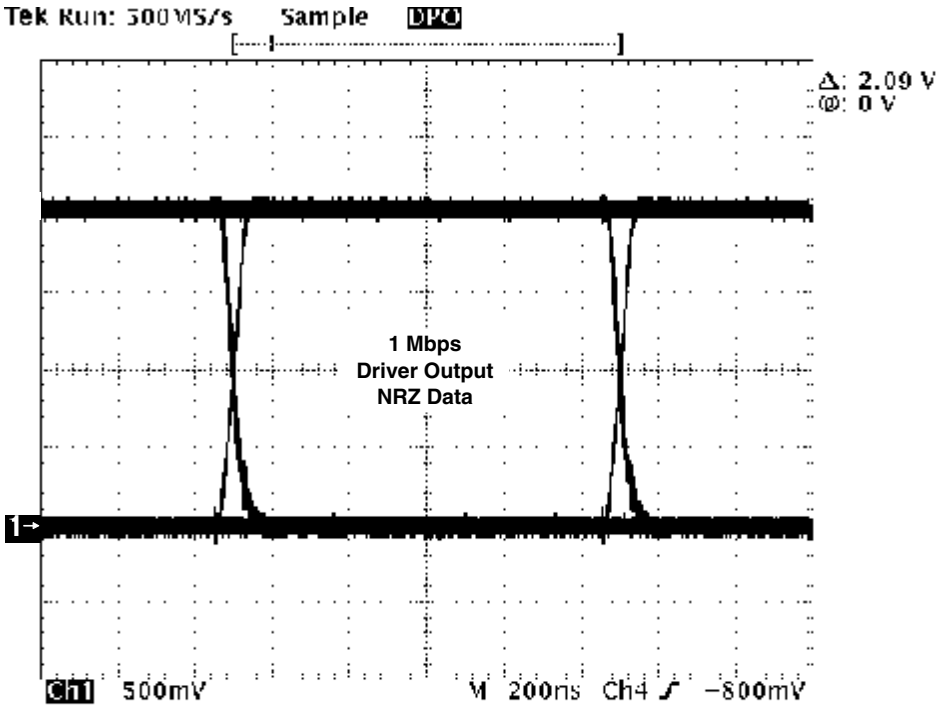



**Figure 30. Typical SN65HVD230Q High-Speed Mode Output Waveform Into a 60-Ω Load**

### slope-control mode

Electromagnetic compatibility is essential in many applications using unshielded bus cable to reduce system cost. To reduce the electromagnetic interference generated by fast rise times and resulting harmonics, the rise and fall slopes of the SN65HVD230Q and SN65HVD231Q driver outputs can be adjusted by connecting a resistor from $R_S$ (pin 8) to ground or to a logic low voltage, as shown in Figure 31. The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 kΩ to achieve a ≈ 15 V/μs slew rate, and up to 100 kΩ to achieve a ≈ 2.0 V/μs slew rate as displayed in Figure 32. Typical driver output waveforms from a pulse input signal with and without slope control are displayed in Figure 33. A pulse input is used rather than NRZ data to clearly display the actual slew rate.

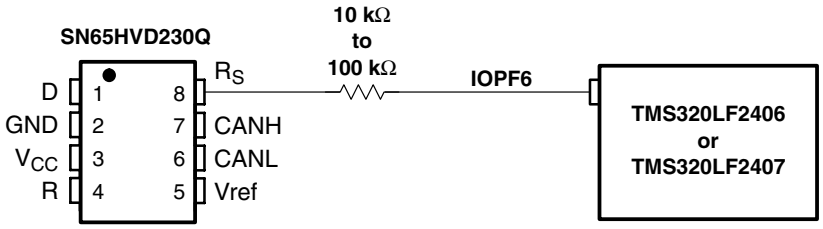



**Figure 31. Slope-Control or Standby Mode Connection to a DSP**

## APPLICATION INFORMATION

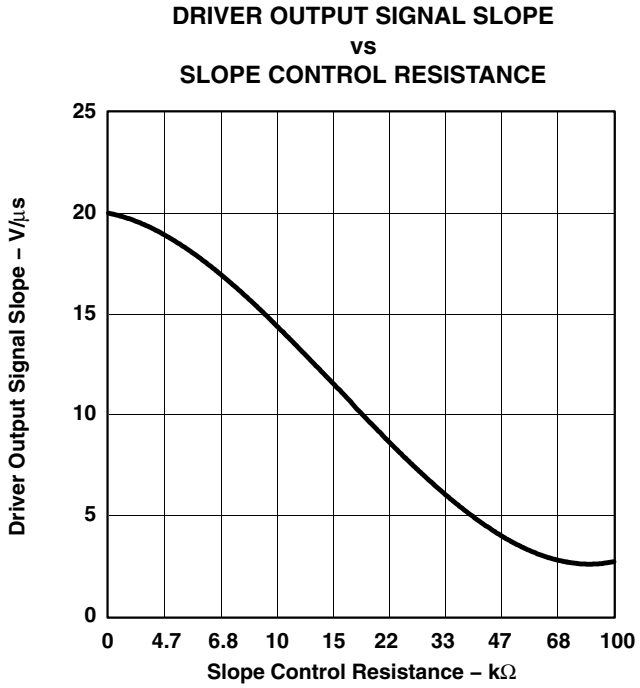



**Figure 32. SN65HVD230Q Driver Output Signal Slope vs Slope Control Resistance Value**

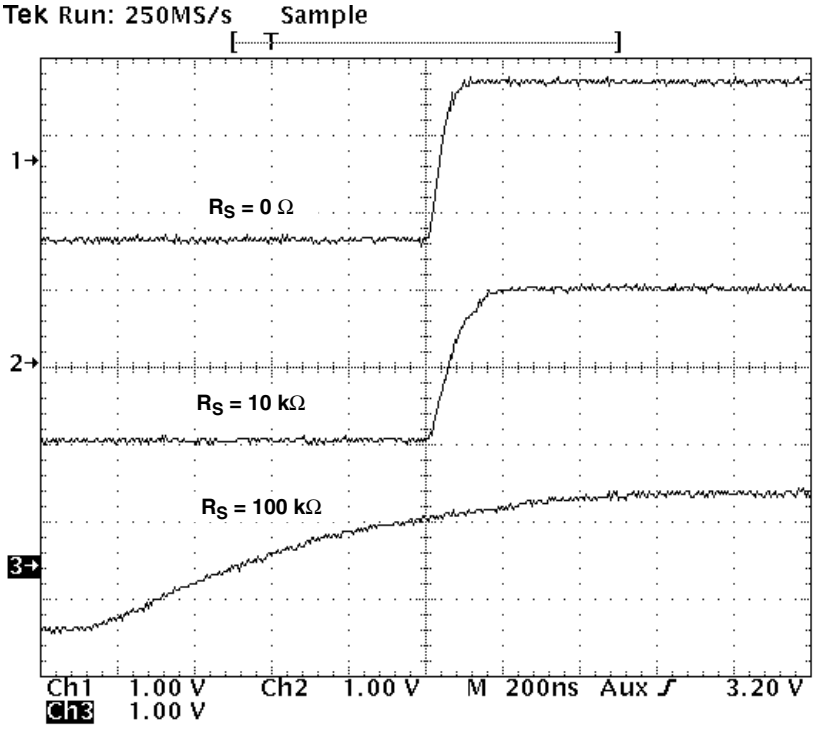



**Figure 33. Typical SN65HVD230Q 250-kbps Output Pulse Waveforms With Slope Control**

## APPLICATION INFORMATION

### standby mode (listen only mode) of the SN65HVD230Q

If a logic high (> 0.75 $V_{CC}$) is applied to $R_S$ (pin 8) in Figures 29 and 31, the circuit of the SN65HVD230Q enters a low-current, *listen only* standby mode during which the driver is switched off and the receiver remains active. In this *listen only* state, the transceiver is completely passive to the bus. It makes no difference if a slope control resistor is in place as shown in Figure 31. The DSP can reverse this low-power standby mode when the rising edge of a dominant state (bus differential voltage > 900 mV typical) occurs on the bus. The DSP, sensing bus activity, reactivates the driver circuit by placing a logic low (< 1.2 V) on $R_S$ (pin 8).

### the babbling idiot protection of the SN65HVD231Q

Occasionally, a runaway CAN controller unintentionally sends messages that completely tie up the bus (what is referred to in CAN jargon as a babbling idiot). When this occurs, the DSP can engage the *listen-only* standby mode to disengage the driver and release the bus, even when access to the CAN controller has been lost. When the driver circuit is deactivated, its outputs default to a high-impedance state.

### sleep mode of the SN65HVD231Q

The unique difference between the SN65HVD230Q and the SN65HVD231Q is that both driver and receiver are switched off in the SN65HVD231Q when a logic high is applied to $R_S$ (pin 8). The device remains in a very low power-sleep mode until the circuit is reactivated with a logic low applied to $R_S$ (pin 8). While in this sleep mode, the bus pins are in a high-impedance state, while the D and R pins default to a logic high.

## loop propagation delay

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input to the differential outputs, plus the delay from the receiver inputs to its output.

The loop delay of the transceiver displayed in Figure 34 increases accordingly when slope control is being used. This increased loop delay means that the total bus length must be reduced to meet the CAN bit-timing requirements of the overall system. The loop delay becomes ≈100 ns when employing slope control with a 10-kΩ resistor, and ≈500 ns with a 100-kΩ resistor. Therefore, considering that the rule-of-thumb propagation delay of typical bus cable is 5 ns/m, slope control with the 100-kΩ resistor decreases the allowable bus length by the difference between the 500-ns max loop delay and the loop delay with no slope control, 70.7 ns. This equates to (500–70.7 ns)/5 ns, or approximately 86 m less bus length. This slew-rate/bus length trade-off to reduce electromagnetic interference to adjoining circuits from the bus can also be solved with a high-quality shielded bus cable.

## APPLICATION INFORMATION

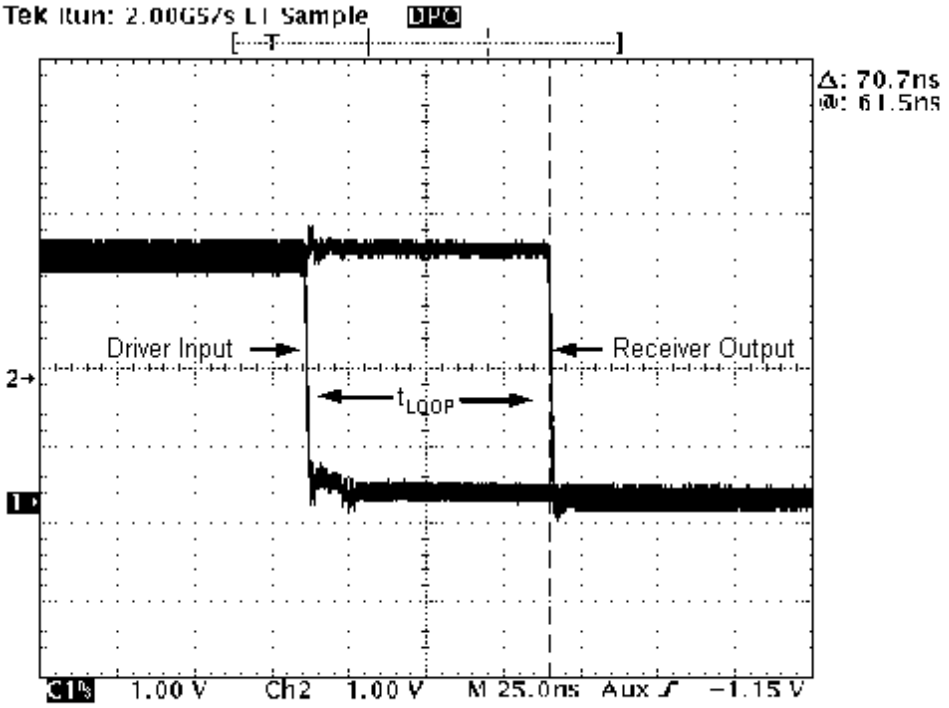



**Figure 34. 70.7-ns Loop Delay Through the SN65HVD230Q With $R_S$ = 0**

## APPLICATION INFORMATION

### interoperability with 5-V CAN systems

It is essential that the 3.3-V SN65HVD230Q family performs seamlessly with 5-V transceivers because of the large number of 5-V devices installed. Figure 35 displays a test bus of a 3.3-V node with the SN65HVD230Q, and three 5-V nodes: one for each of TI's SN65LBC031 and UC5350 transceivers, and one using a competitor X250 transceiver.

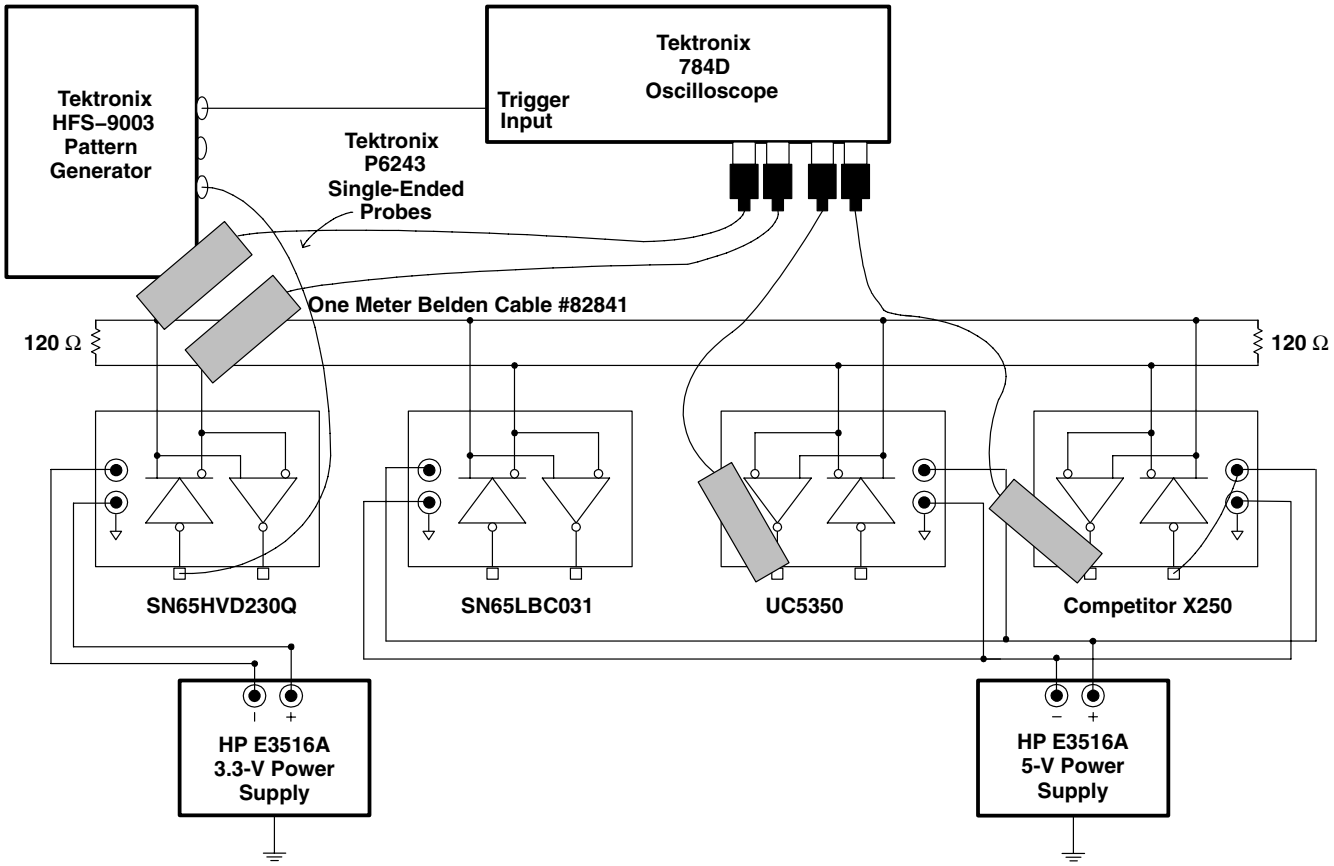



**Figure 35. 3.3-V/5-V CAN Transceiver Test Bed**

## APPLICATION INFORMATION

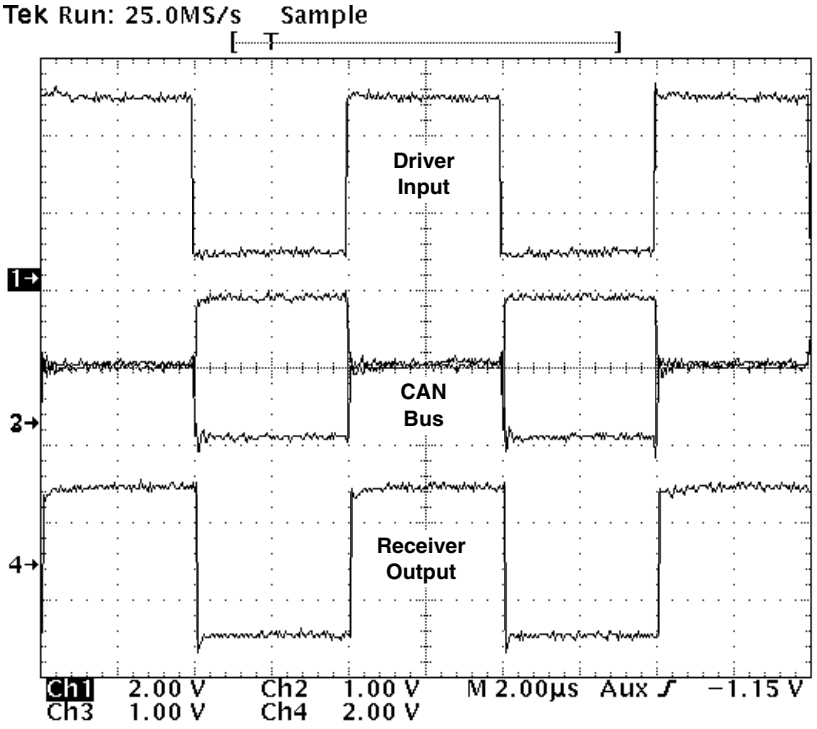



**Figure 36. SN65HVD230Q's Input, CAN Bus, and X250's RXD Output Waveforms**

Figure 36 displays the SN65HVD230Q's input signal, the CAN bus, and the competitor X250's receiver output waveforms. The input waveform from the Tektronix HFS-9003 Pattern Generator in Figure 35 to the SN65HVD230Q is a 250-kbps pulse for this test. The circuit is monitored with Tektronix P6243, 1-GHz single-ended probes in order to display the CAN dominant and recessive bus states.

Figure 36 displays the 250-kbps pulse input waveform to the SN65HVD230Q on channel 1. Channels 2 and 3 display CANH and CANL respectively, with their recessive bus states overlaying each other to clearly display the dominant and recessive CAN bus states. Channel 4 is the receiver output waveform of the competitor X250.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVD230QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HV230Q | Samples |
| SN65HVD230QDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HV230Q | Samples |
| SN65HVD230QDG4Q1 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 230Q1 | Samples |
| SN65HVD230QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HV230Q | Samples |
| SN65HVD230QDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HV230Q | Samples |
| SN65HVD230QDRG4Q1 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 230Q1 | Samples |
| SN65HVD231QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HV231Q | Samples |
| SN65HVD231QDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HV231Q | Samples |
| SN65HVD231QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HV231Q | Samples |
| SN65HVD231QDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HV231Q | Samples |
| SN65HVD231QDRG4Q1 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 231Q1 | Samples |
| SN65HVD231QDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 231Q1 | Samples |
| SN65HVD232QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HV232Q | Samples |
| SN65HVD232QDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HV232Q | Samples |
| SN65HVD232QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HV232Q | Samples |
| SN65HVD232QDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HV232Q | Samples |
| SN65HVD232QDRG4Q1 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 232Q1 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVD232QDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 232Q1 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN65HVD230Q, SN65HVD230Q-Q1, SN65HVD231Q, SN65HVD231Q-Q1, SN65HVD232Q, SN65HVD232Q-Q1 :**

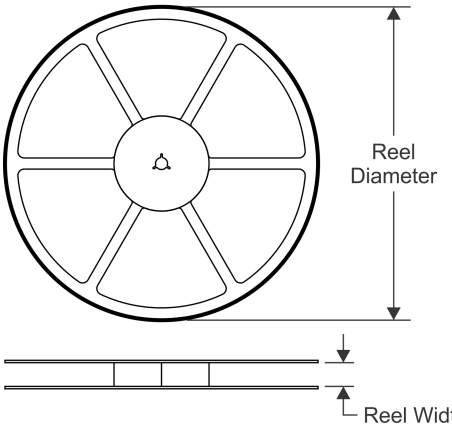
- Catalog: SN65HVD230Q, SN65HVD231Q, SN65HVD232Q
- Automotive: SN65HVD230Q-Q1, SN65HVD231Q-Q1, SN65HVD232Q-Q1

NOTE: Qualified Version Definitions:

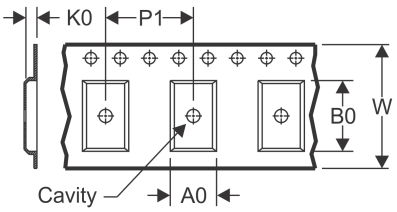
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

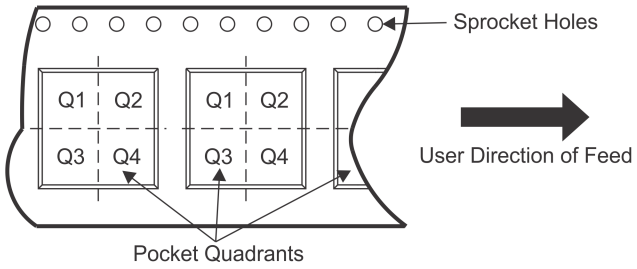



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

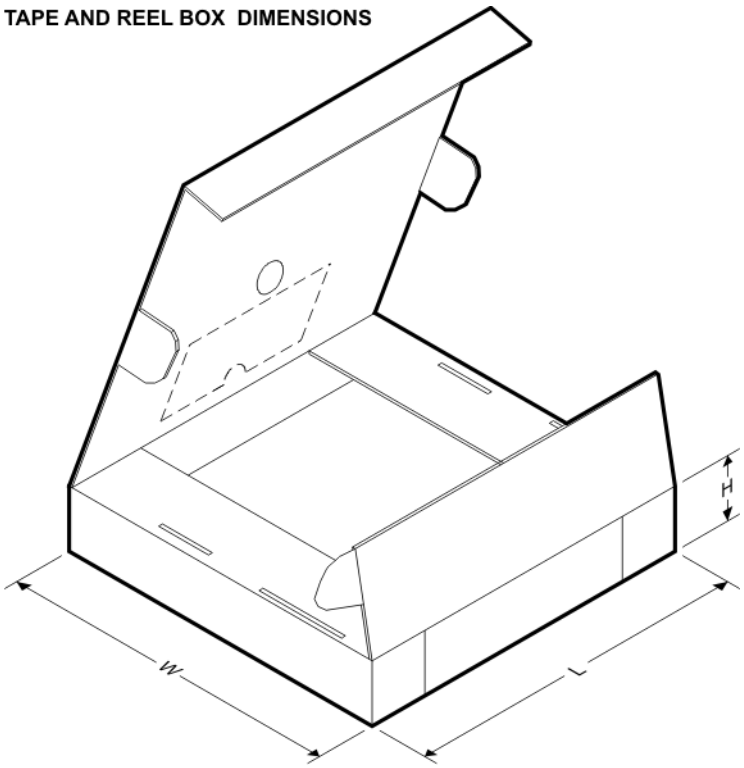
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

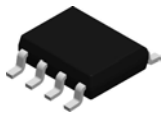
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVD230QDR | SOIC | D | 8 | 2500 | 330.0 | 12.5 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD231QDR | SOIC | D | 8 | 2500 | 330.0 | 12.5 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD232QDR | SOIC | D | 8 | 2500 | 330.0 | 12.5 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65HVD230QDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN65HVD231QDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN65HVD232QDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

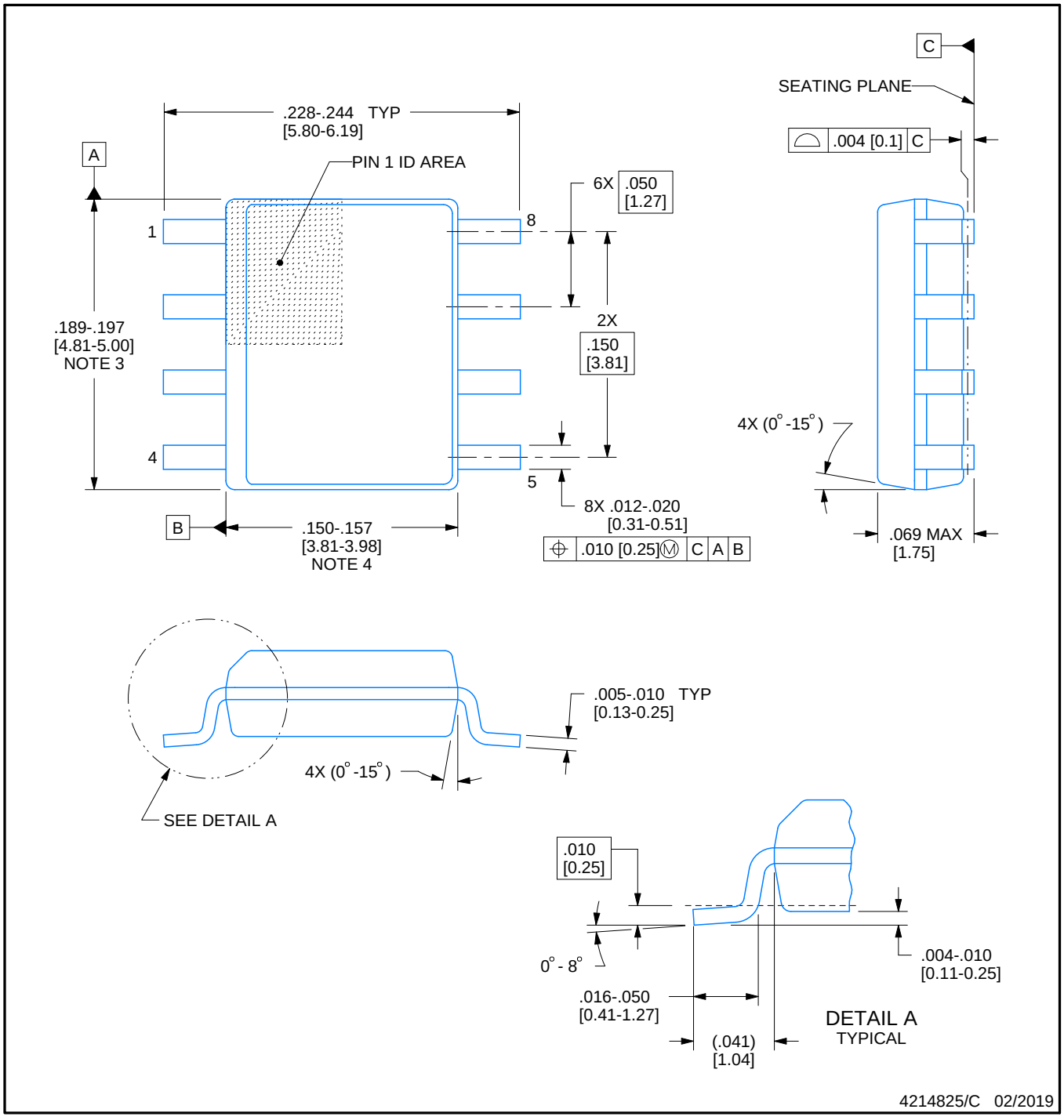


# PACKAGE OUTLINE

## D0008A

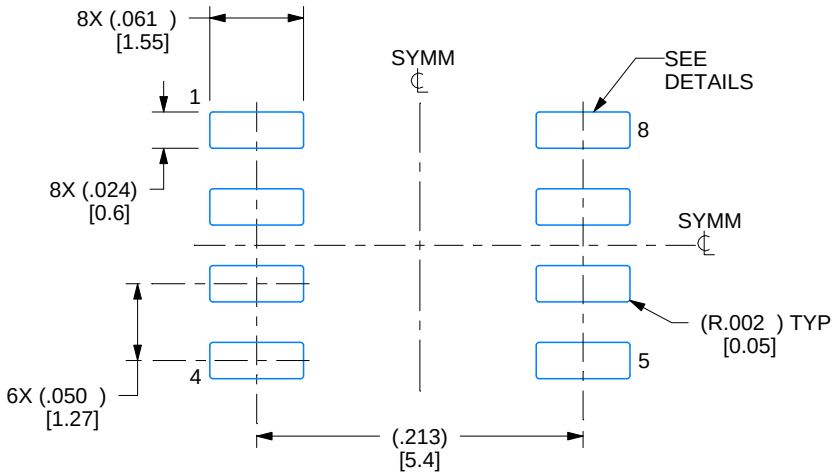
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

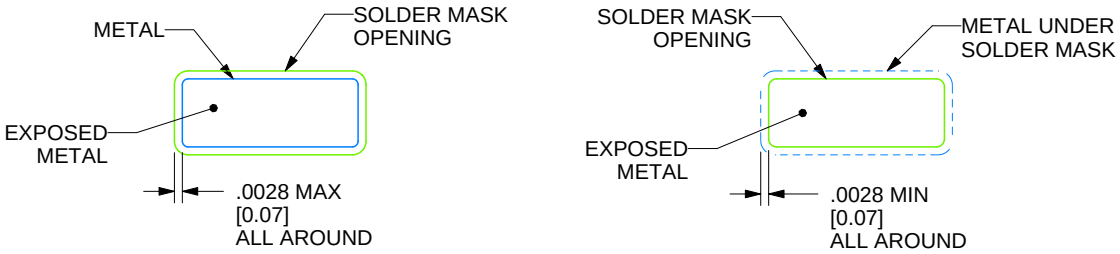



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

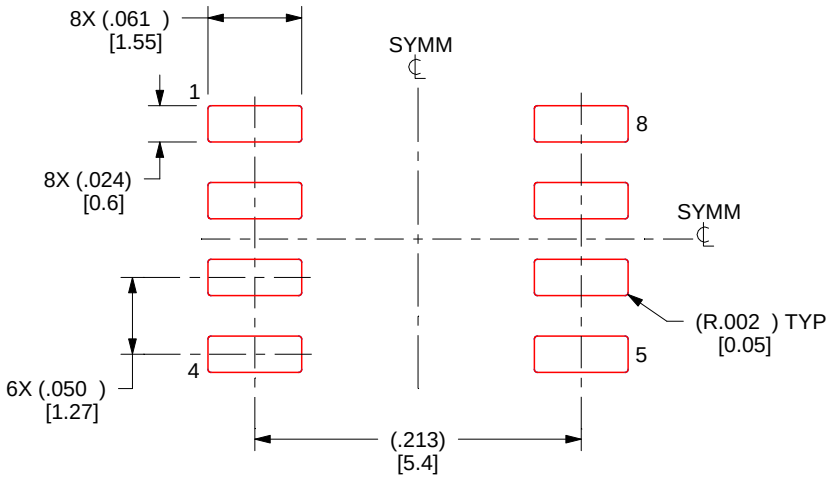
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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