



**THE DATASHEET OF
ADM6918XABT1**



ADM6918/X

18 port 10/100 Mbps Ethernet Switch Controller

ADM6918/X

Communications



Never stop thinking

Edition 2005-11-08

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18 port 10/100 Mbps Ethernet Switch Controller

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| 2005-11-03 | Minor change. Included Green package information |
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1 Product Overview

1.1 Overview

The ADM6918/X is a high performance/low cost, eighteen-port 10/100 Mbps Ethernet Switch Controller with all ports supporting 10/100 Mbps full duplex switch function. The ADM6918/X is intended for applications to stand alone the bridge for the low cost ether-switch market. The ADM6918X is the environmentally friendly “green” package version. ADM6918/X can be programmed trunking port active. The trunking port can be connected to server or stacking two switch boxes to enhance the performance.

The ADM6918/X also supports back-pressure in half duplex mode and 802.3x flow control in full duplex mode. When back-pressure is enabled, and there is no receiving buffer available for the incoming packet, the ADM6918/X will force a JAM pattern on the receiving port in half duplex mode and transmit the 802.3x packet back to receiving end in full duplex mode.

An intelligent address recognition algorithm makes ADM6918/X to recognize up to 4096 different MAC addresses and enables filtering and forwarding at full wire speed.

The ADM6918/X has embedded SRAM for the proprietary buffer management. The SRAM is used to store the incoming/outgoing packets. These buffers provide elastic storage for transferring data between low-speed and high-speed segments and buffers are efficiently allocated to improve the efficiency.

1.2 Features

- Supports sixteen 10/100M auto-detect Half/Full duplex switch ports with SS-SMII interface and two 10/100M Half/Full duplex port with RMII/MII interface
- Supports up to 4096 MAC addresses table (4-way hashing)
- Supports two queue for QOS (1:2 or 1:4 or 1:8 or 1:16)
- Supports Port-base, 802.1p and IP TOS priority
- Supports store & forward architecture and Performs forwarding and filtering at non-blocking full wire speed
- Supports buffer allocation with 256 bytes each
- Supports aging function and 802.3x flow control for full duplex and back-pressure function for half duplex operation in case buffer is full
- Supports packet length up to 1536 bytes
- Supports Congestion Flow Control
- Broadcast storm filter and Alert LED
- Port-base VLAN and adjustable VLAN to support up to 32 VLAN group
- Serial CPU interface for counter and port status output
- CPU can see-through to access PHY
- Flexible port trunking on fault tolerance and load balance
- Per port 32bits smart counter for Rx/Tx byte/packet count, error count and collision count
- Rate-limit control (64K/128K/256K/512K/1M/4M/10M/20M)
- Per port auto learning enable/disable and if disable, forward non-learned packet to CPU]
- MAC address table accessible (in each entry, reserve one bit for CPU to enable/disable aging out)
- Forward special multicast, BPDU, GMRP, GVRP and IGMP packets to CPU port
- 128 pin QFP package with 3.3 V/1.8V power supply

1.3 Package Information

| Product Name | Product Type | Package | Ordering Number |
|----------------------------|--------------|--------------|------------------------------|
| Ethernet Switch Controller | ADM6918/X | P-FQFP-128-1 | Q67801H 70A202 ¹⁾ |

1) contact Infineon for the updated ordering information

1.4 Data Lengths

- qword: 64-bits
- dword: 32-bits
- word: 16-bits
- byte: 8 bits
- nibble: 4 bits

1.5 Block Diagram

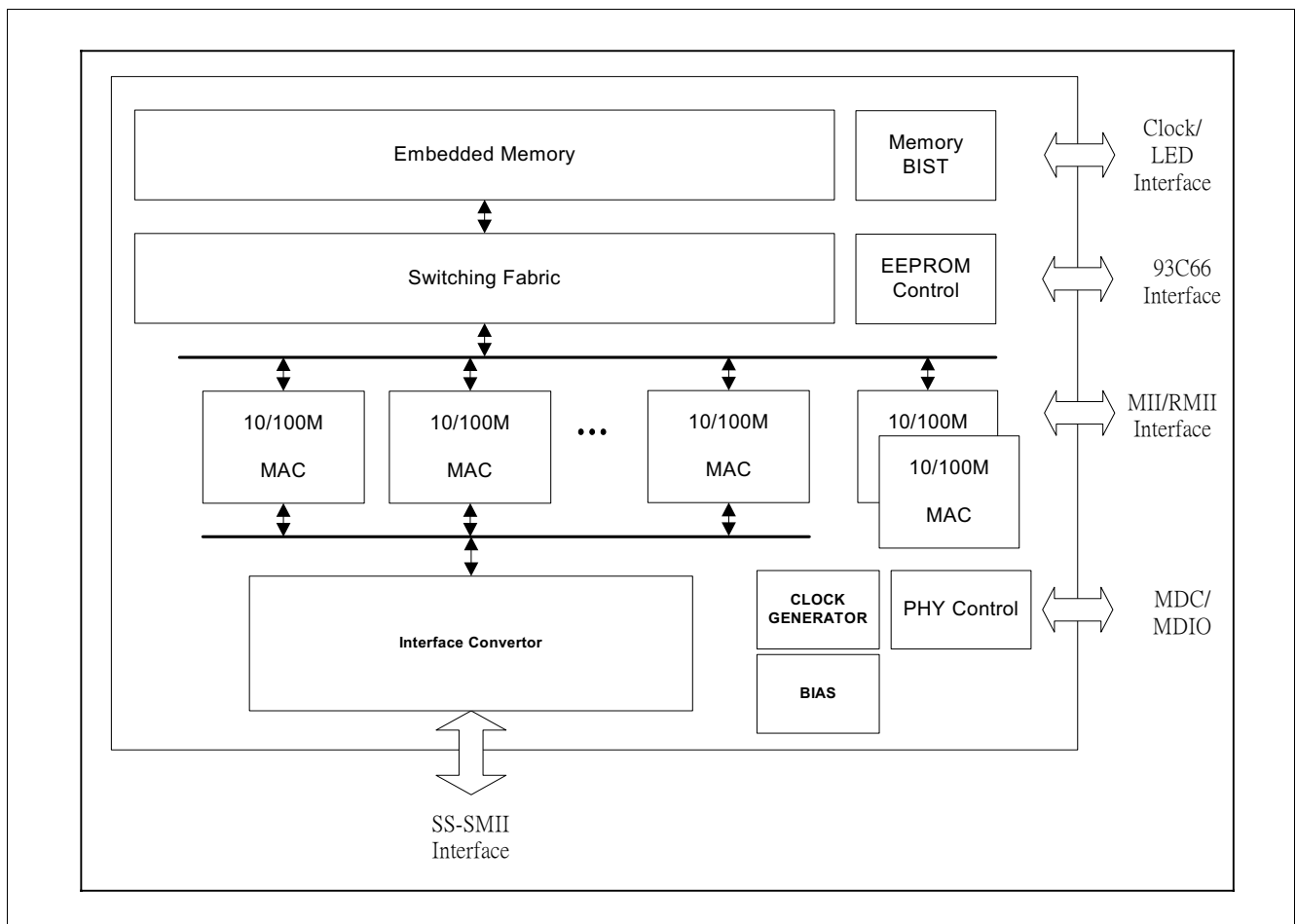


Figure 1 ADM6918/X Block Diagram

2 Interface Description

2.1 Pin Diagram-ADM6918/X (SS-SMII Interface)

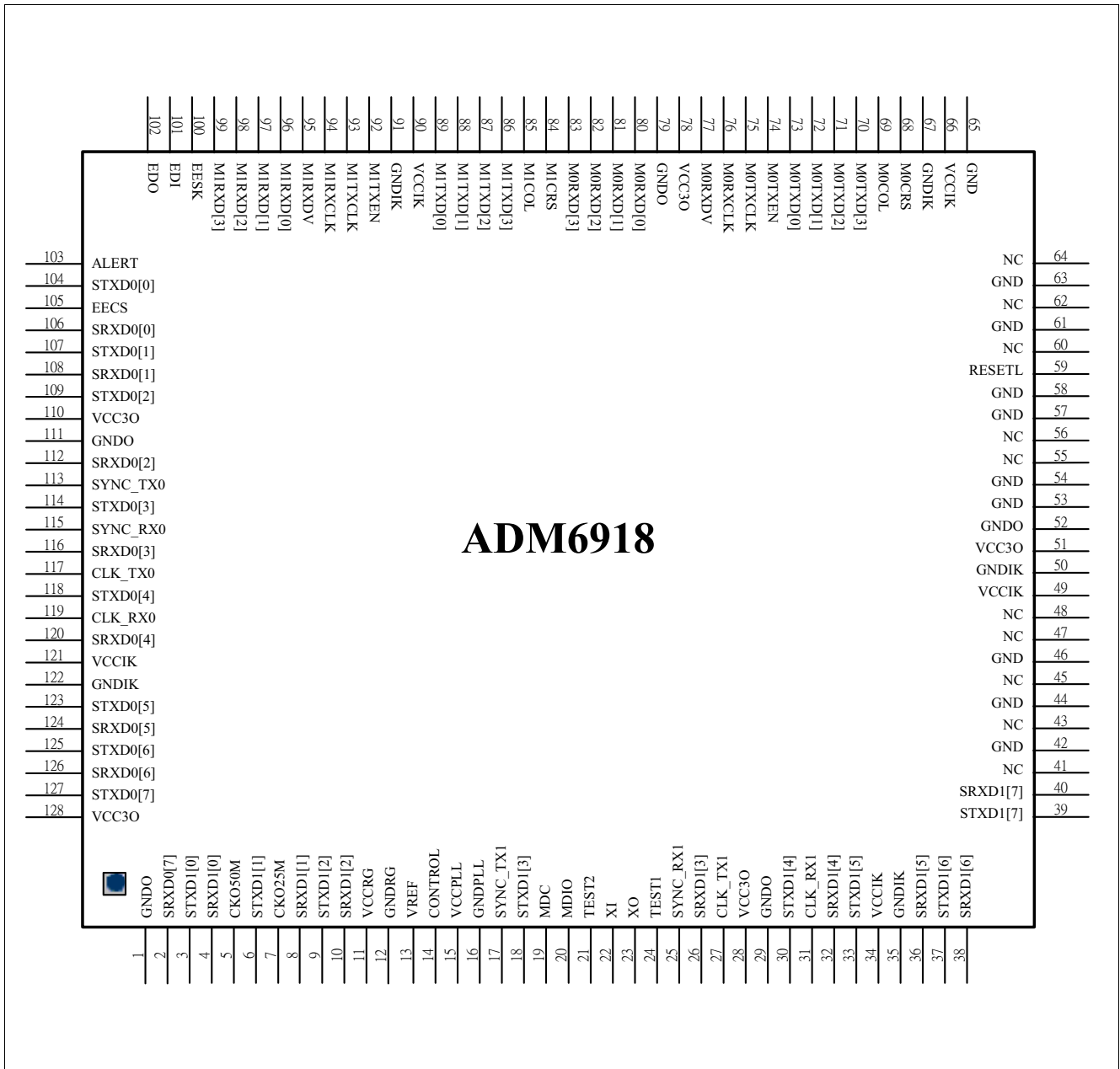


Figure 2 ADM6918/X Pin Diagram (SS-SMII Interface)

2.2 Abbreviations

Standard abbreviations for I/O tables:

Table 1 Abbreviations for Pin Type

| Abbreviations | Description |
|---------------|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| AO | Output. Analog levels. |
| AI/O | Input or Output. Analog levels. |
| PWR | Power |
| GND | Ground |
| MCL | Must be connected to Low (JEDEC Standard) |
| MCH | Must be connected to High (JEDEC Standard) |
| NU | Not Usable (JEDEC Standard) |
| NC | Not Connected (JEDEC Standard) |

Table 2 Abbreviations for Buffer Type

| Abbreviations | Description |
|---------------|--|
| Z | High impedance |
| PU1 | Pull up, 10 k Ω |
| PD1 | Pull down, 10 k Ω |
| PD2 | Pull down, 20 k Ω |
| TS | Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance. |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource. |
| OC | Open Collector |
| PP | Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute). |
| OD/PP | Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute. |
| ST | Schmitt-Trigger characteristics |
| TTL | TTL characteristics |

2.3 Pin Description

ADM6918/X pins are categorized into one of the following groups:

- SS-SMII Networking Interface, 60 pins
- MII/RMII Interface, 28 pins
- Power/Ground
- Miscellaneous pins, 16 pins

Table 3 I/O Signals

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|--|----------|----------|---------------|---|
| SS-SMII Networking Interface, 60 pins | | | | |
| 106 | SRXD0_0 | I | TTL | Port 0 to Port 7 SS-SMII Receive Data Bit The receive data should be synchronous to the rising edge of CLK_RX0. |
| 108 | SRXD0_1 | | | |
| 112 | SRXD0_2 | | | |
| 116 | SRXD0_3 | | | |
| 120 | SRXD0_4 | | | |
| 124 | SRXD0_5 | | | |
| 126 | SRXD0_6 | | | |
| 2 | SRXD0_7 | | | |
| 115 | SYNC_RX0 | I | TTL | Port 0 to Port 7 SS-SMII Synchronous Signal This signal is synchronous to the rising edge of CLK_RX0. Active high indicates the byte boundary. |
| 119 | CLK_RX0 | I | TTL | Reference Receive Clock for Port 0 to Port 7 This signal is 125 MHz input for SS-SMII interface. |
| 104 | STXD0_0 | O | TTL, 8 mA | Port 0 to Port 7 SS-SMII Transmit Data Bit The transmit data is synchronous to the rising edge of CLK_TX0. |
| 107 | STXD0_1 | | | |
| 109 | STXD0_2 | | | |
| 114 | STXD0_3 | | | |
| 118 | STXD0_4 | | | |
| 123 | STXD0_5 | | | |
| 125 | STXD0_6 | | | |
| 127 | STXD0_7 | | | |
| 113 | SYNC_TX0 | O | TTL, 8 mA | Port 0 to Port 7 SS-SMII Synchronous Signal This signal is synchronous to the rising edge of CLK_TX0. Active high indicates the byte boundary. |
| 117 | CLK_TX0 | O | TTL, 16 mA | Reference Transmit Clock for Port 0 to Port 7 This signal is 125 MHz output for SS-SMII interface. |
| 4 | SRXD1_0 | I | TTL | Port 8 to Port 15 SS-SMII Receive Data Bit The receive data should be synchronous to the rising edge of CLK_RX1. |
| 8 | SRXD1_1 | | | |
| 10 | SRXD1_2 | | | |
| 26 | SRXD1_3 | | | |
| 32 | SRXD1_4 | | | |
| 36 | SRXD1_5 | | | |
| 38 | SRXD1_6 | | | |
| 40 | SRXD1_7 | | | |
| 25 | SYNC_RX1 | I | TTL | Port 8 to Port 15 SS-SMII Synchronous Signal This signal is synchronous to the rising edge of CLK_RX1. Active high indicates the byte boundary. |
| 31 | CLK_RX1 | I | TTL | Reference Receive Clock for Port 8 to Port 15 This signal is 125 MHz input for SS-SMII interface. |

Interface Description

Table 3 I/O Signals (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|------------------------------------|----------|----------|------------------|--|
| 3 | STXD1_0 | O | TTL, 8 mA | Port 8 to Port 15 SS-SMII Transmit Data Bit The transmit data is synchronous to the rising edge of CLK_TX1. |
| 6 | STXD1_1 | | | |
| 9 | STXD1_2 | | | |
| 18 | STXD1_3 | | | |
| 30 | STXD1_4 | | | |
| 33 | STXD1_5 | | | |
| 37 | STXD1_6 | | | |
| 39 | STXD1_7 | | | |
| 17 | SYNC_TX1 | O | TTL, 8 mA | Port 8 to Port 15 SS-SMII Synchronous Signal This signal is synchronous to the rising edge of CLK_TX1. Active high indicates the byte boundary. |
| 27 | CLK_TX1 | O | TTL, 16 mA | Reference Transmit Clock for Port 8 to Port 15 This signal is 125 MHz output for SS-SMII interface. |
| MII/RMII Interface, 28 pins | | | | |
| 68 | M0CRS | I | TTL, PD | MII Port0 Carrier Sense This pin is internal pull-down. |
| 69 | M0COL | I | TTL, PD | MII Port0 Collision Input This pin is internal pull-down. |
| 73 | M0TXD_0 | I/O | TTL, 8 mA, PD | MII Port 0 Transmit Data Bit[0:3] Synchronous to the rising edge of M0TXCLK. RMII Port 0 Transmit Data Bit[0:1] Synchronous to the rising edge of M0RXCLK. RMIIMODE[1]: Value on M0TXD_3 will be latched at the rising edge of RESETL to configure port 25 as RMII mode. RMIIMODE[0]: Value on M0TXD[2] will be latched at the rising edge of RESETL to configure port 24 as RMII mode. |
| 72 | M0TXD_1 | | | |
| 71 | M0TXD_2 | | | |
| 70 | M0TXD_3 | | | |
| 74 | M0TXEN | I/O | TTL, 8 mA, PD | MII/RMII Port 0 Transmit Enable AGDIS. Value on this pin will be latched at the rising edge of RESETL to set aging disable. |
| 75 | M0TXCLK | I | TTL, PD | MII Port 0 Transmit Clock Input This pin is 25 MHz input for MII interface. |
| 76 | M0RXCLK | I | TTL, PD | MII/RMII Port 0 Receive Clock Input This pin is 25 MHz input for MII interface and 50 MHz REFCLK input for RMII interface. |
| 77 | M0RXDV | I | TTL, PD | MII Port 0 Receive Data Valid RMII Port 0 Carrier Sense/Receive Data Valid This pin is internal pull-down. |
| 80 | M0RXD_0 | I | TTL, PD | MII Port 0 Receive Data Bit[0:3] RMII Port 0 Receive Data Bit[0:1] If in RMII mode, M0RXD_3 used for ext_dup_enable and M0RXD_2 used for ext_dup_full. Internal pull-down. See Sec3.1.27 for details. |
| 81 | M0RXD_1 | | | |
| 82 | M0RXD_2 | | | |
| 83 | M0RXD_3 | | | |
| 84 | M1CRS | I | TTL, PD | MII Port 1 Carrier Sense This pin is internal pull-down. |

Interface Description

Table 3 I/O Signals (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|-----------------|---------|----------|------------------|---|
| 85 | M1COL | I | TTL, PD | MII Port 1 Collision Input This pin is internal pull-down. |
| 89 | M1TXD_0 | I/O | TTL, 8 mA | MII Port 1 Transmit Data Bit[0:3] Synchronous to the rising edge of M1TXCLK. RMII Port 1 Transmit Data Bit[0:1] Synchronous to the rising edge of M1RXCLK. BPEN. Value on M1TXD[3] will be latched at the rising edge of RESETL to set Back_pressure enable. Internal pull-up. FCEN. Value on M1TXD[2] will be latched at the rising edge of RESETL to set flow control enable. Internal pull-up. TNKEN. Value on M1TXD[1] will be latched at the rising edge of RESETL to set trunking enable. Internal pull-up. IPGLVING. Value on M1TXD[0] will be latched at the rising edge of RESETL to set shorter IPG. Internal pull-down. |
| 88 | M1TXD_1 | | | |
| 87 | M1TXD_2 | | | |
| 86 | M1TXD_3 | | | |
| 92 | M1TXEN | O | TTL, 8 mA, PU | MII Port 1 Transmit Enable ANEN. Value on this pin will be latched at the rising edge of RESETL to set auto_negotiation enable. Internal pull-up. |
| 93 | M1TXCLK | I | TTL, PD | MII Port1 Transmit Clock Input This signal is 25 MHz input for MII interface. |
| 94 | M1RXCLK | I | TTL, PD | MI1 Receive Clock Input This signal is 25 MHz input for MII interface and 50 MHz REFCLK input for RMII interface. |
| 95 | M1RXDV | I | TTL, PD | MII/RMII Port 1 Receive Data Valid This pin is internal pull-down. |
| 96 | M1RXD_0 | I | TTL PD | MII Port 1 Receive Data Bit[0:3] RMII Port 1 Receive Data Bit[0:1] If in RMII mode, M1RXD_3 used for ext_dup_enable and M1RXD_2 used for ext_dup_full. Internal pull-down. See Sec3.1.27 for details. |
| 97 | M1RXD_1 | | | |
| 98 | M1RXD_2 | | | |
| 99 | M1RXD_3 | | | |

Power/Ground

| | | | | |
|------------------------|--------|-------------|---|--|
| 12 | GNDRG | Analog GND | – | Ground for Regulator |
| 11 | VCCRG | Analog PWR | – | 3.3 V Power Supply for Regulator |
| 16 | GNDPLL | Analog GND | – | Ground for PLL |
| 15 | VCCPLL | Analog PWR | – | 1.8 V Power Supply PLL |
| 35, 50, 67, 91, 122 | GNDIK | Digital GND | – | Ground for Core Logic |
| 34, 49, 66, 90, 121 | VCCIK | Digital PWR | – | 1.8 V Power Supply for Core Logic |
| 1, 29, 52, 79, 111 | GNDO | Digital GND | – | Ground for I/O PAD |

Interface Description

Table 3 I/O Signals (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|------------------------------------|--------------|-------------|---------------|--|
| 28, 51, 78, 110, 128 | VCC30 | Digital PWR | – | 3.3 V Power Supply for I/O PAD |
| Miscellaneous Pins, 16 pins | | | | |
| 7 | CK25MO | O | TTL, 16 mA | 25 MHz Clock Output This pin will drive out 25 MHz. |
| 5 | CK50MO | O | TTL, 16 mA | 50 MHz Clock Output This pin will drive out 50 MHz. |
| | COL_LED_10M | O | TTL, 16 mA | COL_LED_10M This pin shows collision LED for 10M domain (see EEPROM Register 1ch, Bit[9]). |
| 22 | XI | AI | – | Crystal or OSC 50 MHz Input This is the clock source of PLL. The PLL will generate 125 MHz for SS-SMII and 50 MHz for RMII and 25 MHz for MII. |
| 23 | XO | AO | – | Crystal 50 MHz Output |
| 59 | RESETL | I | TTL, ST | Reset Signal An active low signal with minimum 100 ms duration is required. |
| 103 | ALERT | O | TTL, 8 mA | Alert LED Display This pin will show the status of power-on-diagnostic and broadcast traffic. |
| | COL_LED_100M | O | TTL, 8 mA | COL_LED_100M This pin shows collision LED for 100M domain (see EEPROM Register 1ch, Bit[9]). |
| 21 | TEST_2 | I | TTL, PD | Industrial Test Pins These pins are internal pull-down. |
| 24 | TEST_1 | | | |
| 19 | MDC | O | TTL, 16 mA | Management Data Clock This pin output 2.2 MHz clock to drive PHY and access corresponding speed and duplex and link status through MDIO. |
| 20 | MDIO | I/O | TTL, 8 mA, PU | Management Data This pin is in-out to PHY. When RESETL is low, this pin will be tristate. This pin is internal pull-up. |
| 100 | EESK | I/O | TTL, 4 mA, PU | EEPROM Serial Clock This pin is clock source for EEPROM. When RESETL is low, it will be tristate. This pin is internal pull-up. |
| 105 | EECS | I/O | TTL, 4 mA, PD | EEPROM Chip Select This pin is chip enable for EEPROM. When RESETL is low, it will be tristate. This pin is internal pull-down. |
| 101 | EDI | I/O | TTL, 4 mA, PU | EEPROM Serial Data Input This pin is output for serial data transfer. When RESETL is low, it will be tristate. This pin is internal pull-up. |

Table 3 I/O Signals (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|--|---------|----------|-------------|---|
| 102 | EDO | I | TTL, PU | EEPROM Serial Data Output This pin is input for serial data transfer. This pin is internal pull-up. |
| 14 | CONTROL | AO | – | FET Control Signal The pin is used to control FET for 3.3 V to 1.8 V regulator. |
| 13 | VREF | AI | – | Regulator Control Input Signal |
| 64, 62, 60, 55, 56, 47, 48, 45, 43, 41 | NC | | | No Connect |
| 65, 63, 61, 58, 57, 53, 54, 46, 44, 42 | GND | | | Ground |

3 Function Description

3.1 Introduction

The ADM6918/X uses a “store & forward” switching approach for the following reasons:

1. Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffers, especially bridging between a server on a 100Mbit/s network and clients on a 10 Mbit/s segment.
2. Store & forward switches improve overall network performance by acting as a “network cache”.
3. Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.1.1 Basic Operation

The ADM6918/X receives incoming packets from one of its ports, uses the source address (SA) and VID to update the address table, and then forwards the packet to the output ports determined by the destination address (DA) and VID.

If the DA and VID are not found in the address table, the ADM6918/X treats the packet as a broadcast packet and forwards the packet to the other ports within the same group.

The ADM6918/X automatically learns the port number of attached network devices by examining the SA and VID of all incoming packets. If the SA and VID are not found in the address table, the device adds it to the table.

3.1.2 Address Learning

The ADM6918/X provides two ways to create the entry in the address table: dynamic learning and manual learning. A four-way hash algorithm is implemented to allow 4 different addresses to be stored at the same location. Up to 4k entries can be created and all entries are stored in the internal SSRAM. Two parameters, SA and VID, are combined to generate the 10-bit hash key to allow that the same addresses with different port number can exist in the table at the same time.

Dynamic Learning

The ADM6918/X searches for SA and VID of an incoming packet in the address table and acts as follows:

If the SA+VID was not found in the address table (a new address), the ADM6918/X waits until the end of the packet (non-error packet) and updates the address table. If the SA+VID was found in the address table, then aging value of each corresponding entry will be reset to 0.

Dynamic learning will be disabled in the following condition:

1. Security violation happened.
2. The packet is a PAUSE frame.
3. The first bit of SA is 1_B.
4. The packet is an error packet (too long, too short or FCS error).
5. The CPU port leaning function is disabled or enabled but the CPU port instructs the switch not to learn the packet.
6. The port is in the Disabled or Blocking-not-Listening state in the Spanning Tree Protocol.

Manual Learning

The ADM6918/X implements the manual learning through the CPU's help. The CPU can create or remove any entry in the address table. Each entry could be static or pointed to the output port map table. “Static” means the entry will not be aged forever. It is useful in the security function (forward unknown packets to the CPU port or discard) or monitor function (forward monitored address to the specific port). Output port map table is also helpful

in the IGMP function (if the number of the output port is more than one) or the users want to redirect the special packets with reserved DA.

3.1.3 Address Aging

The ADM6918/X will periodically (300 ms) remove the non-static address in the address table. This could help to prevent a station leaves the network and occupies a table space for a long time. Aging function can be disabled from the hardware pin.

3.1.4 Address Recognition and Packet Forwarding

The ADM6918/X forwards the incoming packets between bridge ports according to the DA and VID as follows:

Table 4 Address Recognition and Packet Forwarding

| DA | DA+VID was found in the address table (entry not pointed to the output port map table) | DA+VID was found in the address table (entry pointed to the output port map table) | DA+VID was not found in the address table |
|--|--|---|--|
| Unicast Address | No Security Violation | | |
| | Forward packets to the port determined by the address table. The packet may be dropped because of forwarding group boundary violation. | Forward packets to the ports determined by the output port map table constrained by the forwarding group. | Forward packets to the other ports within the same forwarding group. |
| | Security Violation | | |
| | Drop or forward to CPU | Drop or forward to CPU | Drop or forward to CPU |
| Broadcast Address (All 1'b1) | No Security Violation | | |
| | Forwarding packets to the other ports within the same forwarding group. | Forward packets to the ports determined by the output port map table constrained by the forwarding group. | Forward packets to the other ports within the same forwarding group. |
| | Security Violation | | |
| | Drop or forward to CPU | Drop or forward to CPU | Drop or forward to CPU |
| Reserved Address (01-80-c2-00-00-xx, with the option to forward normally) | No Security Violation | | |
| | Forwarding packets to the other ports within the same forwarding group. | Forward packets to the ports determined by the output port map table constrained by the forwarding group. | Forward packets to the other ports within the same forwarding group. |
| | Security Violation | | |
| | Same as the above | Same as the above | Same as the above |
| Reserved Address (01-80-c2-00-00-xx, with the option to forward to CPU) | No Security Violation | | |
| | Forward the packet to the CPU port. | Forward the packet to the CPU port. | Forward the packet to the CPU port. |
| | Security Violation | | |
| | Same as the above | Same as the above | Same as the above |

Function Description
Table 4 Address Recognition and Packet Forwarding (cont'd)

| DA | DA+VID was found in the address table (entry not pointed to the output port map table) | DA+VID was found in the address table (entry pointed to the output port map table) | DA+VID was not found in the address table |
|---|--|---|--|
| Reserved Address (01-80-c2-00-00-xx, with the option to discard) | No Security Violation | | |
| | Discard the packet. | Discard the packet. | Discard the packet. |
| | Security Violation | | |
| | Same as the above | Same as the above | Same as the above |
| IGMP Packet (Port Enable IGMP) | No Security Violation | | |
| | Forward the packet to the CPU port. | Forward the packet to the CPU port. | Forward the packet to the CPU port. |
| | Security Violation | | |
| | Drop or forward to CPU | Drop or forward to CPU | Drop or forward to CPU |
| IGMP Packet (Port Disable IGMP) | No Security Violation | | |
| | Forward packets to the port determined by the address table. The packet may be dropped because of forwarding group boundary violation. | Forward packets to the ports determined by the output port map table constrained by the forwarding group. | Forward packets according the Multicast Option. |
| | Security Violation | | |
| | Drop or forward to CPU | Drop or forward to CPU | Drop or forward to CPU |
| Others | No Security Violation | | |
| | Forward packets to the port determined by the address table. The packet may be dropped because of forwarding group boundary violation. | Forward packets to the ports determined by the output port map table constrained by the forwarding group. | Forward packets according the Multicast Option. |
| | Security Violation | | |
| | Drop or forward to CPU | Drop or forward to CPU | Drop or forward to CPU |

3.1.5 Trunking Port Forwarding

ADM6918/X supports the trunking forwarding and any port could be assigned to the trunking port. When one or more of the members link fail, the ADM6918/X will automatically change the transmitting path from the failed link port to normal link port. Port based load balancing is implemented to distribute the loading.

3.1.6 Illegal Frames

The ADM6918/X will discard all illegal frames such as runt packet (less than 64 bytes), oversize packet (greater than 1518 or 1522 bytes) or bad CRC.

3.1.7 Back off Algorithm

The ADM6918/X implements the truncated exponential back off algorithm compliant to the 802.3 standard. ADM6918/X will restart the back off algorithm by choosing 0-9 collision count. After 16 consecutive retransmit trials, the ADM6918/X resets the collision counter.

3.1.8 Buffers and Queues

The ADM6918/X incorporates 18 transmit queues and receive buffer area for the 18 Ethernet ports. The receive buffers as well as the transmit queues are located within the ADM6918/X along with the switch fabric. The buffers are divided into 640 blocks of 256 bytes each. The queues of each port are managed according to each port's read/write pointer.

Input buffers and output queues are maintained through proprietary patent pending UNIQUE (Universal Queue management) scheme.

3.1.9 Half Duplex Flow Control

Back-pressure is supported for half-duplex operation.

When the ADM6918/X cannot allocate a receiving buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision.

3.1.10 Full Duplex Flow Control

When full duplex port runs out of its receive buffer, a PAUSE command will be issued by ADM6918/X to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. When flow control hardware pin is set to high during power on reset and per port PAUSE is enabled, ADM6918/X will output and accept 802.3x flow control packet.

3.1.11 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The value is 9.6us for 10Mbit/s ETHERNET and 960ns for 100Mbit/s fast Ethernet.

3.1.12 Port VLAN or Tag VLAN Support

Two VLAN settings are supported by the ADM6918/X: the port-based VLAN or the tag-based VLAN. For the port-based VLAN the ADM6918/X will use the port number as the index to lookup the forwarding table. For the tag-based VLAN, the ADM6918/X will use the VID to lookup the forwarding table. Each port is assigned a Port VID as the Default VID if tag-based VLAN is used. The ADM6918/X will check TAG, remove TAG, insert TAG, and recalculate CRC if packet is changed.

Table 5 Packets Received are Untagged

| Force no Tag | Bypass | Output Port is Tagged or not | Action |
|--------------|--------|------------------------------|-----------------------|
| Don't Care | No | No | Untag as the original |
| | Yes | No | Untag as the original |
| | No | Yes | Add Tag |
| | Yes | Yes | Untag as the original |

Table 6 Packets Received are Tagged

| Force no Tag | Bypass | Output Port is Tagged or not | Action |
|--------------|--------|------------------------------|---|
| No | No | No | The Tag is removed. |
| Yes | No | No | Tag as the original. The priority in the TAG header is not checked and VID will not change even if VID is 0 or 1. |

Table 6 Packets Received are Tagged (cont'd)

| Force no Tag | Bypass | Output Port is Tagged or not | Action |
|--------------|--------|------------------------------|--|
| No | Yes | No | Tag as the original. The priority in the TAG header is checked and if the VID is 0 or 1, it may change to PVID (see EEPROM register 1C _H , Bit[3]). |
| No | No | Yes | Tag as the original. The priority in the TAG header is checked and if the VID is 0 or 1, it may change to PVID (see EEPROM register 1ch, Bit[3]). |
| No | Yes | Yes | Tag as the original. The priority in the TAG header is checked and if the VID is 0 or 1, it may change to PVID (see EEPROM register 1ch, Bit[3]). |
| Yes | Yes | No | Tag as the original. The priority in the TAG header is not checked. The VID will not change. |
| Yes | No | Yes | The Tag will be added and packet will be double tagged output. The VID will not change. |
| Yes | Yes | Yes | Tag as the original. The priority in the TAG header is not checked. The VID will not change. |

3.1.13 Priority Control

The ADM6918/X provides two priority queues on each output port. Five ways could be used to assign a priority to a packet.

1. The priority assigned to each receiving port
2. The priority field in the 802.1Q Tag Header
3. The IPv4 TOS field in the IPv4 Header
4. Priority assigned by the CPU
5. Management packet (high priority assigned)

3.1.14 Alert LED Display

Two functions are displayed through the Alert LED.

1. Diagnostic Mode after Power on
 - a) After reset or power up, LED keeps on at least 3 second, and processes internal SSRAM self-test.
 - b) If test passes, the ADM6918/X turns off LED and goes to the broadcast storm mode.
 - c) If SSRAM test fails, the ADM6918/X turns off LED, then keeps on.
2. Broadcast Storm Mode after SSRAM Self-test. Packets with DA = ffffffff_H will be counted into the storm counter.

Two thresholds (rising and falling) are used to control the broadcast storm.

 - a) Time Scale: 50ms is used. The max packet number in 100BaseT is 7490. The max packet number in 10BaseT is 749.
 - b) Port Rising Threshold, see [Table 7](#).
 - c) Port Falling Threshold, see [Table 8](#).

Table 7 Port Rising Threshold

| Broadcast Storm Threshold | 00 | 01 | 10 | 11 |
|---------------------------|---------|-----|-----|-----|
| All 100TX | Disable | 10% | 20% | 40% |
| Not All 100TX | Disable | 1% | 2% | 4% |

Table 8 Port Falling Threshold

| Broadcast Storm Threshold | 00 | 01 | 10 | 11 |
|---------------------------|---------|------|-----|-----|
| All 100TX | Disable | 5% | 10% | 20% |
| Not All 100TX | Disable | 0.5% | 1% | 2% |

3.1.15 Broadcast Storm Filter

If broadcast storming filter is enabled, the broadcast packets (DA = ffff-ffff-ffff_H) over the rising threshold within 50 ms will be discarded when the alert LED is turned on.

3.1.16 Collision LED Display

Two collision LEDs are supported. (see EEPROM Register 1C_H, Bit[9])

- 100M Collision LED. If collision happens in one of the ports configured 100M, the 100M Collision LED will flash in rate of 2 Hz.
- 10M Collision LED. If collision happens in one of the ports configured 10M, the 10M Collision LED will flash in rate of 2 Hz.

3.1.17 Bandwidth Control

The ADM6918/X allows the user to limit the bandwidth for each input or output port. 64k, 128K, 256k, 512K, 1M, 4M, 10M and 20M are supported.

3.1.18 Smart Discard

The ADM6918/X supports a smart mechanism to discard packets early according to their priority to prevent the resource blocked by the low priority. The discard ratio is as follows:

Table 9 Discard Ratio

| Discard Mode Utilization | 00 | 01 | 10 | 11 |
|--------------------------|----|-----|-----|-----|
| 00 | 0% | 0% | 0% | 0% |
| 01 | 0% | 0% | 25% | 50% |
| 11 | 0% | 25% | 50% | 75% |

3.1.19 Security Support

4 level security schemes are supported by the ADM6918/X. All the security violation address will not be automatically learned.

The violated packet could be forwarded to the CPU port for management or discarded. When CPU is not present, ADM6918/X also provides a simple way to lock the first address to prevent illegal address access.

3.1.20 Smart Counter Support

Six counters per port are supported by the ADM6918/X.

1. Receive Packet Count
2. Receive Packet Length Count
3. Transmit Packet Count
4. Transmit Packet Length Count
5. The Error Count
6. The Collision Count

3.1.21 Length 1536 Mode

The ADM6918/X provides a function to enable the port to receive packets up to 1536 Byte.

3.1.22 PHY Management (MDC/MDIO Interface)

The ADM6918/X uses the MDC/MDIO interface to set the PHY status. After the reset or power up, the MDC/MDIO controller will delay about 130 ms to wait for the PHY to ready. The ADM6918/X supports two ways to configure the PHY setting.

1. PHY master. The switch only reads the PHY status (speed, duplex, link, and pause). This mode is useful when users want to configure PHY through the CPU help. The ADM6918/X supports an indirect way (a PHY Control Register) for CPU to access PHYs.
2. PHY slave. The switch uses the EEPROM setting to control the PHY attached (only speed, duplex, link, and pause are supported). After the port setting changed, the ADM6918/X will use the new setting to program the PHY again and update the status. 8 commands are provided in this mode to allow the customer to customize the PHY setting.

Note: The PHY address attached to port 0 is 00008_H, the PHY address attached to port 1 is 00009_H, ..., the PHY address attached to port 23 is 0001f_H, the PHY address attached to port 24 is 00006_H and the PHY address attached to port 25 is 00007_H.

3.1.23 Forward Special Packets to the CPU Port (IGMP and Spanning Tree Support)

ADM6918/X will forward the special packets to the CPU port to provide the management function.

1. DA is 01-80-C2-00-00-00 (BPDU)
2. DA is 01-80-C2-00-00-02 (Slow Protocol)
3. DA is 01-80-C2-00-00-03 (802.1x PAE)
4. DA is 01-80-C2-00-00-04 ~ 01-80-C2-00-00-0f
5. DA is 01-80-C2-00-00-20 (GMRP)
6. DA is 01-80-C2-00-00-21 (GVRP)
7. DA is 01-80-C2-00-00-22 (GVRP)
8. DA is 01-00-5E-xx-xx-xx and protocol field is 2 for IPV4 (IGMP)

3.1.24 Special TAG

The ADM6918/X has an ability to insert 4Byte special TAG when packets transmitted to the CPU port or to remove 8Byte additional TAG in the packets when packets are received from the CPU port. The configuration is shown in the CPU Configuration Register. This special function allows the CPU to know the source port which will be used in the IGMP Snooping, Spanning Tree or the Security function. The CPU also could insert additional 8-byte Tag to instruct the switch to handle the packets. The packets format is as follows:

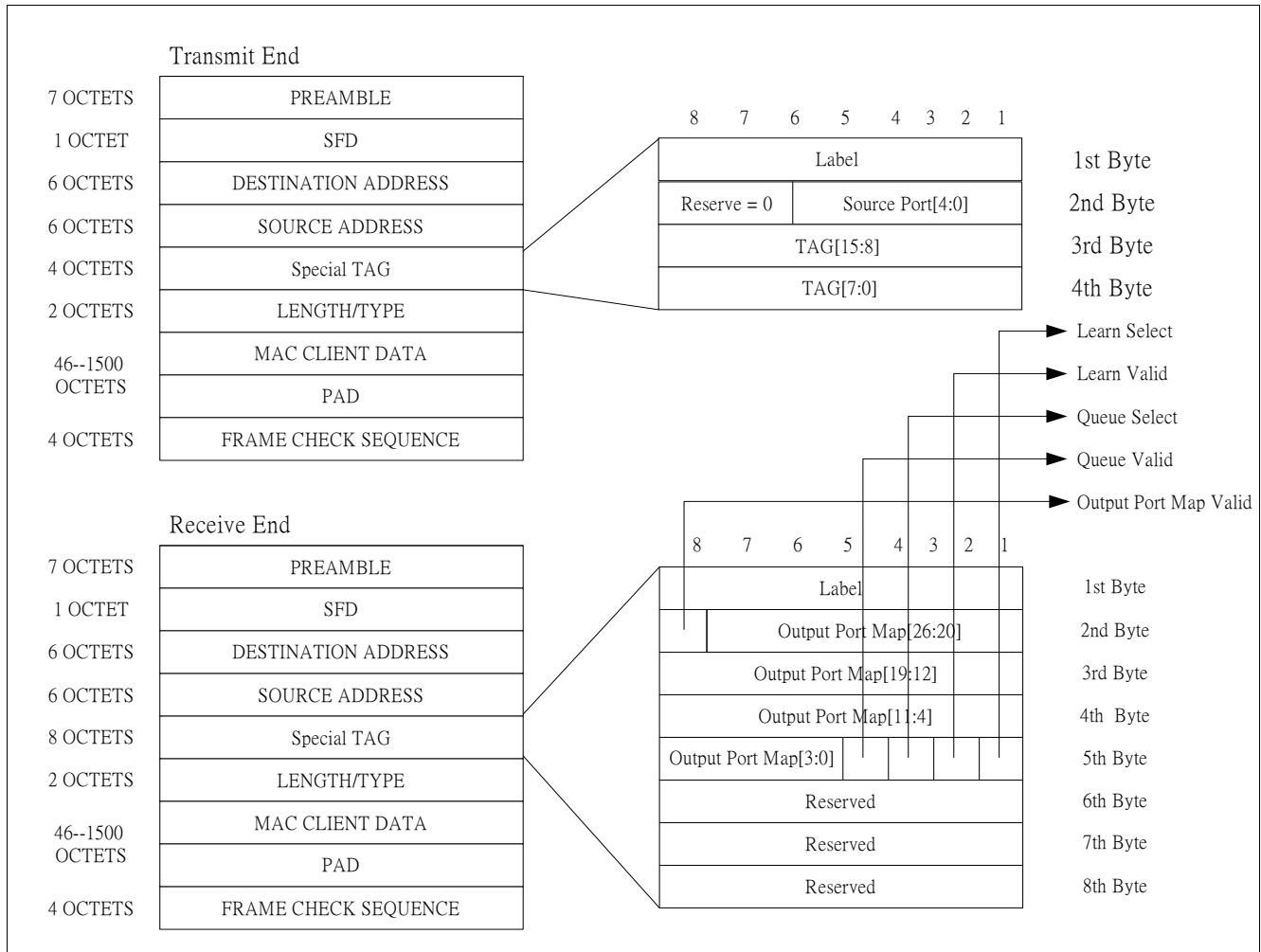


Figure 3 Packet Format

Table 10 Special TAG Fields

| Configuration | Description | Default |
|-----------------------|--|---------|
| Label | The field is used for CPU to decide if the special TAG is valid. If the switch finds the Label doesn't equal to the value assigned by the EEPROM, it must receive as the normal mode. This case exists when user wants the switch to insert 4 byte special tag even for Pause packets. | 8b'0 |
| Output Port Map Valid | 1 _B , The switch is instructed to override the switch operation. It will forward the packets following the Output Port Map field. 0 _B , The switch will treat the packet as the normal mode. | 1'b0 |

Table 10 Special TAG Fields (cont'd)

| Configuration | Description | Default |
|-----------------------|---|---------|
| Output Port Map[26:0] | Bit[26] = 1, the CPU wants to forward packets to more than 2 ports. Bit[26] = 0, the CPU wants to forward packets to only one port. Bit[x], x = 0 ~ 25, the CPU wants to forward packets to Port x. Example: 1. The CPU wants to forward packet to P1 and P2 then the Output Port Map is as follows: Bit 26, 25~24, 23~16, 15~8, 7~0 Map 1, 00, 0000_0000, 0000_0000, 0000_0110 2. The CPU wants to forward packets to P5 only. Bit 26, 25~24, 23~16, 15~8, 7~0 Map 0, 00, 0000_0000, 0000_0000, 0010_0000 | 27'h0 |
| TAG[25:0] | This value is the same as the TAG header if the CPU port is configured to a TAG port. | 16'h0 |
| Source Port[4:0] | This field indicates the source port the packet comes from. | 5'h0 |
| Queue Valid | 1 _B , The switch is instructed to override the switch operation. It will forward the packets using the Queue Select Field. 0 _B , The switch will treat the packets as the normal mode. | 1'b0 |
| Queue Select | 1 _B , Mapped for High Queue 0 _B , Mapped for Low Queue | 1'b0 |
| Learn Valid | 1 _B , The switch is instructed to override the switch operation. The CPU port will use the Learn Field to decide how to learn the packet. 0 _B , The switch will treat the packets as the normal mode. That is, the CPU port will learn or disable learning according the Disable CPU Port Learning Function configured in the CPU Control Register. | 1'b0 |
| Learn Select | 1 _B , Learn the packet 0 _B , Don't learn the packet | 1'b0 |

3.1.25 Port 24 and Port 25 Interface (Only SS-SMII Package Support)

Three interfaces in port 24 and port 25 are supported by the ADM6918/X: (1) MII Interface (2) RMII Interface.

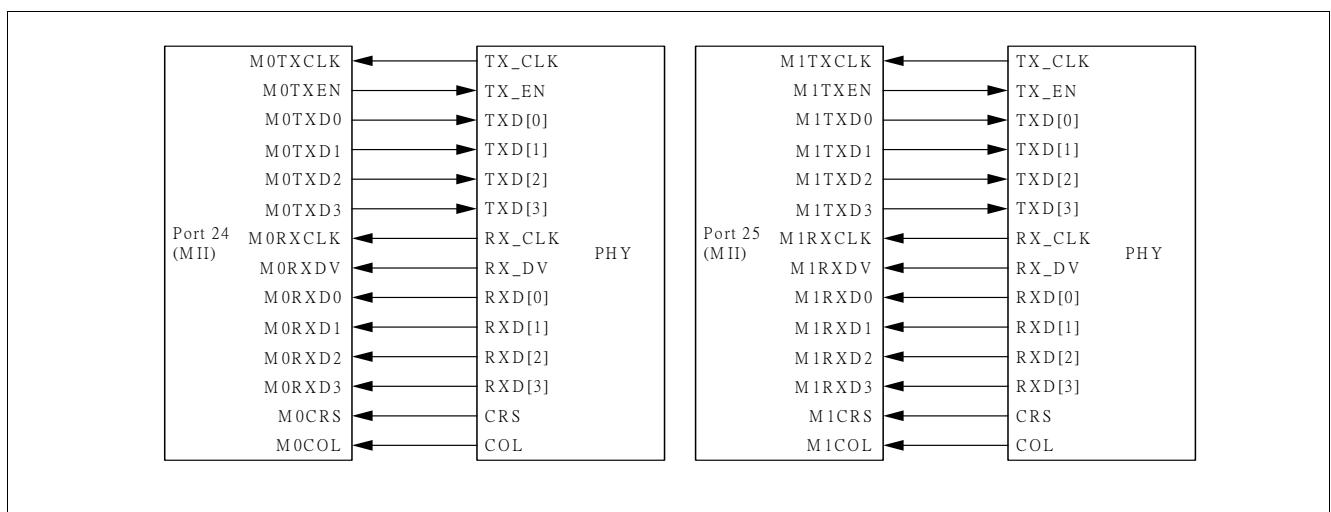
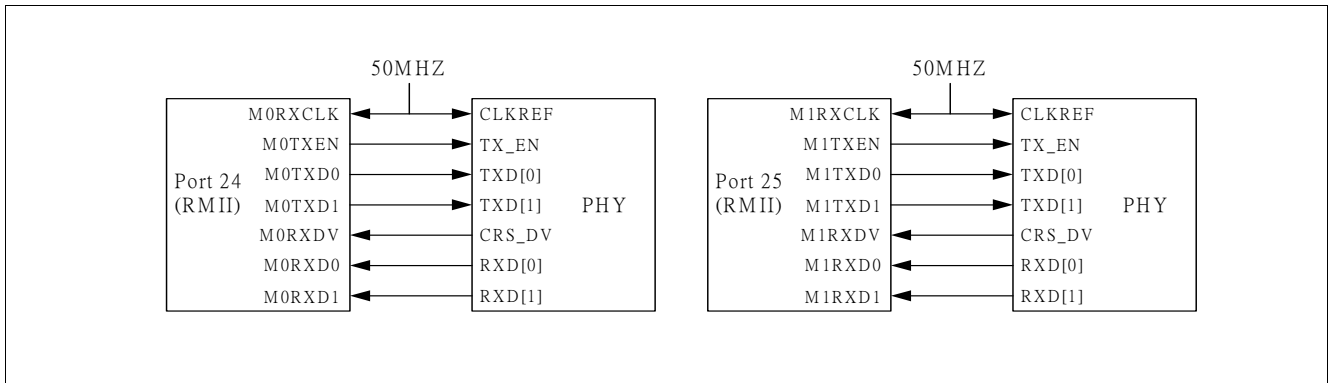
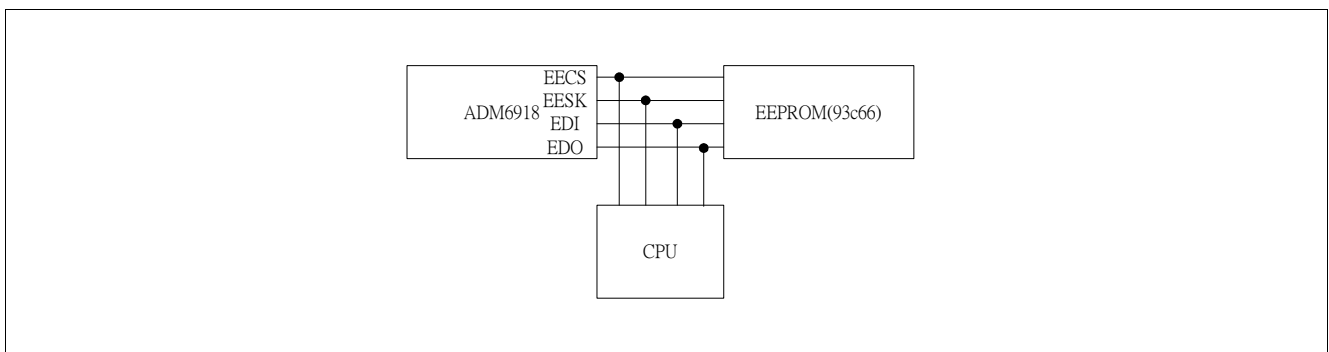


Figure 4 MII Interface Diagram


Figure 5 RMI Interface

3.1.26 Hardware, EEPROM and SMI Interface for Configuration

Three ways are supported to configure the setting in the ADM6918/X: (1) Hardware Setting (2) EEPROM Interface (3) SMI Interface. Users could use EEPROM and SMI interfaces combined with the CPU port to provide proprietary functions. Four pins are needed when using these two interfaces. See the following figure as a description.


Figure 6 Hardware, EEPROM and SMI Interface Configuration

3.1.26.1 Hardware Setting

The ADM6918/X provides some hardware pins where values reside on during power on or reset will be strapped for the default setting.

Table 11 SS-SMII and RMI Pins

| SS-SMII Pin Name | RMI Pin Name | Description |
|------------------|--------------|--|
| M1TXD0 | M1TXD0 | IPG Average 92 bit time. Internally Pulled Down. 0 _B , Disable IPG Average 92 1 _B , Enable IPG Average 92 |
| M1TXD1 | M1TXD1 | Trunk En. Internally Pulled Up. 0 _B , Trunking Disable. The ADM6918/X has no trunking function even if EEPROM sets. 1 _B , Trunking Enable. Use EEPROM to configure the trunk member. |

Function Description

Table 11 SS-SMII and RMII Pins (cont'd)

| SS-SMII Pin Name | RMII Pin Name | Description |
|------------------|---------------|--|
| M1TXD2 | M1TXD2 | Pause. Internally Pulled Up. 0_B , The switch doesn't allow the Pause function even if EEPROM set. The only way to start the Pause function is through the CPU help. 1_B , The switch allows the Pause function. This function can be disabled by the EEPROM. |
| M1TXD3 | M1TXD3 | Back-Pressure. Internally Pulled Up. 0_B , The switch doesn't allow the Back-Pressure function even if EEPROM set. 1_B , The switch allows the Back-Pressure function. This function can be disabled by the EEPROM. |
| M1TXEN | M1TXEN | Auto-Neg En. Internally Pulled Up. 0_B , The switch doesn't allow Auto-Negotiation function even if EEPROM set. The only way to start the Auto-Negotiation function is through the CPU help. 1_B , The switch allows the Auto-Negotiation function. This function can be disabled by the EEPROM. |
| M0TXEN | M0TXEN | Aging Dis. Internally Pulled Down. 0_B , The switch will age the entry in the address table. 1_B , The switch will not age the entry in the address table. |
| M0TXD0 | Don't Support | Port 24 Interface Configuration |
| M0TXD2 | Don't Support | M0TXD0, M0TXD2, Interface 0_B , 0, Port 24 is configured to MII in SS-SMII package (internal value). x_B , 1, Port 24 is configured to RMII in SS-SMII package. |
| M0TXD1 | Don't Support | Port 25 Interface Configuration |
| M0TXD3 | Don't Support | M0TXD1, M0TXD3, Interface configured to MII in SS-SMII package (internal value). x_B , 1, Port 25 is configured to RMII is SS-SMII package |

When port 24 or port 25 is configured to RMII mode in SS-SMII package, we can use the hardware pins to configure duplex status of these two ports.

Table 12 Port 24 Duplex Configuration

| M0RXD3 | M0RXD2 | Description |
|--------|--------|--|
| 0 | 0 | Duplex status is determined as port 0 ~ port 23. |
| 0 | 1 | Duplex status is determined as port 0 ~ port 23. |
| 1 | 0 | Full Duplex is determined. |
| 1 | 1 | Half Duplex is determined. |

Table 13 Port 25 Duplex Configuration

| M1RXD3 | M1RXD2 | Description |
|--------|--------|--|
| 0 | 0 | Duplex status is determined as port 0 ~ port 23. |
| 0 | 1 | Duplex status is determined as port 0 ~ port 23. |
| 1 | 0 | Full Duplex is determined. |
| 1 | 1 | Half Duplex is determined. |

3.1.26.2 EEPROM Interface

The EEPROM Interface is provided so the users could easily configure the setting without CPU's help. Because the EEPROM Interface is the same as the 93c66, it also allows the CPU to write the EEPROM register and renew the 93c66 at the same time. After the power up or reset (default value from the hardware pins fetched in this stage), the ADM6918/X will automatically detect the presence of the EEPROM by reading the address 0 in the 93c66. If the value = 16'h4154, it will read all the data in the 93c66. If not, the ADM6918/X will stop loading the 93c66. The user also could pull down the EDO to force the ADM6918/X not to load the 93c66. The 93c66 loading time is around 30ms. Then CPU should give the high-z value in the EECS, EESK and EDI pins in this period if we really want to use CPU to read or write the registers in the ADM6918/X.

The EEPROM Interface needs only one Write command to complete a writing operation. If updating the 93c66 at the same time is necessary, three commands Write Enable, Write, and Write Disable are needed to complete this job (See 93c66 Spec. for a reference). Users should note that the EEPROM interface only allows the CPU to write the EEPROM register in the ADM6918/X and doesn't support the READ command. If CPU gives the Read Command, ADM6918/X will not respond and 93c66 will respond with the value. Users should also note that one additional EESK cycle is needed between any continuous commands (Read or Write)

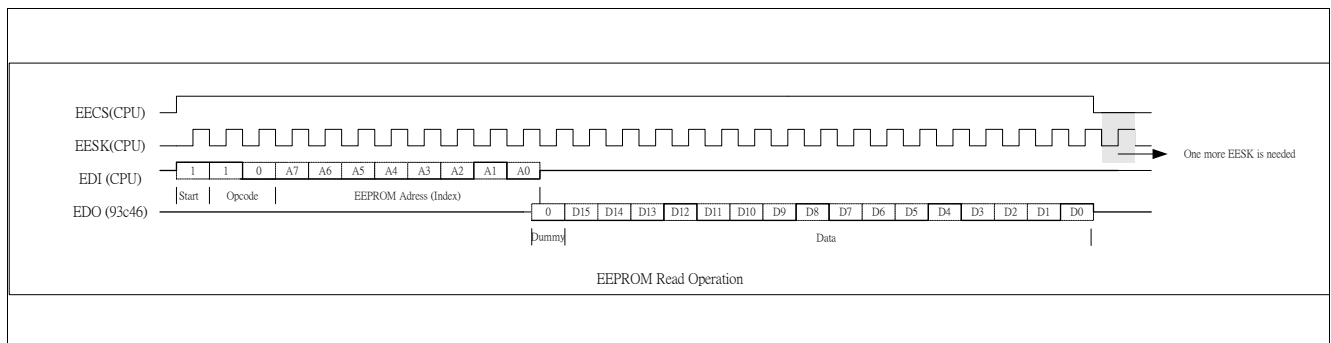


Figure 7 Read 93c66 via the EEPROM Interface (Index = 2, Data = 16'h1111)

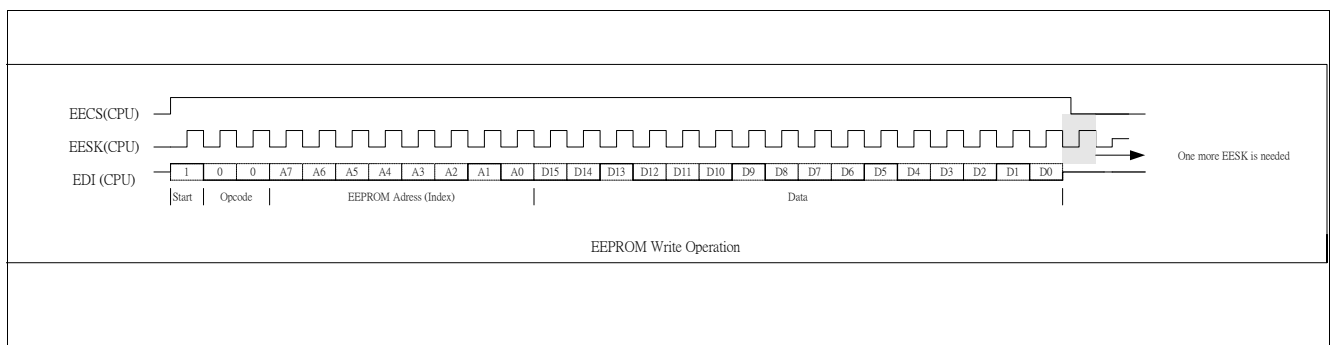


Figure 8 Write EEPROM Registers in the ADM6918/X (Index = 2, Data = 16'h2222)

3.1.26.3 SMI Interface

The SMI consists of two pins, management data clock (EESK) and management data input/output (EDI). The ADM6918/X is designed to support an EESK frequency up to 25 MHz. The EDI pin is bi-directional and may be shared with other devices. EECS pin may be needed (pulled to low) if EEPROM interface is also used.

The EDI pin requires a 1.5 kΩ pull-up which, during idle and turnaround periods, will pull EDI to a logic one state. ADM6918/X requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. The first 32 bits are preamble consisting of 32 contiguous logic one bits on EDI and 32 corresponding cycles on EESK. Following preamble is the start-of-frame field indicated by a <01> pattern. The next field signals the operation code (OP): <10> indicates read from management register operation, and <01> indicates write to

Function Description

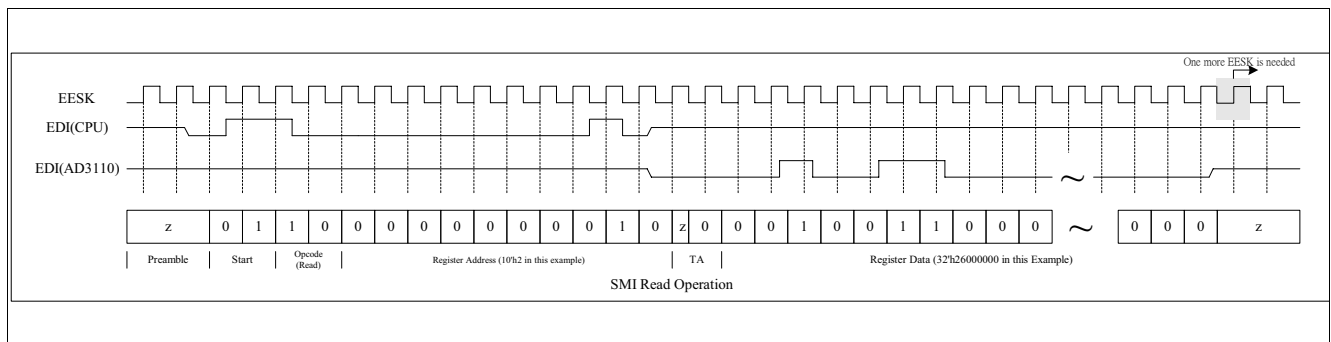
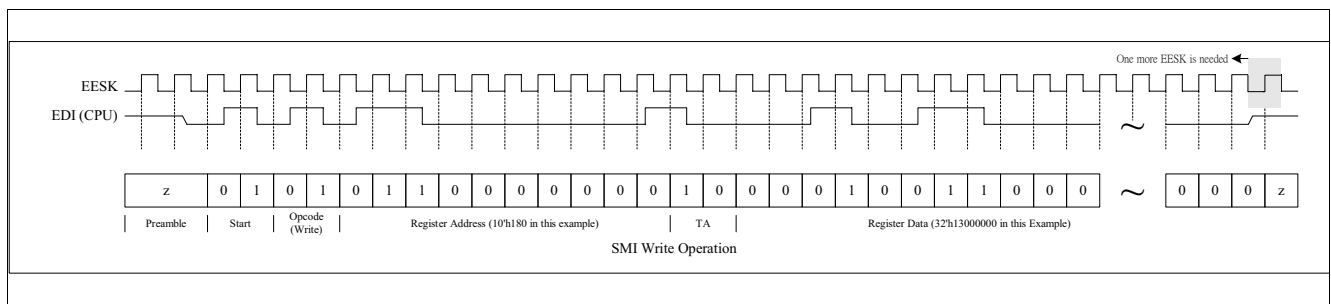
management register operation. The next field is management register address. It is 10 bits wide and the most significant bit is transferred first.

During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the EDI to avoid contention. Following the turnaround time, a 32-bit data stream is read from or written into the management registers of the ADM6918/X.

(A) Preamble Suppression

The SMI of ADM6918/X supports a preamble suppression mode. The ADM6918/X requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. This requirement is generally met by pulling-up the resistor of EDI. While the ADM6918/X will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required.

When ADM6918/X detects that there is address match, then it will enable Read/Write capability for external access. When address is mismatched, then ADM6918/X will tristate the EDI pin.

(B) Read Switch Register via SMI Interface (Offset Hex = 10'h2, Data = 32'h2600_0000)

Figure 9 Read Switch Register via SMI Interface
(C) Write Switch Register via SMI Interface (Offset Hex = 10'h180, Data = 32'h1300_0000)

Figure 10 Write Switch Register via SMI Interface
(D) The Pin Type of EECS, EESK, EDI and EDO during the Operation
Table 14 Pin Type of EECS, EESK, EDI and EDO during Operation

| Pin Name | Reset Operation | Load EEPROM | Write Operation | Read Operation |
|----------|-----------------|-------------|-----------------|----------------|
| EECS | Input | Output | Input | Input |
| EESK | Input | Output | Input | Input |
| EDI | Input | Output | Input | Input / Output |
| EDO | Input | Input | Input | Input |

4 EEPROM Register Format

The EEPROM can be auto-detected by ADM6918/X through the signature register. The ADM6918/X supports C66 EEPROM. After the EEPROM is loaded, the output pins of ADM6918/X are tristate and released to CPU. The release time is about 30ms after end of RESET. Whenever CPU modifies the setting of C66, the new value will be written to ADM6918/X at the same time. If CPU changes the port setting (Duplex/Speed/AEN), the ADM6918/X will restart the auto-negotiation automatically.

Table 15 EEPROM Format

| Offset Hex | | Index | Bit 15 - 8 | Bit 7 - 0 | Type | Default |
|-------------------|------|-----------------|---|-------------------|------|-------------------|
| 0200 _H | Low | 0 _H | Signature | | ro | 4154 _H |
| 0201 _H | High | 1 _H | Global Configuration | | rw | 3800 _H |
| 0202 _H | Low | 2 _H | Port 0 Configuration | | rw | 80FF _H |
| 0203 _H | High | 3 _H | Port 1 Configuration | | rw | 80FF _H |
| 0204 _H | Low | 4 _H | Port 2 Configuration | | rw | 80FF _H |
| 0205 _H | High | 5 _H | Port 3 Configuration | | rw | 80FF _H |
| 0206 _H | Low | 6 _H | Port 4 Configuration | | rw | 80FF _H |
| 0207 _H | High | 7 _H | Port 5 Configuration | | rw | 80FF _H |
| 0208 _H | Low | 8 _H | Port 6 Configuration | | rw | 80FF _H |
| 0209 _H | High | 9 _H | Port 7 Configuration | | rw | 80FF _H |
| 020A _H | Low | A _H | Port 8 Configuration | | rw | 80FF _H |
| 020B _H | High | B _H | Port 9 Configuration | | rw | 80FF _H |
| 020C _H | Low | C _H | Port10 Configuration | | rw | 80FF _H |
| 020D _H | High | D _H | Port 11 Configuration | | rw | 80FF _H |
| 020E | Low | E _H | Port 12 Configuration | | rw | 80FF _H |
| 020f | High | F _H | Port 13 Configuration | | rw | 80FF _H |
| 0210 _H | Low | 10 _H | Port 14 Configuration | | rw | 80FF _H |
| 0211 _H | High | 11 _H | Port 15 Configuration | | rw | 80FF _H |
| 0212 _H | Low | 12 _H | Reserved | | rw | 80FF _H |
| 0213 _H | High | 13 _H | Reserved | | rw | 80FF _H |
| 0214 _H | Low | 14 _H | Reserved | | rw | 80FF _H |
| 0215 _H | High | 15 _H | Reserved | | rw | 80FF _H |
| 0216 _H | Low | 16 _H | Reserved | | rw | 80FF _H |
| 0217 _H | High | 17 _H | Reserved | | rw | 80FF _H |
| 0218 _H | Low | 18 _H | Reserved | | rw | 80FF _H |
| 0219 _H | High | 19 _H | Reserved | | rw | 80FF _H |
| 021A _H | Low | 1A _H | Port 16 Configuration | | rw | 80FF _H |
| 021B _H | High | 1B _H | Port 17 Configuration | | rw | 80FF _H |
| 021C _H | Low | 1C _H | Miscellaneous Configuration | | rw | 820 _H |
| 021D _H | High | 1D _H | TOS Priority Map | VLAN Priority Map | rw | 0 _H |
| 021E _H | Low | 1E _H | Forwarding Group 0 Outbound Port Map Low | | rw | FFFF _H |
| 021F _H | High | 1F _H | Forwarding Group 0 Outbound Port Map High | | rw | 3FF _H |
| 0220 _H | Low | 20 _H | Forwarding Group 1 Outbound Port Map Low | | rw | FFFF _H |
| 0221 _H | High | 21 _H | Forwarding Group 1 Outbound Port Map High | | rw | 3FF |

EEPROM Register Format

Table 15 EEPROM Format (cont'd)

| Offset Hex | | Index | Bit 15 - 8 | Bit 7 - 0 | Type | Default |
|-------------------|------|-----------------|--|-----------|------|-------------------|
| 0222 _H | Low | 22 _H | Forwarding Group 2 Outbound Port Map Low | | rw | FFFF _H |
| 0223 _H | High | 23 _H | Forwarding Group 2 Outbound Port Map High | | rw | 3FF _H |
| 0224 _H | Low | 24 _H | Forwarding Group 3 Outbound Port Map Low | | rw | FFFF _H |
| 0225 _H | High | 25 _H | Forwarding Group 3 Outbound Port Map High | | rw | 3FF _H |
| 0226 _H | Low | 26 _H | Forwarding Group 4 Outbound Port Map Low | | rw | FFFF _H |
| 0227 _H | High | 27 _H | Forwarding Group 4 Outbound Port Map High | | rw | 3FF _H |
| 0228 _H | Low | 28 _H | Forwarding Group 5 Outbound Port Map Low | | rw | FFFF _H |
| 0229 _H | High | 29 _H | Forwarding Group 5 Outbound Port Map High | | rw | 3FF _H |
| 022A _H | Low | 2A _H | Forwarding Group 6 Outbound Port Map Low | | rw | FFFF _H |
| 022B _H | High | 2B _H | Forwarding Group 6 Outbound Port Map High | | rw | 3FF _H |
| 022C _H | Low | 2C _H | Forwarding Group 7 Outbound Port Map Low | | rw | FFFF _H |
| 022D _H | High | 2D _H | Forwarding Group 7 Outbound Port Map High | | rw | 3FF _H |
| 022E _H | Low | 2E _H | Forwarding Group 8 Outbound Port Map Low | | rw | FFFF _H |
| 022F _H | High | 2F _H | Forwarding Group 8 Outbound Port Map High | | rw | 3FF _H |
| 0230 _H | Low | 30 _H | Forwarding Group 9 Outbound Port Map Low | | rw | FFFF _H |
| 0231 _H | High | 31 _H | Forwarding Group 9 Outbound Port Map High | | rw | 3FF _H |
| 0232 _H | Low | 32 _H | Forwarding Group 10 Outbound Port Map Low | | rw | FFFF _H |
| 0233 _H | High | 33 _H | Forwarding Group 10 Outbound Port Map High | | rw | 3FF _H |
| 0234 _H | Low | 34 _H | Forwarding Group 11 Outbound Port Map Low | | rw | FFFF _H |
| 0235 _H | High | 35 _H | Forwarding Group 11 Outbound Port Map High | | rw | 3FF _H |
| 0236 _H | Low | 36 _H | Forwarding Group 12 Outbound Port Map Low | | rw | FFFF _H |
| 0237 _H | High | 37 _H | Forwarding Group 12 Outbound Port Map High | | rw | 3FF _H |
| 0238 _H | Low | 38 _H | Forwarding Group 13 Outbound Port Map Low | | rw | FFFF _H |
| 0239 _H | High | 39 _H | Forwarding Group 13 Outbound Port Map High | | rw | 3FF _H |
| 023A _H | Low | 3A _H | Forwarding Group 14 Outbound Port Map Low | | rw | FFFF _H |
| 023B _H | High | 3B _H | Forwarding Group 14 Outbound Port Map High | | rw | 3FF _H |
| 023C _H | Low | 3C _H | Forwarding Group 15 Outbound Port Map Low | | rw | FFFF _H |
| 023D _H | High | 3D _H | Forwarding Group 15 Outbound Port Map High | | rw | 3FF _H |
| 023E _H | Low | 3E _H | Forwarding Group 16 Outbound Port Map Low | | rw | FFFF _H |
| 023F _H | High | 3F _H | Forwarding Group 16 Outbound Port Map High | | rw | 3FF _H |
| 0240 _H | Low | 40 _H | Forwarding Group 17 Outbound Port Map Low | | rw | FFFF _H |
| 0241 _H | High | 41 _H | Forwarding Group 17 Outbound Port Map High | | rw | 3FF _H |
| 0242 _H | Low | 42 _H | Forwarding Group 18 Outbound Port Map Low | | rw | FFFF _H |
| 0243 _H | High | 43 _H | Forwarding Group 18 Outbound Port Map High | | rw | 3FF _H |
| 0244 _H | Low | 44 _H | Forwarding Group 19 Outbound Port Map Low | | rw | FFFF _H |
| 0245 _H | High | 45 _H | Forwarding Group 19 Outbound Port Map High | | rw | 3FF _H |
| 0246 _H | Low | 46 _H | Forwarding Group 20 Outbound Port Map Low | | rw | FFFF _H |
| 0247 _H | High | 47 _H | Forwarding Group 20 Outbound Port Map High | | rw | 3FF _H |
| 0248 _H | Low | 48 _H | Forwarding Group 21 Outbound Port Map Low | | rw | FFFF _H |
| 0249 _H | High | 49 _H | Forwarding Group 21 Outbound Port Map High | | rw | 3FF _H |

EEPROM Register Format

Table 15 EEPROM Format (cont'd)

| Offset Hex | | Index | Bit 15 - 8 | Bit 7 - 0 | Type | Default |
|-------------------|------|-----------------|--|-----------|------|-------------------|
| 024A _H | Low | 4A _H | Forwarding Group 22 Outbound Port Map Low | | rw | FFFF _H |
| 024B _H | High | 4B _H | Forwarding Group 22 Outbound Port Map High | | rw | 3FF _H |
| 024C _H | Low | 4C _H | Forwarding Group 23 Outbound Port Map Low | | rw | FFFF _H |
| 024D _H | High | 4D _H | Forwarding Group 23 Outbound Port Map High | | rw | 3FF _H |
| 024E _H | Low | 4E _H | Forwarding Group 24 Outbound Port Map Low | | rw | FFFF _H |
| 024F _H | High | 4F _H | Forwarding Group 24 Outbound Port Map High | | rw | 3FF _H |
| 0250 _H | Low | 50 _H | Forwarding Group 25 Outbound Port Map Low | | rw | FFFF _H |
| 0251 _H | High | 51 _H | Forwarding Group 25 Outbound Port Map High | | rw | 3FF _H |
| 0252 _H | Low | 52 _H | Forwarding Group 26 Outbound Port Map Low | | rw | FFFF _H |
| 0253 _H | High | 53 _H | Forwarding Group 26 Outbound Port Map High | | rw | 3FF _H |
| 0254 _H | Low | 54 _H | Forwarding Group 27 Outbound Port Map Low | | rw | FFFF _H |
| 0255 _H | High | 55 _H | Forwarding Group 27 Outbound Port Map High | | rw | 3FF _H |
| 0256 _H | Low | 56 _H | Forwarding Group 28 Outbound Port Map Low | | rw | FFFF _H |
| 0257 _H | High | 57 _H | Forwarding Group 28 Outbound Port Map High | | rw | 3FF _H |
| 0258 _H | Low | 58 _H | Forwarding Group 29 Outbound Port Map Low | | rw | FFFF _H |
| 0259 _H | High | 59 _H | Forwarding Group 29 Outbound Port Map High | | rw | 3FF _H |
| 025A _H | Low | 5A _H | Forwarding Group 30 Outbound Port Map Low | | rw | FFFF _H |
| 025B _H | High | 5B _H | Forwarding Group 30 Outbound Port Map High | | rw | 3FF _H |
| 025C _H | Low | 5C _H | Forwarding Group 31 Outbound Port Map Low | | rw | FFFF _H |
| 025D _H | High | 5D _H | Forwarding Group 31 Outbound Port Map High | | rw | 3FF _H |
| 025E _H | Low | 5E _H | PVID shift | P0 VID | rw | 1 _H |
| 025F _H | High | 5F _H | P1 VID | | rw | 1 _H |
| 0260 _H | Low | 60 _H | P2 VID | | rw | 1 _H |
| 0261 _H | High | 61 _H | P3 VID | | rw | 1 _H |
| 0262 _H | Low | 62 _H | P4 VID | | rw | 1 _H |
| 0263 _H | High | 63 _H | P5 VID | | rw | 1 _H |
| 0264 _H | Low | 64 _H | P6 VID | | rw | 1 _H |
| 0265 _H | High | 65 _H | P7 VID | | rw | 1 _H |
| 0266 _H | Low | 66 _H | P8 VID | | rw | 1 _H |
| 0267 _H | High | 67 _H | P9 VID | | rw | 1 _H |
| 0268 _H | Low | 68 _H | P10 VID | | rw | 1 _H |
| 0269 _H | High | 69 _H | P11 VID | | rw | 1 _H |
| 026A _H | Low | 6A _H | P12 VID | | rw | 1 _H |
| 026B _H | High | 6B _H | P13 VID | | rw | 1 _H |
| 026C _H | Low | 6C _H | P14 VID | | rw | 1 _H |
| 026D _H | High | 6D _H | P15 VID | | rw | 1 _H |
| 026E _H | Low | 6E _H | Reserved | | rw | 1 _H |
| 026F _H | High | 6F _H | Reserved | | rw | 1 _H |
| 0270 _H | Low | 70 _H | Reserved | | rw | 1 _H |
| 0271 _H | High | 71 _H | Reserved | | rw | 1 _H |

EEPROM Register Format

Table 15 EEPROM Format (cont'd)

| Offset Hex | | Index | Bit 15 - 8 | Bit 7 - 0 | Type | Default |
|-------------------|------|-----------------|---|-----------|------|-------------------|
| 0272 _H | Low | 72 _H | Reserved | | rw | 1 _H |
| 0273 _H | High | 73 _H | Reserved | | rw | 1 _H |
| 0274 _H | Low | 74 _H | Reserved | | rw | 1 _H |
| 0275 _H | High | 75 _H | Reserved | | rw | 1 _H |
| 0276 _H | Low | 76 _H | P16 VID | | rw | 1 _H |
| 0277 _H | High | 77 _H | P17 VID | | rw | 1 _H |
| 0278 _H | Low | 78 _H | P0, P1, P2, P3 Bandwidth Control Register | | rw | 0 _H |
| 0279 _H | High | 79 _H | P4, P5, P6, P7 Bandwidth Control Register | | rw | 0 _H |
| 027A _H | Low | 7A _H | P8, P9, P10, P11 Bandwidth Control Register | | rw | 0 _H |
| 027B _H | High | 7B _H | P12, P13, P14, P15 Bandwidth Control Register | | rw | 0 _H |
| 027C _H | Low | 7C _H | Reserved | | rw | 0 _H |
| 027D _H | High | 7D _H | Reserved | | rw | 0 _H |
| 027E _H | Low | 7E _H | P24, P25 Bandwidth Control Register | | rw | 0 _H |
| 027F _H | High | 7F _H | Bandwidth Control Enable Register Low | | rw | 0 _H |
| 0280 _H | Low | 80 _H | Bandwidth Control Enable Register High | | rw | 0 _H |
| 0281 _H | High | 81 _H | Reserved | | rw | 0 _H |
| 0282 _H | Low | 82 _H | Reserved | | rw | 0 _H |
| 0283 _H | High | 83 _H | Reserved | | rw | 100 _H |
| 0284 _H | Low | 84 _H | Reserved | | rw | 0 _H |
| 0285 _H | High | 85 _H | Reserved | | rw | 0 _H |
| 0286 _H | Low | 86 _H | Reserved | | rw | 0 _H |
| 0287 _H | High | 87 _H | Reserved | | rw | 0 _H |
| 0288 _H | Low | 88 _H | Reserved | | rw | 0 _H |
| 0289 _H | High | 89 _H | Reserved | | rw | 0 _H |
| 028A _H | Low | 8A _H | Reserved | | rw | FF00 _H |
| 028B _H | HIGH | 8B _H | Customized PHY Control Group 0 | | rw | 0 _H |
| 028C _H | Low | 8C _H | Customized PHY Control Group 1 | | rw | 0 _H |
| 028D _H | HIGH | 8D _H | Customized PHY Control Group 2 | | rw | 0 _H |
| 028E _H | Low | 8E _H | Customized PHY Control Group 3 | | rw | 0 _H |
| 028F _H | HIGH | 8F _H | Group 0 PHY Customized DATA 0 | | rw | 0 _H |
| 0290 _H | Low | 90 _H | Group 0 PHY Customized DATA 1 | | rw | 0 _H |
| 0291 _H | HIGH | 91 _H | Group 1 PHY Customized DATA 0 | | rw | 0 _H |
| 0292 _H | Low | 92 _H | Group 1 PHY Customized DATA 1 | | rw | 0 _H |
| 0293 _H | HIGH | 93 _H | Group 2 PHY Customized DATA 0 | | rw | 0 _H |
| 0294 _H | Low | 94 _H | Group 2 PHY Customized DATA 1 | | rw | 0 _H |
| 0295 _H | HIGH | 95 _H | Group 3 PHY Customized DATA 0 | | rw | 0 _H |
| 0296 _H | Low | 96 _H | Group 3 PHY Customized DATA 1 | | rw | 0 _H |
| 0297 _H | HIGH | 97 _H | PHY Customized Enable Register | | rw | 0 _H |
| 0298 _H | Low | 98 _H | PPPOE Control Register 0 | | rw | 0 _H |
| 0299 _H | HIGH | 99 _H | PPPOE Control Register 1 | | rw | 0 _H |

EEPROM Register Format
Table 15 EEPROM Format (cont'd)

| Offset Hex | | Index | Bit 15 - 8 | Bit 7 - 0 | Type | Default |
|-------------------|------|-----------------|--------------------------------|-----------|------|-------------------|
| 029A _H | Low | 9A _H | PHY Control Register 0 | | rw | 0 _H |
| 029B _H | HIGH | 9B _H | PHY Control Register 1 | | rw | 0 _H |
| 029C _H | Low | 9C _H | Disable MDIO Active Register 0 | | rw | 0 _H |
| 029D _H | HIGH | 9D _H | Disable MDIO Active Register 1 | | rw | 0 _H |
| 029E _H | Low | 9E _H | Disable Port Register 0 | | rw | 0 _H |
| 029F _H | HIGH | 9F _H | Disable Port Register 1 | | rw | 0 _H |
| 02A0 _H | Low | A0 _H | IGMP Enable Register 0 | | rw | 0 _H |
| 02A1 _H | HIGH | A1 _H | IGMP Enable Register 1 | | rw | 0 _H |
| 02A2 _H | Low | A2 _H | CPU Control Register | | rw | 001F _H |
| 02A3 _H | HIGH | A3 _H | MAC Forward Mode Register 0 | | rw | 4 _H |
| 02A4 _H | Low | A4 _H | MAC Forward Mode Register 1 | | rw | 3 _H |
| 02A5 _H | HIGH | A5 _H | MAC Forward Mode Register 2 | | rw | 0 _H |
| 02A6 _H | Low | A6 _H | Trunking Enable Register 0 | | rw | 0 _H |
| 02A7 _H | HIGH | A7 _H | Trunking Enable Register 1 | | rw | 0 _H |

4.1 EEPROM Registers

Table 16 Registers Address Space

| Module | Base Address | End Address | Note |
|--------|-------------------|-------------------|------|
| EEPROM | 0200 _H | 02A7 _H | |

Table 17 Registers Overview

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---|-------------------|--------------------|
| SIG | Signature | 0200 _H | 41 |
| GCR | Global Configuration Register | 0201 _H | 41 |
| PCR_0 | Port 0 Configuration Register | 0202 _H | 43 |
| PCR_1 | Port 1 Configuration | 0203 _H | 46 |
| PCR_2 | Port 2 Configuration | 0204 _H | 46 |
| PCR_3 | Port 3 Configuration | 0205 _H | 46 |
| PCR_4 | Port 4 Configuration | 0206 _H | 46 |
| PCR_5 | Port 5 Configuration | 0207 _H | 46 |
| PCR_6 | Port 6 Configuration | 0208 _H | 46 |
| PCR_7 | Port 7 Configuration | 0209 _H | 46 |
| PCR_8 | Port 8 Configuration | 020A _H | 46 |
| PCR_9 | Port 9 Configuration | 020B _H | 46 |
| PCR_10 | Port 10 Configuration | 020C _H | 46 |
| PCR_11 | Port 11 Configuration | 020D _H | 46 |
| PCR_12 | Port 12 Configuration | 020E _H | 46 |
| PCR_13 | Port 13 Configuration | 020F _H | 46 |
| PCR_14 | Port 14 Configuration | 0210 _H | 46 |
| PCR_15 | Port 15 Configuration | 0211 _H | 46 |
| RES1 | Reserved Register 1 | 0212 _H | 46 |
| RES2 | Reserved Register 2 | 0213 _H | 47 |
| RES3 | Reserved Register 3 | 0214 _H | 47 |
| RES4 | Reserved Register 4 | 0215 _H | 47 |
| RES5 | Reserved Register 5 | 0216 _H | 47 |
| RES6 | Reserved Register 6 | 0217 _H | 47 |
| RES7 | Reserved Register 7 | 0218 _H | 47 |
| RES8 | Reserved Register 8 | 0219 _H | 47 |
| PCR_16 | Port 16 Configuration | 021A _H | 46 |
| PCR_17 | Port 17 Configuration | 021B _H | 46 |
| MC | Miscellaneous Configuration | 021C _H | 48 |
| VLAN | VLAN(TOS) Priority Map | 021D _H | 48 |
| FGOPML_0 | Forwarding Group 0 Outbound Port Map Low | 021E _H | 50 |
| FGOPMH_0 | Forwarding Group 0 Outbound Port Map High | 021F _H | 52 |
| FGOPML_1 | Forwarding Group 1 Outbound Port Map Low | 0220 _H | 51 |
| FGOPMH_1 | Forwarding Group 1 Outbound Port Map High | 0221 _H | 53 |

EEPROM Register Format

Table 17 Registers Overview (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--|-------------------|-------------|
| FGOPML_2 | Forwarding Group 2 Outbound Port Map Low | 0222 _H | 51 |
| FGOPMH_2 | Forwarding Group 2 Outbound Port Map High | 0223 _H | 53 |
| FGOPML_3 | Forwarding Group 3 Outbound Port Map Low | 0224 _H | 51 |
| FGOPMH_3 | Forwarding Group 3 Outbound Port Map High | 0225 _H | 53 |
| FGOPML_4 | Forwarding Group 4 Outbound Port Map Low | 0226 _H | 51 |
| FGOPMH_4 | Forwarding Group 4 Outbound Port Map High | 0227 _H | 53 |
| FGOPML_5 | Forwarding Group 5 Outbound Port Map Low | 0228 _H | 51 |
| FGOPMH_5 | Forwarding Group 5 Outbound Port Map High | 0229 _H | 53 |
| FGOPML_6 | Forwarding Group 6 Outbound Port Map Low | 022A _H | 51 |
| FGOPMH_6 | Forwarding Group 6 Outbound Port Map High | 022B _H | 53 |
| FGOPML_7 | Forwarding Group 7 Outbound Port Map Low | 022C _H | 51 |
| FGOPMH_7 | Forwarding Group 7 Outbound Port Map High | 022D _H | 53 |
| FGOPML_8 | Forwarding Group 8 Outbound Port Map Low | 022E _H | 51 |
| FGOPMH_8 | Forwarding Group 8 Outbound Port Map High | 022F _H | 53 |
| FGOPML_9 | Forwarding Group 9 Outbound Port Map Low | 0230 _H | 51 |
| FGOPMH_9 | Forwarding Group 9 Outbound Port Map High | 0231 _H | 53 |
| FGOPML_10 | Forwarding Group 10 Outbound Port Map Low | 0232 _H | 51 |
| FGOPMH_10 | Forwarding Group 10 Outbound Port Map High | 0233 _H | 53 |
| FGOPML_11 | Forwarding Group 11 Outbound Port Map Low | 0234 _H | 51 |
| FGOPMH_11 | Forwarding Group 11 Outbound Port Map High | 0235 _H | 53 |
| FGOPML_12 | Forwarding Group 12 Outbound Port Map Low | 0236 _H | 51 |
| FGOPMH_12 | Forwarding Group 12 Outbound Port Map High | 0237 _H | 53 |
| FGOPML_13 | Forwarding Group 13 Outbound Port Map Low | 0238 _H | 51 |
| FGOPMH_13 | Forwarding Group 13 Outbound Port Map High | 0239 _H | 53 |
| FGOPML_14 | Forwarding Group 14 Outbound Port Map Low | 023A _H | 51 |
| FGOPMH_14 | Forwarding Group 14 Outbound Port Map High | 023B _H | 53 |
| FGOPML_15 | Forwarding Group 15 Outbound Port Map Low | 023C _H | 51 |
| FGOPMH_15 | Forwarding Group 15 Outbound Port Map High | 023D _H | 53 |
| FGOPML_16 | Forwarding Group 16 Outbound Port Map Low | 023E _H | 51 |
| FGOPMH_16 | Forwarding Group 16 Outbound Port Map High | 023F _H | 53 |
| FGOPML_17 | Forwarding Group 17 Outbound Port Map Low | 0240 _H | 51 |
| FGOPMH_17 | Forwarding Group 17 Outbound Port Map High | 0241 _H | 53 |
| FGOPML_18 | Forwarding Group 18 Outbound Port Map Low | 0242 _H | 52 |
| FGOPMH_18 | Forwarding Group 18 Outbound Port Map High | 0243 _H | 53 |
| FGOPML_19 | Forwarding Group 19 Outbound Port Map Low | 0244 _H | 52 |
| FGOPMH_19 | Forwarding Group 19 Outbound Port Map High | 0245 _H | 53 |
| FGOPML_20 | Forwarding Group 20 Outbound Port Map Low | 0246 _H | 52 |
| FGOPMH_20 | Forwarding Group 20 Outbound Port Map High | 0247 _H | 53 |
| FGOPML_21 | Forwarding Group 21 Outbound Port Map Low | 0248 _H | 52 |
| FGOPMH_21 | Forwarding Group 21 Outbound Port Map High | 0249 _H | 53 |
| FGOPML_22 | Forwarding Group 22 Outbound Port Map Low | 024A _H | 52 |

Table 17 Registers Overview (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|------------------------|--|-------------------|--------------------|
| FGOPMH_22 | Forwarding Group 22 Outbound Port Map High | 024B _H | 53 |
| FGOPML_23 | Forwarding Group 23 Outbound Port Map Low | 024C _H | 52 |
| FGOPMH_23 | Forwarding Group 23 Outbound Port Map High | 024D _H | 54 |
| FGOPML_24 | Forwarding Group 24 Outbound Port Map Low | 024E _H | 52 |
| FGOPMH_24 | Forwarding Group 24 Outbound Port Map High | 024F _H | 54 |
| FGOPML_25 | Forwarding Group 25 Outbound Port Map Low | 0250 _H | 52 |
| FGOPMH_25 | Forwarding Group 25 Outbound Port Map High | 0251 _H | 54 |
| FGOPML_26 | Forwarding Group 26 Outbound Port Map Low | 0252 _H | 52 |
| FGOPMH_26 | Forwarding Group 26 Outbound Port Map High | 0253 _H | 54 |
| FGOPML_27 | Forwarding Group 27 Outbound Port Map Low | 0254 _H | 52 |
| FGOPMH_27 | Forwarding Group 27 Outbound Port Map High | 0255 _H | 54 |
| FGOPML_28 | Forwarding Group 28 Outbound Port Map Low | 0256 _H | 52 |
| FGOPMH_28 | Forwarding Group 28 Outbound Port Map High | 0257 _H | 54 |
| FGOPML_29 | Forwarding Group 29 Outbound Port Map Low | 0258 _H | 52 |
| FGOPMH_29 | Forwarding Group 29 Outbound Port Map High | 0259 _H | 54 |
| FGOPML_30 | Forwarding Group 30 Outbound Port Map Low | 025A _H | 52 |
| FGOPMH_30 | Forwarding Group 30 Outbound Port Map High | 025B _H | 54 |
| FGOPML_31 | Forwarding Group 31 Outbound Port Map Low | 025C _H | 52 |
| FGOPMH_31 | Forwarding Group 31 Outbound Port Map High | 025D _H | 54 |
| P0VIDS | P0 VID and PVID Shift | 025E _H | 54 |
| P1_VID | P1 VID Configuration | 025F _H | 55 |
| P2_VID | P2 VID Configuration | 0260 _H | 56 |
| P3_VID | P3 VID Configuration | 0261 _H | 56 |
| P4_VID | P4 VID Configuration | 0262 _H | 56 |
| P5_VID | P5 VID Configuration | 0263 _H | 56 |
| P6_VID | P6 VID Configuration | 0264 _H | 56 |
| P7_VID | P7 VID Configuration | 0265 _H | 56 |
| P8_VID | P8 VID Configuration | 0266 _H | 56 |
| P9_VID | P9 VID Configuration | 0267 _H | 56 |
| P10_VID | P10 VID Configuration | 0268 _H | 56 |
| P11_VID | P11 VID Configuration | 0269 _H | 56 |
| P12_VID | P12 VID Configuration | 026A _H | 56 |
| P13_VID | P13 VID Configuration | 026B _H | 56 |
| P14_VID | P14 VID Configuration | 026C _H | 56 |
| P15_VID | P15 VID Configuration | 026D _H | 56 |
| RES9 | Reserved Register 9 | 026E _H | 47 |
| RES10 | Reserved Register 10 | 026F _H | 47 |
| RES11 | Reserved Register 11 | 0270 _H | 47 |
| RES12 | Reserved Register 12 | 0271 _H | 47 |
| RES13 | Reserved Register 13 | 0272 _H | 47 |
| RES14 | Reserved Register 14 | 0273 _H | 47 |

Table 17 Registers Overview (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---|-------------------|-------------|
| RES15 | Reserved Register 15 | 0274 _H | 47 |
| RES16 | Reserved Register 16 | 0275 _H | 47 |
| P24_VID | P24 VID Configuration | 0276 _H | 56 |
| P25_VID | P25 VID Configuration | 0277 _H | 56 |
| P0_3_BCR | P0, P1, P2, P3 Bandwidth Control Register | 0278 _H | 56 |
| P4_7_BCR | P4, P5, P6, P7 Bandwidth Control Register | 0279 _H | 57 |
| P8_11_BCR | P8, P9, P10, P11 Bandwidth Control Register | 027A _H | 59 |
| P12_15_BCR | P12, P13, P14, P15 Bandwidth Control Register | 027B _H | 60 |
| RES17 | Reserved Register 17 | 027C _H | 47 |
| RES18 | Reserved Register 18 | 027D _H | 47 |
| P24_25_BCR | P24, P25 Bandwidth Control Register | 027E _H | 61 |
| BCERL | Bandwidth Control Enable Register Low | 027F _H | 62 |
| BCERH | Bandwidth Control Enable Register High | 0280 _H | 63 |
| RES19 | Reserved Register 19 | 0281 _H | 47 |
| RES20 | Reserved Register 20 | 0282 _H | 47 |
| RES21 | Reserved Register 21 | 0283 _H | 47 |
| RES22 | Reserved Register 22 | 0284 _H | 47 |
| RES23 | Reserved Register 23 | 0285 _H | 47 |
| RES24 | Reserved Register 24 | 0286 _H | 47 |
| RES25 | Reserved Register 25 | 0287 _H | 47 |
| RES26 | Reserved Register 26 | 0288 _H | 47 |
| RES27 | Reserved Register 27 | 0289 _H | 47 |
| RES28 | Reserved Register 28 | 028A _H | 47 |
| CPHYCG0 | Customized PHY Control Group 0 | 028B _H | 63 |
| CPHYCG1 | Customized PHY Control Group 1 | 028C _H | 65 |
| CPHYCG2 | Customized PHY Control Group 2 | 028D _H | 66 |
| CPHYCG3 | Customized PHY Control Group 3 | 028E _H | 66 |
| G0PHYCD0 | Group 0 PHY Customized DATA 0 | 028F _H | 67 |
| G0PHYCD1 | Group 0 PHY Customized DATA 1 | 0290 _H | 67 |
| G1PHYCD0 | Group 1 PHY Customized DATA 0 | 0291 _H | 68 |
| G1PHYCD1 | Group 1 PHY Customized DATA 1 | 0292 _H | 68 |
| G2PHYCD0 | Group 2 PHY Customized DATA 0 | 0293 _H | 68 |
| G2PHYCD1 | Group 2 PHY Customized DATA 1 | 0294 _H | 69 |
| G3PHYCD0 | Group 3 PHY Customized DATA 0 | 0295 _H | 69 |
| G3PHYCD1 | Group 3 PHY Customized DATA 1 | 0296 _H | 69 |
| PHYCE | PHY Customized Enable Register | 0297 _H | 70 |
| PPPOEC0 | PPPOE Control Register 0 | 0298 _H | 71 |
| PPPOEC1 | PPPOE Control Register 1 | 0299 _H | 72 |
| PHYCR0 | PHY Control Register 0 | 029A _H | 72 |
| PHYCR1 | PHY Control Register 1 | 029B _H | 73 |
| DMDIOAR0 | Disable MDIO Active Register 0 | 029C _H | 74 |

EEPROM Register Format

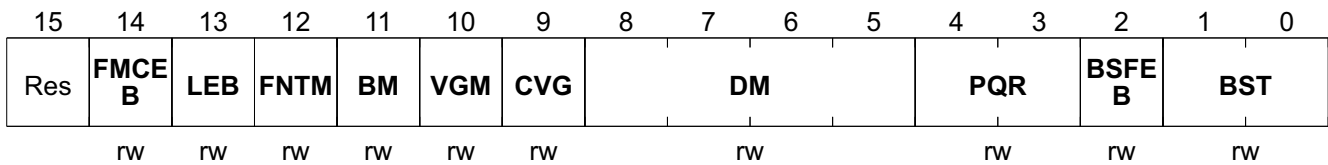
Table 17 Registers Overview (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|--------------------------|--|-------------------|--------------------|
| DMDIOAR1 | Disable MDIO Active Register 1 | 029D _H | 75 |
| PDR0 | Port Disable Register 0 | 029E _H | 75 |
| PDR1 | Port Disable Register 1 | 029F _H | 76 |
| IGMPSCR0 | IGMP Snooping Control Register 0 | 02A0 _H | 76 |
| IGMPSCR1 | IGMP Snooping Control Register 1 | 02A1 _H | 77 |
| CPUCR | CPU Control Register | 02A2 _H | 78 |
| SMACFCR0 | Special MAC Forward Control Register 0 | 02A3 _H | 80 |
| SMACFCR1 | Special MAC Forward Control Register 1 | 02A4 _H | 81 |
| SMACFCR2 | Special MAC Forward Control Register 2 | 02A5 _H | 82 |
| TER0 | Trunking Enable Register 0 | 02A6 _H | 83 |
| TER1 | Trunking Enable Register 1 | 02A7 _H | 84 |

The register is addressed wordwise.

Table 18 Register Access Types

| Mode | Symbol | Description HW | Description SW |
|-------------------------------|--------|---|---|
| read/write | rw | Register is used as input for the HW | Register is read and writable by SW |
| read | r | Register is written by HW (register between input and output -> one cycle delay) | Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.) |
| Read only | ro | Register is set by HW (register between input and output -> one cycle delay) | SW can only read this register |
| Read virtual | rv | Physically, there is no new register, the input of the signal is connected directly to the address multiplexer. | SW can only read this register |
| Latch high, self clearing | lhsc | Latch high signal at high level, clear on read | SW can read the register |
| Latch low, self clearing | llsc | Latch high signal at low-level, clear on read | SW can read the register |
| Latch high, mask clearing | lhmk | Latch high signal at high level, register cleared with written mask | SW can read the register, with write mask the register can be cleared (1 clears) |
| Latch low, mask clearing | llmk | Latch high signal at low-level, register cleared on read | SW can read the register, with write mask the register can be cleared (1 clears) |
| Interrupt high, self clearing | ihsc | Differentiate the input signal (low->high) register cleared on read | SW can read the register |
| Interrupt low, self clearing | ilsc | Differentiate the input signal (high->low) register cleared on read | SW can read the register |
| Interrupt high, mask clearing | ihmk | Differentiate the input signal (high->low) register cleared with written mask | SW can read the register, with write mask the register can be cleared |
| Interrupt low, mask clearing | ilmk | Differentiate the input signal (low->high) register cleared with written mask | SW can read the register, with write mask the register can be cleared |

EEPROM Register Format


| Field | Bits | Type | Description |
|-------|------|------|--|
| FMCEB | 14 | rw | Fast Management Clock Enable Bit 0 _B , The switch will use 2.5 M clock to configure the phys. 1 _B , The switch will use 10 M clock to configure the phys. |
| LEB | 13 | rw | Length 1536 Enable Bit 0 _B , The switch can receive packets of less then 1518 bytes. 1 _B , The switch can receive packets of less than 1536 bytes. |
| FNTM | 12 | rw | Force No Tag Mode 0 _B , The switch is not configured to Force No Tag Mode. 1 _B , The switch is configured to Force No Tag Mode. In this mode, the ADM6918/X will not recognize the VLAN TAG even if they contain a Tag Header. |
| BM | 11 | rw | Bypass Mode 0 _B , The switch is not configured to Bypass Mode. 1 _B , The switch is configured to Bypass Mode. The packets will not be modified when they are transmitted. |
| VGM | 10 | rw | VLAN Group Mode 1 _B , The switch is configured to Tagged Based VLAN 0 _B , The switch is configured to Port Based VLAN. |
| CVG | 9 | rw | Check VLAN Group 0 _B , The ADM6918/X will disable the Check VLAN Group function. 1 _B , The ADM6918/X will check if the packets and the receiving port are at the same Forwarding Group. That is, the output port map for the receiving packet must contain the receiving port. If they belong to different Forwarding Group, the receiving packets will be discarded. <i>Note: Example: Port 3 receives a packet and finds Forwarding Group contains P0, P1, and P2 (doesn't contain P3). This packet will be dropped.</i> |
| DM | 8:5 | rw | Discard Mode This function enables the switch to discard packets according to their priorities if the receiving port disables the flow control function. Users could use this to prevent packets with the low priority to block those with high priority. Bit[8:7] = High Queue Discard Mode (see Sec. 3.1.18) Bit[6:5] = Low Queue Discard Mode |

EEPROM Register Format

| Field | Bits | Type | Description |
|-------|------|------|--|
| PQR | 4:3 | rw | Priority Queue Ratio The ADM6918/X supports two priorities on each output port using weighted round robin scheme. The ratio between the low and high queue is as follows: Bit[4:3] Ratio 00 _B , 1:2 01 _B , 1:4 10 _B , 1:8 11 _B , 1:16 |
| BSFEB | 2 | rw | Broadcast Storm Filtering Enable Bit 0 _B , The ADM6918/X disables the broadcast storm filtering function. 1 _B , The ADM6918/X enables the broadcast storm filtering function. |
| BST | 1:0 | rw | Broadcast Storm Threshold |

Port 0 Configuration Register

PCR_0 **Offset**
Port 0 Configuration Register **0202_H** **Reset Value**
80FF_H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------|------------|------------|------------|------------|-----------|-----------|-----------|--------------------|-------------------|----------------------|----------------------|---------------------|---------------------|----|
| BPEB | FSM | PPM | EPP | TVP | SFE | TP | DA | SA | ANEM CR | FCAF D | 100F DAAR | 100H DAAR | 10FD AAR | 10HD AAR | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|-------|------|------|--|
| BPEB | 15 | rw | Back Pressure Enable Bit 0 _B , The MAC controller doesn't support back-pressure function in half duplex. 1 _B , The MAC controller supports back-pressure function in half duplex. |

EEPROM Register Format

| Field | Bits | Type | Description |
|-------|-------|------|--|
| FSM | 14:13 | rw | Four Security Mode 00 _B , The switch will forward packets with “unknown source addresses” to the CPU port and not learn it if the receiving port is configured to enable security function. The “unknown source address” means that we can’t find an equal address existed in the learning table and its corresponding port number equals to the receiving port. This function needs CUP’s help because we need to create a “static address” to the learning table from the CPU. “Static” means this address will always exist in the leaning table and can only be removed through the CPU. When the address is configured to “Static”, we can prevent this address from overlapping when it is received from a port without the security function enabled. 01 _B , The switch will discard packets with “unknown source addresses” and not learn it if the receiving port is configured to enable security function. Only packets with source addresses existed in the learning table will be forwarded. 10 _B , The first received packets will be locked at the receiving port if the receiving port is configured to enable security function. Only the packets with the source address same as the locked one will be forwarded and learned. 11 _B , The first received packets will be locked as above. The difference is that the receiving port will not receive and learn packets any more after the link goes down even it links up again (it may happen if the station moves to the other port). |
| PPM | 12 | rw | Port-base Priority Mapping 0 _B , Mapped for the Low Queue. 1 _B , Mapped for the High Queue. |
| EPP | 11 | rw | Enable Port-base Priority 0 _B , The switch will use the IPv4 or Tag priority fields for the queue mapping (See Bit [10]). If the packets contain no priority field, then the switch will use the Port-Priority for the default priority. 1 _B , The switch will always use the Port-Priority for the queue mapping even if the receiving packets contain IPv4 or Tag information. |
| TVP | 10 | rw | TOS over VLAN Priority 0 _B , When the receiving packets contain the IPv4 and Tag Priority at the same time, the switch will use Tag priority field for the queue mapping. 1 _B , When the receiving packets contain the IPv4 and Tag Priority at the same time, the switch will use IPv4 priority field for the queue mapping. |
| SFE | 9 | rw | Security Function Enable 0 _B , The switch disables the security function. 1 _B , The switch enables the security function. Four security modes could be selected through Bit[14:13]. |

EEPROM Register Format

| Field | Bits | Type | Description |
|----------|------|------|--|
| TP | 8 | rw | Tagged Port 0 _B , The transmitted port is configured to an untagged port. The transmitted packets from an untagged port will not contain a Tag Header except the transmitted packets are management packet or the Bypass Mode is enabled. 1 _B , The transmitted port is configured to a tagged port. The transmitted packets from a tagged port will always contain a Tag Header except the transmitted packets are management packet or the Bypass Mode is enabled. |
| DA | 7 | rw | Duplex Ability This bit will be used as Bit 8 (Duplex Select) in the Basic Mode Control Register if bypass management function is not enabled, and be used as Duplex Desired if bypass management function is enabled. 0 _B , Half Duplex Enabled. 1 _B , Full Duplex Enabled. |
| SA | 6 | rw | Speed Ability This bit will be used as Bit 13 (Speed Select) in the Basic Mode Control Register if bypass management function is not enabled, and be used as Speed Desired if bypass management function is enabled. 0 _B , 10 Mbit/s Enabled. 1 _B , 100 Mbit/s Enabled. |
| ANEMCR | 5 | rw | Auto Negotiation Enable in Basic Mode Control Register 0 _B , Auto-Negotiation is Disabled. 1 _B , Auto-Negotiation is Enabled. |
| FCAFD | 4 | rw | 802.3x Flow Control Ability in Full Duplex 0 _B , (1). Mac controller doesn't support Pause Frames when the port is configured to bypass management function from MDC/MDIO. (2). If the port is not configured to bypass management function form MDC/MDIO, then it will be used as the Pause bit in Auto-Negotiation Advertisement Register and the Pause function will not be advertised. If Auto-Negotiation function is disabled, then this bit is used and Pause is not supported. (3). If the port is not configured to bypass management function from MDC/MDIO and no PHY is attached to this port, the MAC controller will not support Pause Frames in the full duplex. 1 _B , (1). MAC controller supports Pause Frames when the port is configured to bypass management function from MDC/MDIO. (2). If the port is not configured to bypass management function form MDC/MDIO, then it will be used as the Pause bit in Auto-Negotiation Advertisement Register and the Pause function will be advertised. If Auto-Negotiation function is disabled, then this bit is used and Pause is supported. (3). If the port is not configured to bypass management function from MDC/MDIO and no PHY is attached to this port, the MAC controller will support Pause Frames in the full duplex. |
| 100FDAAR | 3 | rw | 100Base-TX Full Duplex Ability in Auto-Negotiation Advertisement Register 0 _B , 100Base-Tx Full Duplex is not advertised. 1 _B , 100Base-TX Full Duplex is advertised. |

EEPROM Register Format

| Field | Bits | Type | Description |
|----------|------|------|--|
| 100HDAAR | 2 | rw | 100Base-TX Half Duplex Ability in Auto-Negotiation Advertisement Register 0 _B , 100Base-TX Half Duplex is not advertised. 1 _B , 100Base-TX Half Duplex is advertised. |
| 10FDAAR | 1 | rw | 10Base-T Full Duplex Ability in Auto-Negotiation Advertisement Register 0 _B , 10Base-T Full Duplex is not advertised. 1 _B , 10Base-T Full Duplex is advertised. |
| 10HDAAR | 0 | rw | 10Base-T Half Duplex Ability in Auto-Negotiation Advertisement Register 0 _B , 10Base-T Half Duplex is not advertised. 1 _B , 10Base-T Half Duplex is advertised. |

All PCR_x registers have the same structure and characteristics, see [PCR_0](#).
 The offset addresses of the other PCR_x registers are listed in [Table 20](#).

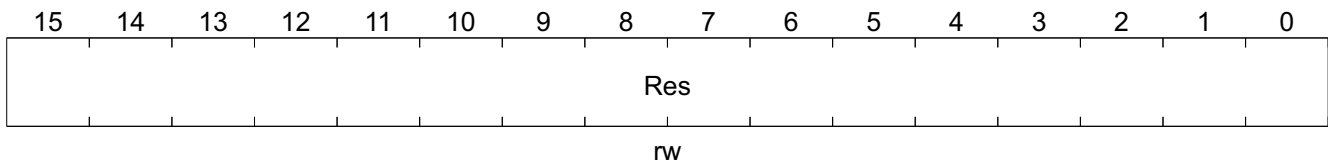
Table 20 PCR_x Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|-----------------------|-------------------|-------------|
| PCR_1 | Port 1 Configuration | 0203 _H | |
| PCR_2 | Port 2 Configuration | 0204 _H | |
| PCR_3 | Port 3 Configuration | 0205 _H | |
| PCR_4 | Port 4 Configuration | 0206 _H | |
| PCR_5 | Port 5 Configuration | 0207 _H | |
| PCR_6 | Port 6 Configuration | 0208 _H | |
| PCR_7 | Port 7 Configuration | 0209 _H | |
| PCR_8 | Port 8 Configuration | 020A _H | |
| PCR_9 | Port 9 Configuration | 020B _H | |
| PCR_10 | Port 10 Configuration | 020C _H | |
| PCR_11 | Port 11 Configuration | 020D _H | |
| PCR_12 | Port 12 Configuration | 020E _H | |
| PCR_13 | Port 13 Configuration | 020F _H | |
| PCR_14 | Port 14 Configuration | 0210 _H | |
| PCR_15 | Port 15 Configuration | 0211 _H | |
| PCR_16 | Port 16 Configuration | 021A _H | |
| PCR_17 | Port 17 Configuration | 021B _H | |

Reserved Register 1

| | | |
|---------------------|-------------------|--------------------------|
| RES1 | Offset | Reset Value |
| Reserved Register 1 | 0212 _H | Table 15 |

EEPROM Register Format



| Field | Bits | Type | Description |
|-------|------|------|--|
| Res | 15:0 | rw | Reserved For the future use and don't modify the values. Default: See Chapter 4 |

All RESx registers have the same structure and characteristics, see [RES1](#). The offset addresses of the other RESx registers are listed in [Table 21](#).

Table 21 Resx Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|----------------------|-------------------|-------------|
| RES2 | Reserved Register 2 | 0213 _H | |
| RES3 | Reserved Register 3 | 0214 _H | |
| RES4 | Reserved Register 4 | 0215 _H | |
| RES5 | Reserved Register 5 | 0216 _H | |
| RES6 | Reserved Register 6 | 0217 _H | |
| RES7 | Reserved Register 7 | 0218 _H | |
| RES8 | Reserved Register 8 | 0219 _H | |
| RES9 | Reserved Register 9 | 026E _H | |
| RES10 | Reserved Register 10 | 026F _H | |
| RES11 | Reserved Register 11 | 0270 _H | |
| RES12 | Reserved Register 12 | 0271 _H | |
| RES13 | Reserved Register 13 | 0272 _H | |
| RES14 | Reserved Register 14 | 0273 _H | |
| RES15 | Reserved Register 15 | 0274 _H | |
| RES16 | Reserved Register 16 | 0275 _H | |
| RES17 | Reserved Register 17 | 027C _H | |
| RES18 | Reserved Register 18 | 027D _H | |
| RES19 | Reserved Register 19 | 0281 _H | |
| RES20 | Reserved Register 20 | 0282 _H | |
| RES21 | Reserved Register 21 | 0283 _H | |
| RES22 | Reserved Register 22 | 0284 _H | |
| RES23 | Reserved Register 23 | 0285 _H | |
| RES24 | Reserved Register 24 | 0286 _H | |
| RES25 | Reserved Register 25 | 0287 _H | |
| RES26 | Reserved Register 26 | 0288 _H | |
| RES27 | Reserved Register 27 | 0289 _H | |
| RES28 | Reserved Register 28 | 028A _H | |

EEPROM Register Format
Miscellaneous Configuration

MC **Offset** **Reset Value**
Miscellaneous Configuration **021C_H** **0820_H**

| | | | | | | | | | | | | | | | |
|-----|----|-----|----|----|----|-----------|-----|---|---|---|------|-----|-----|-----|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | Res | | | | CLED E | Res | | | | ERID | Res | RCD | DBF | |
| rw | | rw | | | | rw | rw | | | | rw | rw | rw | rw | |

| Field | Bits | Type | Description |
|-------|-------|------|---|
| Res | 13:10 | rw | Reserved |
| CLEDE | 9 | rw | Collision LED Enable 0 _B , The switch will not provide two collision LEDs for 10M and 100M domain individually 1 _B , The switch will provide two collision LEDs for 10M and 100M domain individually and flash in rate of 2 Hz. |
| Res | 8:4 | rw | Reserved |
| ERID | 3 | rw | Enable Replace VLAN ID 0 _B , The switch will use the original VID received from the Tag Header. 1 _B , The switch will replace the VID with the PVID associated with the receiving port when the received packets are priority tagged or its VID in the Tag Header equals to 1. |
| Res | 2 | rw | Reserved |
| RCD | 1 | rw | Recommend 16th Collision Drop 0 _B , The Mac controller will retransmit packets even when the collision count is larger than 16. 1 _B , The Mac controller will drop packets when the collision count is larger than 16. |
| DBF | 0 | rw | Disable CSMA/CD Back-off Function 0 _B , The Mac controller supports random back off function. 1 _B , The MAC controller will disable random back off function. |

VLAN(TOS) Priority Map

VLAN **Offset** **Reset Value**
VLAN(TOS) Priority Map **021D_H** **0000_H**

| | | | | | | | | | | | | | | | |
|------|------|------|------|------|------|------|------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MPQ7 | MPQ6 | MPQ5 | MPQ4 | MPQ3 | MPQ2 | MPQ1 | MPQ0 | MPQT 7 | MPQT 6 | MPQT 5 | MPQT 4 | MPQT 3 | MPQT 2 | MPQT 1 | MPQT 0 |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|-------|------|------|--|
| MPQ7 | 15 | rw | Mapped Priority Queue of TOS 7 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQ6 | 14 | rw | Mapped Priority Queue of TOS 6 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQ5 | 13 | rw | Mapped Priority Queue of TOS 5 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQ4 | 12 | rw | Mapped Priority Queue of TOS 4 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQ3 | 11 | rw | Mapped Priority Queue of TOS 3 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQ2 | 10 | rw | Mapped Priority Queue of TOS 2 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQ1 | 9 | rw | Mapped Priority Queue of TOS 1 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQ0 | 8 | rw | Mapped Priority Queue of TOS 0 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQT7 | 7 | rw | Mapped Priority Queue of Tag Value 7 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQT6 | 6 | rw | Mapped Priority Queue of Tag Value 6 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQT5 | 5 | rw | Mapped Priority Queue of Tag Value 5 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQT4 | 4 | rw | Mapped Priority Queue of Tag Value 4 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQT3 | 3 | rw | Mapped Priority Queue of Tag Value 3 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQT2 | 2 | rw | Mapped priority Queue of Tag Value 2 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |
| MPQT1 | 1 | rw | Mapped Priority Queue of Tag Value 1 0 _B , Mapped for Low Queue 1 _B , Mapped for High Queue |

EEPROM Register Format

| Field | Bits | Type | Description |
|-------|------|------|--|
| FG_6 | 6 | rw | Forwarding Group Port 6 0 _B , Port 6 is not in the Forwarding Group 1 _B , Port 6 is in the Forwarding Group |
| FG_5 | 5 | rw | Forwarding Group Port 5 0 _B , Port 5 is not in the Forwarding Group 1 _B , Port 5 is in the Forwarding Group |
| FG_4 | 4 | rw | Forwarding Group Port 4 0 _B , Port 4 is not in the Forwarding Group 1 _B , Port 4 is in the Forwarding Group |
| FG_3 | 3 | rw | Forwarding Group Port 3 0 _B , Port 3 is not in the Forwarding Group 1 _B , Port 3 is in the Forwarding Group |
| FG_2 | 2 | rw | Forwarding Group Port 2 0 _B , Port 2 is not in the Forwarding Group 1 _B , Port 2 is in the Forwarding Group |
| FG_1 | 1 | rw | Forwarding Group Port 1 0 _B , Port 1 is not in the Forwarding Group 1 _B , Port 1 is in the Forwarding Group |
| FG_0 | 0 | rw | Forwarding Group Port 0 0 _B , Port 0 is not in the Forwarding Group 1 _B , Port 0 is in the Forwarding Group |

All FGOPML_x registers have the same structure and characteristics, see [FGOPML_0](#). The offset addresses of the other FGOPML_x registers are listed in [Table 22](#).

Table 22 FGOPML_x Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---|-------------------|-------------|
| FGOPML_1 | Forwarding Group 1 Outbound Port Map Low | 0220 _H | |
| FGOPML_2 | Forwarding Group 2 Outbound Port Map Low | 0222 _H | |
| FGOPML_3 | Forwarding Group 3 Outbound Port Map Low | 0224 _H | |
| FGOPML_4 | Forwarding Group 4 Outbound Port Map Low | 0226 _H | |
| FGOPML_5 | Forwarding Group 5 Outbound Port Map Low | 0228 _H | |
| FGOPML_6 | Forwarding Group 6 Outbound Port Map Low | 022A _H | |
| FGOPML_7 | Forwarding Group 7 Outbound Port Map Low | 022C _H | |
| FGOPML_8 | Forwarding Group 8 Outbound Port Map Low | 022E _H | |
| FGOPML_9 | Forwarding Group 9 Outbound Port Map Low | 0230 _H | |
| FGOPML_10 | Forwarding Group 10 Outbound Port Map Low | 0232 _H | |
| FGOPML_11 | Forwarding Group 11 Outbound Port Map Low | 0234 _H | |
| FGOPML_12 | Forwarding Group 12 Outbound Port Map Low | 0236 _H | |
| FGOPML_13 | Forwarding Group 13 Outbound Port Map Low | 0238 _H | |
| FGOPML_14 | Forwarding Group 14 Outbound Port Map Low | 023A _H | |
| FGOPML_15 | Forwarding Group 15 Outbound Port Map Low | 023C _H | |
| FGOPML_16 | Forwarding Group 16 Outbound Port Map Low | 023E _H | |
| FGOPML_17 | Forwarding Group 17 Outbound Port Map Low | 0240 _H | |

| Field | Bits | Type | Description |
|-------|------|------|---|
| FG_20 | 4 | rw | Forwarding Group Port 20 0 _B , Port 20 is not in the Forwarding Group 1 _B , Port 20 is in the Forwarding Group |
| FG_19 | 3 | rw | Forwarding Group Port 19 0 _B , Port 19 is not in the Forwarding Group 1 _B , Port 19 is in the Forwarding Group |
| FG_18 | 2 | rw | Forwarding Group Port 18 0 _B , Port 18 is not in the Forwarding Group 1 _B , Port 18 is in the Forwarding Group |
| FG_17 | 1 | rw | Forwarding Group Port 17 0 _B , Port 17 is not in the Forwarding Group 1 _B , Port 17 is in the Forwarding Group |
| FG_16 | 0 | rw | Forwarding Group Port 16 0 _B , Port 16 is not in the Forwarding Group 1 _B , Port 16 is in the Forwarding Group |

All FGOPMH_x registers have the same structure and characteristics, see [FGOPMH_0](#). The offset addresses of the other FGOPMH_x registers are listed in [Table 23](#).

Table 23 FGOPMH_x Registers

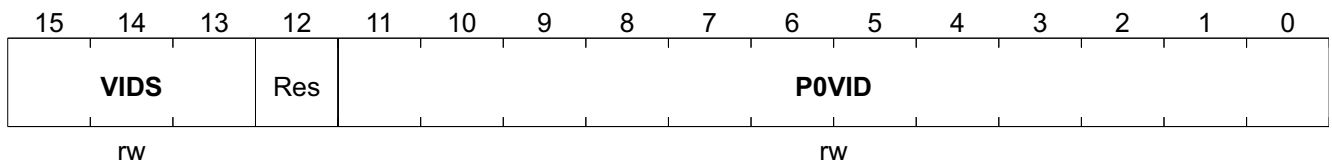
| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--|-------------------|-------------|
| FGOPMH_1 | Forwarding Group 1 Outbound Port Map High | 0221 _H | |
| FGOPMH_2 | Forwarding Group 2 Outbound Port Map High | 0223 _H | |
| FGOPMH_3 | Forwarding Group 3 Outbound Port Map High | 0225 _H | |
| FGOPMH_4 | Forwarding Group 4 Outbound Port Map High | 0227 _H | |
| FGOPMH_5 | Forwarding Group 5 Outbound Port Map High | 0229 _H | |
| FGOPMH_6 | Forwarding Group 6 Outbound Port Map High | 022B _H | |
| FGOPMH_7 | Forwarding Group 7 Outbound Port Map High | 022D _H | |
| FGOPMH_8 | Forwarding Group 8 Outbound Port Map High | 022F _H | |
| FGOPMH_9 | Forwarding Group 9 Outbound Port Map High | 0231 _H | |
| FGOPMH_10 | Forwarding Group 10 Outbound Port Map High | 0233 _H | |
| FGOPMH_11 | Forwarding Group 11 Outbound Port Map High | 0235 _H | |
| FGOPMH_12 | Forwarding Group 12 Outbound Port Map High | 0237 _H | |
| FGOPMH_13 | Forwarding Group 13 Outbound Port Map High | 0239 _H | |
| FGOPMH_14 | Forwarding Group 14 Outbound Port Map High | 023B _H | |
| FGOPMH_15 | Forwarding Group 15 Outbound Port Map High | 023D _H | |
| FGOPMH_16 | Forwarding Group 16 Outbound Port Map High | 023F _H | |
| FGOPMH_17 | Forwarding Group 17 Outbound Port Map High | 0241 _H | |
| FGOPMH_18 | Forwarding Group 18 Outbound Port Map High | 0243 _H | |
| FGOPMH_19 | Forwarding Group 19 Outbound Port Map High | 0245 _H | |
| FGOPMH_20 | Forwarding Group 20 Outbound Port Map High | 0247 _H | |
| FGOPMH_21 | Forwarding Group 21 Outbound Port Map High | 0249 _H | |
| FGOPMH_22 | Forwarding Group 22 Outbound Port Map High | 024B _H | |

Table 23 FGOPMH_x Registers (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--|-------------------|-------------|
| FGOPMH_23 | Forwarding Group 23 Outbound Port Map High | 024D _H | |
| FGOPMH_24 | Forwarding Group 24 Outbound Port Map High | 024F _H | |
| FGOPMH_25 | Forwarding Group 25 Outbound Port Map High | 0251 _H | |
| FGOPMH_26 | Forwarding Group 26 Outbound Port Map High | 0253 _H | |
| FGOPMH_27 | Forwarding Group 27 Outbound Port Map High | 0255 _H | |
| FGOPMH_28 | Forwarding Group 28 Outbound Port Map High | 0257 _H | |
| FGOPMH_29 | Forwarding Group 29 Outbound Port Map High | 0259 _H | |
| FGOPMH_30 | Forwarding Group 30 Outbound Port Map High | 025B _H | |
| FGOPMH_31 | Forwarding Group 31 Outbound Port Map High | 025D _H | |

P0 VID and PVID Shift

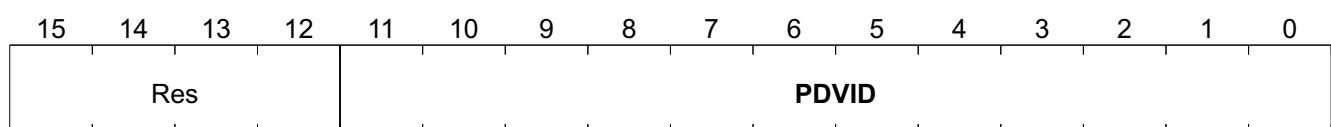
| | | |
|------------------------------|-------------------------|-------------------------|
| P0VIDS | Offset | Reset Value |
| P0 VID and PVID Shift | 025E_H | 0001_H |



| Field | Bits | Type | Description |
|-------|-------|------|--|
| VIDS | 15:13 | rw | <p>VID Shift</p> <p>This function maps 4096 VLAN into 32 Forwarding Groups</p> <p>1. In Tagged Based VLAN, the ADM6918/X will use 5 bits from VID as the Index to map into forwarding groups. 32 forwarding groups are defined in the ADM6918/X. We use F0, F1, ... F31 to call each forwarding group. This looking scheme is different from the Port Based VLAN because Port Based VLAN uses port number as the Index to map into the forwarding groups and then F26 ~ F31 will not be used. The VID is defined as follows:</p> <ul style="list-style-type: none"> The port's Default VID is used if the frame is not 802.3ac Tagged (No Tag Header in the frame). The port's Default VID is used if the frame is 802.3ac Tagged (Tag Header in the frame) and the frame's VID is 0000_H or 0001_H and the Enable Replace VLAN ID function is enabled. The VID in the Tag Header is used if the frame is 802.3 Tagged and the frame's VID is not 0000_H or 0001_H. The VID in the Tag Header is used if the frame is 802.3 Tagged and the frame's VID is 0000_H or 0001_H and Enable Replace VLAN ID function is not enabled. <p>2. The relation between VID Shift, VID and the forwarding group is as follows:</p> <p>Bit[15:13] Forwarding Group</p> <p>000_B , VID[4:0] 001_B , VID[5:1] 010_B , VID[6:2] 011_B , VID[7:3] 100_B , VID[8:4] 101_B , VID[9:5] 110_B , VID[10:6] 111_B , VID[11:7]</p> |
| POVID | 11:0 | rw | <p>Port 0 VID</p> <p>The port's Default VID is used if the frame is untagged or if the frame's VID is 0000_H or 0001_H and Enable Replace VLAN ID function (also see Miscellaneous Configuration Register) is enabled.</p> |

P1 VID Configuration

| | | |
|-----------------------------|-------------------------|-------------------------|
| P1_VID | Offset | Reset Value |
| P1 VID Configuration | 025F_H | 0001_H |



rw

EEPROM Register Format

| Field | Bits | Type | Description |
|-------|------|------|------------------------|
| PDVID | 11:0 | rw | The Port's Default VID |

All P_x_VID registers have the same structure and characteristics, see [P1_VID](#). The offset addresses of the other P_x_VID registers are listed in [Table 24](#).

Table 24 P_x_VID Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|-----------------------|-------------------|-------------|
| P2_VID | P2 VID Configuration | 0260 _H | |
| P3_VID | P3 VID Configuration | 0261 _H | |
| P4_VID | P4 VID Configuration | 0262 _H | |
| P5_VID | P5 VID Configuration | 0263 _H | |
| P6_VID | P6 VID Configuration | 0264 _H | |
| P7_VID | P7 VID Configuration | 0265 _H | |
| P8_VID | P8 VID Configuration | 0266 _H | |
| P9_VID | P9 VID Configuration | 0267 _H | |
| P10_VID | P10 VID Configuration | 0268 _H | |
| P11_VID | P11 VID Configuration | 0269 _H | |
| P12_VID | P12 VID Configuration | 026A _H | |
| P13_VID | P13 VID Configuration | 026B _H | |
| P14_VID | P14 VID Configuration | 026C _H | |
| P15_VID | P15 VID Configuration | 026D _H | |
| P24_VID | P24 VID Configuration | 0276 _H | |
| P25_VID | P25 VID Configuration | 0277 _H | |

P0, P1, P2, P3 Bandwidth Control Register

| | | |
|--|-------------------------|-------------------------|
| P0_3_BCR | Offset | Reset Value |
| P0, P1, P2, P3 Bandwidth Control Register | 0278_H | 0000_H |

| | | | | | | | | | | | | | | | |
|---------------|--------------|----|----|---------------|--------------|---|---|---------------|--------------|---|---|---------------|--------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| P3RPLC | P3MTC | | | P2RPLC | P2MTC | | | P1RPLC | P1MTC | | | P0RPLC | P0MTC | | |
| rw | rw | | | rw | rw | | | rw | rw | | | rw | rw | | |

| Field | Bits | Type | Description |
|--------|------|------|--|
| P3RPLC | 15 | rw | Port 3 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P3 counter, default |

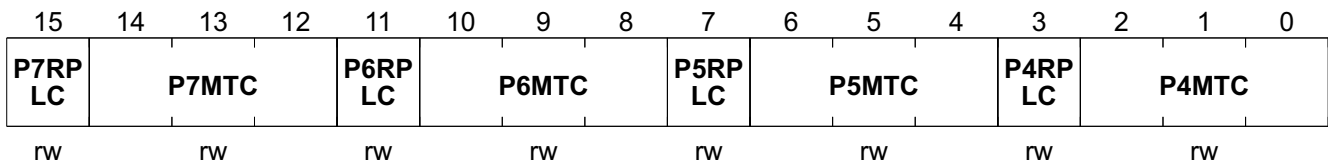
EEPROM Register Format

| Field | Bits | Type | Description |
|--------|-------|------|---|
| P3MTC | 14:12 | rw | Port 3 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |
| P2RPLC | 11 | rw | Port 2 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P2 counter, default |
| P2MTC | 10:8 | rw | Port 2 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |
| P1RPLC | 7 | rw | Port 1 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P1 counter, default |
| P1MTC | 6:4 | rw | Port 1 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |
| P0RPLC | 3 | rw | Port 0 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P0 counter, default |
| P0MTC | 2:0 | rw | Port 0 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |

P4, P5, P6, P7 Bandwidth Control Register

| | | |
|--|-------------------------|-------------------------|
| P4_7_BCR | Offset | Reset Value |
| P4, P5, P6, P7 Bandwidth Control Register | 0279_H | 0000_H |

EEPROM Register Format



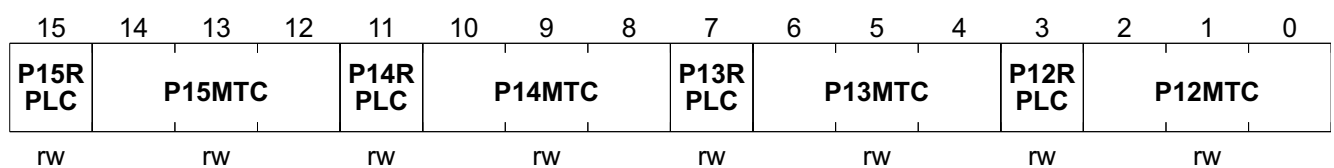
| Field | Bits | Type | Description |
|--------|-------|------|---|
| P7RPLC | 15 | rw | Port 7 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P7 counter, default |
| P7MTC | 14:12 | rw | Port 7 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |
| P6RPLC | 11 | rw | Port 6 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P6 counter, default |
| P6MTC | 10:8 | rw | Port 6 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |
| P5RPLC | 7 | rw | Port 5 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P5 counter, default |
| P5MTC | 6:4 | rw | Port 5 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |
| P4RPLC | 3 | rw | Port 4 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P4 counter, default |

EEPROM Register Format

| Field | Bits | Type | Description |
|--------|------|------|---|
| P9MTC | 6:4 | rw | Port 9 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |
| P8RPLC | 3 | rw | Port 8 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P8 counter, default |
| P8MTC | 2:0 | rw | Port 8 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |

P12, P13, P14, P15 Bandwidth Control Register

| | | |
|--|-------------------------|-------------------------|
| P12_15_BCR | Offset | Reset Value |
| P12, P13, P14, P15 Bandwidth Control Register | 027B_H | 0000_H |



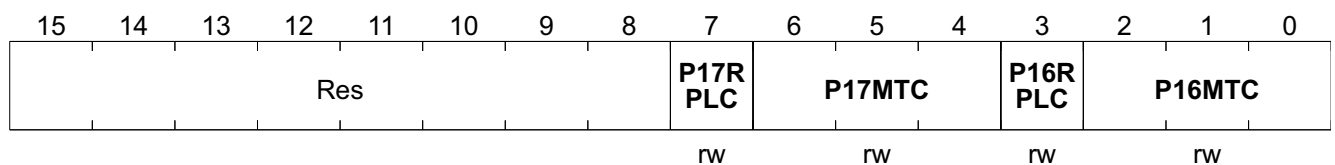
| Field | Bits | Type | Description |
|---------|-------|------|--|
| P15RPLC | 15 | rw | Port 15 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P15 counter, default |
| P15MTC | 14:12 | rw | Port 15 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |

EEPROM Register Format

| Field | Bits | Type | Description |
|---------|------|------|--|
| P14RPLC | 11 | rw | Port 14 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P14 counter, default |
| P14MTC | 10:8 | rw | Port 14 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |
| P13RPLC | 7 | rw | Port 13 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P13 counter, default |
| P13MTC | 6:4 | rw | Port 13 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |
| P12RPLC | 3 | rw | Port 12 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P12 counter, default |
| P12MTC | 2:0 | rw | Port 12 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |

P24, P25 Bandwidth Control Register

| P24_25_BCR | Offset | Reset Value |
|-------------------------------------|-------------------|-------------------|
| P24, P25 Bandwidth Control Register | 027E _H | 0000 _H |



| Field | Bits | Type | Description |
|---------|------|------|--|
| P17RPLC | 7 | rw | Port 25 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P25 counter, default |
| P17MTC | 6:4 | rw | Port 25 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |
| P16RPLC | 3 | rw | Port 24 Receive Packet Length Counted on the Source Port 0 _B , The switch will add length to the P24 counter, default |
| P16MTC | 2:0 | rw | Port 24 Meter Threshold Control 000 _B , 64k, default 001 _B , 128k 010 _B , 256k 011 _B , 512k 100 _B , 1M 101 _B , 4M 110 _B , 10M 111 _B , 20M |

Bandwidth Control Enable Register Low

BCERL **Offset** **Reset Value**
Bandwidth Control Enable Register Low **027F_H** **0000_H**

| | | | | | | | | | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BCEP | BCEP | BCEP | BCEP | BCEP | BCEP | BCEP | BCEP | BCEP | BCEP | BCEP | BCEP | BCEP | BCEP | BCEP | BCEP |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

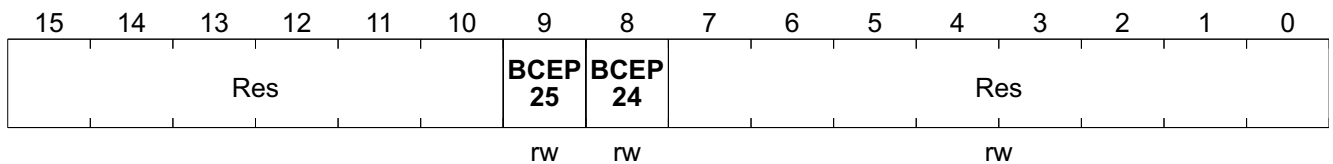
| Field | Bits | Type | Description |
|--------|------|------|---|
| BCEP15 | 15 | rw | Bandwidth Control Enable for Port 15 |
| BCEP14 | 14 | rw | Bandwidth Control Enable for Port 14 |
| BCEP13 | 13 | rw | Bandwidth Control Enable for Port 13 |
| BCEP12 | 12 | rw | Bandwidth Control Enable for Port 12 |
| BCEP11 | 11 | rw | Bandwidth Control Enable for Port 11 |
| BCEP10 | 10 | rw | Bandwidth Control Enable for Port 10 |
| BCEP9 | 9 | rw | Bandwidth Control Enable for Port 9 |
| BCEP8 | 8 | rw | Bandwidth Control Enable for Port 8 |

EEPROM Register Format

| Field | Bits | Type | Description |
|-------|------|------|--|
| BCEP7 | 7 | rw | Bandwidth Control Enable for Port 7 |
| BCEP6 | 6 | rw | Bandwidth Control Enable for Port 6 |
| BCEP5 | 5 | rw | Bandwidth Control Enable for Port 5 |
| BCEP4 | 4 | rw | Bandwidth Control Enable for Port 4 |
| BCEP3 | 3 | rw | Bandwidth Control Enable for Port 3 |
| BCEP2 | 2 | rw | Bandwidth Control Enable for Port 2 |
| BCEP1 | 1 | rw | Bandwidth Control Enable for Port 1 |
| BCEP0 | 0 | rw | Bandwidth Control Enable for Port 0 0_B , Port 0 disables the bandwidth control. 1_B , Port 0 enables the bandwidth control. |

Bandwidth Control Enable Register High

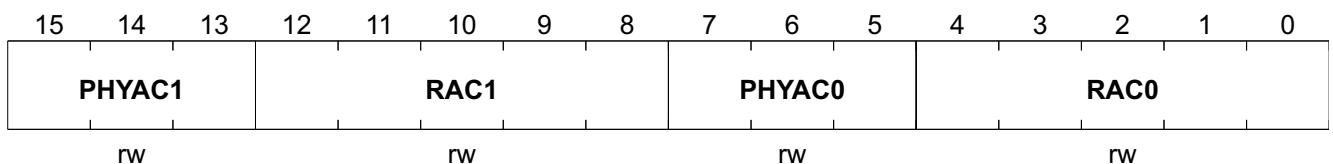
BCERH Offset
 Bandwidth Control Enable Register High 0280_H Reset Value
 0000_H



| Field | Bits | Type | Description |
|--------|------|------|--------------------------------------|
| BCEP25 | 9 | rw | Bandwidth Control Enable for Port 25 |
| BCEP24 | 8 | rw | Bandwidth Control Enable for Port 24 |
| Res | 7:0 | rw | Reserved |

Customized PHY Control Group 0

CPHYCG0 Offset
 Customized PHY Control Group 0 $028B_H$ Reset Value
 0000_H

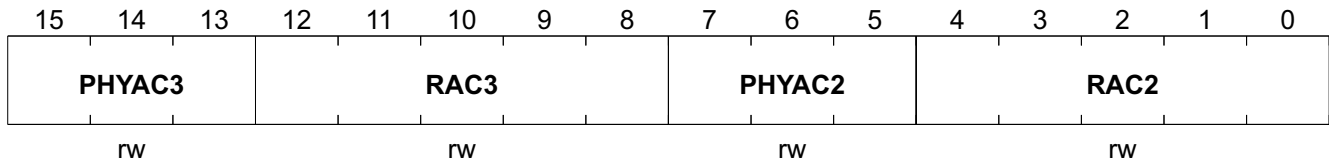


| Field | Bits | Type | Description |
|--------|-------|------|---|
| PHYAC1 | 15:13 | rw | PHY Address of the Command 1 If Bit[2:0] in PHY Customized Enable Register = 010 _B or 011 _B . 000 _B , The switch will write command 1 into Port 0 (PHY Address = 32'h8). 001 _B , The switch will write command 1 into Port 1 (PHY Address = 32'h9). 010 _B , The switch will write command 1 into Port 2 (PHY Address = 32'ha). 011 _B , The switch will write command 1 into Port 3 (PHY Address = 32'hb). 100 _B , The switch will write command 1 into Port 4 (PHY Address = 32'hc). 101 _B , The switch will write command 1 into Port 5 (PHY Address = 32'hd). 110 _B , The switch will write command 1 into Port 6 (PHY Address = 32'he). 111 _B , The switch will write command 1 into Port 7 (PHY Address = 32'hf). |
| RAC1 | 12:8 | rw | Register Address of the Command 1 |
| PHYAC0 | 7:5 | rw | PHY Address of the Command 0 If Bit[2:0] in PHY Customized Enable Register = 001 _B or 011 _B . 000 _B , The switch will write command 0 into Port 0 (PHY Address = 32'h8). 001 _B , The switch will write command 0 into Port 1 (PHY Address = 32'h9). 010 _B , The switch will write command 0 into Port 2 (PHY Address = 32'ha). 011 _B , The switch will write command 0 into Port 3 (PHY Address = 32'hb). 100 _B , The switch will write command 0 into Port 4 (PHY Address = 32'hc). 101 _B , The switch will write command 0 into Port 5 (PHY Address = 32'hd). 110 _B , The switch will write command 0 into Port 6 (PHY Address = 32'he). 111 _B , The switch will write command 0 into Port 7 (PHY Address = 32'hf). |
| RAC0 | 4:0 | rw | Register Address of the Command 0 |

Note: The ADM6918/X supports eight additional commands for the customer to configure the PHY attached. Four groups are defined and each group shares two commands. Group 0 contains P0, P1, P2, P3, P4, P5, P6 and P7. Group 1 contains P8, P9, P10, P11, P12, P13, P14 and P15. Group 2 contains P16, P17, P18, P19, P20, P21, P22 and P23. Group 3 contains P24 and P25. 3 bits enable register is associated with each group. Each command is associated with a PHY address, a register address, and data for writing.

Customized PHY Control Group 1

| | | |
|--------------------------------|-------------------|--------------------|
| CPHYCG1 | Offset | Reset Value |
| Customized PHY Control Group 1 | 028C _H | 0000 _H |



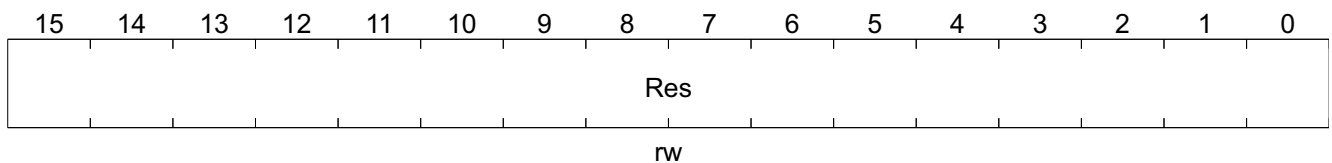
| Field | Bits | Type | Description |
|--------|-------|------|--|
| PHYAC3 | 15:13 | rw | PHY Address of the Command 3 Bit[5:3] in PHY Customized Enable Register = 010 _B or 011 _B . 000 _B , The switch will write command 3 into Port 8 (PHY Address = 32'h10). 001 _B , The switch will write command 3 into Port 9 (PHY Address = 32'h11). 010 _B , The switch will write command 3 into Port 10 (PHY Address = 32'h12). 011 _B , The switch will write command 3 into Port 11 (PHY Address = 32'h13). 100 _B , The switch will write command 3 into Port 12 (PHY Address = 32'h14). 101 _B , The switch will write command 3 into Port 13 (PHY Address = 32'h15). 110 _B , The switch will write command 3 into Port 14 (PHY Address = 32'h16). 111 _B , The switch will write command 3 into Port 15 (PHY Address = 32'h17). |
| RAC3 | 12:8 | rw | Register Address of the Command 3 |

EEPROM Register Format

| Field | Bits | Type | Description |
|--------|------|------|--|
| PHYAC2 | 7:5 | rw | PHY Address of the Command 2 Bit[5:3] in PHY Customized Enable Register = 001 _B or 011 _B . 000 _B , The switch will write command 2 into Port 8 (PHY Address = 32'h10). 001 _B , The switch will write command 2 into Port 9 (PHY Address = 32'h11). 010 _B , The switch will write command 2 into Port 10 (PHY Address = 32'h12). 011 _B , The switch will write command 2 into Port 11 (PHY Address = 32'h13). 100 _B , The switch will write command 2 into Port 12 (PHY Address = 32'h14). 101 _B , The switch will write command 2 into Port 13 (PHY Address = 32'h15). 110 _B , The switch will write command 2 into Port 14 (PHY Address = 32'h16). 111 _B , The switch will write command 2 into Port 15 (PHY Address = 32'h17). |
| RAC2 | 4:0 | rw | Register Address of the Command 2 |

Customized PHY Control Group 2

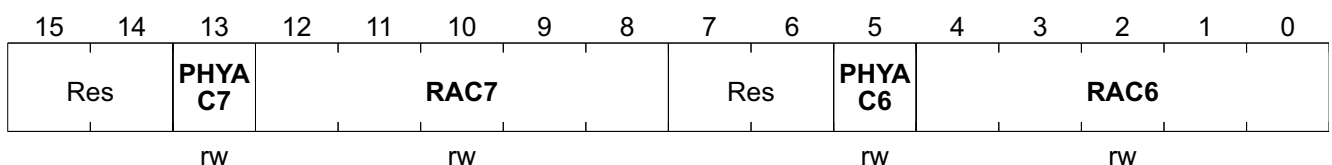
CPHYCG2 Offset
 Customized PHY Control Group 2 028D_H Reset Value
0000_H



| Field | Bits | Type | Description |
|-------|------|------|--|
| Res | 15:0 | rw | Reserved Default 0000 _H |

Customized PHY Control Group 3

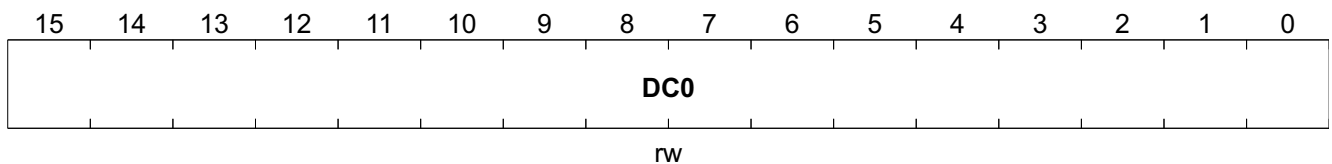
CPHYCG3 Offset
 Customized PHY Control Group 3 028E_H Reset Value
0000_H



| Field | Bits | Type | Description |
|--------|------|------|---|
| PHYAC7 | 13 | rw | PHY Address of the Command 7 Bit[11:9] in PHY Customized Enable Register = 010 _B or 011 _B . 0 _B , The switch will write command 7 into Port 24 (PHY Address = 32'h6). 1 _B , The switch will write command 7 into Port 25 (PHY Address = 32'h7). |
| RAC7 | 12:8 | rw | Register Address of the Command 7 |
| PHYAC6 | 5 | rw | PHY Address of the Command 6 Bit[11:9] in PHY Customized Enable Register = 001 _B or 011 _B . 0 _B , The switch will write command 6 into Port 24 (PHY Address = 32'h6). 1 _B , The switch will write command 6 into Port 25 (PHY Address = 32'h7). |
| RAC6 | 4:0 | rw | Register Address of the Command 6 |

Group 0 PHY Customized DATA 0

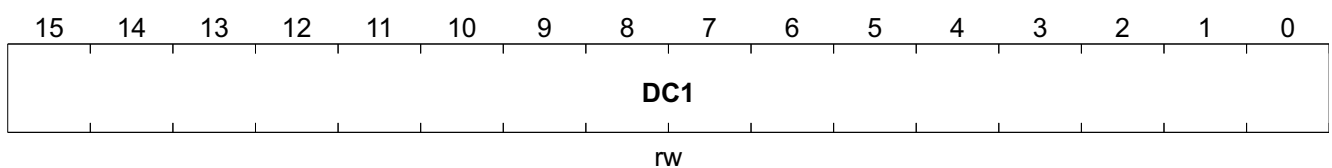
| | | |
|-------------------------------|-------------------|--------------------|
| G0PHYCD0 | Offset | Reset Value |
| Group 0 PHY Customized DATA 0 | 028F _H | 0000 _H |



| Field | Bits | Type | Description |
|-------|------|------|---------------------------|
| DC0 | 15:0 | rw | Data for Command 0 |

Group 0 PHY Customized DATA 1

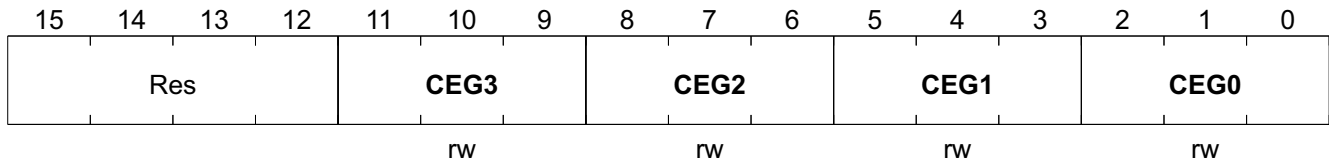
| | | |
|-------------------------------|-------------------|--------------------|
| G0PHYCD1 | Offset | Reset Value |
| Group 0 PHY Customized DATA 1 | 0290 _H | 0000 _H |



| Field | Bits | Type | Description |
|-------|------|------|---------------------------|
| DC1 | 15:0 | rw | Data for Command 1 |

PHY Customized Enable Register

| | | |
|--------------------------------|-------------------|--------------------|
| PHYCE | Offset | Reset Value |
| PHY Customized Enable Register | 0297 _H | 0000 _H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| CEG3 | 11:9 | rw | PHY Customized Enable For Group 3 000 _B , Disable writing additional commands into any PHYs in Group 3. 001 _B , Write command 6 into related port specified by the Customized PHY Control Group 3. 010 _B , Write command 7 into related port specified by the Customized PHY Control Group 3. 100 _B , Disable writing additional commands into any PHYs in Group 3. 101 _B , Write command 6 into all PHYs in Group 3. 110 _B , Write command 7 into all PHYs in Group 3. 111 _B , Write command 6 and command 7 into all PHYs in Group 3. |
| CEG2 | 8:6 | rw | PHY Customized Enable For Group 2 000 _B , Disable writing additional commands into any PHYs in Group 2. 001 _B , Write command 4 into related port specified by the Customized PHY Control Group 2. 010 _B , Write command 5 into related port specified by the Customized PHY Control Group 2. 100 _B , Disable writing additional commands into any PHYs in Group 2. 101 _B , Write command 4 into all PHYs in Group 2. 110 _B , Write command 5 into all PHYs in Group 2. 111 _B , Write command 5 and command 5 into all PHYs in Group 2. |
| CEG1 | 5:3 | rw | PHY Customized Enable For Group 1 000 _B , Disable writing additional commands into any PHYs in Group 1. 001 _B , Write command 2 into related port specified by the Customized PHY Control Group 1. 010 _B , Write command 3 into related port specified by the Customized PHY Control Group 1. 100 _B , Disable writing additional commands into any PHYs in Group 1. 101 _B , Write command 2 into all PHYs in Group 1. 110 _B , Write command 3 into all PHYs in Group 1. 111 _B , Write command 2 and command 3 into all PHYs in Group 1. |

EEPROM Register Format

| Field | Bits | Type | Description |
|-------|------|------|--|
| CEG0 | 2:0 | rw | PHY Customized Enable For Group 0 000 _B , Disable writing additional commands into any PHYs in Group 0. 001 _B , Write command 0 into related port specified by the Customized PHY Control Group 0. 010 _B , Write command 1 into related port specified by the Customized PHY Control Group 0. 100 _B , Disable writing additional commands into any PHYs in Group 0. 101 _B , Write command 0 into all PHYs in Group 0. 110 _B , Write command 1 into all PHYs in Group 0. 111 _B , Write command 0 and command 1 into all PHYs in Group 0. |

PPPOE Control Register 0

| | | |
|--------------------------|-------------------|-------------------|
| PPPOEC0 | Offset | Reset Value |
| PPPOE Control Register 0 | 0298 _H | 0000 _H |

| | | | | | | | | | | | | | | | |
|------------|------------|------------|------------|------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EP15 TP | EP14 TP | EP13 TP | EP12 TP | EP11 TP | EP10 TP | EP9T P | EP8T P | EP7T P | EP6T P | EP5T P | EP4T P | EP3T P | EP2T P | EP1T P | EP0T P |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|--------|------|------|--|
| EP15TP | 15 | rw | Enable Port 15 to Transmit PPPoE Packet Only |
| EP14TP | 14 | rw | Enable Port 14 to Transmit PPPoE Packet Only |
| EP13TP | 13 | rw | Enable Port 13 to Transmit PPPoE Packet Only |
| EP12TP | 12 | rw | Enable Port 12 to Transmit PPPoE Packet Only |
| EP11TP | 11 | rw | Enable Port 11 to Transmit PPPoE Packet Only |
| EP10TP | 10 | rw | Enable Port 10 to Transmit PPPoE Packet Only |
| EP9TP | 9 | rw | Enable Port 9 to Transmit PPPoE Packet Only |
| EP8TP | 8 | rw | Enable Port 8 to Transmit PPPoE Packet Only |
| EP7TP | 7 | rw | Enable Port 7 to Transmit PPPoE Packet Only |
| EP6TP | 6 | rw | Enable Port 6 to Transmit PPPoE Packet Only |
| EP5TP | 5 | rw | Enable Port 5 to Transmit PPPoE Packet Only |
| EP4TP | 4 | rw | Enable Port 4 to Transmit PPPoE Packet Only |
| EP3TP | 3 | rw | Enable Port 3 to Transmit PPPoE Packet Only |
| EP2TP | 2 | rw | Enable Port 2 to Transmit PPPoE Packet Only |
| EP1TP | 1 | rw | Enable Port 1 to Transmit PPPoE Packet Only |
| EP0TP | 0 | rw | Enable Port 0 to Transmit PPPoE Packet Only The ADM6918/X will recognize packets with length-type = 8863 _H or 8864 _H as the PPPOE packets. 0 _B , The port 0 is not configured to transmit PPPOE packets only. 1 _B , The port 0 is configured to transmit PPPOE packets only. |

PPPOE Control Register 1

PPPOEC1 **Offset**
PPPOE Control Register 1 **0299_H** **Reset Value**
0000_H

| | | | | | | | | | | | | | | | |
|-----|----|----|----|------|---------|---------|-----|---|---|---|----|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | EMPC | EP25 TP | EP24 TP | Res | | | | | | | | |
| | | | | rw | rw | rw | | | | | rw | | | | |

| Field | Bits | Type | Description |
|--------|------|------|--|
| EMPC | 10 | rw | Enable Management Packet Cross PPPOE PORT Function 0 _B , Management packets could not be transmitted by the PPPOE port. 1 _B , Management packets could be transmitted by any port even if it is configured to PPPOE port. |
| EP25TP | 9 | rw | Enable Port 25 to Transmit PPPoE Packet Only |
| EP24TP | 8 | rw | Enable Port 24 to Transmit PPPoE Packet Only |
| Res | 7:0 | rw | Reserved |

PHY Control Register 0

PHYCR0 **Offset**
PHY Control Register 0 **029A_H** **Reset Value**
0000_H

| | | | | | | | | | | | | | | | |
|--------|--------|--------|--------|--------|--------|------|------|------|------|------|------|------|------|------|------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHY1 5 | PHY1 4 | PHY1 3 | PHY1 2 | PHY1 1 | PHY1 0 | PHY9 | PHY8 | PHY7 | PHY6 | PHY5 | PHY4 | PHY3 | PHY2 | PHY1 | PHY0 |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|-------|------|------|---|
| PHY15 | 15 | rw | PHY Port 15 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 15 acts as the master. |
| PHY14 | 14 | rw | PHY Port 14 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 14 acts as the master. |
| PHY13 | 13 | rw | PHY Port 13 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 13 acts as the master. |

EEPROM Register Format

| Field | Bits | Type | Description |
|-------|------|------|--|
| PHY12 | 12 | rw | PHY Port 12 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 12 acts as the master. |
| PHY11 | 11 | rw | PHY Port 11 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 11 acts as the master. |
| PHY10 | 10 | rw | PHY Port 10 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 10 acts as the master. |
| PHY9 | 9 | rw | PHY Port 9 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 9 acts as the master. |
| PHY8 | 8 | rw | PHY Port 8 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 8 acts as the master. |
| PHY7 | 7 | rw | PHY Port 7 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 7 acts as the master. |
| PHY6 | 6 | rw | PHY Port 6 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 6 acts as the master. |
| PHY5 | 5 | rw | PHY Port 5 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 5 acts as the master. |
| PHY4 | 4 | rw | PHY Port 4 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 4 acts as the master. |
| PHY3 | 3 | rw | PHY Port 3 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 3 acts as the master. |
| PHY2 | 2 | rw | PHY Port 2 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 2 acts as the master. |
| PHY1 | 1 | rw | PHY Port 1 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 1 acts as the master. |
| PHY0 | 0 | rw | PHY Port 0 0 _B , PHY acts as the slave. The switch will use the setting in the eeprom register to manage PHY attached. 1 _B , PHY attached to port 0 acts as the master. That is the switch will not configure the PHY attached and it will only poll the PHY to know the state that PHY operates. |

PHY Control Register 1

EEPROM Register Format

PHYCR1 **Offset**
PHY Control Register 1 **029B_H** **Reset Value**
0000_H

| | | | | | | | | | | | | | | | |
|-----|----|----|----|----|----|-----------|-----------|-----|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | | | PHY2 5 | PHY2 4 | Res | | | | | | | |
| | | | | | | rw | rw | | | | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|---|
| PHY25 | 9 | rw | PHY Port 25 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 25 acts as the master. |
| PHY24 | 8 | rw | PHY Port 24 0 _B , PHY acts as the slave. 1 _B , PHY attached to port 24 acts as the master. |
| Res | 7:0 | rw | Reserved |

Disable MDIO Active Register 0

DMDIOAR0 **Offset**
Disable MDIO Active Register 0 **029C_H** **Reset Value**
0000_H

| | | | | | | | | | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| P15B MFE | P14B MFE | P13B MFE | P12B MFE | P11B MFE | P10B MFE | P9BM FE | P8BM FE | P7BM FE | P6BM FE | P5BM FE | P4BM FE | P3BM FE | P2BM FE | P1BM FE | P0BM FE |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---------|------|------|--|
| P15BMFE | 15 | rw | Port 15 Bypass MDIO Function Enable |
| P14BMFE | 14 | rw | Port 14 Bypass MDIO Function Enable |
| P13BMFE | 13 | rw | Port 13 Bypass MDIO Function Enable |
| P12BMFE | 12 | rw | Port 12 Bypass MDIO Function Enable |
| P11BMFE | 11 | rw | Port 11 Bypass MDIO Function Enable |
| P10BMFE | 10 | rw | Port 10 Bypass MDIO Function Enable |
| P9BMFE | 9 | rw | Port 9 Bypass MDIO Function Enable |
| P8BMFE | 8 | rw | Port 8 Bypass MDIO Function Enable |
| P7BMFE | 7 | rw | Port 7 Bypass MDIO Function Enable |
| P6BMFE | 6 | rw | Port 6 Bypass MDIO Function Enable |
| P5BMFE | 5 | rw | Port 5 Bypass MDIO Function Enable |
| P4BMFE | 4 | rw | Port 4 Bypass MDIO Function Enable |
| P3BMFE | 3 | rw | Port 3 Bypass MDIO Function Enable |

EEPROM Register Format

| Field | Bits | Type | Description |
|--------|------|------|---|
| P2BMFE | 2 | rw | Port 2 Bypass MDIO Function Enable |
| P1BMFE | 1 | rw | Port 1 Bypass MDIO Function Enable |
| P0BMFE | 0 | rw | Port 0 Bypass MDIO Function Enable 0 _B , Bypass MDIO Disable. The status is dominated by the MDC/MDIO function except the linkup status, which may be disabled, by the port disable function or the spanning protocol. 1 _B , Bypass MDIO Enable. The effect by the function is as follows: Link Status: Port 0 is forced to link up unless the port is disabled or the spanning tree is in disabled state. Speed Status: Port 0 is configured to Bit [6] in the Port Configuration Register. Duplex Status: Port 0 is configured to Bit [7] in the Port Configuration Register. Pause Status: Port 0 is configured to Bit [4] in the Port Configuration Register. Back Pressure Status: Port 0 is configured to Bit[15] in the Port Configuration Register. |

Disable MDIO Active Register 1

| | | |
|---------------------------------------|-------------------------|-------------------------|
| DMDIOAR1 | Offset | Reset Value |
| Disable MDIO Active Register 1 | 029D_H | 0000_H |

| | | | | | | | | | | | | | | | |
|-----|----|----|----|----|----|-----------------|-----------------|-----|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | | | P25B MFE | P24B MFE | Res | | | | | | | |
| | | | | | | rw | rw | rw | | | | | | | |

| Field | Bits | Type | Description |
|---------|------|------|--|
| P25BMFE | 9 | rw | Port 25 Bypass MDIO Function Enable |
| P24BMFE | 8 | rw | Port 24 Bypass MDIO Function Enable |
| Res | 7:0 | rw | Reserved |

Port Disable Register 0

| | | |
|--------------------------------|-------------------------|-------------------------|
| PDR0 | Offset | Reset Value |
| Port Disable Register 0 | 029E_H | 0000_H |

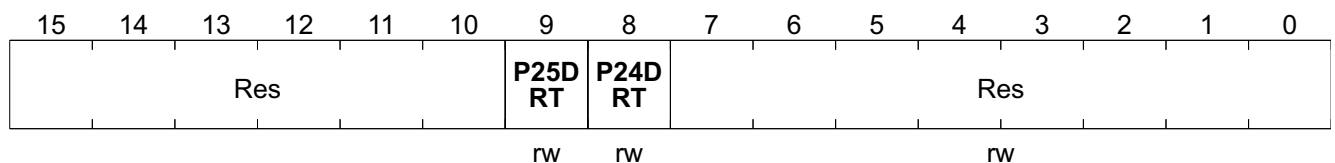
| | | | | | | | | | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| P15D RT | P14D RT | P13D RT | P12D RT | P11D RT | P10D RT | P9DR T | P8DR T | P7DR T | P6DR T | P5DR T | P4DR T | P3DR T | P2DR T | P1DR T | P0DR T |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

EEPROM Register Format

| Field | Bits | Type | Description |
|--------|------|------|--|
| P15DRT | 15 | rw | Port 15 Disable Receive and Transmit |
| P14DRT | 14 | rw | Port 14 Disable Receive and Transmit |
| P13DRT | 13 | rw | Port 13 Disable Receive and Transmit |
| P12DRT | 12 | rw | Port 12 Disable Receive and Transmit |
| P11DRT | 11 | rw | Port 11 Disable Receive and Transmit |
| P10DRT | 10 | rw | Port 10 Disable Receive and Transmit |
| P9DRT | 9 | rw | Port 9 Disable Receive and Transmit |
| P8DRT | 8 | rw | Port 8 Disable Receive and Transmit |
| P7DRT | 7 | rw | Port 7 Disable Receive and Transmit |
| P6DRT | 6 | rw | Port 6 Disable Receive and Transmit |
| P5DRT | 5 | rw | Port 5 Disable Receive and Transmit |
| P4DRT | 4 | rw | Port 4 Disable Receive and Transmit |
| P3DRT | 3 | rw | Port 3 Disable Receive and Transmit |
| P2DRT | 2 | rw | Port 2 Disable Receive and Transmit |
| P1DRT | 1 | rw | Port 1 Disable Receive and Transmit |
| P0DRT | 0 | rw | Port 0 Disable Receive and Transmit 0 _B , The port acts as the normal mode. 1 _B , The port will not receive or transmit packets. Learning is disabled in the disabled port. |

Port Disable Register 1

PDR1 **Offset**
Port Disable Register 1 **029F_H** **Reset Value**
0000_H



| Field | Bits | Type | Description |
|--------|------|------|--------------------------------------|
| P25DRT | 9 | rw | Port 25 Disable Receive and Transmit |
| P24DRT | 8 | rw | Port 24 Disable Receive and Transmit |
| Res | 7:0 | rw | Reserved |

IGMP Snooping Control Register 0

IGMPSCR0 **Offset**
IGMP Snooping Control Register 0 **02A0_H** **Reset Value**
0000_H

EEPROM Register Format

| | | | | | | | | | | | | | | | |
|----------|----------|----------|----------|----------|----------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| P15E ISF | P14E ISF | P13E ISF | P12E ISF | P11E ISF | P10E ISF | P9E ISF | P8E ISF | P7E ISF | P6E ISF | P5E ISF | P4E ISF | P3E ISF | P2E ISF | P1E ISF | P0E ISF |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---------|------|------|--|
| P15EISF | 15 | rw | Port 15 Enable IGMP Snooping Function |
| P14EISF | 14 | rw | Port 14 Enable IGMP Snooping Function |
| P13EISF | 13 | rw | Port 13 Enable IGMP Snooping Function |
| P12EISF | 12 | rw | Port 12 Enable IGMP Snooping Function |
| P11EISF | 11 | rw | Port 11 Enable IGMP Snooping Function |
| P10EISF | 10 | rw | Port 10 Enable IGMP Snooping Function |
| P9EISF | 9 | rw | Port 9 Enable IGMP Snooping Function |
| P8EISF | 8 | rw | Port 8 Enable IGMP Snooping Function |
| P7EISF | 7 | rw | Port 7 Enable IGMP Snooping Function |
| P6EISF | 6 | rw | Port 6 Enable IGMP Snooping Function |
| P5EISF | 5 | rw | Port 5 Enable IGMP Snooping Function |
| P4EISF | 4 | rw | Port 4 Enable IGMP Snooping Function |
| P3EISF | 3 | rw | Port 3 Enable IGMP Snooping Function |
| P2EISF | 2 | rw | Port 2 Enable IGMP Snooping Function |
| P1EISF | 1 | rw | Port 1 Enable IGMP Snooping Function |
| P0EISF | 0 | rw | Port 0 Enable IGMP Snooping Function The packets with the header (DA = 01005exxxxxx, Length_Type = 0800, IP version = 4, and Protocol type = 2) will be recognized as the IGMP packets, and the switch will forward it to the CPU port. 0 _B , The port 0 is not configured to enable IGMP Snooping Function. And the IGMP packets will be handled as the normal multicast packets. 1 _B , The port 0 is configured to enable IGMP Snooping Function. |

IGMP Snooping Control Register 1

| | | |
|---|-------------------------|-------------------------|
| IGMPSCR1 | Offset | Reset Value |
| IGMP Snooping Control Register 1 | 02A1_H | 0000_H |

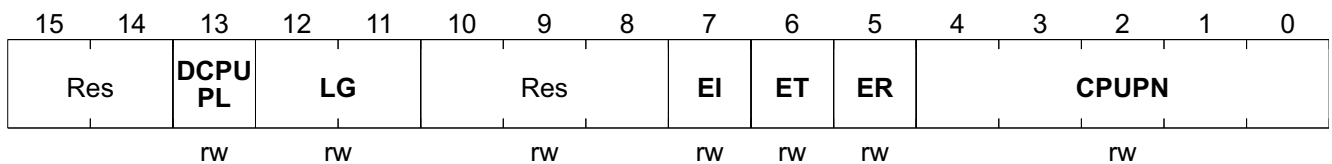
| | | | | | | | | | | | | | | | |
|-----|----|----|----|-----|----|----------|----------|-----|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | MCR | | P25E ISF | P24E ISF | Res | | | | | | | |
| | | | | rw | | rw | rw | | | | | | | | |

EEPROM Register Format

| Field | Bits | Type | Description |
|---------|-------|------|---|
| MCR | 11:10 | rw | Multicast Control Register Packets with the following conditions will follow the Multicast Control Register to handle packets. Conditions: Destination address is not found in the address table. AND Destination address is a multicast address. AND Destination address is not all 1'b1. AND Destination address is not a reserved address(0180c2000~~). OR IGMP packets received by the port which disables the IGMP function. Multicast Control, Action 00 _B , Forward to all ports within the same forwarding group except the self port. 01 _B , Send to the CPU port. 10 _B , Discard. 11 _B , Reserved. |
| P25EISF | 9 | rw | Port 25 Enable IGMP Snooping Function |
| P24EISF | 8 | rw | Port 24 Enable IGMP Snooping Function |
| Res | 7:0 | rw | Reserved |

CPU Control Register

CPUCR Offset
CPU Control Register 02A2_H Reset Value
001F_H



| Field | Bits | Type | Description |
|--------|------|------|---|
| DCPUPL | 13 | rw | Disable CPU Port Learning Function 0 _B , The packets received from the CPU port will be learned. 1 _B , The packets received from the CPU port will not be learned. |

EEPROM Register Format

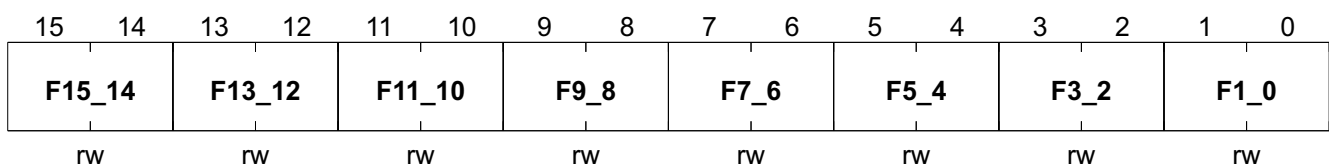
| Field | Bits | Type | Description |
|-------|-------|------|--|
| LG | 12:11 | rw | <p>Learning Group ADM6918/X has an ability to learn packets according their forwarding groups. The ADM6918/X could be divided into 32 learning groups. We use L0, L1, ... and L31 to call each learning group.</p> <p>0x_B , Normal mode, learning with SA only. 10_B , MAC Clone mode, learning with SA and VID[0]. When packets are received and could be learned, they are learned divided into two Groups. Even forwarding groups are learned into L0 and odd forwarding groups are learned into L1. 11_B , Learning with SA and VID[4:0]. When packets are received and could be learned, they are learned according to their forwarding group. That is packets belonging to F0 is learned into L0, packets belonging to F1 is learned into L1, ... and packets belonging to F31 is leaned into L31.</p> |
| Res | 10:8 | rw | Reserved |
| EI | 7 | rw | <p>Enable Insert Enable insert 4-byte special tag when Pause happens and Bit[6] is enabled.</p> <p>0_B , ADM6918/X will add 4-byte special TAG when pause happens. 1_B , ADM6918/X will add 4-byte special TAG when pause happens.</p> |
| ET | 6 | rw | <p>Enable Transmit Enable transmit 4-byte special tag to the CPU port to support IGMP snooping, spanning tree or the security function.</p> <p>0_B , ADM6918/X will transmit packets as the normal mode. 1_B , ADM6918/X will insert addition 4-byte special TAG when it has packets to be transmitted to the CPU port.</p> |
| ER | 5 | rw | <p>Enable Receive Enable receive 8-byte special tag from the CPU port to support IGMP snooping, spanning tree or the security function.</p> <p>0_B , CPU will transmit packets as the normal state. 1_B , CPU will transmit packets with additional 8-byte special TAG and the ADM6918/X will remove this special TAG, use information contained to forward packets and recalculate CRC value when this packet is re-transmitted.</p> |

EEPROM Register Format

| Field | Bits | Type | Description |
|-------|------|------|---|
| CPUPN | 4:0 | rw | CPU Port Number The ADM6918/X allows any port to be configured to be the CPU port. The default CPU port is port 31. That is CPU port is not present. 0000 _B , CPU port is configured to port 0. 00001 _B , CPU port is configured to port 1. 00010 _B , CPU port is configured to port 2. 00011 _B , CPU port is configured to port 3. 00100 _B , CPU port is configured to port 4. 00101 _B , CPU port is configured to port 5. 00110 _B , CPU port is configured to port 6. 00111 _B , CPU port is configured to port 7. 01000 _B , CPU port is configured to port 8. 01001 _B , CPU port is configured to port 9. 01010 _B , CPU port is configured to port 10. 01011 _B , CPU port is configured to port 11. 01100 _B , CPU port is configured to port 12. 01101 _B , CPU port is configured to port 13. 01110 _B , CPU port is configured to port 14. 01111 _B , CPU port is configured to port 15. 10000 _B , CPU port is configured to port 16. 10001 _B , CPU port is configured to port 17. 10010 _B , CPU port is configured to port 18. 10011 _B , CPU port is configured to port 19. 10100 _B , CPU port is configured to port 20. 10101 _B , CPU port is configured to port 21. 10110 _B , CPU port is configured to port 22. 10111 _B , CPU port is configured to port 23. 11000 _B , CPU port is configured to port 24. 11001 _B , CPU port is configured to port 25. |

Special MAC Forward Control Register 0

| | | |
|--|-------------------|--------------------|
| SMACFCR0 | Offset | Reset Value |
| Special MAC Forward Control Register 0 | 02A3 _H | 0004 _H |



| Field | Bits | Type | Description |
|--------|-------|------|--|
| F15_14 | 15:14 | rw | Forwarding 15_14 The forwarding option for destination address = 0180c2000023 ~0180c20000ff |

EEPROM Register Format

| Field | Bits | Type | Description |
|--------|-------|------|---|
| F13_12 | 13:12 | rw | Forwarding 13_12 The forwarding option for destination address = 0180c2000020 ~0180c2000022 (GMRP, GVRP, GARP) |
| F11_10 | 11:10 | rw | Forwarding 11_10 The forwarding option for destination address = 0180c2000010 ~0180c200001f |
| F9_8 | 9:8 | rw | Forwarding 9_8 The forwarding option for destination address = 0180c2000004 ~0180c200000f |
| F7_6 | 7:6 | rw | Forwarding 7_6 The forwarding option for destination address = 0180c2000003 (802.1x PAE address) |
| F5_4 | 5:4 | rw | Forwarding 5_4 The forwarding option for destination address = 48'h0180c2000002 (Slow Protocol) |
| F3_2 | 3:2 | rw | Forwarding 3_2 The forwarding option for destination address = 0180c2000001 (Reserved for Pause address), MAC control field = 8808, OP Code != 0001 |
| F1_0 | 1:0 | rw | Forwarding 1_0 The forwarding option for destination address = 48'h0180c2000000 (BPDU) |

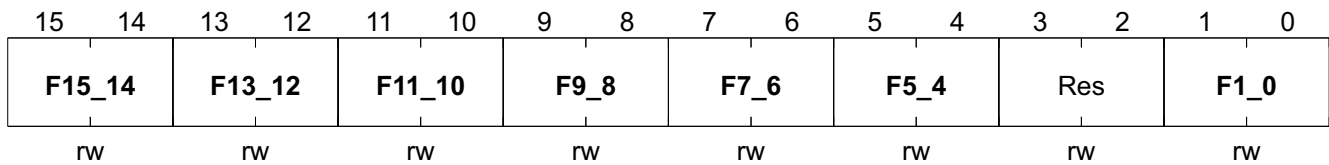
Notes

- The options are defined here: 00_B = The switch will forward the packets as the normal mode. That is for reserved addresses existed in the learning table (because reserved address is multicast address, it could only be created through the CPU help if it really exists in the learning table). We will use "output port field" as the index to lookup the multicast table. At last, the looked output port map (may be modified by the forwarding process) is used as the output ports to forward packets. For reserved addresses, which don't exist in the learning table, it will be broadcast to the forwarding group except the receiving port. 01_B = The switch will discard the packets. 10_B = The switch will forward the packets to the CPU port. If the packet is received from the CPU port, the packet will be forwarded as the normal mode. 11_B = The switch will forward the packet to CPU port. If this packet is received from CPU Port, this packet will be discard.
- The forwarding options stated above will be of no effect for the CPU port when users enable the "Special Tag Function" and its output vector field is valid.

Special MAC Forward Control Register 1

| | | |
|---|-------------------------|-------------------------|
| SMACFCR1 | Offset | Reset Value |
| Special MAC Forward Control Register 1 | 02A4_H | 0003_H |

EEPROM Register Format



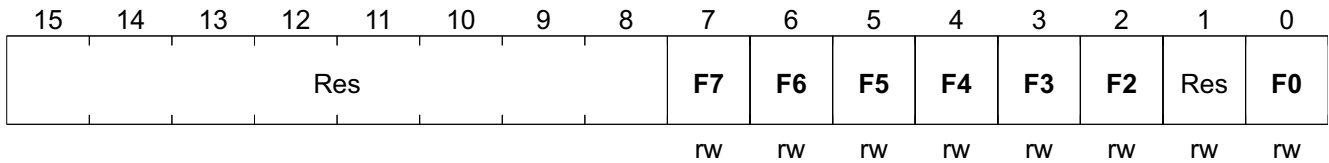
| Field | Bits | Type | Description |
|--------|-------|------|--|
| F15_14 | 15:14 | rw | Forwarding 15_14 The forwarding option for destination address = 0180c2000023 ~0180c20000ff |
| F13_12 | 13:12 | rw | Forwarding 13_12 The forwarding option for destination address = 0180c2000020 ~0180c2000022 (GMRP, GVRP, GARP) |
| F11_10 | 11:10 | rw | Forwarding 11_10 The forwarding option for destination address = 0180c2000010 ~0180c200001f |
| F9_8 | 9:8 | rw | Forwarding 9_8 The forwarding option for destination address = 0180c2000004 ~0180c200000f |
| F7_6 | 7:6 | rw | Forwarding 7_6 The forwarding option for destination address = 0180c2000003 (802.1x PAE address) |
| F5_4 | 5:4 | rw | Forwarding 5_4 The forwarding option for destination address = 48'h0180c2000002 (Slow Protocol) |
| Res | 3:2 | rw | Reserved |
| F1_0 | 1:0 | rw | Forwarding 1_0 The forwarding option for destination address = 48'h0180c2000000 (BPDU) |

Note: The ADM6918/X will divide packets into management or unmanagement packets. Management packets will not be dropped even if the buffer is full for no flow control environment. Only management packets will be forwarded or received in Blocking-N-Listening or the Learning state.

The options are defined here: 00_B = The packets will not be classified as the management packets and it will be treated as the normal packet. 01_B = The packets will be classified as the management packets and it will be transmitted no modified. 10_B = The packets will be classified as the management packets and it will be transmitted without tag. 11_B = The packets will be classified as the management packets and it will be transmitted with tag or without tag as the system configuration.

Special MAC Forward Control Register 2

| | | |
|--|-------------------|--------------------|
| SMACFCR2 | Offset | Reset Value |
| Special MAC Forward Control Register 2 | 02A5 _H | 0000 _H |

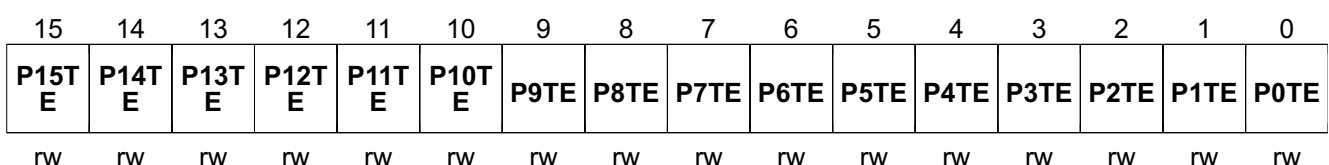
EEPROM Register Format


| Field | Bits | Type | Description |
|-------|------|------|--|
| F7 | 7 | rw | Forwarding 7 The forwarding option for destination address = 0180c2000023 ~0180c20000ff |
| F6 | 6 | rw | Forwarding 6 The forwarding option for destination address = 0180c2000020 ~0180c2000022 (GMRP, GVRP, GARP) |
| F5 | 5 | rw | Forwarding 5 The forwarding option for destination address = 0180c2000010 ~0180c200001f |
| F4 | 4 | rw | Forwarding 4 The forwarding option for destination address = 0180c2000004 ~0180c200000f |
| F3 | 3 | rw | Forwarding 3 The forwarding option for destination address = 0180c2000003 (802.1x PAE address) |
| F2 | 2 | rw | Forwarding 2 The forwarding option for destination address = 48'h0180c2000002 (Slow Protocol) |
| Res | 1 | rw | Reserved |
| F0 | 0 | rw | Forwarding 0 The forwarding option for destination address = 48'h0180c2000000 (BPDU) |

Note: The options are defined here: 1_B = The packets will cross forwarding group. 0_B = The packets will not cross the forwarding packet.

Trunking Enable Register 0

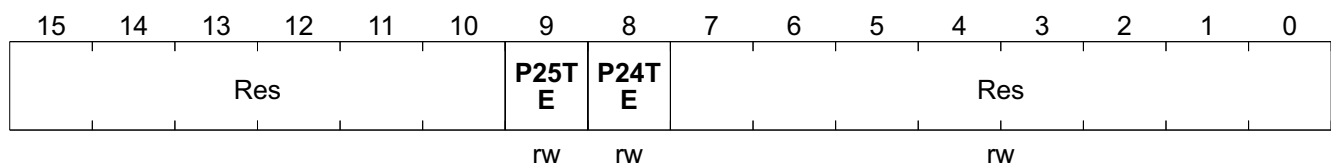
| | | |
|-----------------------------------|-------------------------|-------------------------|
| TER0 | Offset | Reset Value |
| Trunking Enable Register 0 | 02A6_H | 0000_H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| P15TE | 15 | rw | Port 15 Trunking Enable |
| P14TE | 14 | rw | Port 14 Trunking Enable |
| P13TE | 13 | rw | Port 13 Trunking Enable |
| P12TE | 12 | rw | Port 12 Trunking Enable |
| P11TE | 11 | rw | Port 11 Trunking Enable |
| P10TE | 10 | rw | Port 10 Trunking Enable |
| P9TE | 9 | rw | Port 9 Trunking Enable |
| P8TE | 8 | rw | Port 8 Trunking Enable |
| P7TE | 7 | rw | Port 7 Trunking Enable |
| P6TE | 6 | rw | Port 6 Trunking Enable |
| P5TE | 5 | rw | Port 5 Trunking Enable |
| P4TE | 4 | rw | Port 4 Trunking Enable |
| P3TE | 3 | rw | Port 3 Trunking Enable |
| P2TE | 2 | rw | Port 2 Trunking Enable |
| P1TE | 1 | rw | Port 1 Trunking Enable |
| P0TE | 0 | rw | Port 0 Trunking Enable The ADM6918/X supports one trunking port. Any port could be assigned to the trunking port. The trunking function is of the effect only the trunking hardware setting = 1. 0_B , Port 0 is not assigned to a member of the trunking port. 1_B , Port 0 is assigned to a member of the trunking port. |

Trunking Enable Register 1

TER1 **Offset**
Trunking Enable Register 1 **02A7_H** **Reset Value**
0000_H



| Field | Bits | Type | Description |
|-------|------|------|-------------------------|
| P25TE | 9 | rw | Port 25 Trunking Enable |
| P24TE | 8 | rw | Port 24 Trunking Enable |
| Res | 7:0 | rw | Reserved |

5 Switch Register Map

Table 25 Switch Register Map

| Offset Hex | Bit 31 ~ 0 | Type |
|------------------|------------------------------------|------|
| 0 _H | Version ID | ro |
| 1 _H | Link Status | ro |
| 2 _H | Speed Status | ro |
| 3 _H | Duplex Status | ro |
| 4 _H | Flow Control Status | ro |
| 5 _H | Address Table Control Register 0 | rw |
| 6 _H | Address Table Control Register 1 | rw |
| 7 _H | Address Table Control Register 2 | rw |
| 8 _H | Address Table Status Register 0 | ro |
| 9 _H | Address Table Status Register 1 | ro |
| A _H | Address Table Status Register 2 | ro |
| B _H | PHY Control/Status Register | rw |
| C _H | Reserved | ro |
| D _H | Hardware Status | ro |
| E _H | RxPKT Overflow | roc |
| F _H | RxLEN Overflow | roc |
| 10 _H | TxPKT Overflow | roc |
| 11 _H | TxLEN Overflow | roc |
| 12 _H | RxERR Overflow | roc |
| 13 _H | RxCOL Overflow | roc |
| 14 _H | Renew Counter Register | rw |
| 15 _H | Read Counter Control Register | rw |
| 16 _H | Read Counter Status Register | ro |
| 17 _H | Reload MDIO Register | rw |
| 18 _H | P0 ~ P15 Spanning Tree Port State | rw |
| 19 _H | P16 ~ P25 Spanning Tree Port State | rw |
| 1A _H | Source Port Register | ro |
| 1B _H | Transmit Port Register | rw |
| 1C _H | Buffer Status Register 0 | roc |
| 1D _H | Buffer Status Register 1 | roc |
| 1E _H | Buffer Status Register 2 | roc |
| 1F _H | Buffer Status Register 3 | roc |
| 1xx _H | Counter Register | rw |
| 2xx _H | EEPROM Register | rw |

5.1 Switch Registers

Table 26 Registers Address Space Registers Address Space

| Module | Base Address | End Address | Note |
|--------|-----------------|-----------------|------|
| Switch | 00 _H | 1B _H | |

Table 27 Registers Overview

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---------------------------------------|-----------------|-------------|
| VID | Version ID | 00 _H | 87 |
| LS | Link Status | 01 _H | 88 |
| SS | Speed Status | 02 _H | 89 |
| DS | Duplex Status | 03 _H | 89 |
| FCS | Flow Control Status | 04 _H | 90 |
| PHYCR | PHY Control Register | 0B _H | 97 |
| HS | Hardware Status | 0D _H | 98 |
| RPCO | Receive Packet Count Overflow | 0E _H | 99 |
| RPLCO | Receive Packet Length Count Overflow | 0F _H | 99 |
| TPCO | Transmit Packet Count Overflow | 10 _H | 100 |
| TPLCO | Transmit Packet Length Count Overflow | 11 _H | 101 |
| ECO | Error Count Overflow | 12 _H | 102 |
| CCO | Collision Count Overflow | 13 _H | 103 |
| RCR | Renew Counter Register | 14 _H | 103 |
| RCCR | Read Counter Control Register | 15 _H | 105 |
| RCSR | Read Counter Status Register | 16 _H | 105 |
| RMDIOR | Reload MDIO Register | 17 _H | 106 |
| STPS0 | Spanning Tree Port State 0 | 18 _H | 107 |
| STPS1 | Spanning Tree Port State 1 | 19 _H | 108 |
| SCPR | Source Port Register | 1A _H | 108 |
| TRPR | Transmit Port Register | 1B _H | 109 |

The register is addressed wordwise.

Table 28 Register Access Types

| Mode | Symbol | Description HW | Description SW |
|------------|--------|--|---|
| read/write | rw | Register is used as input for the HW | Register is read and writable by SW |
| read | r | Register is written by HW (register between input and output -> one cycle delay) | Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.) |
| Read only | ro | Register is set by HW (register between input and output -> one cycle delay) | SW can only read this register |

Switch Register Map
Table 28 Register Access Types (cont'd)

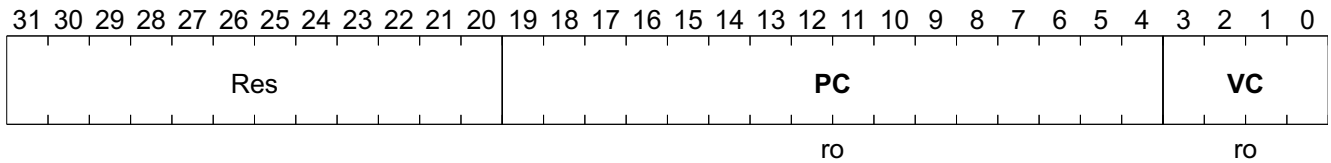
| Mode | Symbol | Description HW | Description SW |
|-------------------------------|--------|---|---|
| Read virtual | rv | Physically, there is no new register, the input of the signal is connected directly to the address multiplexer. | SW can only read this register |
| Latch high, self clearing | lhsc | Latch high signal at high level, clear on read | SW can read the register |
| Latch low, self clearing | llsc | Latch high signal at low-level, clear on read | SW can read the register |
| Latch high, mask clearing | lhmk | Latch high signal at high level, register cleared with written mask | SW can read the register, with write mask the register can be cleared (1 clears) |
| Latch low, mask clearing | llmk | Latch high signal at low-level, register cleared on read | SW can read the register, with write mask the register can be cleared (1 clears) |
| Interrupt high, self clearing | ihsc | Differentiate the input signal (low->high) register cleared on read | SW can read the register |
| Interrupt low, self clearing | ilsc | Differentiate the input signal (high->low) register cleared on read | SW can read the register |
| Interrupt high, mask clearing | ihmk | Differentiate the input signal (high->low) register cleared with written mask | SW can read the register, with write mask the register can be cleared |
| Interrupt low, mask clearing | ilmk | Differentiate the input signal (low->high) register cleared with written mask | SW can read the register, with write mask the register can be cleared |
| Interrupt enable register | ien | Enables the interrupt source for interrupt generation | SW can read and write this register |
| latch_on_reset | lor | rw register, value is latched after first clock cycle after reset | Register is read and writable by SW |
| Read/write self clearing | rwsc | Register is used as input for the hw, the register will be cleared due to a HW mechanism. | Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW. |

Table 29 Registers Clock DomainsRegisters Clock Domains

| Clock Short Name | Description |
|------------------|-------------|
| | |

5.1.1 Switch Register Descriptions
Version ID

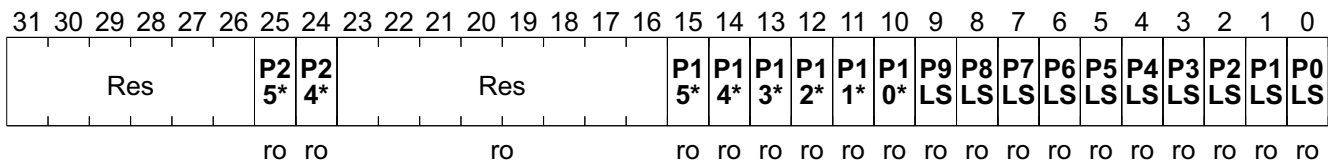
| VID | Offset | Reset Value |
|------------|-----------------|------------------------|
| Version ID | 00 _H | 0003 1100 _H |

Switch Register Map


| Field | Bits | Type | Description |
|-------|------|------|--------------|
| PC | 19:4 | ro | Project Code |
| VC | 3:0 | ro | Version Code |

Link Status

| | | |
|--------------------|-----------------------|------------------------------|
| LS | Offset | Reset Value |
| Link Status | 01_H | 0000 0000_H |



| Field | Bits | Type | Description |
|-------|-------|------|--|
| P25LS | 25 | ro | Port 25 Link Status |
| P24LS | 24 | ro | Port 24 Link Status |
| Res | 23:16 | ro | Reserved |
| P15LS | 15 | ro | Port 15 Link Status |
| P14LS | 14 | ro | Port 14 Link Status |
| P13LS | 13 | ro | Port 13 Link Status |
| P12LS | 12 | ro | Port 12 Link Status |
| P11LS | 11 | ro | Port 11 Link Status |
| P10LS | 10 | ro | Port 10 Link Status |
| P9LS | 9 | ro | Port 9 Link Status |
| P8LS | 8 | ro | Port 8 Link Status |
| P7LS | 7 | ro | Port 7 Link Status |
| P6LS | 6 | ro | Port 6 Link Status |
| P5LS | 5 | ro | Port 5 Link Status |
| P4LS | 4 | ro | Port 4 Link Status |
| P3LS | 3 | ro | Port 3 Link Status |
| P2LS | 2 | ro | Port 2 Link Status |
| P1LS | 1 | ro | Port 1 Link Status |
| P0LS | 0 | ro | Port 0 Link Status 0 _B , Port 0 links down. 1 _B , Port 0 links up. |

Switch Register Map

Speed Status

SS **Offset** **Reset Value**
Speed Status **02_H** **03FF FFFF_H**

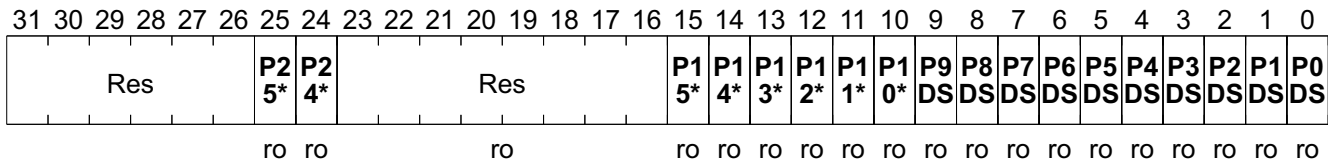
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----|----|----|----|----|----|----------|----------|-----|----|----|----|----|----|----|----|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Res | | | | | | P2 5* | P2 4* | Res | | | | | | | | P1 5* | P1 4* | P1 3* | P1 2* | P1 1* | P1 0* | P9 SS | P8 SS | P7 SS | P6 SS | P5 SS | P4 SS | P3 SS | P2 SS | P1 SS | P0 SS | | |
| | | | | | | ro | ro | | | | | | | | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|-------|-------|------|---|
| P25SS | 25 | ro | Port 25 Speed Status |
| P24SS | 24 | ro | Port 24 Speed Status |
| Res | 23:16 | ro | Reserved |
| P15SS | 15 | ro | Port 15 Speed Status |
| P14SS | 14 | ro | Port 14 Speed Status |
| P13SS | 13 | ro | Port 13 Speed Status |
| P12SS | 12 | ro | Port 12 Speed Status |
| P11SS | 11 | ro | Port 11 Speed Status |
| P10SS | 10 | ro | Port 10 Speed Status |
| P9SS | 9 | ro | Port 9 Speed Status |
| P8SS | 8 | ro | Port 8 Speed Status |
| P7SS | 7 | ro | Port 7 Speed Status |
| P6SS | 6 | ro | Port 6 Speed Status |
| P5SS | 5 | ro | Port 5 Speed Status |
| P4SS | 4 | ro | Port 4 Speed Status |
| P3SS | 3 | ro | Port 3 Speed Status |
| P2SS | 2 | ro | Port 2 Speed Status |
| P1SS | 1 | ro | Port 1 Speed Status |
| P0SS | 0 | ro | Port 0 Speed Status 0 _B , Port 0 operates in 10M. 1 _B , Port 0 operates in 100M. |

Duplex Status

DS **Offset** **Reset Value**
Duplex Status **03_H** **03FF FFFF_H**

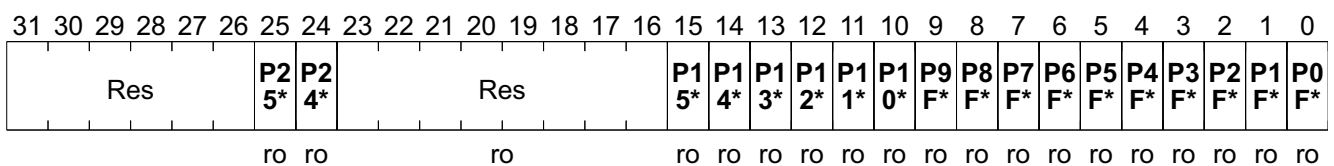
Switch Register Map



| Field | Bits | Type | Description |
|-------|-------|------|--|
| P25DS | 25 | ro | Port 25 Duplex Status |
| P24DS | 24 | ro | Port 24 Duplex Status |
| Res | 23:16 | ro | Reserved |
| P15DS | 15 | ro | Port 15 Duplex Status |
| P14DS | 14 | ro | Port 14 Duplex Status |
| P13DS | 13 | ro | Port 13 Duplex Status |
| P12DS | 12 | ro | Port 12 Duplex Status |
| P11DS | 11 | ro | Port 11 Duplex Status |
| P10DS | 10 | ro | Port 10 Duplex Status |
| P9DS | 9 | ro | Port 9 Duplex Status |
| P8DS | 8 | ro | Port 8 Duplex Status |
| P7DS | 7 | ro | Port 7 Duplex Status |
| P6DS | 6 | ro | Port 6 Duplex Status |
| P5DS | 5 | ro | Port 5 Duplex Status |
| P4DS | 4 | ro | Port 4 Duplex Status |
| P3DS | 3 | ro | Port 3 Duplex Status |
| P2DS | 2 | ro | Port 2 Duplex Status |
| P1DS | 1 | ro | Port 1 Duplex Status |
| P0DS | 0 | ro | Port 0 Duplex Status 0 _B , Port 0 operates in half duplex. 1 _B , Port 0 operates in full duplex. |

Flow Control Status

| | | |
|----------------------------|-----------------------|------------------------------|
| FCS | Offset | Reset Value |
| Flow Control Status | 04_H | 03FF FFFF_H |



| Field | Bits | Type | Description |
|--------|------|------|-----------------------------|
| P25FCS | 25 | ro | Port 25 Flow Control Status |
| P24FCS | 24 | ro | Port 24 Flow Control Status |

Switch Register Map

| Field | Bits | Type | Description |
|--------|-------|------|---|
| Res | 23:16 | ro | Reserved |
| P15FCS | 15 | ro | Port 15 Flow Control Status |
| P14FCS | 14 | ro | Port 14 Flow Control Status |
| P13FCS | 13 | ro | Port 13 Flow Control Status |
| P12FCS | 12 | ro | Port 12 Flow Control Status |
| P11FCS | 11 | ro | Port 11 Flow Control Status |
| P10FCS | 10 | ro | Port 10 Flow Control Status |
| P9FCS | 9 | ro | Port 9 Flow Control Status |
| P8FCS | 8 | ro | Port 8 Flow Control Status |
| P7FCS | 7 | ro | Port 7 Flow Control Status |
| P6FCS | 6 | ro | Port 6 Flow Control Status |
| P5FCS | 5 | ro | Port 5 Flow Control Status |
| P4FCS | 4 | ro | Port 4 Flow Control Status |
| P3FCS | 3 | ro | Port 3 Flow Control Status |
| P2FCS | 2 | ro | Port 2 Flow Control Status |
| P1FCS | 1 | ro | Port 1 Flow Control Status |
| P0FCS | 0 | ro | Port 0 Flow Control Status 0 _B , Port 0 disables flow control function. 1 _B , Port 0 enables Pause function in full duplex or Back Pressure function in half duplex. |

Address Table Control and Status Registers

Address Table Control Register 0 (Offset: 5_H)

Address Table Control Register 1 (Offset: 6_H)

Address Table Control Register 2 (Offset: 7_H)

Address Table Status Register 0 (Offset: 8_H)

Address Table Status Register 1 (Offset: 9_H)

Address Table Status Register 2 (Offset: A_H)

The ADM6918/X provides custom commands to access the address table as well as the multicast output port map table. Six registers are used and they mean differently when different tables are accessed.

1. The Control and Status Register Description for the Address Table

Table 30 Control Register Description

| Command Field | Entry State | Control Field | Output Port/ Multicast Index | Forwarding Group | MAC Address |
|----------------|------------------|------------------|---------------------------------|---------------------|---------------------------------------|
| Control_2[2:0] | Control_1[31:30] | Control_1[29:26] | Control_1[25:21] | Control_1[20:16] | {Control_1[15:0], Control_0[31:0]} |

Table 31 Field Description in the Control Register

| Field | Description |
|-----------------------|--|
| MAC Address[47:0] | This field is 48-bit layer-2 address. The address could be the unicast address or the multicast address. |
| Forwarding Group[4:0] | This field describes the Learning Group the address belongs to. |

Table 31 Field Description in the Control Register (cont'd)

| Field | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------------------|---|--|---------------|-----------|-----|------|----------------------|-----|------|------------------------------|-----|------|--------------------------|-----|------|-------------------------|-----|------|---|-----|------|--|-----|------|--|-----|------|--|-----|------|---------------------------------------|-----|------|--|-----|------|---|-----|------|--|-----|------|------------------------------|
| Output Port[4:0]/Multicast Index[4:0] | This field has two means. One is described as the output port and the other is described as the multicast index. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Entry State[0] | The Static Bit. When this bit is set to a one, then the address entry will not be aged forever. This bit could be changed only through the CUP's help. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Entry State[1] | <p>This bit is used to distinguish the output port/ multicast index field.</p> <p>When a match (the same MAC address and the same forwarding group in the address table) is found, the value in the output port field is returned as the output port, and may be modified by the forwarding group before the packet is transferred to the output queue.</p> <p>When a match (the same MAC address and the same forwarding group in the address table) is found, the multicast output port map entry addressed by the multicast index is returned as the output port map, and may be modified by the forwarding group before the packet is transferred to the output queue.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command Field[2:0]/Control Field[3:0] | <p>The command and control fields are combined to provide different operations. Before the operation is initiated, users should confirm if the search engine is available. See the busy bit in the status register.</p> <table border="1"> <thead> <tr> <th>Command Field</th> <th>Control Field</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>0111</td> <td>Create a new address</td> </tr> <tr> <td>000</td> <td>1111</td> <td>Overwrite an existed address</td> </tr> <tr> <td>001</td> <td>1111</td> <td>Erase an existed address</td> </tr> <tr> <td>010</td> <td>0000</td> <td>Search an empty address</td> </tr> <tr> <td>010</td> <td>1001</td> <td>Search by the port in the Output Port field</td> </tr> <tr> <td>010</td> <td>1010</td> <td>Search by the forwarding group specified in the Forwarding Group field</td> </tr> <tr> <td>010</td> <td>1100</td> <td>Search by the address specified in the MAC Address field</td> </tr> <tr> <td>010</td> <td>1110</td> <td>Search by the address and forwarding group</td> </tr> <tr> <td>010</td> <td>1101</td> <td>Search by the address and output port</td> </tr> <tr> <td>010</td> <td>1011</td> <td>Search by the forwarding group and the output port</td> </tr> <tr> <td>010</td> <td>1111</td> <td>Search by the address, the forwarding group and the output port</td> </tr> <tr> <td>011</td> <td>0100</td> <td>Initial to location by the address field</td> </tr> <tr> <td>011</td> <td>0000</td> <td>Initial to the first address</td> </tr> </tbody> </table> | Command Field | Control Field | Operation | 000 | 0111 | Create a new address | 000 | 1111 | Overwrite an existed address | 001 | 1111 | Erase an existed address | 010 | 0000 | Search an empty address | 010 | 1001 | Search by the port in the Output Port field | 010 | 1010 | Search by the forwarding group specified in the Forwarding Group field | 010 | 1100 | Search by the address specified in the MAC Address field | 010 | 1110 | Search by the address and forwarding group | 010 | 1101 | Search by the address and output port | 010 | 1011 | Search by the forwarding group and the output port | 010 | 1111 | Search by the address, the forwarding group and the output port | 011 | 0100 | Initial to location by the address field | 011 | 0000 | Initial to the first address |
| Command Field | Control Field | Operation | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000 | 0111 | Create a new address | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000 | 1111 | Overwrite an existed address | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 001 | 1111 | Erase an existed address | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 0000 | Search an empty address | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 1001 | Search by the port in the Output Port field | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 1010 | Search by the forwarding group specified in the Forwarding Group field | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 1100 | Search by the address specified in the MAC Address field | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 1110 | Search by the address and forwarding group | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 1101 | Search by the address and output port | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 1011 | Search by the forwarding group and the output port | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 1111 | Search by the address, the forwarding group and the output port | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011 | 0100 | Initial to location by the address field | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011 | 0000 | Initial to the first address | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 32 Status Register Description

| Busy | Command Result | Bad State | Entry State | Occupy | Output Port/ Multicast Index | Forwarding Group | MAC Address |
|-------------|----------------|---------------|------------------|---------------|---------------------------------|------------------|---------------------------------------|
| Status_2[3] | Status_2 [2:0] | Status_1 [29] | Status_1 [28:27] | Status_1 [26] | Status_1 [25:21] | Status_1 [20:16] | {Status_1 [15:0], Status_0 [31:0]} |

Table 33 Field Description in the Status Register

| Field | Description |
|--|---|
| MAC Address[47:0] | After the search operation is successful, the switch will return the MAC address in this field. If the search fails, this field doesn't mean anything. |
| Forwarding Group[4:0] | After the search operation is successful, the switch will return the Forwarding Group in this. If the search fails, this field doesn't mean anything. |
| Output Port[4:0]/ Multicast Index[4:0] | After the search operation is successful, the switch will return output port / multicast index in this field. The users could use the entry_state[1] returned to distinguish if the entry should point to the multicast output port map table. |
| Occupy | After the search is successful, the switch will return the value indicating if the entry existed. 0 _B , The searched entry doesn't exist. 1 _B , The searched entry exists. |
| Entry State[0] | After the search is successful, the switch will return the value in this field indicating if value is static. 0 _B , The searched entry is not static and will be aged. 1 _B , The searched entry is static. |
| Entry State[1] | After the search is successful, the switch will return the value in this field indicating if the entry points to the multicast output port map table. 0 _B , The entry doesn't point to the multicast output port map table. 1 _B , The entry points to the multicast output port map table. |
| Bad State | After the search is successful, the switch will return the value indicating if the entry is bad. 0 _B , The entry is not bad and will be used for data storage. 1 _B , The entry is bad and isn't used for data storage. |
| Command Result[2:0] | This field indicates the access result. 000 _B , Command OK. 001 _B , All Entry Used. This result happens only for the create operation. ADM6918/X uses the 4-way address lookup engine so it allows 4 different addresses stored at each hash location. If these 4 entries are all static, then CPU will not successfully create 5th different address hashed to the same location and 001 will be returned. The only way to create 5th different address is to remove one of early addresses. 010 _B , Entry Not Found. 011 _B , Try Next Entry. 101 _B , Command Error. |
| Busy | This bit indicates if the table engine for access is available. 0 _B , The engine is available. 1 _B , The engine is busy and it will not access the command from the CPU. |

2. Rules to Access the Address Table

1. Check the Busy Bit in the status register to see if the access engine is available. If the engine is busy, wait until the engine is free. If the engine is available, go to the following step.
2. Write the MAC address[31:0] into the control register 0.
3. Write the MAC address[47:32], Forwarding Group, Output Port/Multicast Index, Control Field and the Entry State into the control register 1.
4. Write the Command into the control register 2 to define the operation.
5. Wait for the engine to complete (Check the Busy Bit).

6. Read the desired result returned in the status register.

Note: Before the “Search command”, the CPU should execute the “Initial command” to initial the search pointer. The search engine could search the aim from the top to the bottom. The search engine has an ability to automatically move the pointer to the associated location (The result will be returned). Because more than one entry may match the searching condition (by port, by address, etc.) at the same time, the CPU should continue to restart the search engine until the Command Result = Entry Not is found to confirm that no other matching entries exist.

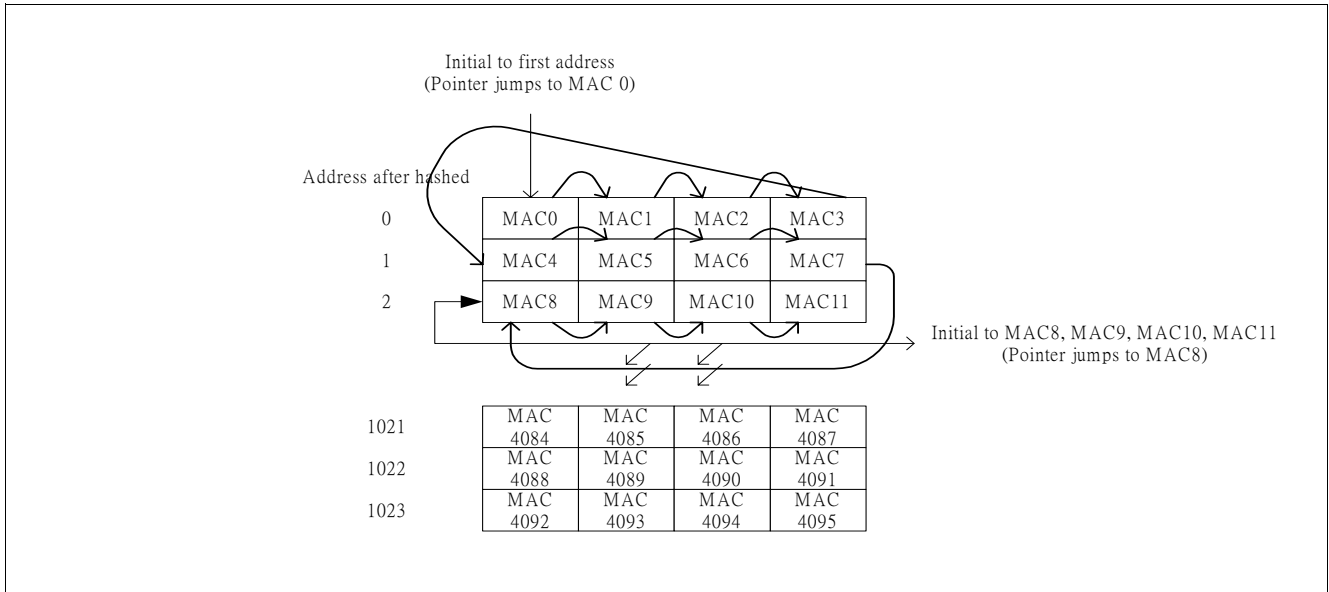


Figure 11 The Search Pointer

3. Example

Table 34 Example

| Example | Step |
|---|---|
| The user needs ADM6918/X to forward the specified unicast packet (DA = 0012_3456_789A _H and Forwarding Group = 2) to port 3 forever. | <p>Step 1: Check the Busy bit. If Busy = 0_B, go to the step 2. If Busy = 1_B, wait.</p> <p>Step 2: Write 3456_789A_H into control register 0.</p> <p>Step 3: Write 5C62_0012_H into the control register 1.</p> <p>Step 4: Write 0000_0000_H into the control register 2 to start the “Create” operation.</p> <p>Step 5: Read the status register 2 to check the busy bit. If Busy = 0_B, check the Command Result to see if the create operation is successful. If Busy = 1_B, wait for completion.</p> |

Table 34 Example (cont'd)

| Example | Step |
|--|---|
| The user needs the ADM6918/X to forward the specified multicast packet (DA = 0123_4567_89AB _H and Forwarding Group = 3) to port 5 only. This address could be aged. | <p>Step 1: Check the Busy bit. If Busy = 0_B, go to the step 2. If Busy = 1_B, wait.</p> <p>Step 2: Write 4567_89AB_H into control register 0.</p> <p>Step 3: Write 1CA3_0123_H into the control register 1.</p> <p>Step 4: Write 0000_0000_H into the control register 2 to start the “Create” operation.</p> <p>Step 5: Read the status register 2 to check the busy bit. If Busy = 0_B, check the Command Result to see if the create operation is successful. If Busy = 1_B, wait for completion.</p> |
| The user wants to know how many stations attached to port 4. | <p>Step 1: Check the Busy bit. If Busy = 0_B, go to the step 2. If Busy = 1_B, wait.</p> <p>Step 2: Write 0000_0000_H into control register 1.</p> <p>Step 3: Write 0000_0003_H into control register 2 to start the “Initial to the first address” operation.</p> <p>Step 4: Read the status register 2 to check the busy bit. If Busy = 0_B, check the Command Result to see if the initial operation is successful. If Busy = 1_B, wait for completion.</p> <p>Step 5: Write 2480_0000_H into control register 1.</p> <p>Step 6: Write 0000_0002_H into control register 2 to start the “Search by port” operation.</p> <p>Step 7: Read the status register 2 to check the busy bit. If Busy = 0_B, check the Command Result to see if the search operation is successful (the Mac address attached to port 4 could be derived from the MAC address in the status register). If Busy = 1_B, wait for completion.</p> <p>Step 8: If Command Result = “Command OK”, it means some other MAC addresses attached to port 4 may exist. We should restart the “Search by port” command again to let the search engine to look another addresses.</p> <p>Step 9: If the Command Result = “Entry Not Found”, it means no other addresses attached to port 4 exist.</p> |

Control and Status Register for the Multicast Output Port Map Table

1. The Control and Status Register Descriptions

Table 35 Control Register Description

| Command Field | Multicast Index | Output Port Map |
|----------------|------------------|-----------------|
| Control_2[2:0] | Control_0[30:26] | Control_0[25:0] |

Table 36 Field Description in the Control Register

| Field | Description |
|-----------------|--|
| Output Port Map | This field describes the output ports associated with the multicast index. Bit [0] is for port 0, Bit[1] is for port 1, ... and Bit[25] for port 25. |
| Multicast Index | refer to Figure 12 . |
| Command Field | 100 _B , Create an entry in the output port map table (indexed by the Multicast Index). 101 _B , Search an entry in the output port map table (indexed by the Multicast Index). |

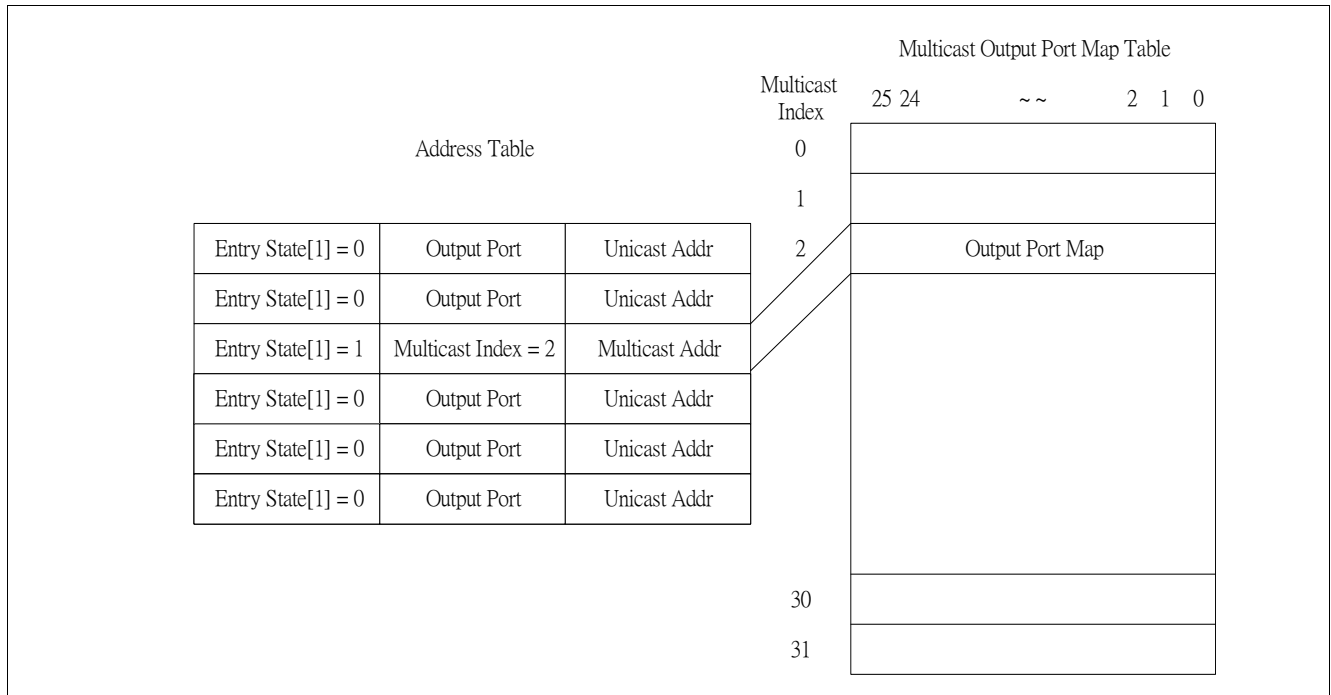


Figure 12 Address Table Mapping to Output Port MAP

Table 37 Status Register Description

| Busy | Command Result | Output Port Map |
|-------------|----------------|-----------------|
| Status_2[3] | Status_2[2:0] | Status_0[25:0] |

Table 38 Field Description in the Status Register

| Field | Description |
|-----------------|---|
| Output Port Map | The content associated with the multicast index will be here after searching. |
| Command Result | 000 _B = Command OK |
| Busy | This bit indicates if the output port map engine is available. 0 _B , The engine is available. 1 _B , The engine is busy and it will not access the command from the CPU. |

2. Rules to Access the Multicast Output Port Map Table

1. Check the Busy Bit to see if the access engine is available. If the engine is busy, wait until the engine is free. If the engine is available, go to the following step.
2. Write output port map and the multicast index into the control register 0.
3. Write the command into the control register 2.
4. Read the Busy Bit. If Busy = 1_B, wait. If Busy = 0_B, the operation completes.

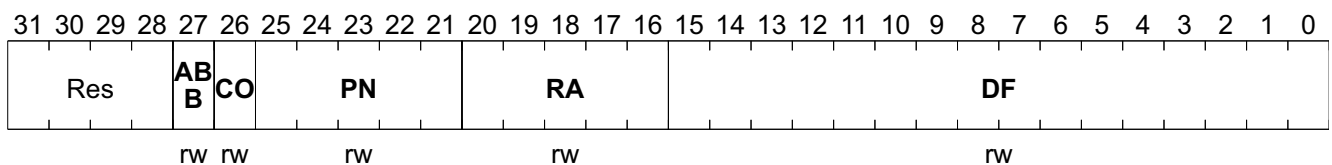
3. Example

Table 39 Example

| Example | Step |
|---|---|
| The user needs the ADM6918/X to forward the specified multicast packet (DA = 0123_4567_89AB _H and Forwarding Group = 3) to port 1, port2 and port 25. This address could be aged. We assume the CPU wants to write output port map into index 1. | <p>Step 1: Check the Busy bit. If Busy = 0_B, go to the step 2. If Busy = 1_B, wait.</p> <p>Step 2: Write 0060_0006_H into control register 0.</p> <p>Step 3: Write 0000_0004_H into control register 2 start the “Write” command.</p> <p>Step 4: Check the Busy bit. If Busy = 1_B, wait. If Busy = 1_B, go to the next step.</p> <p>Step 5: Write 4567_89AB_H into control register 0.</p> <p>Step 6: Write 9c23_0123_H into the control register 1.</p> <p>Step 7: Write 0000_0000_H into the control register 2 to start the “Create” operation.</p> <p>Step 8: Read the status register 2 to check the busy bit. If Busy = 0_B, check the Command Result to see if the create operation is successful. If Busy = 1_B, wait for completion.</p> |

PHY Control Register

| | | |
|-----------------------------|-----------------------|------------------------------|
| PHYCR | Offset | Reset Value |
| PHY Control Register | 0B_H | 0000 0000_H |



| Field | Bits | Type | Description |
|-------|-------|------|--|
| ABB | 27 | rw | Access (Busy) Bit |
| CO | 26 | rw | Command Option 0 _B , Write 1 _B , Read |
| PN | 25:21 | rw | Port Number |
| RA | 20:16 | rw | Register Address |
| DF | 15:0 | rw | Data Field This field indicates the data for reading or writing. |

Notes

1. This register allows the user to control the PHY attached through the CUP's help.
2. Rule for Read Operation:
 - Step 1: Poll the Busy bit (Bit[27]) to check if the PHY control module is busy.
 - Step 2: Write the port number (Bit[25:21]), register address (Bit[20:16]), command (Bit[26]) and Access

Switch Register Map

bit(Bit[27]) to start the read operation.

Step 3: Poll the Busy bit (Bit[27]). If Busy = 1_B, wait. If Busy = 0_B, data is returned in the data field.

3. Rule for Write Operation:

Step 1: Poll the Busy bit (Bit[27]) to check if the PHY control module is busy.

Step 2: Write the port number (Bit[25:21]), register address (Bit[20:16]), command (Bit[26]), data field (Bit[15:0]) and Access bit(Bit[27]) to start the write operation.

Step 3: Poll the Busy bit (Bit[27]). If Busy = 1_B, wait. If Busy = 0_B, writing operation completes.

4. Example: The user wants to read the Basic Control Register in Port 1.

Step 1: Read Bit[27] to check if PHY module is in progress.

Step 2: If Bit[27] = 0_B, write Bit[27] = 1_B, Bit[26] = 1_B, Bit[25:21] = 5'h1 and Bit[20:16] = 5'h0.

Step 3: Poll the Busy bit. If Bit[27] = 0_B, data is returned in the data field. If Bit[27] = 1_B, wait.

Hardware Status

The Reset Value is done by hardware setting.

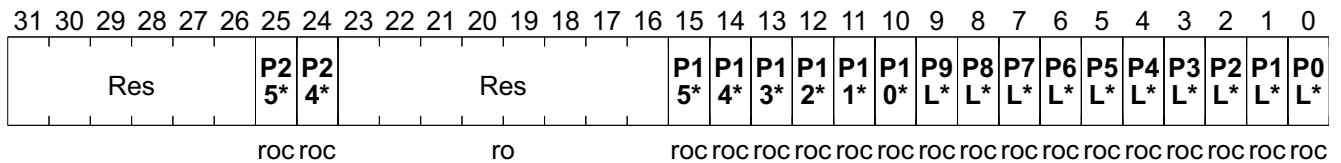
| HS | Offset | Reset Value |
|-----------------|-----------------|-------------------------------|
| Hardware Status | 0D _H | Hardware Setting _H |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|----------|-------------|----|----------|---------|---------|---------|----|---|--|--|--|--|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Res | | | | | | | | | | | | | | | | | | | | | | | BR M* | P24 25OM | TE | IP G* | FC E | BP E | AN E | AD | | | | | | | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|----------|------|------|---|
| BRMII | 8 | ro | Bond RMII (SS-SMII or Pure RMII Mode) 0 _B , The switch is in SS-SMII package. 1 _B , The switch is in RMII package. |
| P24_25OM | 7:6 | ro | Port 24 or Port 25 Operate in RMII or MII Mode 00 _B , Port 24 and Port 25 are both configured to MII mode. 01 _B , Port 24 is configured to RMII; Port 25 is configured to MII. 10 _B , Port 24 is configured to MII; Port 25 is configured to RMII. 11 _B , Port 24 and Port 25 are both configured to RMII. |
| TE | 5 | ro | Trunking Enable From Hardware 0 _B , Trunking Disable. 1 _B , Trunking Enable. |
| IPG92TE | 4 | ro | IPG 92 Bit Time Enable From Hardware Pin 0 _B , IPG 92 Disable. 1 _B , IPG 92 Enable. |
| FCE | 3 | ro | Flow Control Enable For Full Duplex From Hardware Pin 0 _B , Flow Control Disable. 1 _B , Flow Control Enable. |
| BPE | 2 | ro | Back Pressure Enable From Hardware Pin 0 _B , Back Pressure Disable. 1 _B , Back Pressure Enable. |
| ANE | 1 | ro | Auto-Negotiation Enable From Hardware Pin 0 _B , Auto-Negotiation Disable. 1 _B , Auto-Negotiation Enable. |

Switch Register Map

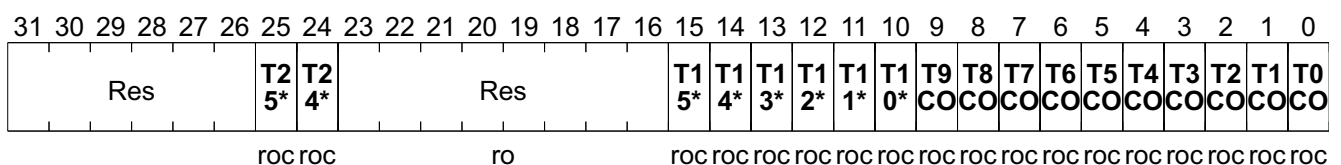
RPLCO **Offset** **Reset Value**
Receive Packet Length Count Overflow **0F_H** **0000 0000_H**



| Field | Bits | Type | Description |
|--------|-------|------|---|
| P25LCO | 25 | roc | Port 25 Receive Packet Length Count Overflow |
| P24LCO | 24 | roc | Port 24 Receive Packet Length Count Overflow |
| Res | 23:16 | ro | Reserved |
| P15LCO | 15 | roc | Port 15 Receive Packet Length Count Overflow |
| P14LCO | 14 | roc | Port 14 Receive Packet Length Count Overflow |
| P13LCO | 13 | roc | Port 13 Receive Packet Length Count Overflow |
| P12LCO | 12 | roc | Port 12 Receive Packet Length Count Overflow |
| P11LCO | 11 | roc | Port 11 Receive Packet Length Count Overflow |
| P10LCO | 10 | roc | Port 10 Receive Packet Length Count Overflow |
| P9LCO | 9 | roc | Port 9 Receive Packet Length Count Overflow |
| P8LCO | 8 | roc | Port 8 Receive Packet Length Count Overflow |
| P7LCO | 7 | roc | Port 7 Receive Packet Length Count Overflow |
| P6LCO | 6 | roc | Port 6 Receive Packet Length Count Overflow |
| P5LCO | 5 | roc | Port 5 Receive Packet Length Count Overflow |
| P4LCO | 4 | roc | Port 4 Receive Packet Length Count Overflow |
| P3LCO | 3 | roc | Port 3 Receive Packet Length Count Overflow |
| P2LCO | 2 | roc | Port 2 Receive Packet Length Count Overflow |
| P1LCO | 1 | roc | Port 1 Receive Packet Length Count Overflow |
| P0LCO | 0 | roc | Port 0 Receive Packet Length Count Overflow _{1B} , Receive packet length count in port 0 overflows and it will be cleared after read from CPU. |

Transmit Packet Count Overflow

TPCO **Offset** **Reset Value**
Transmit Packet Count Overflow **10_H** **0000 0000_H**



Switch Register Map

| Field | Bits | Type | Description |
|-------|-------|------|---|
| T25CO | 25 | roc | Port 25 Transmit Packet Count Overflow |
| T24CO | 24 | roc | Port 24 Transmit Packet Count Overflow |
| Res | 23:16 | ro | Reserved |
| T15CO | 15 | roc | Port 15 Transmit Packet Count Overflow |
| T14CO | 14 | roc | Port 14 Transmit Packet Count Overflow |
| T13CO | 13 | roc | Port 13 Transmit Packet Count Overflow |
| T12CO | 12 | roc | Port 12 Transmit Packet Count Overflow |
| T11CO | 11 | roc | Port 11 Transmit Packet Count Overflow |
| T10CO | 10 | roc | Port 10 Transmit Packet Count Overflow |
| T9CO | 9 | roc | Port 9 Transmit Packet Count Overflow |
| T8CO | 8 | roc | Port 8 Transmit Packet Count Overflow |
| T7CO | 7 | roc | Port 7 Transmit Packet Count Overflow |
| T6CO | 6 | roc | Port 6 Transmit Packet Count Overflow |
| T5CO | 5 | roc | Port 5 Transmit Packet Count Overflow |
| T4CO | 4 | roc | Port 4 Transmit Packet Count Overflow |
| T3CO | 3 | roc | Port 3 Transmit Packet Count Overflow |
| T2CO | 2 | roc | Port 2 Transmit Packet Count Overflow |
| T1CO | 1 | roc | Port 1 Transmit Packet Count Overflow |
| T0CO | 0 | roc | Port 0 Transmit Packet Count Overflow 1 _B , Transmit packet count in port 0 overflows and it will be cleared after read from CPU. |

Transmit Packet Length Count Overflow

| | | |
|---------------------------------------|-----------------|------------------------|
| TPLCO | Offset | Reset Value |
| Transmit Packet Length Count Overflow | 11 _H | 0000 0000 _H |

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----|----|----|----|----|----|----------|----------|-----|----|----|----|----|----|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|-----|-----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | | | T2 5* | T2 4* | Res | | | | | | T1 5* | T1 4* | T1 3* | T1 2* | T1 1* | T1 0* | T9 L* | T8 L* | T7 L* | T6 L* | T5 L* | T4 L* | T3 L* | T2 L* | T1 L* | T0 L* | | |
| | | | | | | roc | roc | | | | | | | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc |

| Field | Bits | Type | Description |
|--------|-------|------|---|
| T25LCO | 25 | roc | Port 25 Transmit Packet Length Count Overflow |
| T24LCO | 24 | roc | Port 24 Transmit Packet Length Count Overflow |
| Res | 23:16 | ro | Reserved |
| T15LCO | 15 | roc | Port 15 Transmit Packet Length Count Overflow |
| T14LCO | 14 | roc | Port 14 Transmit Packet Length Count Overflow |
| T13LCO | 13 | roc | Port 13 Transmit Packet Length Count Overflow |
| T12LCO | 12 | roc | Port 12 Transmit Packet Length Count Overflow |

Switch Register Map

| Field | Bits | Type | Description |
|--------|------|------|--|
| T11LCO | 11 | roc | Port 11 Transmit Packet Length Count Overflow |
| T10LCO | 10 | roc | Port 10 Transmit Packet Length Count Overflow |
| T9LCO | 9 | roc | Port 9 Transmit Packet Length Count Overflow |
| T8LCO | 8 | roc | Port 8 Transmit Packet Length Count Overflow |
| T7LCO | 7 | roc | Port 7 Transmit Packet Length Count Overflow |
| T6LCO | 6 | roc | Port 6 Transmit Packet Length Count Overflow |
| T5LCO | 5 | roc | Port 5 Transmit Packet Length Count Overflow |
| T4LCO | 4 | roc | Port 4 Transmit Packet Length Count Overflow |
| T3LCO | 3 | roc | Port 3 Transmit Packet Length Count Overflow |
| T2LCO | 2 | roc | Port 2 Transmit Packet Length Count Overflow |
| T1LCO | 1 | roc | Port 1 Transmit Packet Length Count Overflow |
| T0LCO | 0 | roc | Port 0 Transmit Packet Length Count Overflow 1 _B , Transmit packet length count in port 0 overflows and it will be cleared after read from CPU. |

Error Count Overflow

| | | |
|-----------------------------|-----------------------|------------------------------|
| ECO | Offset | Reset Value |
| Error Count Overflow | 12_H | 0000 0000_H |

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----|----|----|----|----|----|----------|----------|-----|----|----|----|----|----|----|----|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|-----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Res | | | | | | P2 5* | P2 4* | Res | | | | | | | | P1 5* | P1 4* | P1 3* | P1 2* | P1 1* | P1 0* | P9 E* | P8 E* | P7 E* | P6 E* | P5 E* | P4 E* | P3 E* | P2 E* | P1 E* | P0 E* | |
| | | | | | | roc | roc | ro | | | | | | | | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc | roc |

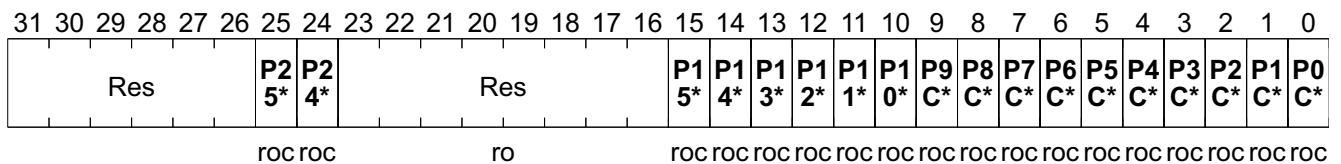
| Field | Bits | Type | Description |
|--------|-------|------|-------------------------------------|
| P25ECO | 25 | roc | Port 25 Error Count Overflow |
| P24ECO | 24 | roc | Port 24 Error Count Overflow |
| Res | 23:16 | ro | Reserved |
| P15ECO | 15 | roc | Port 15 Error Count Overflow |
| P14ECO | 14 | roc | Port 14 Error Count Overflow |
| P13ECO | 13 | roc | Port 13 Error Count Overflow |
| P12ECO | 12 | roc | Port 12 Error Count Overflow |
| P11ECO | 11 | roc | Port 11 Error Count Overflow |
| P10ECO | 10 | roc | Port 10 Error Count Overflow |
| P9ECO | 9 | roc | Port 9 Error Count Overflow |
| P8ECO | 8 | roc | Port 8 Error Count Overflow |
| P7ECO | 7 | roc | Port 7 Error Count Overflow |
| P6ECO | 6 | roc | Port 6 Error Count Overflow |
| P5ECO | 5 | roc | Port 5 Error Count Overflow |
| P4ECO | 4 | roc | Port 4 Error Count Overflow |

Switch Register Map

| Field | Bits | Type | Description |
|-------|------|------|--|
| P3ECO | 3 | roc | Port 3 Error Count Overflow |
| P2ECO | 2 | roc | Port 2 Error Count Overflow |
| P1ECO | 1 | roc | Port 1 Error Count Overflow |
| P0ECO | 0 | roc | Port 0 Error Count Overflow 1 _B , Error count in port 0 overflows and it will be cleared after read from CPU. |

Collision Count Overflow

| | | |
|---------------------------------|-----------------------|------------------------------|
| CCO | Offset | Reset Value |
| Collision Count Overflow | 13_H | 0000 0000_H |

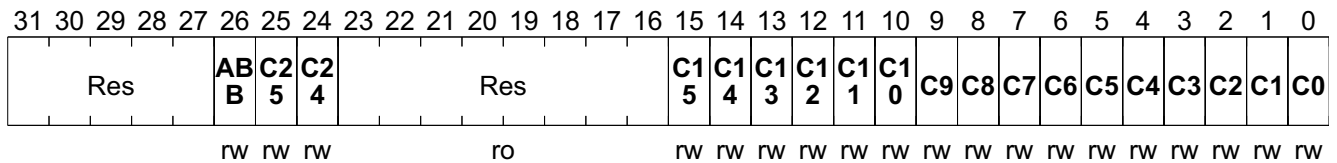


| Field | Bits | Type | Description |
|--------|-------|------|--|
| P25CCO | 25 | roc | Port 25 Collision Count Overflow |
| P24CCO | 24 | roc | Port 24 Collision Count Overflow |
| Res | 23:16 | ro | Reserved |
| P15CCO | 15 | roc | Port 15 Collision Count Overflow |
| P14CCO | 14 | roc | Port 14 Collision Count Overflow |
| P13CCO | 13 | roc | Port 13 Collision Count Overflow |
| P12CCO | 12 | roc | Port 12 Collision Count Overflow |
| P11CCO | 11 | roc | Port 11 Collision Count Overflow |
| P10CCO | 10 | roc | Port 10 Collision Count Overflow |
| P9CCO | 9 | roc | Port 9 Collision Count Overflow |
| P8CCO | 8 | roc | Port 8 Collision Count Overflow |
| P7CCO | 7 | roc | Port 7 Collision Count Overflow |
| P6CCO | 6 | roc | Port 6 Collision Count Overflow |
| P5CCO | 5 | roc | Port 5 Collision Count Overflow |
| P4CCO | 4 | roc | Port 4 Collision Count Overflow |
| P3CCO | 3 | roc | Port 3 Collision Count Overflow |
| P2CCO | 2 | roc | Port 2 Collision Count Overflow |
| P1CCO | 1 | roc | Port 1 Collision Count Overflow |
| P0CCO | 0 | roc | Port 0 Collision Count Overflow 1 _B , Collision Count in port 0 overflows and it will be cleared after read from CPU. |

Renew Counter Register

Switch Register Map

RCR **Offset** **Reset Value**
Renew Counter Register **14_H** **0000 0000_H**



| Field | Bits | Type | Description |
|-------|-------|------|---|
| ABB | 26 | rw | Access (Busy) Bit |
| C25 | 25 | rw | Counter Port 25 1 _B , Clear Port 25 Corresponding Counters |
| C24 | 24 | rw | Counter Port 24 1 _B , Clear Port 24 Corresponding Counters |
| Res | 23:16 | ro | Reserved |
| C15 | 15 | rw | Counter Port 15 1 _B , Clear Port 15 Corresponding Counters |
| C14 | 14 | rw | Counter Port 14 1 _B , Clear Port 14 Corresponding Counters |
| C13 | 13 | rw | Counter Port 13 1 _B , Clear Port 13 Corresponding Counters |
| C12 | 12 | rw | Counter Port 12 1 _B , Clear Port 12 Corresponding Counters |
| C11 | 11 | rw | Counter Port 11 1 _B , Clear Port 11 Corresponding Counters |
| C10 | 10 | rw | Counter Port 10 1 _B , Clear Port 10 Corresponding Counters |
| C9 | 9 | rw | Counter Port 9 1 _B , Clear Port 9 Corresponding Counters |
| C8 | 8 | rw | Counter Port 8 1 _B , Clear Port 8 Corresponding Counters |
| C7 | 7 | rw | Counter Port 7 1 _B , Clear Port 7 Corresponding Counters |
| C6 | 6 | rw | Counter Port 6 1 _B , Clear Port 6 Corresponding Counters |
| C5 | 5 | rw | Counter Port 5 1 _B , Clear Port 5 Corresponding Counters |
| C4 | 4 | rw | Counter Port 4 1 _B , Clear Port 4 Corresponding Counters |
| C3 | 3 | rw | Counter Port 3 1 _B , Clear Port 3 Corresponding Counters |
| C2 | 2 | rw | Counter Port 2 1 _B , Clear Port 2 Corresponding Counters |

Switch Register Map

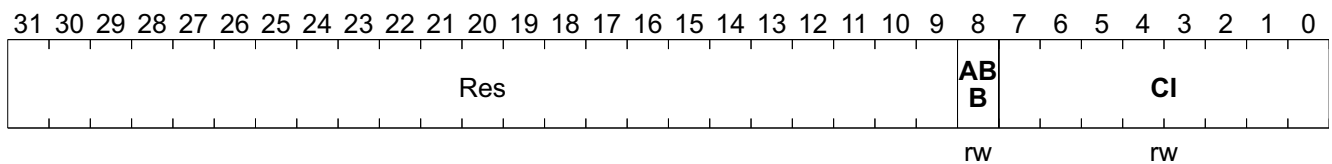
| Field | Bits | Type | Description |
|-------|------|------|---|
| C1 | 1 | rw | Counter Port 1 1 _B , Clear Port 1 Corresponding Counters |
| C0 | 0 | rw | Counter Port 0 1 _B , Clear Port 0 Corresponding Counters |

Notes

- This register allows the user to reset all counters for the corresponding port. If the renew counter module is busy all other modules about counters are not accessible.
- Rule:
 - Step 1: Poll the busy bit to check if the renew counter module is busy.
 - Step 2: If the renew counter module is available, write the port (Bit[25:0]) the user wants to reset and the busy bit(Bit[26]) to 1.
 - Step 3: Poll the busy bit to check if the renew counter module completes the job.
- Example:
 - Users want to reset P0, P1, P2, P3 corresponding counters.
 - Step 1: Read Bit[26] to check if reset is in progress.
 - Step 2: If Bit[26] = 0, write Bit[26] = 1_B, Bit[25:0] = 00_0000_0000_0000_0000_0000_1111_B into the register.
 - Step 3: Poll the busy bit to check if reset completes.

Read Counter Control Register

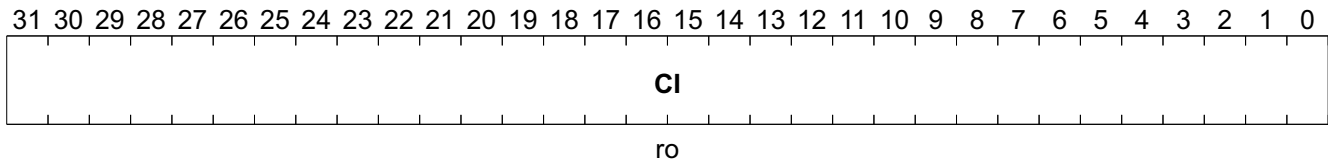
| | | |
|--------------------------------------|-----------------------|------------------------------|
| RCCR | Offset | Reset Value |
| Read Counter Control Register | 15_H | 0000_0000_H |



| Field | Bits | Type | Description |
|-------|------|------|--------------------------|
| ABB | 8 | rw | Access (Busy) Bit |
| CI | 7:0 | rw | Counter Index |

Read Counter Status Register

| | | |
|-------------------------------------|-----------------------|------------------------------|
| RCSR | Offset | Reset Value |
| Read Counter Status Register | 16_H | 0000 0000_H |

Switch Register Map


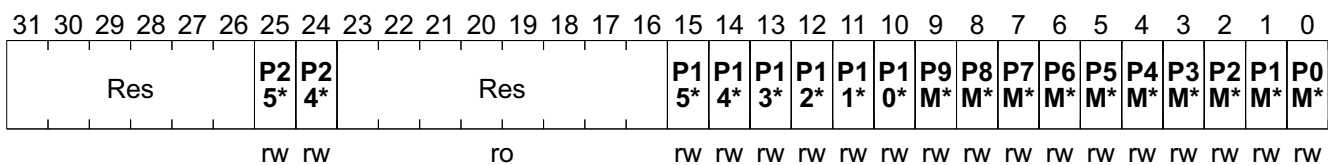
| Field | Bits | Type | Description |
|-------|------|------|---|
| CI | 31:0 | ro | Counter Index The corresponding counter index by the Bit[7:0] is returned here. |

Notes

1. The Read Counter Control Register and the Read Counter Status Register provide users to read counter if he wants to use fast management clock (fast than 5 MHz).
2. Rules:
 - Step 1: Read the Busy bit to check if the read counter module is busy
 - Step 2: If the module is free, write the counter index and access bit into the control register
 - Step 3: Poll the Busy bit. If Busy = 1_B, wait. If Busy = 0_B read the status register
3. Example: Users want to read Port 1 Receive Packet Count
 - Step 1: Read Bit[8] to check if the read counter module is busy
 - Step 3: Then Port 1 Receive Packet Count will be loaded into the Counter Status Register (Offset: 16_H)
 - Step 2: If Bit[8] = 0, then write bit[8] = 1_B, Bit[7:0] = 8'b1 into the register
 - Step 4: Read Counter Status Register (Offset: 16_H) and the content read is the Port 1 Receive Packet Count

Reload MDIO Register

| | | |
|-----------------------------|-----------------------|------------------------------|
| RMDIOR | Offset | Reset Value |
| Reload MDIO Register | 17_H | 0000 0000_H |



| Field | Bits | Type | Description |
|---------|-------|------|-------------------------------------|
| P25MDIO | 25 | rw | Port 25 MDIO Register Reload |
| P24MDIO | 24 | rw | Port 24 MDIO Register Reload |
| Res | 23:16 | ro | Reserved |
| P15MDIO | 15 | rw | Port 15 MDIO Register Reload |
| P14MDIO | 14 | rw | Port 14 MDIO Register Reload |
| P13MDIO | 13 | rw | Port 13 MDIO Register Reload |
| P12MDIO | 12 | rw | Port 12 MDIO Register Reload |
| P11MDIO | 11 | rw | Port 11 MDIO Register Reload |

Switch Register Map

| Field | Bits | Type | Description |
|---------|------|------|--|
| P10MDIO | 10 | rw | Port 10 MDIO Register Reload |
| P9MDIO | 9 | rw | Port 9 MDIO Register Reload |
| P8MDIO | 8 | rw | Port 8 MDIO Register Reload |
| P7MDIO | 7 | rw | Port 7 MDIO Register Reload |
| P6MDIO | 6 | rw | Port 6 MDIO Register Reload |
| P5MDIO | 5 | rw | Port 5 MDIO Register Reload |
| P4MDIO | 4 | rw | Port 4 MDIO Register Reload |
| P3MDIO | 3 | rw | Port 3 MDIO Register Reload |
| P2MDIO | 2 | rw | Port 2 MDIO Register Reload |
| P1MDIO | 1 | rw | Port 1 MDIO Register Reload |
| P0MDIO | 0 | rw | Port 0 MDIO Register Reload 1 _B , Status of Port 0 PHY attached will be reloaded and updated to the switch. After PHY is reloaded, Bit[0] will be cleared. |

Spanning Tree Port State 0

| | | |
|-----------------------------------|-----------------------|------------------------------|
| STPS0 | Offset | Reset Value |
| Spanning Tree Port State 0 | 18_H | 0000 0000_H |

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| P15S TPS | P14S TPS | P13S TPS | P12S TPS | P11S TPS | P10S TPS | P9ST PS | P8ST PS | P7ST PS | P6ST PS | P5ST PS | P4ST PS | P3ST PS | P2ST PS | P1ST PS | P0ST PS | | | | | | | | | | | | | | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---------|-------|------|-----------------------------------|
| P15STPS | 31:30 | rw | Port 15 Spanning Tree Port Status |
| P14STPS | 29:28 | rw | Port 14 Spanning Tree Port Status |
| P13STPS | 27:26 | rw | Port 13 Spanning Tree Port Status |
| P12STPS | 25:24 | rw | Port 12 Spanning Tree Port Status |
| P11STPS | 23:22 | rw | Port 11 Spanning Tree Port Status |
| P10STPS | 21:20 | rw | Port 10 Spanning Tree Port Status |
| P9STPS | 19:18 | rw | Port 9 Spanning Tree Port Status |
| P8STPS | 17:16 | rw | Port 8 Spanning Tree Port Status |
| P7STPS | 15:14 | rw | Port 7 Spanning Tree Port Status |
| P6STPS | 13:12 | rw | Port 6 Spanning Tree Port Status |
| P5STPS | 11:10 | rw | Port 5 Spanning Tree Port Status |
| P4STPS | 9:8 | rw | Port 4 Spanning Tree Port Status |
| P3STPS | 7:6 | rw | Port 3 Spanning Tree Port Status |
| P2STPS | 5:4 | rw | Port 2 Spanning Tree Port Status |
| P1STPS | 3:2 | rw | Port 1 Spanning Tree Port Status |
| P0STPS | 1:0 | rw | Port 0 Spanning Tree Port Status |

Note: The ADM6918/X supports 4 port status to support Spanning Tree

Protocol.

00_B = Forwarding State. The port acts as the normal

mode.

01_B = Disabled State. The port entity will not transmit

and receive any packets. Learning is disabled in this

state.

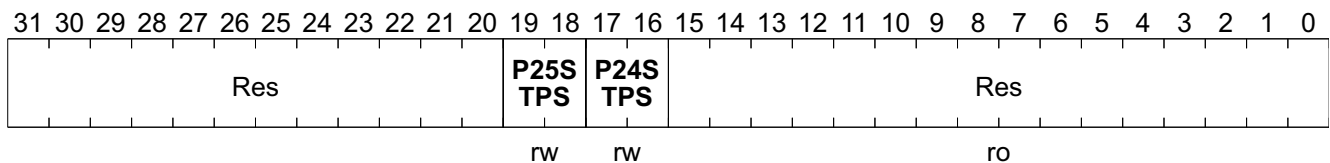
10_B = Learning State. The port entity will only transmit and receive management packets. All other packets are discarded. Learning is enabled for all good frames.

11_B = Blocking-not-Listening. Only the management packets defined by the ADM6918/X will be received and transmitted.

All other packets are discarded by the port entity. Learning is disabled in this state.

Spanning Tree Port State 1

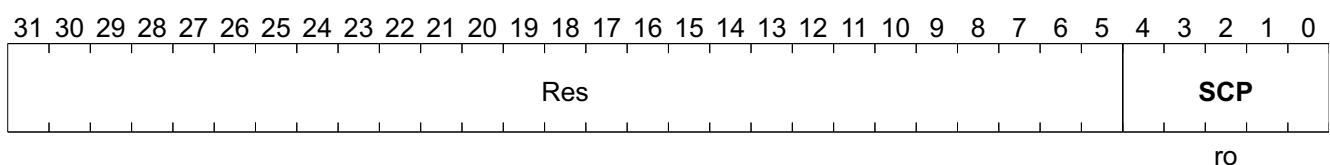
STPS1 **Offset** **Reset Value**
Spanning Tree Port State 1 **19_H** **0000 0000_H**



| Field | Bits | Type | Description |
|---------|-------|------|--|
| P25STPS | 19:18 | rw | Port 25 Spanning Tree Port Status |
| P24STPS | 17:16 | rw | Port 24 Spanning Tree Port Status |
| Res | 15:0 | ro | Reserved |

Source Port Register

SCPR **Offset** **Reset Value**
Source Port Register **1A_H** **0000_0000_H**

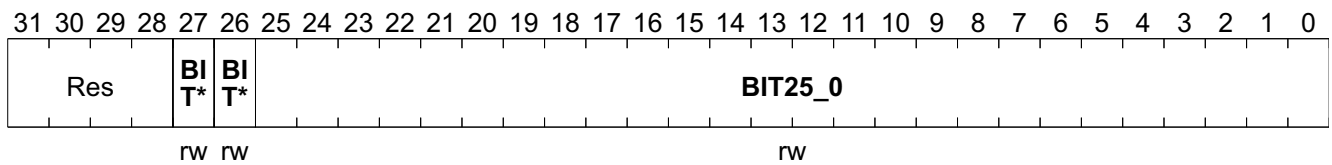


| Field | Bits | Type | Description |
|-------|------|------|--|
| SCP | 4:0 | ro | The Source Port The CPU can read this register to get the source port when he receives a packet. |

Note: The value will be correct after the SA is transmitted.

Transmit Port Register

TRPR **Offset**
Transmit Port Register **1B_H** **Reset Value**
0000 0000_H



| Field | Bits | Type | Description |
|---------|------|------|---|
| BIT27 | 27 | rw | Bit 27 0 _B , The command is not valid. 1 _B , The command is valid. |
| BIT26 | 26 | rw | Bit 26 The destination ports is more than 1 |
| BIT25_0 | 25:0 | rw | Bit 25_0 The destination ports the CPU wants to forward. |

Note: The value should be written before CPU transmits a packet.

Counter Register

Offset **0100_H ~ 019B_H**

Table 40 Counter Register: Offset 0100_H ~ 0167_H

| Offset Hex | Index | Description | Offset Hex | Index | Description |
|--------------------------|-------|-----------------------------|------------|-------|------------------------------------|
| The Receive Count | | | | | |
| 0100 | 0 | Port 0 Receive Packet Count | 011A | 1A | Port 0 Receive Packet Length Count |
| 0101 | 1 | Port 1 Receive Packet Count | 011B | 1B | Port 1 Receive Packet Length Count |
| 0102 | 2 | Port 2 Receive Packet Count | 011C | 1C | Port 2 Receive Packet Length Count |
| 0103 | 3 | Port 3 Receive Packet Count | 011D | 1D | Port 3 Receive Packet Length Count |
| 0104 | 4 | Port 4 Receive Packet Count | 011E | 1E | Port 4 Receive Packet Length Count |
| 0105 | 5 | Port 5 Receive Packet Count | 011F | 1F | Port 5 Receive Packet Length Count |

Table 40 Counter Register: Offset 0100_H ~ 0167_H (cont'd)

| Offset Hex | Index | Description | Offset Hex | Index | Description |
|---------------------------|-------|------------------------------|------------|-------|-------------------------------------|
| 0106 | 6 | Port 6 Receive Packet Count | 0120 | 20 | Port 6 Receive Packet Length Count |
| 0107 | 7 | Port 7 Receive Packet Count | 0121 | 21 | Port 7 Receive Packet Length Count |
| 0108 | 8 | Port 8 Receive Packet Count | 0122 | 22 | Port 8 Receive Packet Length Count |
| 0109 | 9 | Port 9 Receive Packet Count | 0123 | 23 | Port 9 Receive Packet Length Count |
| 010A | A | Port 10 Receive Packet Count | 0124 | 24 | Port 10 Receive Packet Length Count |
| 010B | B | Port 11 Receive Packet Count | 0125 | 25 | Port 11 Receive Packet Length Count |
| 010C | C | Port 12 Receive Packet Count | 0126 | 26 | Port 12 Receive Packet Length Count |
| 010D | D | Port 13 Receive Packet Count | 0127 | 27 | Port 13 Receive Packet Length Count |
| 010E | E | Port 14 Receive Packet Count | 0128 | 28 | Port 14 Receive Packet Length Count |
| 010F | F | Port 15 Receive Packet Count | 0129 | 29 | Port 15 Receive Packet Length Count |
| 0110 | 10 | Port 16 Receive Packet Count | 012A | 2A | Port 16 Receive Packet Length Count |
| 0111 | 11 | Port 17 Receive Packet Count | 012B | 2B | Port 17 Receive Packet Length Count |
| 0112 | 12 | Port 18 Receive Packet Count | 012C | 2C | Port 18 Receive Packet Length Count |
| 0113 | 13 | Port 19 Receive Packet Count | 012D | 2D | Port 19 Receive Packet Length Count |
| 0114 | 14 | Port 20 Receive Packet Count | 012E | 2E | Port 20 Receive Packet Length Count |
| 0115 | 15 | Port 21 Receive Packet Count | 012F | 2F | Port 21 Receive Packet Length Count |
| 0116 | 16 | Port 22 Receive Packet Count | 0130 | 30 | Port 22 Receive Packet Length Count |
| 0117 | 17 | Port 23 Receive Packet Count | 0131 | 31 | Port 23 Receive Packet Length Count |
| 0118 | 18 | Port 24 Receive Packet Count | 0132 | 32 | Port 24 Receive Packet Length Count |
| 0119 | 19 | Port 25 Receive Packet Count | 0133 | 33 | Port 25 Receive Packet Length Count |
| The Transmit Count | | | | | |
| 0134 | 34 | Port 0 Transmit Packet Count | 014E | 4E | Port 0 Transmit Packet Length Count |

Switch Register Map

Table 40 Counter Register: Offset 0100_H ~ 0167_H (cont'd)

| Offset Hex | Index | Description | Offset Hex | Index | Description |
|------------|-------|-------------------------------|------------|-------|--------------------------------------|
| 0135 | 35 | Port 1 Transmit Packet Count | 014F | 4F | Port 1 Transmit Packet Length Count |
| 0136 | 36 | Port 2 Transmit Packet Count | 0150 | 50 | Port 2 Transmit Packet Length Count |
| 0137 | 37 | Port 3 Transmit Packet Count | 0151 | 51 | Port 3 Transmit Packet Length Count |
| 0138 | 38 | Port 4 Transmit Packet Count | 0152 | 52 | Port 4 Transmit Packet Length Count |
| 0139 | 39 | Port 5 Transmit Packet Count | 0153 | 53 | Port 5 Transmit Packet Length Count |
| 013A | 3A | Port 6 Transmit Packet Count | 0154 | 54 | Port 6 Transmit Packet Length Count |
| 013B | 3B | Port 7 Transmit Packet Count | 0155 | 55 | Port 7 Transmit Packet Length Count |
| 013C | 3C | Port 8 Transmit Packet Count | 0156 | 56 | Port 8 Transmit Packet Length Count |
| 013D | 3D | Port 9 Transmit Packet Count | 0157 | 57 | Port 9 Transmit Packet Length Count |
| 013E | 3E | Port 10 Transmit Packet Count | 0158 | 58 | Port 10 Transmit Packet Length Count |
| 013F | 3F | Port 11 Transmit Packet Count | 0159 | 59 | Port 11 Transmit Packet Length Count |
| 0140 | 40 | Port 12 Transmit Packet Count | 015A | 5A | Port 12 Transmit Packet Length Count |
| 0141 | 41 | Port 13 Transmit Packet Count | 015B | 5B | Port 13 Transmit Packet Length Count |
| 0142 | 42 | Port 14 Transmit Packet Count | 015C | 5C | Port 14 Transmit Packet Length Count |
| 0143 | 43 | Port 15 Transmit Packet Count | 015D | 5D | Port 15 Transmit Packet Length Count |
| 0144 | 44 | Port 16 Transmit Packet Count | 015E | 5E | Port 16 Transmit Packet Length Count |
| 0145 | 45 | Port 17 Transmit Packet Count | 015F | 5F | Port 17 Transmit Packet Length Count |
| 0146 | 46 | Port 18 Transmit Packet Count | 0160 | 60 | Port 18 Transmit Packet Length Count |
| 0147 | 47 | Port 19 Transmit Packet Count | 0161 | 61 | Port 19 Transmit Packet Length Count |
| 0148 | 48 | Port 20 Transmit Packet Count | 0162 | 62 | Port 20 Transmit Packet Length Count |
| 0149 | 49 | Port 21 Transmit Packet Count | 0163 | 63 | Port 21 Transmit Packet Length Count |
| 014A | 4A | Port 22 Transmit Packet Count | 0164 | 64 | Port 22 Transmit Packet Length Count |

Table 40 Counter Register: Offset 0100_H ~ 0167_H (cont'd)

| Offset Hex | Index | Description | Offset Hex | Index | Description |
|------------|-------|-------------------------------|------------|-------|--------------------------------------|
| 014B | 4B | Port 23 Transmit Packet Count | 0165 | 65 | Port 23 Transmit Packet Length Count |
| 014C | 4C | Port 24 Transmit Packet Count | 0166 | 66 | Port 24 Transmit Packet Length Count |
| 014D | 4D | Port 25 Transmit Packet Count | 0167 | 67 | Port 25 Transmit Packet Length Count |

Error and Collision Count

| | | | | | |
|------|----|-----------------------------|------|----|-------------------------|
| 0168 | 68 | Port 0 Receive Error Count | 0182 | 82 | Port 0 Collision Count |
| 0169 | 69 | Port 1 Receive Error Count | 0183 | 83 | Port 1 Collision Count |
| 016A | 6A | Port 2 Receive Error Count | 0184 | 84 | Port 2 Collision Count |
| 016B | 6B | Port 3 Receive Error Count | 0185 | 85 | Port 3 Collision Count |
| 016C | 6C | Port 4 Receive Error Count | 0186 | 86 | Port 4 Collision Count |
| 016D | 6D | Port 5 Receive Error Count | 0187 | 87 | Port 5 Collision Count |
| 016E | 6E | Port 6 Receive Error Count | 0188 | 88 | Port 6 Collision Count |
| 016F | 6F | Port 7 Receive Error Count | 0189 | 89 | Port 7 Collision Count |
| 0170 | 70 | Port 8 Receive Error Count | 018A | 8A | Port 8 Collision Count |
| 0171 | 71 | Port 9 Receive Error Count | 018B | 8B | Port 9 Collision Count |
| 0172 | 72 | Port 10 Receive Error Count | 018C | 8C | Port 10 Collision Count |
| 0173 | 73 | Port 11 Receive Error Count | 018D | 8D | Port 11 Collision Count |
| 0174 | 74 | Port 12 Receive Error Count | 018E | 8E | Port 12 Collision Count |
| 0175 | 75 | Port 13 Receive Error Count | 018F | 8F | Port 13 Collision Count |
| 0176 | 76 | Port 14 Receive Error Count | 0190 | 90 | Port 14 Collision Count |
| 0177 | 77 | Port 15 Receive Error Count | 0191 | 91 | Port 15 Collision Count |
| 0178 | 78 | Port 16 Receive Error Count | 0192 | 92 | Port 16 Collision Count |
| 0179 | 79 | Port 17 Receive Error Count | 0193 | 93 | Port 17 Collision Count |
| 017A | 7A | Port 18 Receive Error Count | 0194 | 93 | Port 18 Collision Count |
| 017B | 7B | Port 19 Receive Error Count | 0195 | 95 | Port 19 Collision Count |
| 017C | 7C | Port 20 Receive Error Count | 0196 | 96 | Port 20 Collision Count |
| 017D | 7D | Port 21 Receive Error Count | 0197 | 97 | Port 21 Collision Count |
| 017E | 7E | Port 22 Receive Error Count | 0198 | 98 | Port 22 Collision Count |
| 017F | 7F | Port 23 Receive Error Count | 0199 | 99 | Port 23 Collision Count |
| 0180 | 80 | Port 24 Receive Error Count | 019A | 9A | Port 24 Collision Count |
| 0181 | 81 | Port 25 Receive Error Count | 019B | 9B | Port 25 Collision Count |

6 Electrical Specifications

6.1 DC Characteristics

6.1.1 Absolute Maximum Ratings

Table 41 Electrical Absolute Maximum Ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------|------------|--------|------|------------------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| 3.3 V Power Supply | V_{CCO} | 3.0 | – | 3.6 | V | – |
| 1.8 V Power Supply | V_{CCIK} | 1.71 | – | 1.89 | V | – |
| Input Voltage | V_{IN} | -0.3 | – | $V_{CC33} + 0.3$ | V | – |
| Output Voltage | V_{out} | -0.3 | – | $V_{CC33} + 0.3$ | V | – |
| Storage Temperature | T_{STG} | -55 | – | 155 | °C | – |
| Power Dissipation | P_D | – | – | 1.0 | W | – |
| ESD Rating | ESD | – | – | 3000 | V | – |

6.1.2 Recommended Operating Conditions

Table 42 Recommended Operating Conditions

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------|----------|--------|------|----------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Power Supply | V_{CC} | 3.135 | 3.3 | 3.465 | V | – |
| Input Voltage | V_{IN} | 0 | – | V_{CC} | V | – |
| Junction Operating Temperature | T_j | 0 | 25 | 115 | °C | – |

6.1.3 DC Electrical Characteristics for 3.3 V Operation

Under $V_{cc} = 3.0\text{ V} \sim 3.6\text{ V}$, $T_j = 0^\circ\text{C} \sim 115^\circ\text{C}$

Table 43 DC Electrical Characteristics for 3.3 V Operation

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------------|----------|--------|------|------|------------|--|
| | | Min. | Typ. | Max. | | |
| Input Low Voltage | V_{IL} | – | – | 0.8 | V | TTL |
| Input High Voltage | V_{IH} | 2.0 | – | – | V | TTL |
| Output Low Voltage | V_{OL} | – | – | 0.4 | V | TTL |
| Output High Voltage | V_{OH} | 2.3 | – | – | V | TTL |
| Input Pull-up/down Resistance | R_I | – | 50 | – | K Ω | $V_{IL} = 0\text{ V}$ or $V_{IH} = V_{CC}$ |

6.2 AC Characteristics

6.2.1 XI/OSCI (Crystal/Oscillator) Timing

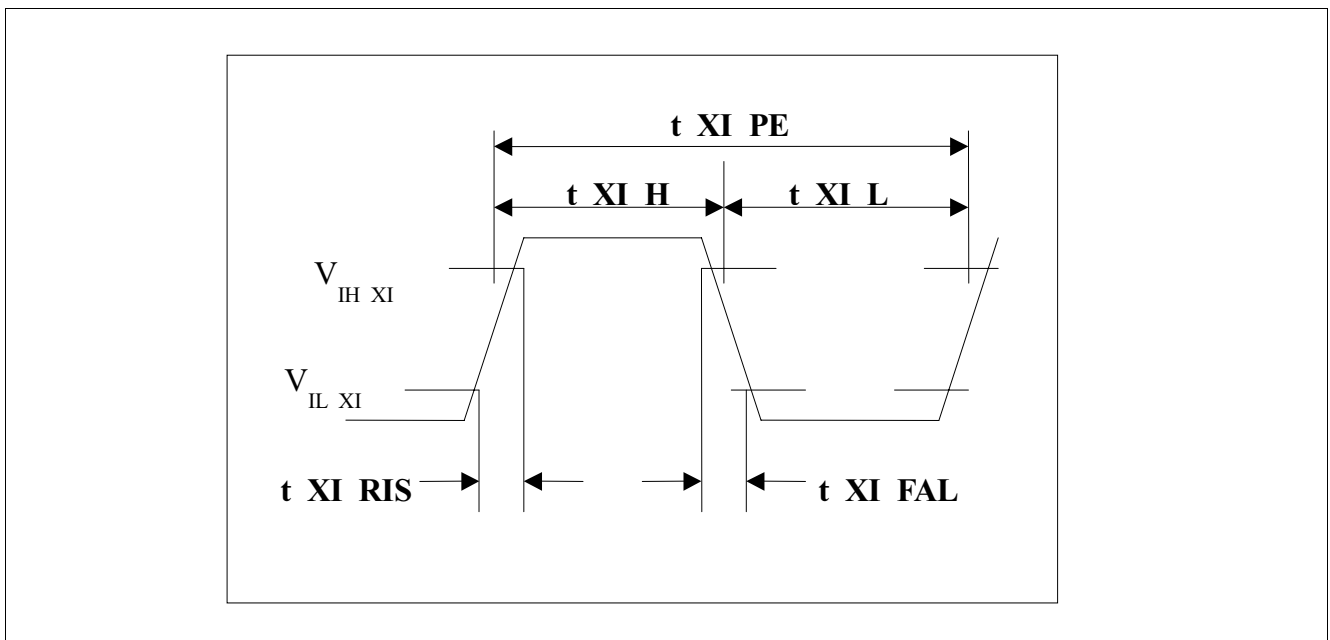


Figure 13 Crystal/Oscillator Timing

Table 44 Crystal/Oscillator Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|----------------|--------------|------|--------------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| XI/OSCI Clock Period | t_{XI_PER} | 20.0 - 50ppm | 20.0 | 20.0 + 50ppm | ns | – |
| XI/OSCI Clock High | t_{XI_HI} | 8 | 10.0 | – | ns | – |
| XI/OSCI Clock Low | t_{XI_LO} | 8 | 10.0 | – | ns | – |
| XI/OSCI Clock Rise Time, V_{IL} (max) to V_{IH} (min) | t_{XI_RISE} | – | – | 2 | ns | – |
| XI/OSCI Clock Fall Time, V_{IH} (min) to V_{IL} (max) | t_{XI_FALL} | – | – | 2 | ns | – |

6.2.2 Power On Reset

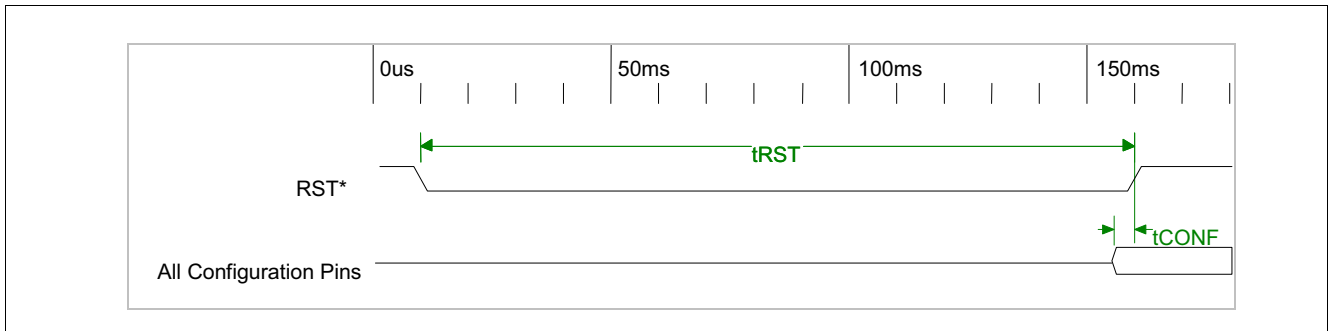


Figure 14 Power on Reset Timing

Table 45 Power on Reset Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------------|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| RST Low Period | t_{RST} | 150 | – | – | ms | – |
| Start of Configuration Pins | t_{CONF} | 100 | – | – | ns | – |

6.2.3 EEPROM Interface Timing

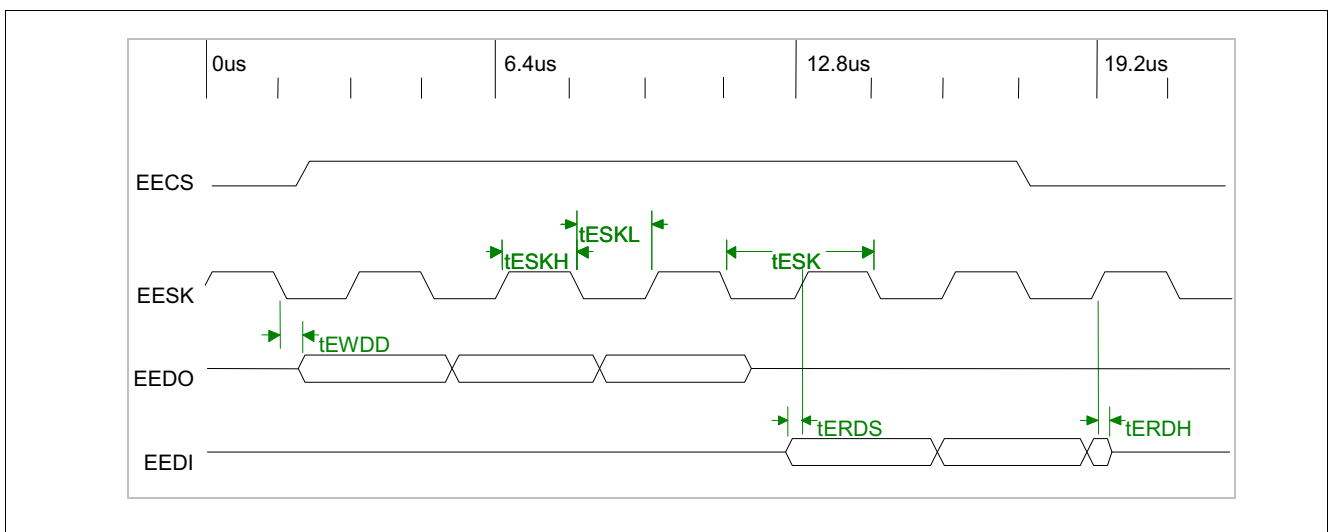


Figure 15 EEPROM Interface Timing

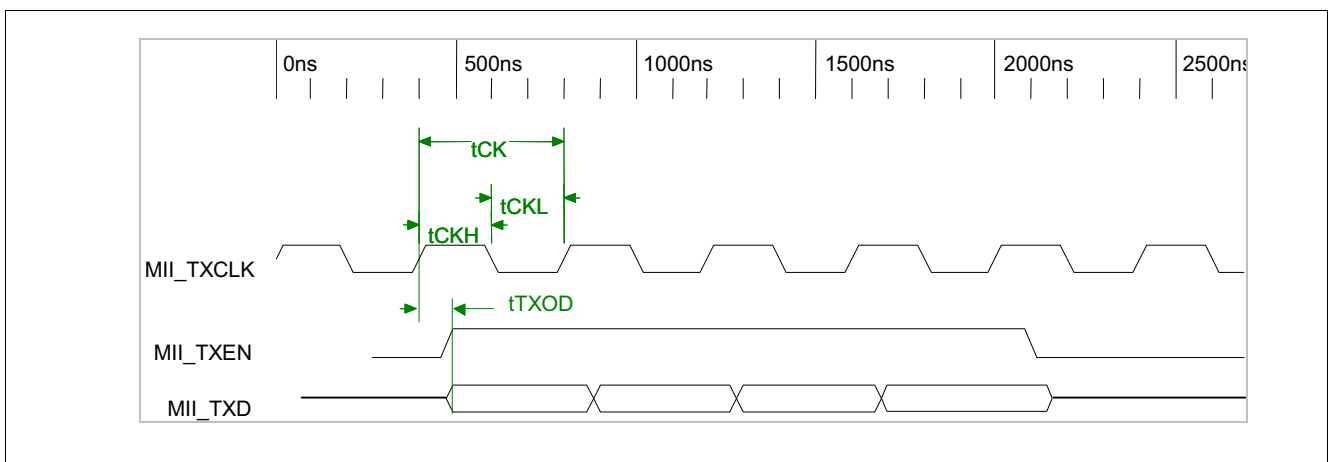
Table 46 EEPROM Interface Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------|------------|--------|------|------|---------------|-----------------------|
| | | Min. | Typ. | Max. | | |
| EESK Period | t_{ESK} | – | 3.2 | – | μs | – |
| EESK Low Period | t_{ESKL} | – | 1.6 | – | μs | – |
| EESK High Period | t_{ESKH} | – | 1.6 | – | μs | – |
| EEDI to EESK Rising Setup Time | t_{ERDS} | 10 | – | – | ns | – |

Table 46 EEPROM Interface Timing (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| EEDI to EESK Rising Hold Time | t_{ERDH} | 10 | – | – | ns | – |
| EESK Falling to EEDO Output Delay Time | t_{EWDD} | – | – | 20 | ns | – |

6.2.4 10Base-TX MII Output Timing


Figure 16 10Base-TX MII Output Timing
Table 47 10Base-TX MII Output Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| MII_TXCLK Period | t_{CK} | – | 400 | – | ns | – |
| MII_TXCLK Low Period | t_{CKL} | 160 | – | 240 | ns | – |
| MII_TXCLK High Period | t_{CKH} | 160 | – | 240 | ns | – |
| MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay | t_{TXOD} | 10 | – | 20 | ns | – |

6.2.5 10Base-TX MII Input Timing

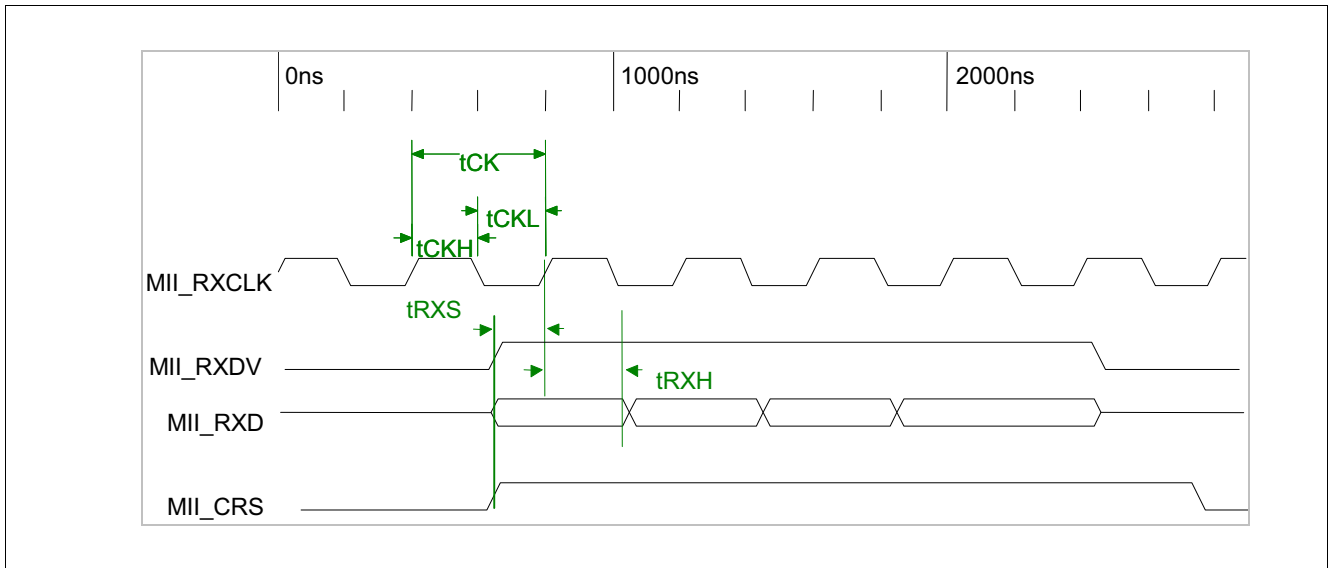


Figure 17 10Base-TX MII Input Timing

Table 48 10Base-TX MII Input Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| MII_RXCLK Period | t_{CK} | – | 400 | – | ns | – |
| MII_RXCLK Low Period | t_{CKL} | 160 | – | 240 | ns | – |
| MII_RXCLK High Period | t_{CKH} | 160 | – | 240 | ns | – |
| MII_CRD, MII_RXDV and MII_RXD to MII_RXCLK rising setup | t_{RXS} | 10 | – | – | ns | – |
| MII_CRD, MII_RXDV and MII_RXD to MII_RXCLK rising hold | t_{RXH} | 10 | – | – | ns | – |

6.2.6 100Base-TX MII Output Timing

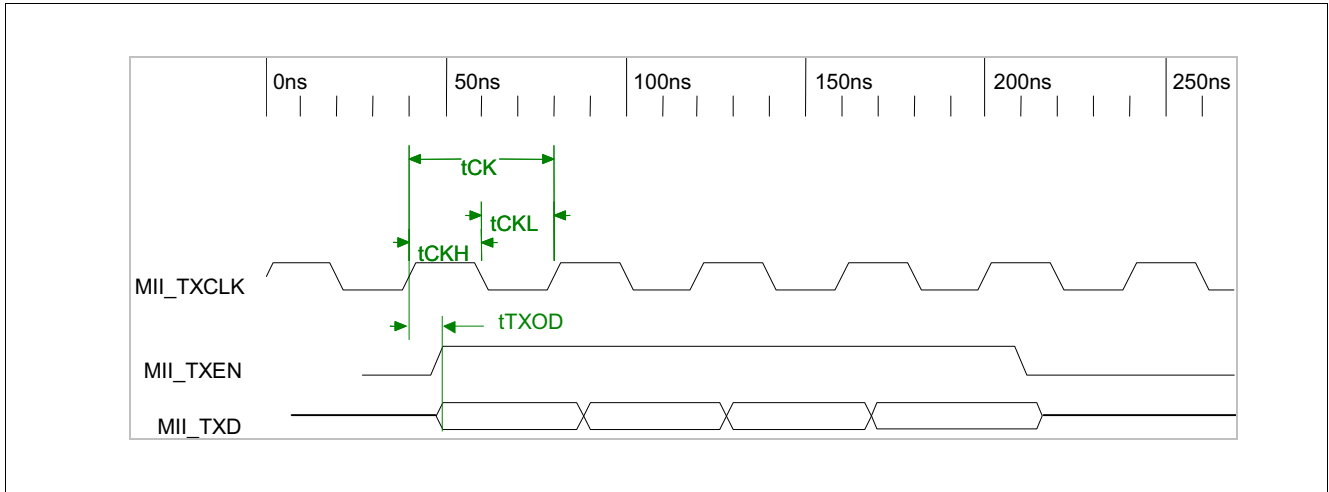


Figure 18 100Base-TX MII Output Timing

Table 49 100Base-TX MII Output Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| MII_TXCLK Period | t_{CK} | – | 40 | – | ns | – |
| MII_TXCLK Low Period | t_{CKL} | 16 | – | 24 | ns | – |
| MII_TXCLK High Period | t_{CKH} | 16 | – | 24 | ns | – |
| MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay | t_{TXOD} | 10 | – | 20 | ns | – |

6.2.7 100Base-TX MII Input Timing

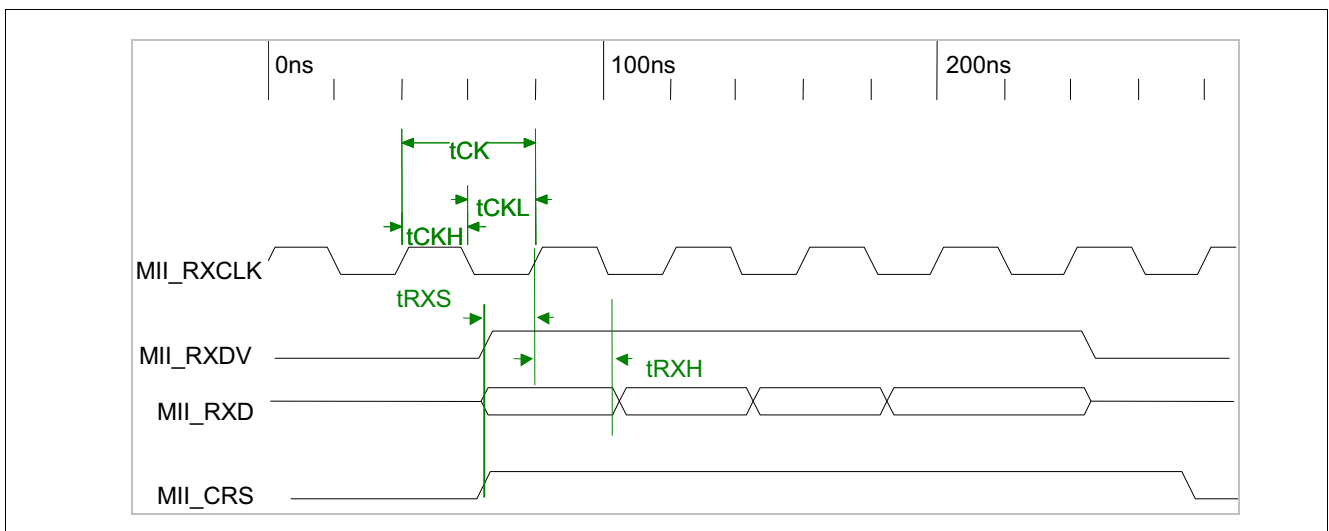


Figure 19 100Base-TX MII Input Timing

Table 50 100Base-TX MII Input Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| MII_RXCLK Period | t_{CK} | – | 40 | – | ns | – |
| MII_RXCLK Low Period | t_{CKL} | 16 | – | 24 | ns | – |
| MII_RXCLK High Period | t_{CKH} | 16 | – | 24 | ns | – |
| MII_CRSDV, MII_RXDV and MII_RXD to MII_RXCLK rising setup | t_{RXS} | 10 | – | – | ns | – |
| MII_CRSDV, MII_RXDV and MII_RXD to MII_RXCLK rising hold | t_{RXH} | 10 | – | – | ns | – |

6.2.8 Reduced MII Timing

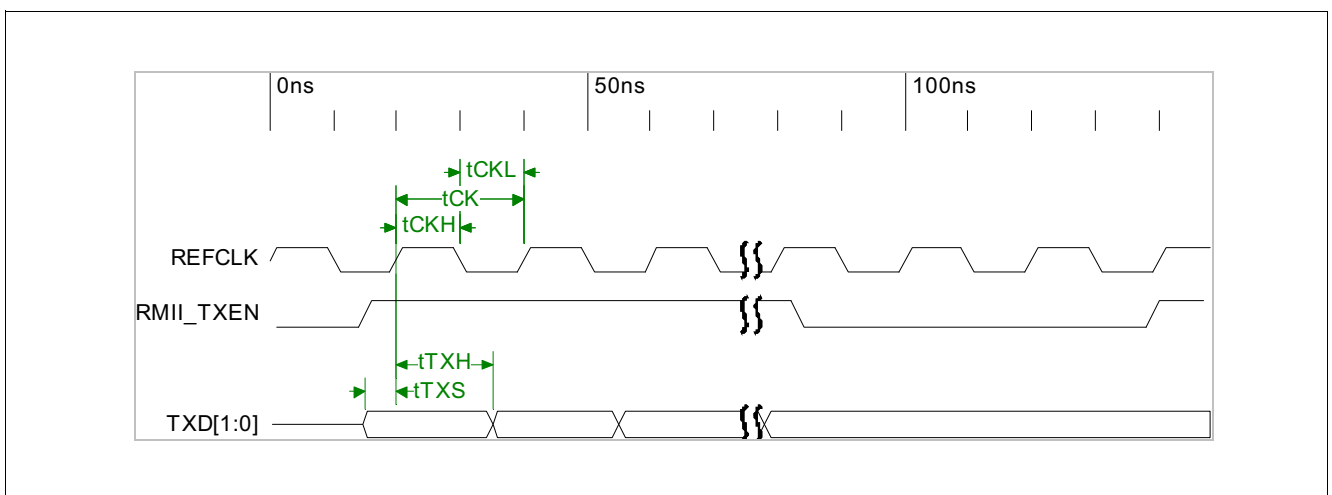
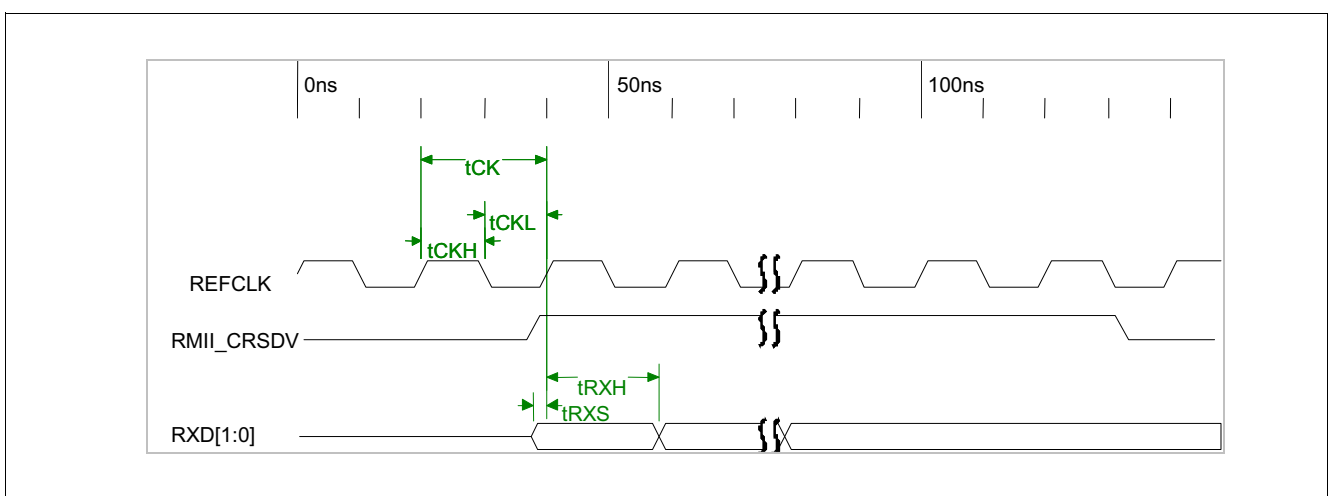
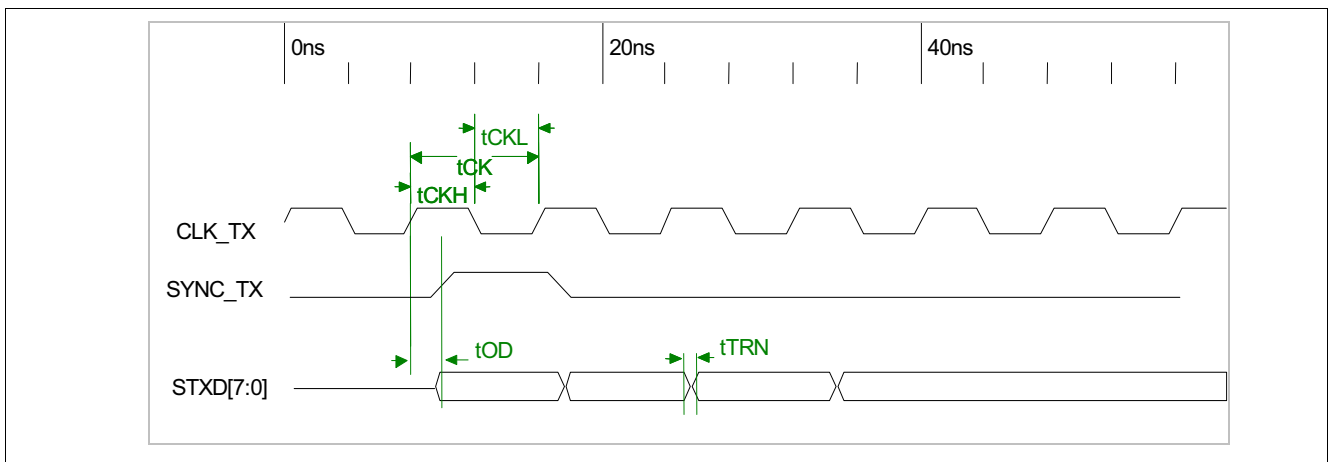

Figure 20 Reduced MII Timing (1 of 2)

Figure 21 Reduced MII Timing (2 of 2)

Table 51 Reduced MII Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| RMII_REFCLK Period | t_{CK} | – | 20 | – | ns | – |
| RMII_REFCLK Low Period | t_{CKL} | – | 10 | – | ns | – |
| RMII_REFCLK High Period | t_{CKH} | – | 10 | – | ns | – |
| TXEN, TXD to REFCLK rising setup time | t_{TXS} | 4 | – | – | ns | – |
| TXEN, TXD to REFCLK rising hold time | t_{TXH} | 2 | – | – | ns | – |
| CSRDV, RXD to REFCLK rising setup time | t_{RXS} | 4 | – | – | ns | – |
| CRSDV, RXD to REFCLK rising hold time | t_{RXH} | 2 | – | – | ns | – |

6.2.9 SS_SMIIT Transmit Timing


Figure 22 SS_SMIIT Transmit Timing
Table 52 SS_SMIIT Transmit Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------------|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| SS_SMIIT Output Clock Period | t_{CK} | – | 8 | – | ns | – |
| SS_SMIIT Output Clock Low Period | t_{CKL} | – | 4 | – | ns | – |
| R SS_SMIIT Output Clock High Period | t_{CKH} | – | 4 | – | ns | – |
| Txdata/TxSync output delay to CLK_TX | t_{OD} | 2 | – | 5 | ns | – |
| Txdata/RxSync Rise/Fall Time | t_{TRN} | – | 1 | – | ns | – |

6.2.10 SS_SMI_I Receive Timing

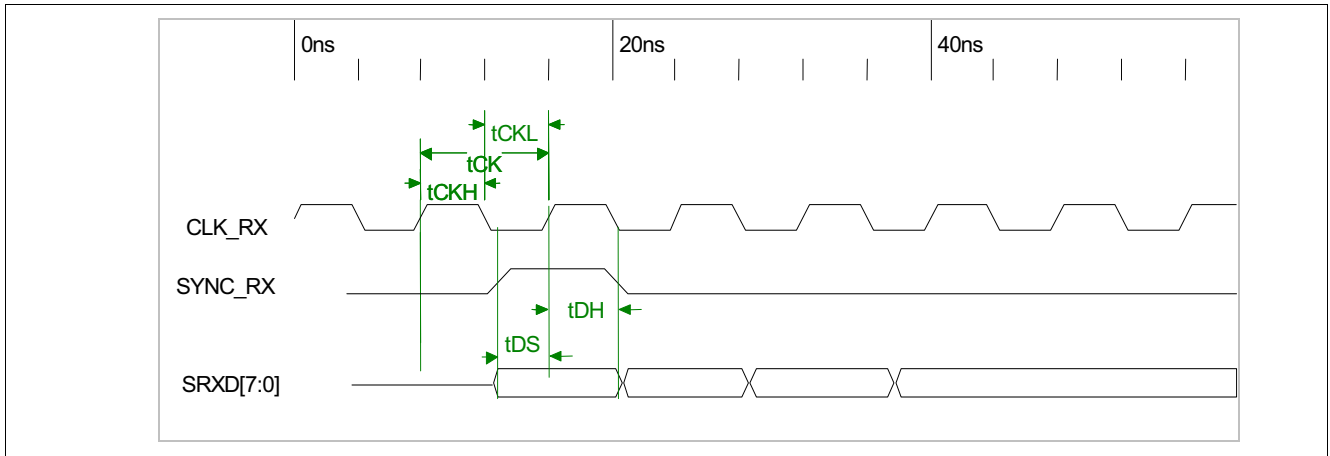


Figure 23 SS_SMI_I Receive Timing

Table 53 SS_SMI_I Receive Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| SS_SMI _I CLK_RX Clock Period | t_{CK} | – | 8 | – | ns | – |
| SS_SMI _I CLK_RX Low Period | t_{CKL} | – | 4 | – | ns | – |
| SS_SMI _I CLK_RX High Period | t_{CKH} | – | 4 | – | ns | – |
| Rxdata/RxSync setup to CLK_RX rising edge | t_{DS} | 1.5 | – | – | ns | – |
| Rxdata/RxSync hold from CLK_RX rising edge | t_{DH} | 1 | – | – | ns | – |

6.2.11 Serial Management Interface (SDC/SDIO) Timing

SDC/SDIO timing is same as MDC/MDIO except Data Length is 32 bits.

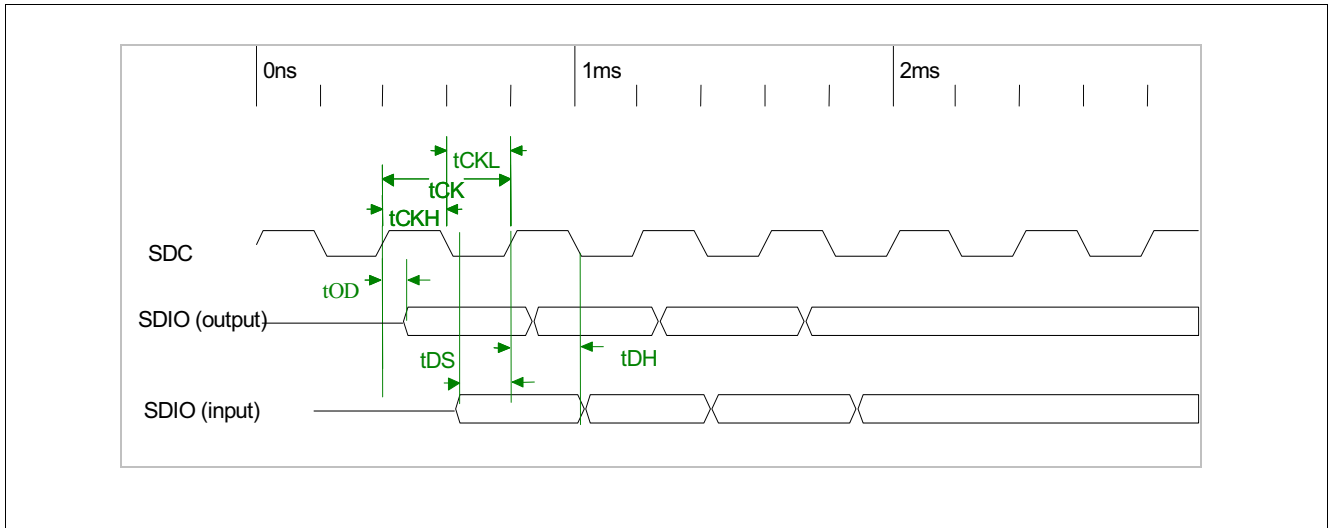


Figure 24 Serial Management Interface (SDC/SDIO) Timing

Table 54 Serial Management Interface (SDC/SDIO) Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| SS_SMI CLK_RX Clock Period | t_{CK} | – | 400 | – | ns | – |
| SS_SMI CLK_RX Low Period | t_{CKL} | – | 200 | – | ns | – |
| SS_SMI CLK_RX High Period | t_{CKH} | – | 200 | – | ns | – |
| S DC to S DIO Output Delay | t_{OD} | – | – | 20 | ns | – |
| S DIO Input to S DC Setup Time | t_{DS} | 10 | – | – | ns | – |
| S DIO Input to S DC Hold Time | t_{DH} | 10 | – | – | ns | – |

7 Packaging

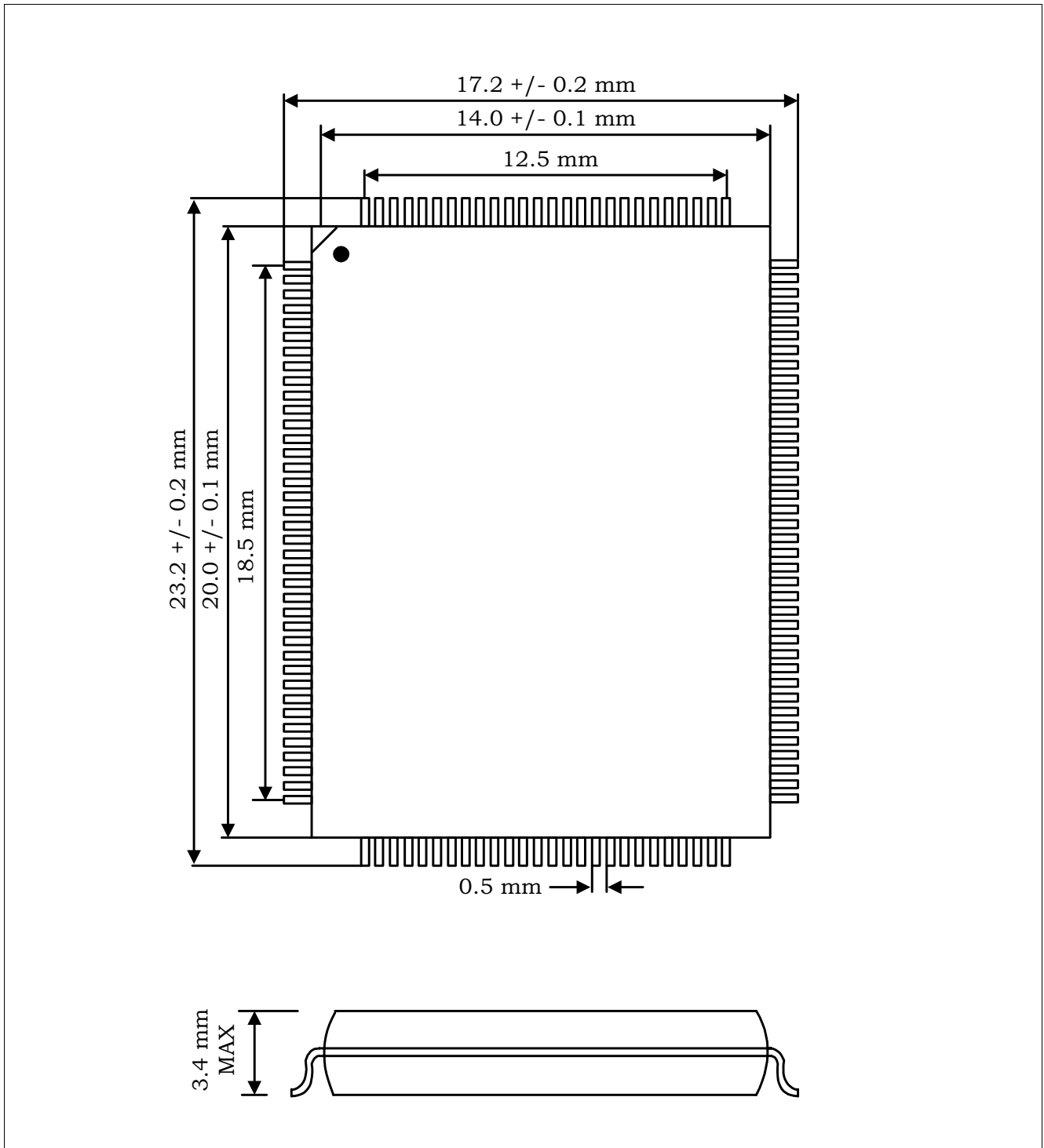


Figure 25 ADM6918/X Packaging

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