



THE DATASHEET OF DG418BDY



Precision Monolithic Quad SPST CMOS Analog Switches

DESCRIPTION

The DG417B, DG418B, DG419B monolithic CMOS analog switches were designed to provide high performance switching of analog signals. Combining low power, low leakages, high speed, low on-resistance and small physical size, the DG417B series is ideally suited for portable and battery powered industrial and military applications requiring high performance and efficient use of board space.

To achieve high-voltage ratings and superior switching performance, the DG417B series is built on Vishay Siliconix's high voltage silicon gate (HVSG) process. Break-before-make is guaranteed for the DG419B, which is an SPDT configuration. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

The DG417B and DG418B respond to opposite control logic levels as shown in the Truth Table.

FEATURES

- ± 15 V analog signal range
- On-resistance - $R_{DS(on)}$: 15Ω
- Fast switching action - t_{ON} : 110 ns
- TTL and CMOS compatible
- MSOP-8 and SOIC-8 package
- Compliant to RoHS directive 2002/95/EC



RoHS*
COMPLIANT

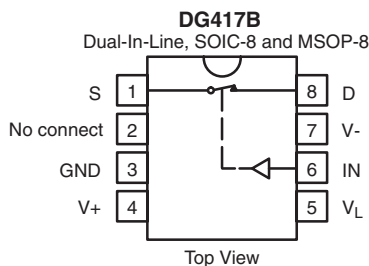
BENEFITS

- Widest dynamic range
- Low signal errors and distortion
- Break-before-make switching action
- Simple interfacing
- Reduced board space
- Improved reliability

APPLICATIONS

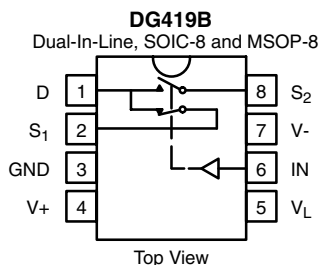
- Precision test equipment
- Precision instrumentation
- Battery powered systems
- Sample-and-hold circuits
- Military radios
- Guidance and control systems
- Hard disk drivers

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



| TRUTH TABLE | | |
|-------------|--------|--------|
| Logic | DG417B | DG418B |
| 0 | ON | OFF |
| 1 | OFF | ON |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V



| TRUTH TABLE - DG419B | | |
|----------------------|-----------------|-----------------|
| Logic | SW ₁ | SW ₂ |
| 0 | ON | OFF |
| 1 | OFF | ON |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Pb containing terminations are not RoHS compliant, exemptions may apply

| ORDERING INFORMATION | | |
|-----------------------|-----------------------|--|
| Temp Range | Package | Part Number |
| DG417B, DG418B | | |
| - 40 °C to 85 °C | 8-Pin Plastic MiniDIP | DG417BDJ DG417BDJ-E3 |
| | | DG418BDJ DG418BDJ-E3 |
| | 8-Pin Narrow SOIC | DG417BDY DG417BDY-E3 DG417BDY-T1 DG417BDY-T1-E3 |
| | | DG418BDY DG418BDY-E3 DG418BDY-T1 DG418BDY-T1-E3 |
| | 8-Pin MSOP | DG417BDQ-T1-E3 |
| | | DG418BDQ-T1-E3 |
| DG419B | | |
| - 40 °C to 85 °C | 8-Pin Plastic MiniDIP | DG419BDJ DG419BDJ-E3 |
| | 8-Pin Narrow SOIC | DG419BDY DG419BDY-E3 DG419BDY-T1 DG419BDY-T1-E3 |
| | 8-Pin MSOP | DG419BDQ-T1-E3 |

| ABSOLUTE MAXIMUM RATINGS | | | |
|---|--|------|----|
| Parameter | Limit | Unit | |
| V- | - 20 | V | |
| V+ | 20 | | |
| GND | 25 | | |
| V _L | (GND - 0.3) to (V+) + 0.3 | | |
| Digital Inputs ^a , V _S , V _D | (V-) - 2 V to (V+) + 2 or 30 mA, whichever occurs first | | |
| Current, (Any Terminal) Continuous | 30 | mA | |
| Current (S or D) Pulsed at 1 ms, 10 % Duty Cycle | 100 | | |
| Storage Temperature | - 65 to 150 | °C | |
| Power Dissipation (Package) ^b | 8-Pin Plastic MiniDIP ^c | 400 | mW |
| | 8-Pin Narrow SOIC ^c | 400 | |
| | 8-Pin MSOP ^d | 400 | |
| | 8-Pin CerDIP ^e | 600 | |

Notes:

- Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC board.
- Derate 5.3 mW/°C above 75 °C.
- Derate 4 mW/°C above 70 °C.
- Derate 8 mW/°C above 75 °C.

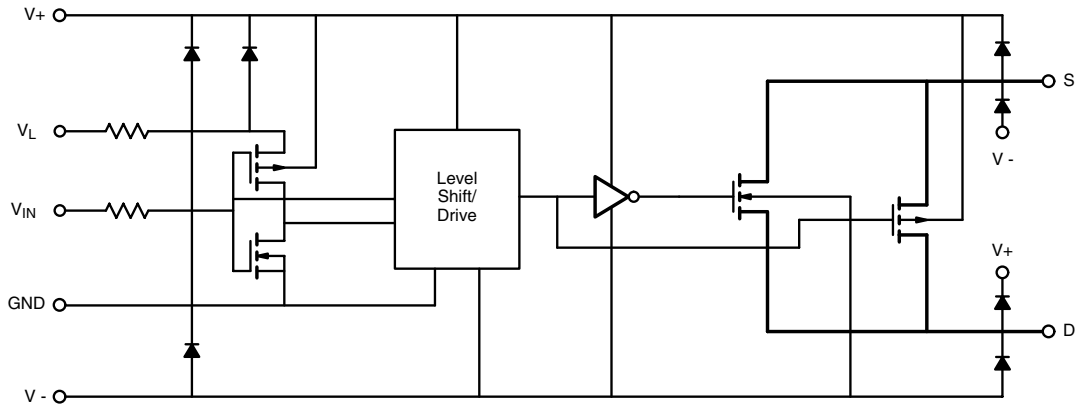
SCHEMATIC DIAGRAM Typical Channel


Figure 1.

| SPECIFICATIONS^a | | | | | | | | | | | |
|---|--------------|--|-------------------|-------------------|--------------------|-------------------|------------------------------|----------|-----------------------------|---------------|----------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$ $V_L = 5\text{ V}$, $V_{IN} = 2.4\text{ V}$, 0.8 V^f | | | Temp. ^b | Typ. ^c | A Suffix -55 °C to 125 °C | | D Suffix -40 °C to 85 °C | | Unit |
| | | Min. ^d | Max. ^d | Min. ^d | | | Max. ^d | | | | |
| Analog Switch | | | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | | Full | | | - 15 | 15 | - 15 | 15 | V |
| Drain-Source On-Resistance | $R_{DS(on)}$ | $I_S = -10\text{ mA}$, $V_D = \pm 12.5\text{ V}$ $V_+ = 13.5\text{ V}$, $V_- = -13.5\text{ V}$ | | | Room Full | 15 | | 25 34 | | 25 29 | Ω |
| Switch Off Leakage Current | $I_{S(off)}$ | $V_+ = 16.5\text{ V}$, $V_- = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}$, $V_S = \pm 15.5\text{ V}$ | DG417B | Room | - 0.1 | - 0.25 | 0.25 | - 0.25 | 0.25 | nA | |
| | $I_{D(off)}$ | | DG418B | Room Full | - 0.1 | - 20 | 20 | - 5 | 5 | | |
| | | | DG419B | Room Full | - 0.1 | - 0.75 | 0.75 | - 0.75 | 0.75 | | |
| Channel On Leakage Current | $I_{D(on)}$ | $V_+ = 16.5\text{ V}$, $V_- = -16.5\text{ V}$ $V_S = V_D = \pm 15.5\text{ V}$ | DG417B | Room | - 0.4 | - 0.4 | 0.4 | - 0.4 | 0.4 | | |
| | | | DG418B | Room Full | - 0.4 | - 40 | 40 | - 10 | 10 | | |
| | | | DG419B | Room Full | - 0.4 | - 0.75 | 0.75 | - 0.75 | 0.75 | | |
| Digital Control | | | | | | | | | | | |
| Input Current, V_{IN} Low | I_{IL} | | | Full | | - 0.5 | 0.5 | - 0.5 | 0.5 | μA | |
| Input Current, V_{IN} High | I_{IH} | | | Full | | - 0.5 | 0.5 | - 0.5 | 0.5 | μA | |
| Dynamic Characteristics | | | | | | | | | | | |
| Turn-On Time | t_{ON} | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$, See Switching Time Test Circuit | DG417B | Room | 62 | | 89 | | 89 | ns | |
| Turn-Off Time | t_{OFF} | | DG418B | Room Full | 62 | | 106 | | 99 | | |
| | | DG417B | Room | 53 | | 80 | | 80 | | | |
| | | DG418B | Room Full | 53 | | 88 | | 86 | | | |
| Transition Time | t_{TRANS} | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = \pm 10\text{ V}$, $V_{S2} = \pm 10\text{ V}$ | DG419B | Room Full | 60 | | 87 96 | | 87 93 | | |
| Break-Before-Make Time Delay | t_D | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = \pm 10\text{ V}$ | DG419B | Room | 16 | 3 | | 3 | | | |
| Charge Injection | Q | $C_L = 10\text{ nF}$ $V_{gen} = 0\text{ V}$, $R_{gen} = 0\ \Omega$ | | Room | 38 | | | | | pC | |
| Off Isolation ^e | OIRR | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$ | | Room | - 82 | | | | | dB | |
| Channel-to-Channel Crosstalk ^e | X_{TALK} | | DG419B | Room | - 88 | | | | | | |

| SPECIFICATIONS ^a | | | | | | | | | |
|-------------------------------------|--------------|--|--------------------|-------------------|-------------------------------|-------------------|------------------------------|-------------------|---------------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$ $V_L = 5\text{ V}$, $V_{IN} = 2.4\text{ V}$, 0.8 V^f | Temp. ^b | Typ. ^c | A Suffix - 55 °C to 125 °C | | D Suffix - 40 °C to 85 °C | | Unit |
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Dynamic Characteristics | | | | | | | | | |
| Source Off Capacitance ^e | $C_{S(off)}$ | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ | Room | 12 | | | | | pF |
| Drain Off Capacitance ^e | $C_{D(off)}$ | | DG417B DG418B | Room | 12 | | | | |
| Channel On Capacitance ^e | $C_{D(on)}$ | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ | DG417B DG418B | Room | 50 | | | | |
| | | | DG419B | Room | 57 | | | | |
| Power Supplies | | | | | | | | | |
| Positive Supply Current | I_+ | $V_+ = 16.5\text{ V}$, $V_- = -16.5\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$ | Room Full | 0.001 | | 1 5 | | 1 5 | μA |
| Negative Supply Current | I_- | | Room Full | - 0.001 | - 1 - 5 | | - 1 - 5 | | |
| Logic Supply Current | I_L | | Room Full | 0.001 | | 1 5 | | 1 5 | |
| Ground Current | I_{GND} | | Room Full | - 0.001 | - 1 - 5 | | - 1 - 5 | | |

| SPECIFICATIONS ^a | | | | | | | | | |
|----------------------------------|--------------|--|--------------------|-------------------|-------------------------------|-------------------|------------------------------|-------------------|---------------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}$, $V_- = 0\text{ V}$ $V_L = 5\text{ V}$, $V_{IN} = 2.4\text{ V}$, 0.8 V^f | Temp. ^b | Typ. ^c | A Suffix - 55 °C to 125 °C | | D Suffix - 40 °C to 85 °C | | Unit |
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Analog Switch | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | | 0 | 12 | 0 | 12 | V |
| Drain-Source On-Resistance | $R_{DS(on)}$ | $I_S = -10\text{ mA}$, $V_D = 3.8\text{ V}$ $V_+ = 10.8\text{ V}$ | Room Full | 26 | | 35 52 | | 35 45 | Ω |
| Dynamic Characteristics | | | | | | | | | |
| Turn-On Time | t_{ON} | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$, See Switching Time Test Circuit | Room Full | 100 | | 125 155 | | 125 143 | ns |
| Turn-Off Time | t_{OFF} | | Room Full | 38 | | 66 73 | | 66 69 | |
| Break-Before-Make Time Delay | t_D | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ | DG419B Room | 62 | 25 | | 25 | | |
| Transition Time | t_{TRANS} | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = 0\text{ V}$, 8 V , $V_{S2} = 8\text{ V}$, 0 V | Room Full | 95 | | 119 153 | | 119 141 | pC |
| Charge Injection | Q | $C_L = 10\text{ nF}$, $V_{gen} = 0\text{ V}$, $R_{gen} = 0\ \Omega$ | Room | 18 | | | | | |
| Power Supplies | | | | | | | | | |
| Positive Supply Current | I_+ | $V_+ = 13.2\text{ V}$, $V_L = 5.25\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$ | Room Full | 0.001 | | 1 5 | | 1 5 | μA |
| Negative Supply Current | I_- | | Room | - 0.001 | - 1 - 5 | | - 1 - 5 | | |
| Logic Supply Current | I_L | | Room | 0.001 | | 1 5 | | 1 5 | |
| Ground Current | I_{GND} | | Room | - 0.001 | - 1 - 5 | | - 1 - 5 | | |

Notes:

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 °C, full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

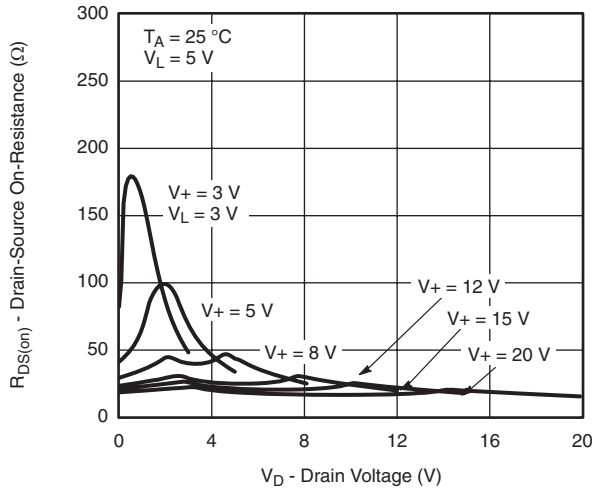
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.

e. Guaranteed by design, not subject to production test.

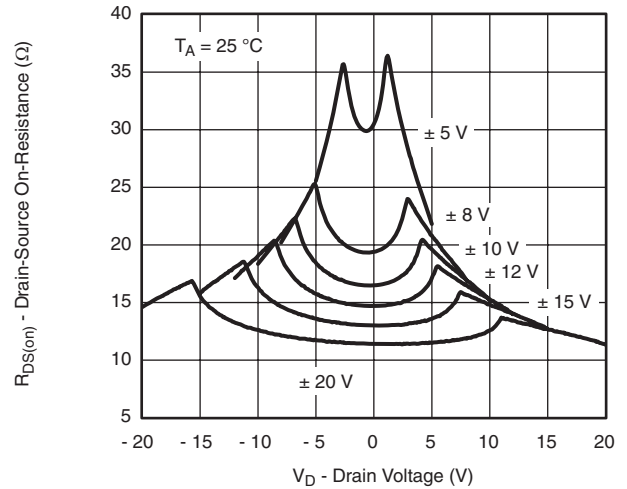
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

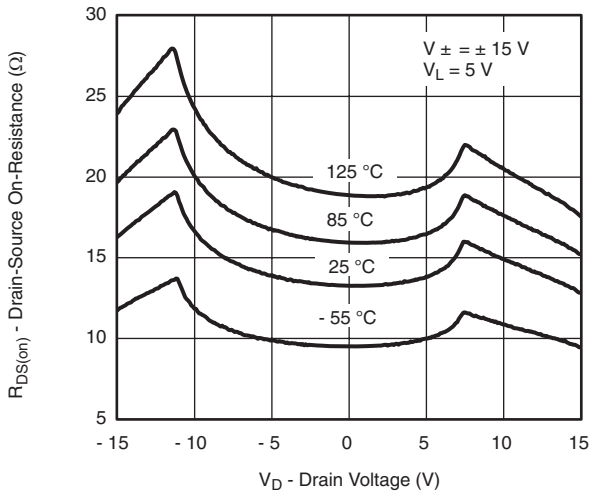
TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted



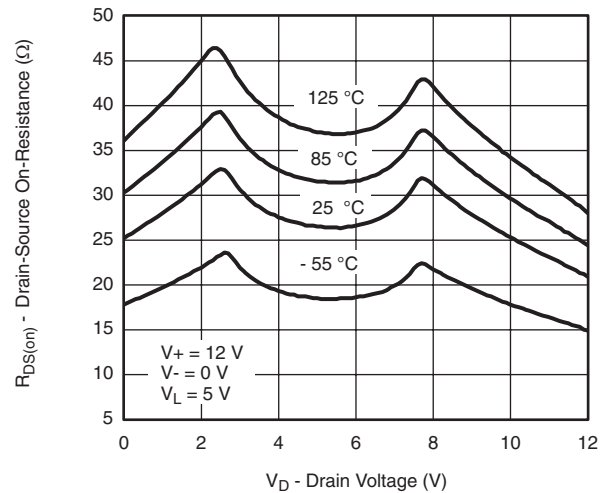
On-Resistance vs. V_D and Unipolar Power Supply Voltage



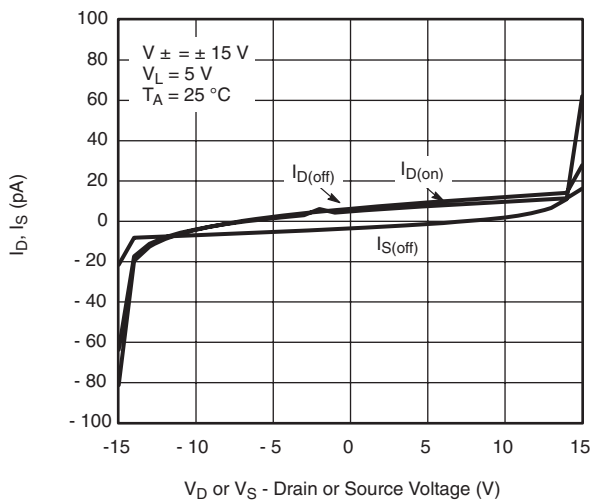
On-Resistance vs. V_D and Dual Supply Voltage



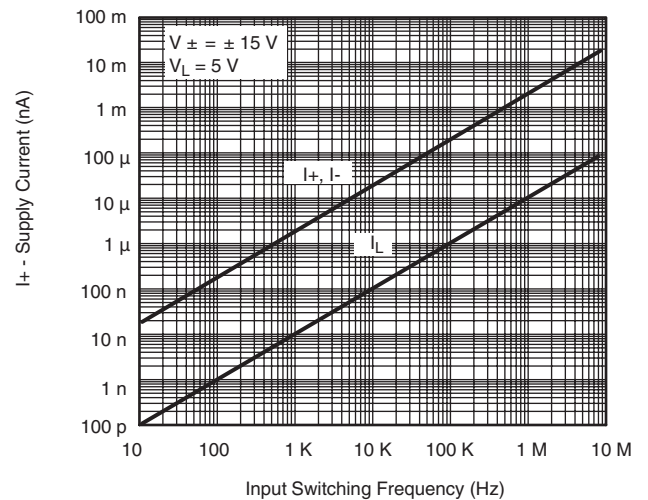
On-Resistance vs. V_D and Temperature



On-Resistance vs. V_D and Temperature

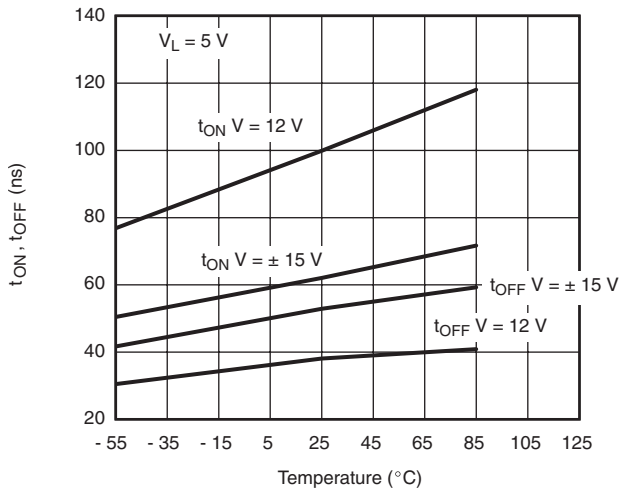


Leakage vs. Analog Voltage

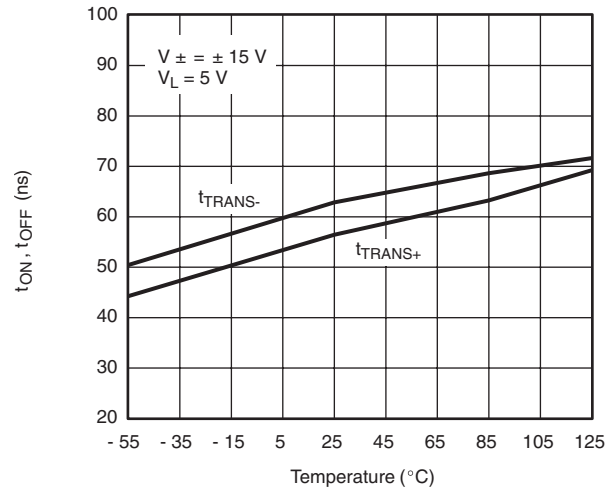


Supply Current vs. Input Switching Frequency

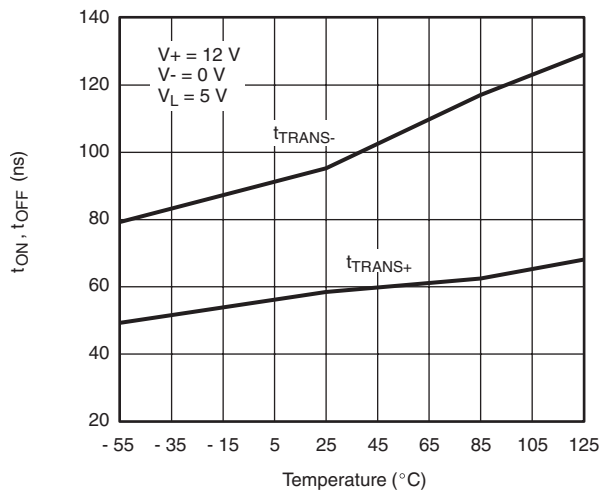
TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



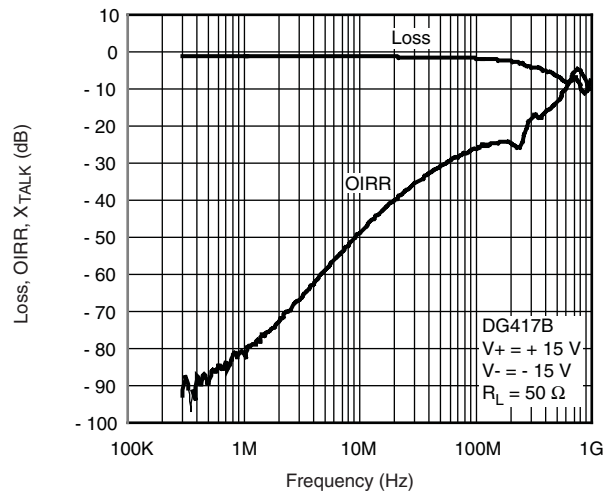
Switching Time vs. Temperature



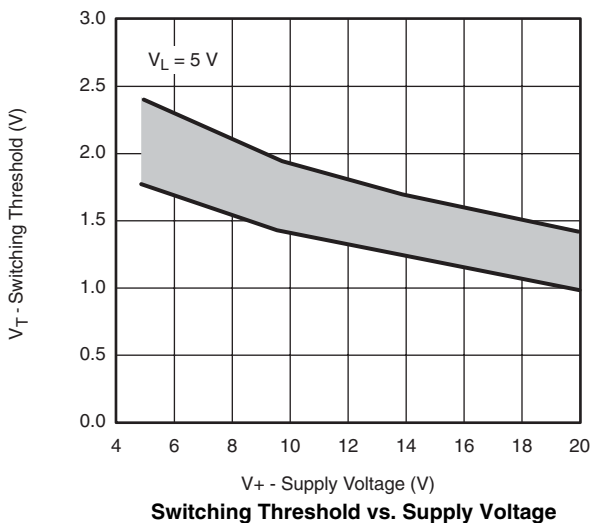
Transition Time vs. Temperature



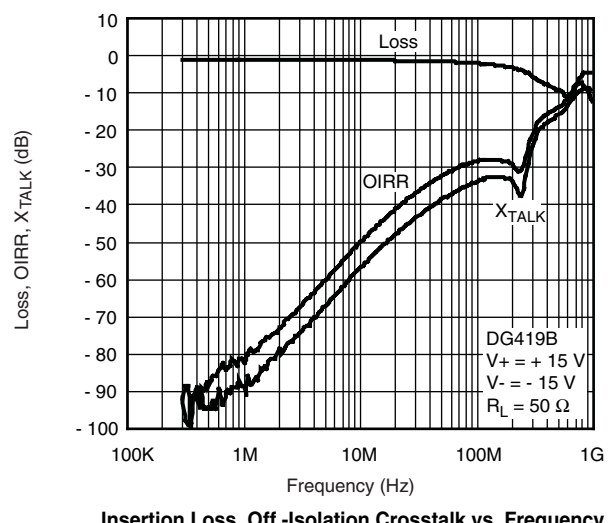
Transition Time vs. Temperature



Insertion Loss, Off-Isolation Crosstalk vs. Frequency

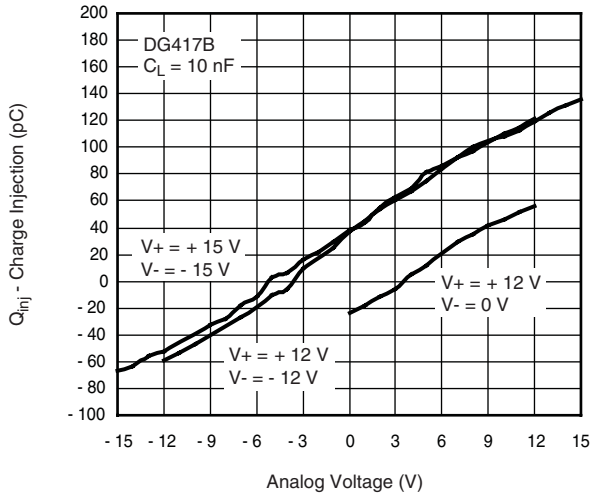


Switching Threshold vs. Supply Voltage

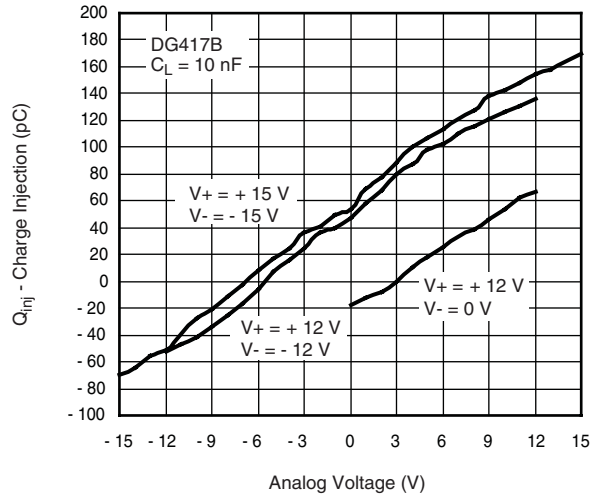


Insertion Loss, Off-Isolation Crosstalk vs. Frequency

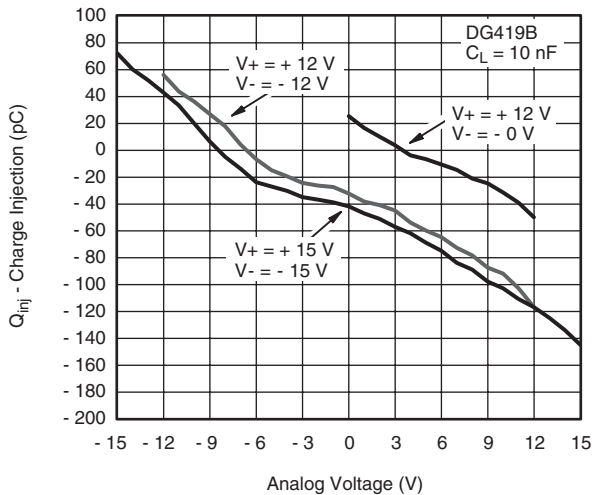
TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted



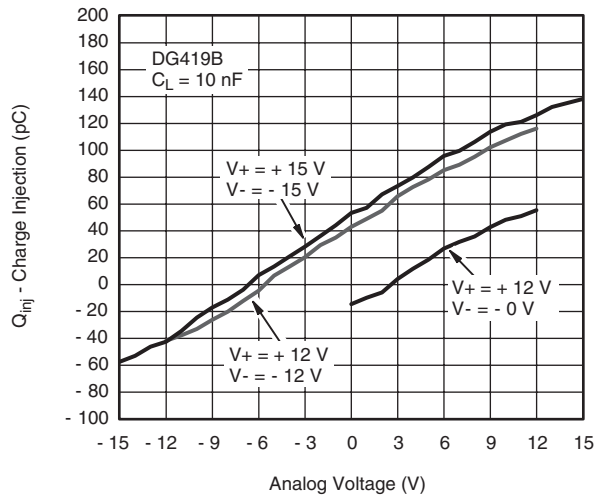
**Charge Injection vs. Analog Voltage
(Measured at drain pin)**



**Charge Injection vs. Analog Voltage
(Measured at source pin)**



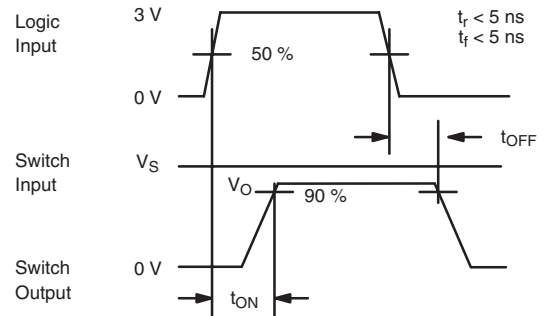
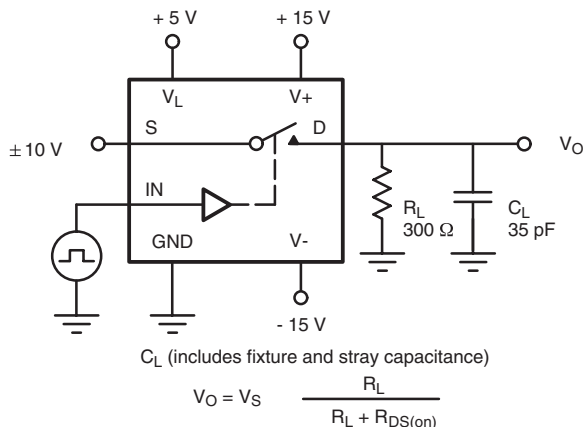
**Charge Injection vs. Analog Voltage
(Measured at drain pin)**



**Charge Injection vs. Analog Voltage
(Measured at source pin)**

TEST CIRCUITS

V_O is the steady state output with the switch on.



Note: Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 2. Switching Time (DG417B/418B)

TEST CIRCUITS

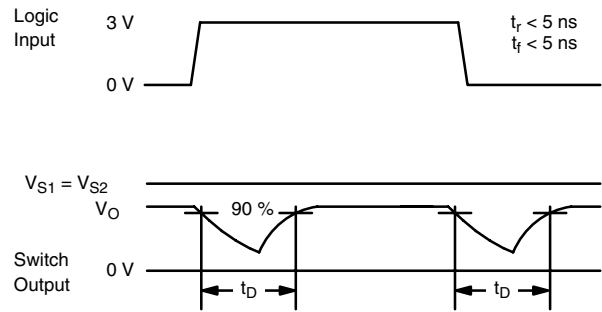
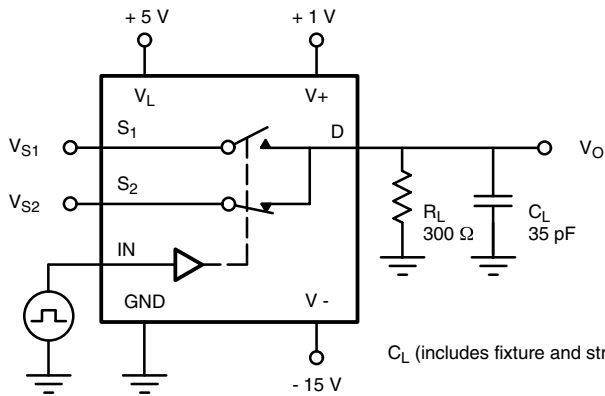
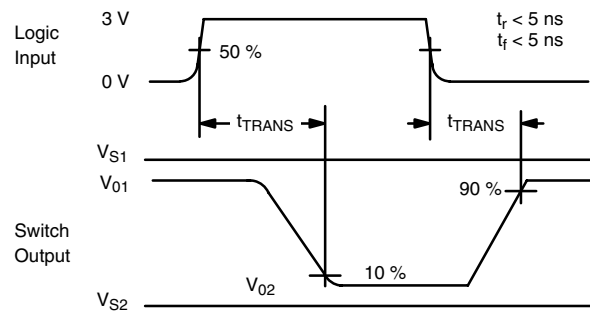
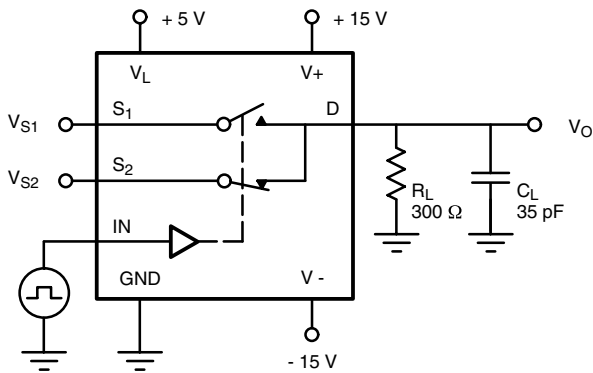


Figure 3. Break-Before-Make (DG419B)



$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 4. Transition Time (DG419B)

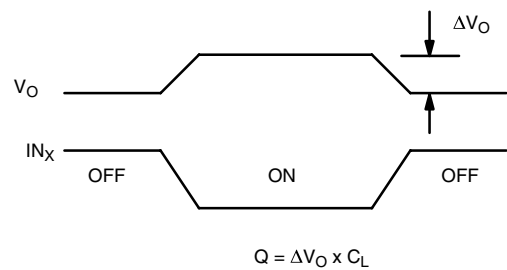
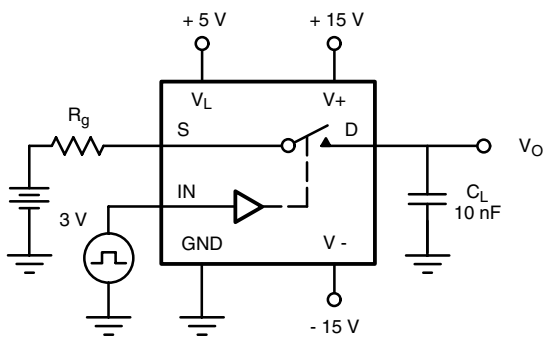


Figure 5. Charge Injection

TEST CIRCUITS

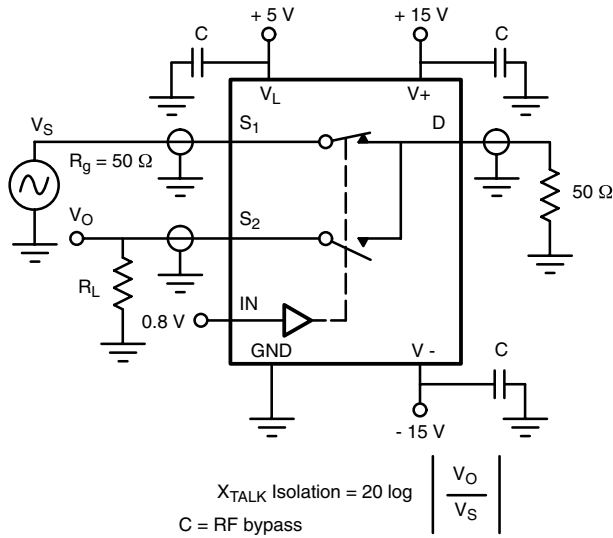


Figure 6. Crosstalk

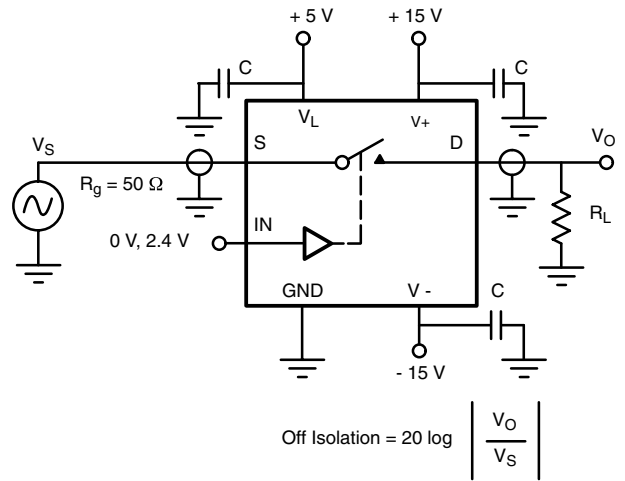


Figure 7. Off isolation

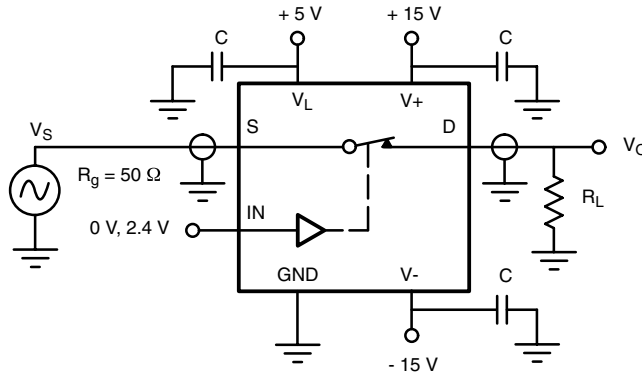


Figure 8. Insertion Loss

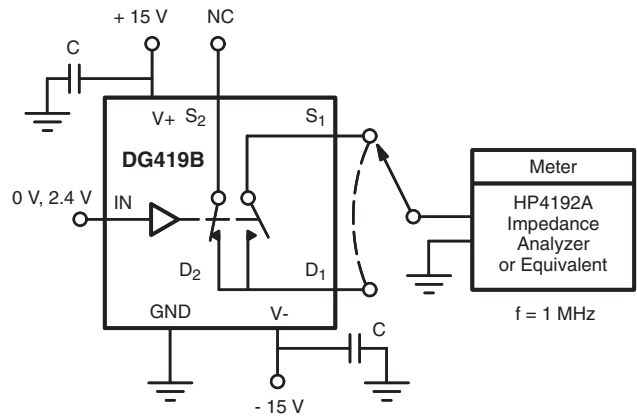
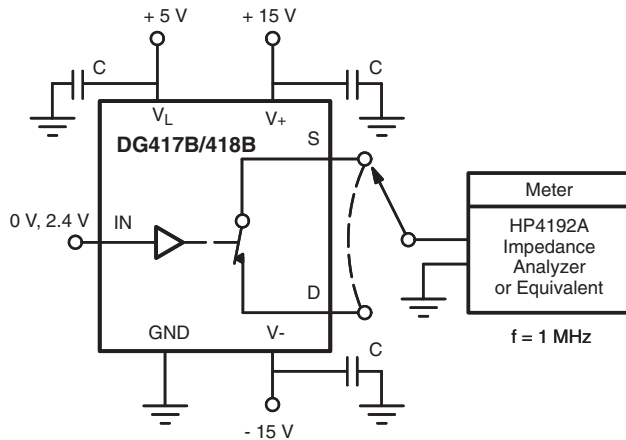


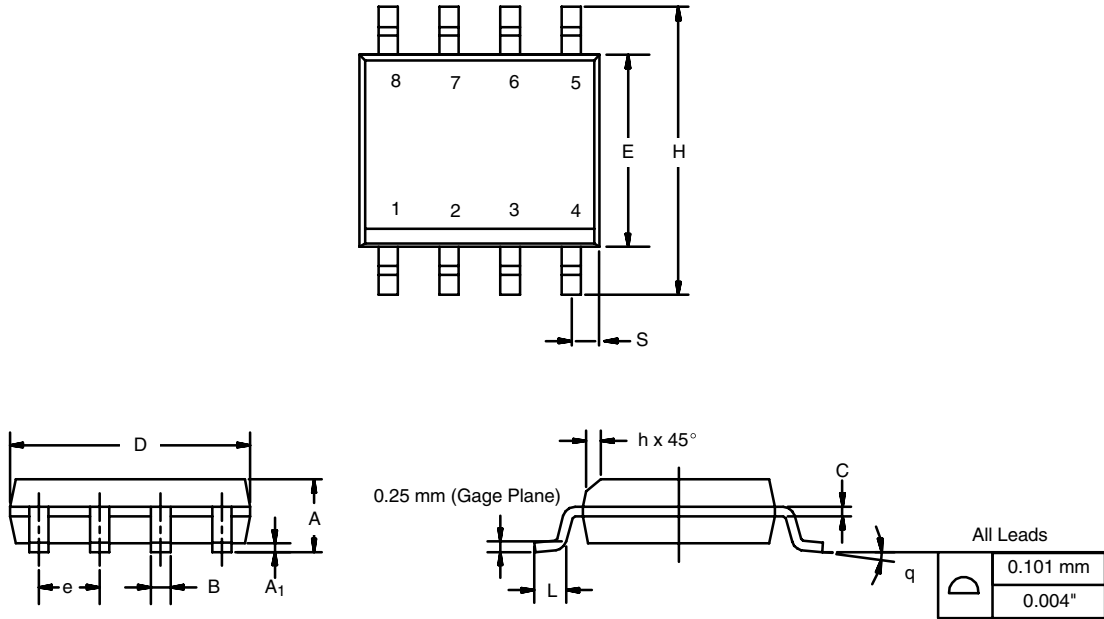
Figure 9. Source/Drain Capacitances

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?272107.



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012

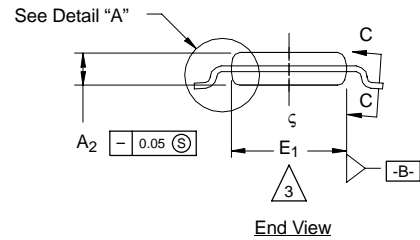
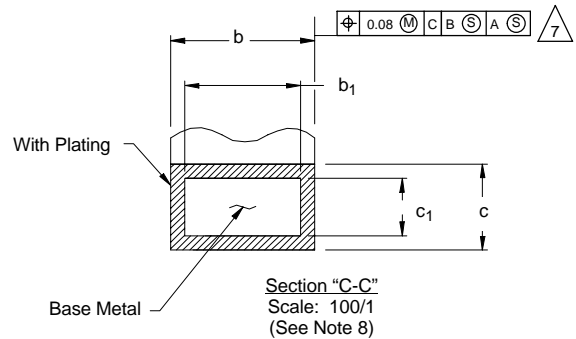
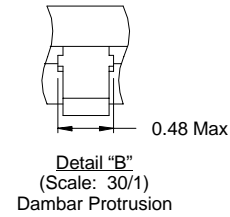
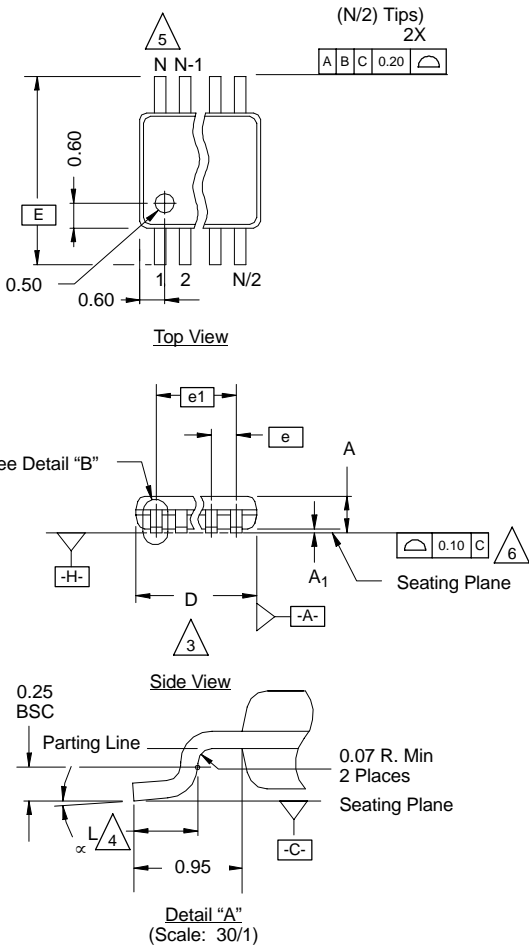


| DIM | MILLIMETERS | | INCHES | |
|---|-------------|------|-----------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A ₁ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.35 | 0.51 | 0.014 | 0.020 |
| C | 0.19 | 0.25 | 0.0075 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.196 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| q | 0° | 8° | 0° | 8° |
| S | 0.44 | 0.64 | 0.018 | 0.026 |
| ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498 | | | | |



MSOP: 8-LEADS

JEDEC Part Number: MO-187, (Variation AA and BA)



NOTES:

- Die thickness allowable is 0.203 ± 0.0127 .
- Dimensioning and tolerances per ANSI.Y14.5M-1994.
- Dimensions "D" and "E₁" do not include mold flash or protrusions, and are measured at Datum plane [-H-], mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimension is the length of terminal for soldering to a substrate.
- Terminal positions are shown for reference only.
- Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
- The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
- Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
- Controlling dimension: millimeters.
- This part is compliant with JEDEC registration MO-187, variation AA and BA.
- Datums [-A-] and [-B-] to be determined Datum plane [-H-].
- Exposed pad area in bottom side is the same as teh leadframe pad size.

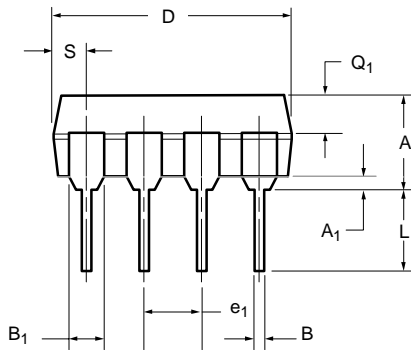
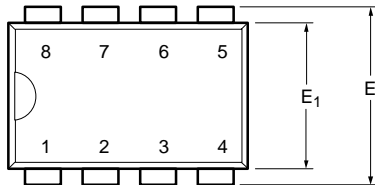
N = 8L

| Dim | MILLIMETERS | | | Note |
|----------------|-------------|------|------|------|
| | Min | Nom | Max | |
| A | - | - | 1.10 | |
| A ₁ | 0.05 | 0.10 | 0.15 | |
| A ₂ | 0.75 | 0.85 | 0.95 | |
| b | 0.25 | - | 0.38 | 8 |
| b ₁ | 0.25 | 0.30 | 0.33 | 8 |
| c | 0.13 | - | 0.23 | |
| c ₁ | 0.13 | 0.15 | 0.18 | |
| D | 3.00 BSC | | | 3 |
| E | 4.90 BSC | | | |
| E ₁ | 2.90 | 3.00 | 3.10 | 3 |
| e | 0.65 BSC | | | |
| e ₁ | 1.95 BSC | | | |
| L | 0.40 | 0.55 | 0.70 | 4 |
| N | 8 | | | 5 |
| α | 0° | 4° | 6° | |

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 DWG: 5867



PDIP: 8-LEAD



| Dim | MILLIMETERS | | INCHES | |
|----------------------|-------------|-------|--------|-------|
| | Min | Max | Min | Max |
| A | 3.81 | 5.08 | 0.150 | 0.200 |
| A₁ | 0.38 | 1.27 | 0.015 | 0.050 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| B₁ | 0.89 | 1.65 | 0.035 | 0.065 |
| C | 0.20 | 0.30 | 0.008 | 0.012 |
| D | 9.02 | 10.92 | 0.355 | 0.430 |
| E | 7.62 | 8.26 | 0.300 | 0.325 |
| E₁ | 5.59 | 7.11 | 0.220 | 0.280 |
| e₁ | 2.29 | 2.79 | 0.090 | 0.110 |
| e_A | 7.37 | 7.87 | 0.290 | 0.310 |
| L | 2.79 | 3.81 | 0.110 | 0.150 |
| Q₁ | 1.27 | 2.03 | 0.050 | 0.080 |
| S | 0.76 | 1.65 | 0.030 | 0.065 |

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DWG: 5478

NOTE: End leads may be half leads.

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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