THE DATASHEET OF

ADM1027ARQZ

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ON Semiconductor®

*dB*COOL™ Remote Thermal Controller and Voltage Monitor

ADM1027*

FEATURES

Monitors up to 5 Supply Voltages
Controls and Monitors up to 4 Fan Speeds
1 On-Chip and 2 Remote Temperature Sensors
Monitors up to 5 Processor VID Bits
Automatic Fan Speed Control Mode Controls System Cooling Based on Measured Temperature
Enhanced Acoustic Mode Dramatically Reduces User Perception of Changing Fan Speeds
2-Wire and 3-Wire Fan Speed Measurement
Limit Comparison of All Monitored Values
Meets SMBus 2.0 Electrical Specifications (Fully SMBus 1.1 Compliant)

APPLICATIONS

Low Acoustic Noise PCs
Networking and Telecommunications Equipment

GENERAL DESCRIPTION

The ADM1027 *dB*COOL controller is a complete systems monitor and multiple PWM fan controller for noise sensitive applications requiring active system cooling. It can monitor 12 V, 5 V, 2.5 V CPU supply voltage, plus its own supply voltage. It can monitor the temperature of up to two remote sensor diodes, plus its own internal temperature. It can measure and control the speed of up to four fans so that they operate at the lowest possible speed for minimum acoustic noise. The automatic fan speed control loop optimizes fan speed for a given temperature. Once the control loop parameters are programmed, the ADM1027 can vary fan speed without CPU intervention.

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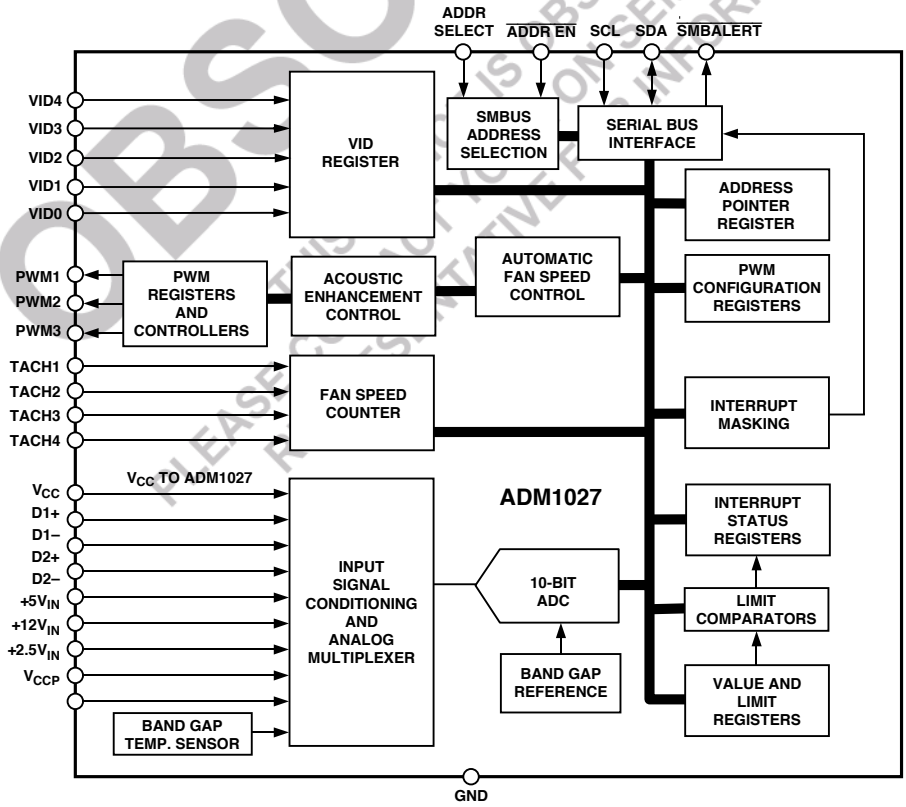
FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent Nos. 6,188,189; 6,169,442; 6,097,239; 5,982,221; and 5,867,012. Other patents pending.

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ADM1027–SPECIFICATIONS[1, 2, 3, 4] ($T_A = T_{MIN}$ to T_{MAX} (0°C to 105°C), $V_{CC} = V_{MIN}$ to V_{MAX} (3 V to 5.5 V), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
Supply Voltage	3.0	3.3	5.5	V	
Supply Current, I_{CC}		1.4	3	mA	Interface Inactive, ADC Active
TEMP-TO-DIGITAL CONVERTER					
Local Sensor Accuracy			±3	°C	$0°C \le T_A \le 105°C$
			±2	°C	$0°C \le T_A \le 70°C$
		±1		°C	$T_A = 40°C$
Resolution		0.25		°C	
Remote Diode Sensor Accuracy			±3	°C	$0°C \le T_D \le 120°C$
			±1.5	°C	$0°C \le T_D \le 120°C$; $0°C \le T_A \le 70°C$
		±1		°C	$T_A = 40°C$
				°C	$0°C \le T_D \le 120°C$; $T_A = 40°C$
Resolution		0.25		°C	
Remote Sensor Source Current		200		µA	High Level
		12		µA	Low Level
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error, TUE		±0.5	±1	%	All ADC Inputs except 12 V
			±1.5	%	12 V Input
Differential Nonlinearity, DNL			±1	LSB	8 Bits
Power Supply Sensitivity		±0.1		%/V	
Conversion Time (Voltage Input)		11.38	12.29	ms	Averaging Enabled
Conversion Time (Local Temperature)		12.09	13.05	ms	Averaging Enabled
Conversion Time (Remote Temperature)		25.59	27.64	ms	Averaging Enabled
Total Monitoring Cycle Time		120.17	129.78	ms	Averaging Enabled
Total Monitoring Cycle Time		13.51	14.59	ms	Averaging Disabled
Input Resistance	80	140	250	kΩ	
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy			±6	%	$0°C \le T_A \le 70°C$
			±8	%	$3.0 V \le V_{CC} \le 3.6 V$
Full-Scale Count			65,535		
Nominal Input RPM		109		RPM	Fan Count = 0xBFFF
		329		RPM	Fan Count = 0x3FFF
		5,000		RPM	Fan Count = 0x0438
		10,000		RPM	Fan Count = 0x021C
Internal Clock Frequency	82.8	90	97.2	kHz	
OPEN-DRAIN DIGITAL OUTPUTS, PWM1–PWM3, XTO					
Current Sink, I_{OL}			8.0	mA	
Output Low Voltage, V_{OL}			0.4	V	$I_{OUT} = -8.0$ mA, $V_{CC} = 3.3$ V
High Level Output Current, I_{OH}		0.1	1	µA	$V_{OUT} = V_{CC}$

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Parameter	Min	Typ	Max	Unit	Test Conditions/Comment
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = –4.0 mA, V_{CC} = 3.3 V
High Level Output Current, I_{OH}		0.1	1	µA	V_{OUT} = V_{CC}
SMBUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.4	V	
Hysteresis		500		mV	
DIGITAL INPUT LOGIC LEVELS (VID0–4)					
Input High Voltage, V_{IH}	1.7			V	
Input Low Voltage, V_{IL}			0.8	V	
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Input High Voltage, V_{IH}	2.0			V	
			5.5	V	Maximum Input Voltage
Input Low Voltage, V_{IL}			0.8	V	
	–0.3			V	Minimum Input Voltage
Hysteresis		0.5		V p-p	
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	–1			µA	V_{IN} = V_{CC}
Input Low Current, I_{IL}			1	µA	V_{IN} = 0
Input Capacitance, C_{IN}		5		pF	
SERIAL BUS TIMING					
Clock Frequency, f_{SCLK}	10		100	kHz	See Figure 1
Glitch Immunity, t_{SW}			50	ns	See Figure 1
Bus Free Time, t_{BUF}	4.7			µs	See Figure 1
Start Setup Time, $t_{SU;STA}$	4.7			µs	See Figure 1
Start Hold Time, $t_{HD;STA}$	4.0			µs	See Figure 1
SCL Low Time, t_{LOW}	4.7			µs	See Figure 1
SCL High Time, t_{HIGH}	4.0		50	µs	See Figure 1
SCL, SDA Rise Time, t_r			1000	ns	See Figure 1
SCL, SDA Fall Time, t_f			300	µs	See Figure 1
Data Setup Time, $t_{SU;DAT}$	250			ns	See Figure 1
Data Hold Time, $t_{HD;DAT}$	300			ns	See Figure 1
Detect Clock Low Timeout, $t_{TIMEOUT}$	15		35	ms	Can Be Optionally Disabled

NOTES
[1]All voltages are measured with respect to GND, unless otherwise specified.
[2]Typicals are at T_A = 40°C and represent the most likely parametric norm.
[3]Logic inputs will accept input high voltages up to V_{MAX} even when the device is operating down to V_{MIN}.
[4]Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge and V_{IH} = 2.0 V for a rising edge.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS*

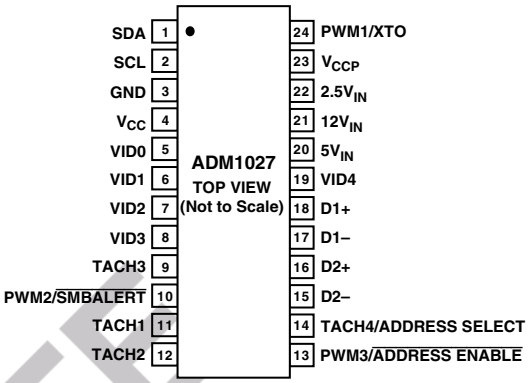
Positive Supply Voltage (V_{CC}) . . . . . 6.5 V
Voltage on 12 V_{IN} Pin . . . . . 20 V
Voltage on Any Other Input or Output Pin . . . . –0.3 V to +6.5 V
Input Current at Any Pin . . . . . ±5 mA
Package Input Current . . . . . ±20 mA
Maximum Junction Temperature ($T_{J\,MAX}$) . . . . . 150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 200°C
ESD Rating . . . . . 2000 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

24-Lead QSOP Package:
θ_{JA} = 123°C/W, θ_{JC} = 27°C/W

PIN CONFIGURATION



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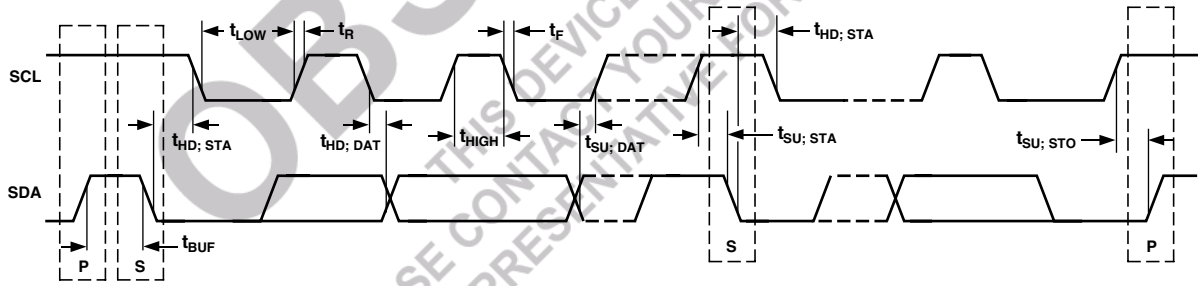

Figure 1. Diagram for Serial Bus Timing

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM1027 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description
1	SDA	Digital I/O (Open-Drain). SMBus bidirectional serial data. Requires SMBus pull-up.
2	SCL	Digital Input (Open-Drain). SMBus serial clock input. Requires SMBus pull-up.
3	GND	Ground Pin for the ADM1027.
4	V_{CC}	Power Supply. Can be powered by 3.3 V standby if monitoring in low power states is required. V_{CC} is also monitored through this pin. The ADM1027 can also be powered from a 5 V supply. Setting Bit 7 of Configuration Register 1 (Reg. 0x40) rescales the V_{CC} input attenuators to correctly measure a 5 V supply.
5	VID0	Digital Input (Open-Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
6	VID1	Digital Input (Open-Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
7	VID2	Digital Input (Open-Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
8	VID3	Digital Input (Open-Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
9	TACH3	Digital Input (Open-Drain). Fan tachometer input to measure speed of Fan 3. Can be reconfigured as an analog input (AIN3) to measure the speed of 2-wire fans.
10	PWM2/$\overline{\text{SMBALERT}}$	Digital Output (Open-Drain). Requires 10 kΩ typical pull-up. Pulsewidth modulated output to control Fan 2 speed. This pin may be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
11	TACH1	Digital Input (Open-Drain). Fan tachometer input to measure speed of Fan 1. Can be reconfigured as an analog input (AIN1) to measure the speed of 2-wire fans.
12	TACH2	Digital Input (Open-Drain). Fan tachometer input to measure speed of Fan 2. Can be reconfigured as an analog input (AIN2) to measure the speed of 2-wire fans.
13	PWM3/$\overline{\text{ADDRESS ENABLE}}$	Digital I/O (Open-Drain). Pulsewidth modulated output to control Fan 3 speed. Requires 10 kΩ typical pull-up. If pulled low on power-up, this places the ADM1027 into address select mode, and the state of Pin 14 will determine the ADM1027's slave address.
14	TACH4/ADDRESS SELECT	Digital Input (Open-Drain). Fan tachometer input to measure speed of Fan 4. Can be reconfigured as an analog input (AIN4) to measure the speed of 2-wire fans. If in address select mode, this pin determines the SMBus device address.
15	D2–	Cathode Connection to Second Thermal Diode.
16	D2+	Anode Connection to Second Thermal Diode.
17	D1–	Cathode Connection to First Thermal Diode.
18	D1+	Anode Connection to First Thermal Diode.
19	VID4	Digital Input (Open-Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
20	$5V_{IN}$	Analog Input. Monitors 5 V power supply.
21	$12V_{IN}$	Analog Input. Monitors 12 V power supply.
22	$2.5V_{IN}$	Analog Input. Monitors 2.5 V supply, typically a chipset voltage.
23	V_{CCP}	Analog Input. Monitors processor core voltage (0 V to 3 V).
24	PWM1/XTO	Digital Output (Open-Drain). Pulsewidth modulated output to control Fan 1 speed. Requires 10 kΩ typical pull-up. Also functions as the output from the XOR tree in XOR test mode.

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FUNCTIONAL DESCRIPTION

General Description

The ADM1027 is a complete systems monitor and multiple fan controller for any system requiring monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has an optional address line for device selection (Pin 14), a serial data line for reading and writing addresses and data (Pin 1), and an input line for the serial clock (Pin 2). All control and programming functions of the ADM1027 are performed over the serial bus. In addition, one of the pins can be reconfigured as an $\overline{\text{SMBALERT}}$ output to indicate out-of-limit conditions.

Measurement Inputs

The device has six measurement inputs, four for voltage and two for temperature. It can also measure its own supply voltage and can measure ambient temperature with its on-chip temperature sensor.

Pins 20 to 23 are analog inputs with on-chip attenuators, configured to monitor 5 V, 12 V, 2.5 V, and the processor core voltage (2.25 V input), respectively.

Power is supplied to the chip via Pin 4, which the system also uses to monitor V_{CC}. In PCs, this pin is normally connected to a 3.3 V standby supply. This pin can, however, be connected to a 5 V supply and monitor it without overranging.

Remote temperature sensing is provided by the D1+/– and D2+/– inputs, to which diode-connected, external temperature-sensing transistors such as a 2N3906 or CPU thermal diode may be connected.

The ADC also accepts input from an on-chip band gap temperature sensor that monitors system ambient temperature.

Sequential Measurement

When the ADM1027 monitoring sequence is started, it cycles sequentially through the measurement of analog inputs and the temperature sensors. Measured values from these inputs are stored in value registers. These can be read out over the serial bus, or can be compared with programmed limits stored in the limit registers. The results of out-of-limit comparisons are stored in the status registers, which can be read over the serial bus to flag out-of-limit conditions.

Processor Voltage ID

Five digital inputs (VID0 to VID4 — Pins 5 to 8 and 19) read the processor Voltage ID code and store it in the VID register, from which it can be read out by the management system over the serial bus. The VID code monitoring function is compatible with both VRM9.x and future VRM10 solutions. The VID code monitoring function is compatible with VRM9.x.

ADM1027 Address Selection

Pin 13 is the dual function PWM3/$\overline{\text{ADDRESS ENABLE}}$ pin. If Pin 13 is pulled low on power-up, the ADM1027 will read the state of Pin 14 (TACH4/ADDRESS SELECT pin) to determine the ADM1027 slave address. If Pin 13 is high on power-up, then the ADM1027 will default to SMBus slave address 0x5C. This function is described later in more detail.

Internal Registers of the ADM1027

A brief description of the ADM1027's principal internal registers follows. More detailed information on the function of each register is given in Tables IV to XXXVI.

Configuration Registers

Provide control and configuration of the ADM1027, including alternate pinout functionality.

Address Pointer Register

Contains the address that selects one of the other internal registers. When writing to the ADM1027, the first byte of data is always a register address, which is written to the Address Pointer Register.

Status Registers

Provide the status of each limit comparison and are used to signal out-of-limit conditions on the temperature, voltage, or fan speed channels. If Pin 10 is configured as $\overline{\text{SMBALERT}}$, then this pin will assert low whenever a status bit gets set.

Interrupt Mask Registers

Allow each interrupt status event to be masked when Pin 10 is configured as an $\overline{\text{SMBALERT}}$ output. This affects only the $\overline{\text{SMBALERT}}$ output and not the bits in the status register.

VID Register

The status of the VID0 to VID4 pins of the processor can be read from this register.

Value and Limit Registers

The results of analog voltage inputs, temperature, and fan speed measurements are stored in these registers, along with their limit values.

Offset Registers

Allow each temperature channel reading to be offset by a twos complement value written to these registers.

T_{MIN} Registers

Program the starting temperature for each fan under automatic fan speed control.

T_{RANGE} Registers

Program the temperature-to-fan speed control slope in automatic Fan Speed Control Mode for each PWM output.

Enhance Acoustics Registers

Allow each PWM output controlling fan to be tweaked to enhance the system's acoustics.

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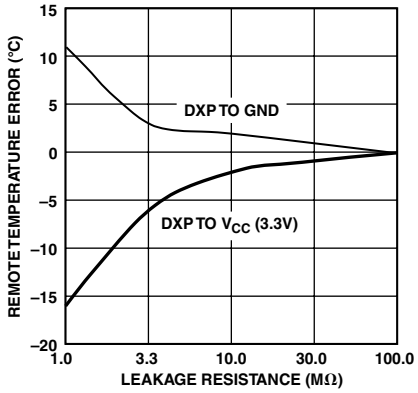
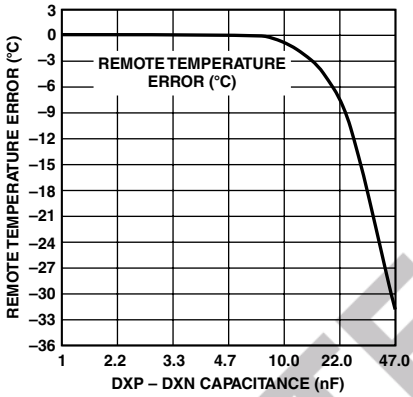
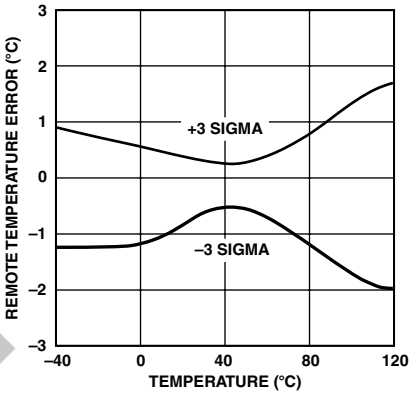


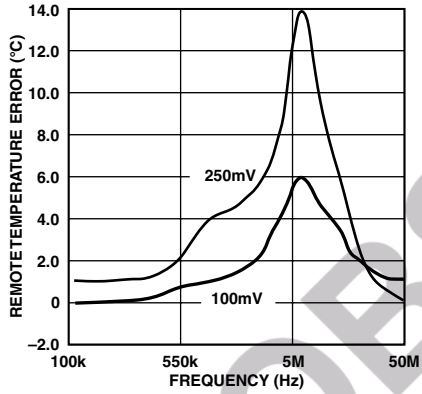
TPC 1. Remote Temperature Error vs. Leakage Resistance



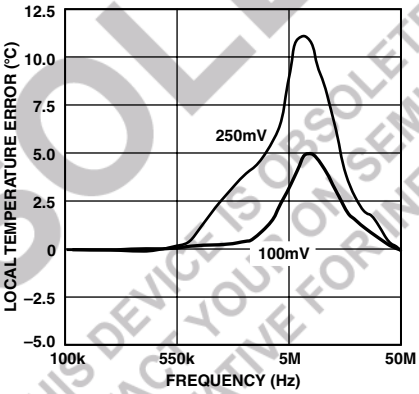
TPC 2. Remote Temperature Error vs. Capacitance between D+ and D–



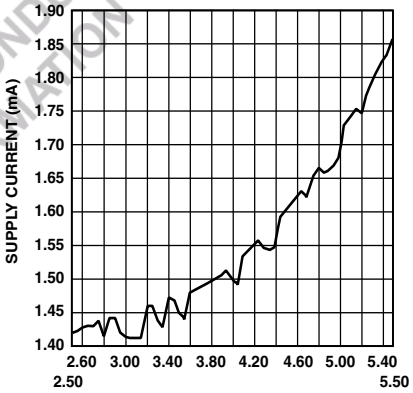
TPC 3. Remote Temperature Error vs. Actual Temperature



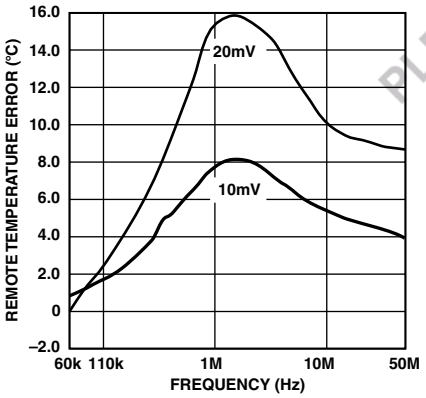
TPC 4. Remote Temperature Error vs. Power Supply Noise Frequency



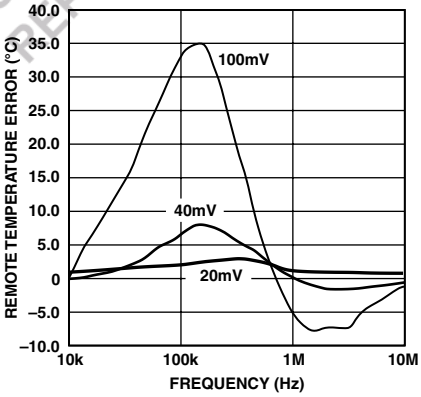
TPC 5. Local Temperature Error vs. Power Supply Noise Frequency



TPC 6. Supply Current vs. Supply Voltage



TPC 7. Remote Temperature Error vs. Differential Mode Noise Frequency



TPC 8. Remote Temperature Error vs. Common Mode Noise Frequency

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SERIAL BUS INTERFACE

Control of the ADM1027 is carried out using the serial System Management Bus (SMBus). The ADM1027 is connected to this bus as a slave device, under the control of a master controller.

The ADM1027 has a 7-bit serial bus address. When the device is powered up with Pin 13 (PWM3/$\overline{\text{ADDRESS ENABLE}}$) high, the ADM1027 will have a default SMBus address of 0101110 or 0x5C. If more than one ADM1027 is to be used in a system, then each ADM1027 should be placed in address select mode by strapping Pin 13 low on power-up. The logic state of Pin 14 then determines the device's SMBus address.

Table I. ADM1027 Address Select Mode

Pin 13 State	Pin 14 State	Address
0	Low (10 kΩ to GND)	0101100 (0x58)
0	High (10 kΩ pull-up)	0101101 (0x5A)
1	Don't Care	0101110 (0x5C) (default)

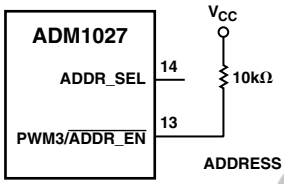

Figure 2. Default SMBus Address = 0x5C

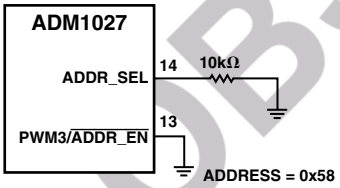

Figure 3. SMBus Address = 0x58 (Pin 14 = 0)

The device address is sampled and latched on the first valid SMBus transaction, so any attempted addressing changes made thereafter will have no immediate effect.

The facility to make hardwired changes to the SMBus slave address allows the user to avoid conflicts with other devices sharing the same serial bus (for example, if more than one ADM1027 is used in a system).

Once the SMBus address has been assigned, these pins return to their original function. However, since the circuits required to set up the SMBus address are unworkable with the PWM and TACH circuits, it would require the use of muxes to switch in and out the correct circuit at the correct time.

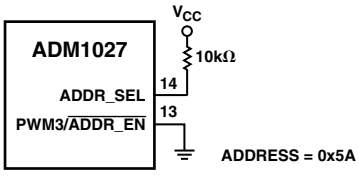

Figure 4. SMBus Address = 0x5A (Pin 14 = 1)

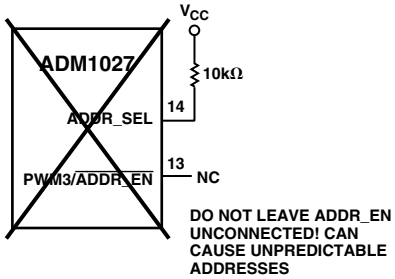

Figure 5. Unpredictable SMBus Address if Pin 13 is Unconnected

Care should be taken to ensure that Pin 13 (PWM3/$\overline{\text{ADDR_EN}}$) is either tied high or low. Leaving Pin 13 floating could cause the ADM1027 to power up with an unexpected address.

Note that if the ADM1027 is placed into address select mode, Pins 13 and 14 can be used as their alternate functions once address assignment has taken place (PWM3, TACH4). Care should be taken using muxes to connect in the appropriate circuit at the appropriate time.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, defined as a high to low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus the R/$\overline{\text{W}}$ bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device.

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{\text{W}}$ bit is a 0, the master will write to the slave device. If the R/$\overline{\text{W}}$ bit is a 1, the master will read from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

3. When all data bytes have been read or written, stop conditions are established. In write mode, the master will pull the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device will override the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a stop condition.

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Any number of bytes of data can be transferred over the serial bus in one operation. However, it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and subsequently cannot be changed without starting a new operation.

In the case of the ADM1027, write operations contain either one or two bytes, and read operations contain one byte and perform the following functions:

To write data to one of the device data registers or read data from it, the address pointer register must be set so the correct data register is addressed, then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, then the write operation contains a second data byte that is written to the register selected by the address pointer register.

This is illustrated in Figure 6. The device address is sent over the bus followed by R/$\overline{W}$ being set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities:

1. If the ADM1027 address pointer register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the ADM1027 as before, but only sending the data byte containing the register address, as data is not to be written to the register. This is shown in Figure 7.

   A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 8.
2. If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, so Figure 7 can be omitted.

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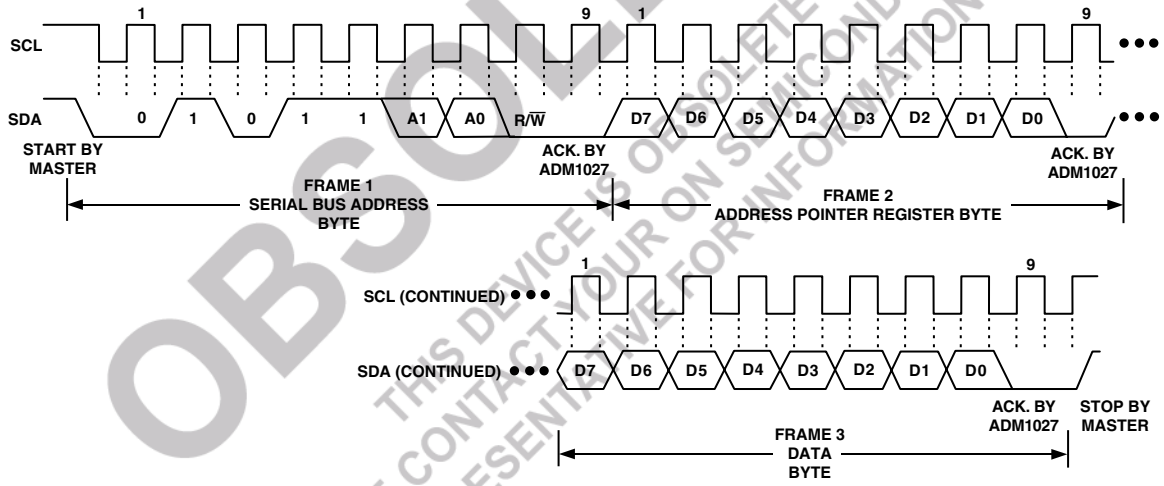


Figure 6. Writing a Register Address to the Address Pointer Register, Then Writing Data to the Selected Register

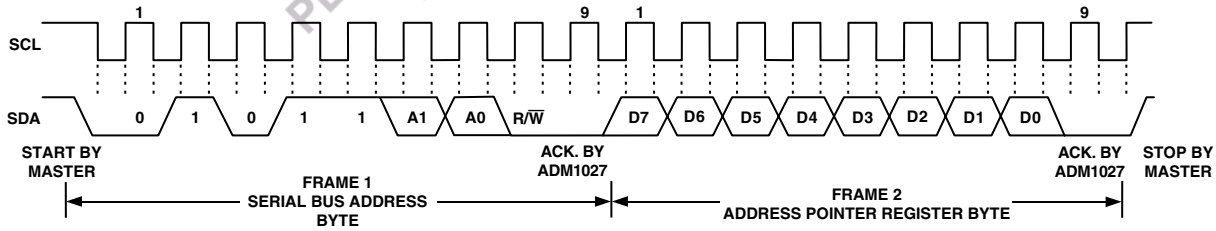
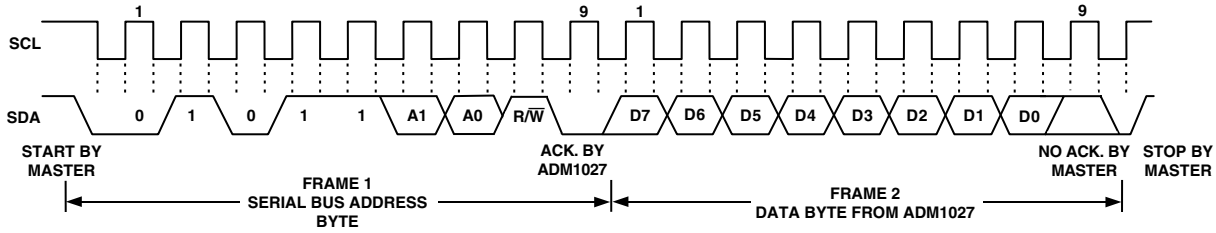


Figure 7. Writing to the Address Pointer Register Only



Notes

1. It is possible to *read* a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to *write* data to a register without writing to the address pointer register, because the first data byte of a write is always written to the address pointer register.
2. In Figures 6 to 8, the serial bus address is shown as the default value 01011(A1)(A0), where A1 and A0 are set by the address select mode function previously defined.
3. In addition to supporting the send byte and receive byte protocols, the ADM1027 also supports the read byte protocol (see System Management Bus specifications Rev. 2.0 for more information).
4. If it is required to perform several read or write operations in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

ADM1027 WRITE OPERATIONS

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADM1027 are discussed below. The following abbreviations are used in the diagrams:

S – START
P – STOP
R – READ
W – WRITE
A – ACKNOWLEDGE
$\overline{A}$ – NO ACKNOWLEDGE

The ADM1027 uses the following SMBus write protocols:

Send Byte

In this operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the ADM1027, the send byte protocol is used to write a register address to RAM for a subsequent single byte read from the same address. This is illustrated in Figure 9.

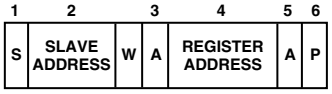


Figure 9. Setting a Register Address for Subsequent Read

If it is required to read data from the register immediately after setting up the address, the master can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

This is illustrated in Figure 10.

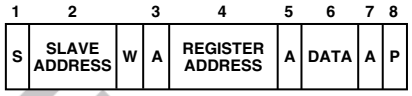


Figure 10. Single Byte Write to a Register

ADM1027 READ OPERATIONS

The ADM1027 uses the following SMBus read protocols:

Receive Byte

This is useful when repeatedly reading a single register. The register address needs to have been set up previously. In this operation, the master device receives a single byte from a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

In the ADM1027, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation.

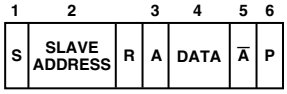


Figure 11. Single Byte Read from a Register

Alert Response Address

Alert Response Address (ARA) is a feature of SMBus devices, which allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as an interrupt output or can be used as an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. Master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and it can be interrogated in the usual way.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address will have priority, in accordance with normal SMBus arbitration.

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5. Once the ADM1027 has responded to the alert response address, the master must read the status registers and the $\overline{\text{SMBALERT}}$ will only be cleared if the error condition has gone away.

SMBus Timeout

The ADM1027 includes an SMBus timeout feature. If there is no SMBus activity for a minimum of 15 ms and a maximum of 35 ms, the ADM1027 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

CONFIGURATION REGISTER 1 – Register 0x40
<6> TODIS = 0; SMBus timeout enabled (default)
<6> TODIS = 1; SMBus timeout disabled

VOLTAGE MEASUREMENT INPUTS

The ADM1027 has four external voltage measurement channels. It can also measure its own supply voltage, V_{CC}.

Pins 20 to 23 are dedicated to measuring 5 V, 12 V, 2.5 V supplies and the processor core voltage V_{CCP} (0 V to 3 V input). The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 4). Setting Bit 7 of Configuration Register 1 (Reg. 0x40) allows a 5 V supply to power the ADM1027 and be measured without overranging the V_{CC} measurement channel. The 2.5 V input can be used to monitor a chipset supply voltage in computer systems.

ANALOG-TO-DIGITAL CONVERTER

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the inputs have built-in attenuators to allow measurement of 2.5 V, 3.3 V, 5 V, 12 V and the processor core voltage V_{CCP}, without any external components. To allow for the tolerance of these supply voltages, the ADC produces an output of 3/4 full scale (768 decimal or 300 hex) for the nominal input voltage, and so has adequate headroom to cope with overvoltages.

INPUT CIRCUITRY

The internal structure for the analog inputs is shown in Figure 12. Each input circuit consists of an input protection diode, an attenuator, and a capacitor to form a first order low-pass filter that gives the input immunity to high frequency noise.

VOLTAGE MEASUREMENT REGISTERS

Reg. 0x20 **2.5 V Reading** = 0x00 default

Reg. 0x21 **V_{CCP} Reading** = 0x00 default

Reg. 0x22 **V_{CC} Reading** = 0x00 default

Reg. 0x23 **5 V Reading** = 0x00 default

Reg. 0x24 **12 V Reading** = 0x00 default

VOLTAGE MEASUREMENT LIMIT REGISTERS

Associated with each voltage measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Reg. 0x44 **2.5 V Low Limit** = 0x00 default

Reg. 0x45 **2.5 V High Limit** = 0xFF default

Reg. 0x46 **V_{CCP} Low Limit** = 0x00 default

Reg. 0x47 **V_{CCP} High Limit** = 0xFF default

Reg. 0x48 **V_{CC} Low Limit** = 0x00 default

Reg. 0x49 **V_{CC} High Limit** = 0xFF default

Reg. 0x4A **5 V Low Limit** = 0x00 default

Reg. 0x4B **5 V High Limit** = 0xFF default

Reg. 0x4C **12 V Low Limit** = 0x00 default

Reg. 0x4D **12 V High Limit** = 0xFF default

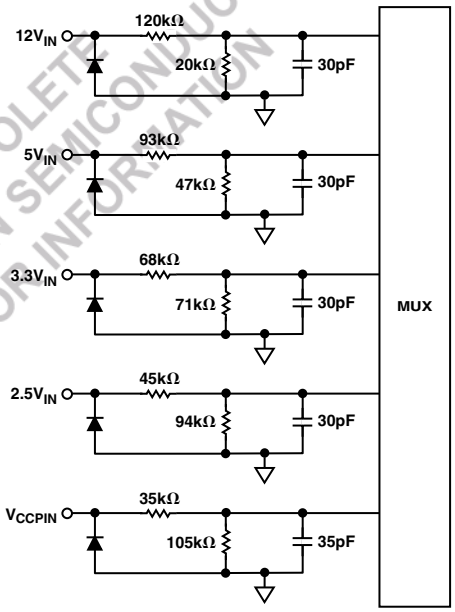

Figure 12. Structure of Analog Inputs

Table II shows the input ranges of the analog inputs and output codes of the 10-bit A/D converter.

When the ADC is running, it samples and converts a voltage input in 711 μs, and averages 16 conversions to reduce noise. Therefore a measurement on any input takes nominally 11.38 ms.

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Table II. 10-Bit A/D Output Code vs. V_{IN}

Input Voltage					A/D Output	
12 V_{IN}	5 V_{IN}	V_{CC} (3.3 V_{IN})*	2.5 V_{IN}	V_{CCPIN}	Decimal	Binary (10 Bits)
<0.0156	<0.0065	<0.0042	<0.0032	<0.00293	0	00000000 00
0.0156 – 0.0312	0.0065 – 0.0130	0.0042 – 0.0085	0.0032 – 0.0065	0.0293 – 0.0058	1	00000000 01
0.0312 – 0.0469	0.0130 – 0.0195	0.0085 – 0.0128	0.0065 – 0.0097	0.0058 – 0.0087	2	00000000 10
0.0469 – 0.0625	0.0195 – 0.0260	0.0128 – 0.0171	0.0097 – 0.0130	0.0087 – 0.0117	3	00000000 11
0.0625 – 0.0781	0.0260 – 0.0325	0.0171 – 0.0214	0.0130 – 0.0162	0.0117 – 0.0146	4	00000001 00
0.0781 – 0.0937	0.0325 – 0.0390	0.0214 – 0.0257	0.0162 – 0.0195	0.0146 – 0.0175	5	00000001 01
0.0937 – 0.1093	0.0390 – 0.0455	0.0257 – 0.0300	0.0195 – 0.0227	0.0175 – 0.0205	6	00000001 10
0.1093 – 0.1250	0.0455 – 0.0521	0.0300 – 0.0343	0.0227 – 0.0260	0.0205 – 0.0234	7	00000001 11
0.1250 – 0.1406	0.0521 – 0.0586	0.0343 – 0.0386	0.0260 – 0.0292	0.0234 – 0.0263	8	00000010 00
4.0000 – 4.0156	1.6675 – 1.6740	1.1000 – 1.1042	0.8325 – 0.8357	0.7500 – 0.7529	256 (1/4 scale)	01000000 00
8.0000 – 8.0156	3.3300 – 3.3415	2.2000 – 2.2042	1.6650 – 1.6682	1.5000 – 1.5029	512 (1/2 scale)	10000000 00
12.0000 – 12.0156	5.0025 – 5.0090	3.3000 – 3.3042	2.4975 – 2.5007	2.2500 – 2.2529	768 (3/4 scale)	11000000 00
15.8281 – 15.8437	6.5983 – 6.6048	4.3527 – 4.3570	3.2942 – 3.2974	2.9677 – 2.9707	1013	11111101 01
15.8437 – 15.8593	6.6048 – 6.6113	4.3570 – 4.3613	3.2974 – 3.3007	2.9707 – 2.9736	1014	11111101 10
15.8593 – 15.8750	6.6113 – 6.6178	4.3613 – 4.3656	3.3007 – 3.3039	2.9736 – 2.9765	1015	11111101 11
15.8750 – 15.8906	6.6178 – 6.6244	4.3656 – 4.3699	3.3039 – 3.3072	2.9765 – 2.9794	1016	11111110 00
15.8906 – 15.9062	6.6244 – 6.6309	4.3699 – 4.3742	3.3072 – 3.3104	2.9794 – 2.9824	1017	11111110 01
15.9062 – 15.9218	6.6309 – 6.6374	4.3742 – 4.3785	3.3104 – 3.3137	2.9824 – 2.9853	1018	11111110 10
15.9218 – 15.9375	6.6374 – 6.4390	4.3785 – 4.3828	3.3137 – 3.3169	2.9853 – 2.9882	1019	11111110 11
15.9375 – 15.9531	6.6439 – 6.6504	4.3828 – 4.3871	3.3169 – 3.3202	2.9882 – 2.9912	1020	11111111 00
15.9531 – 15.9687	6.6504 – 6.6569	4.3871 – 4.3914	3.3202 – 3.3234	2.9912 – 2.9941	1021	11111111 01
15.9687 – 15.9843	6.6569 – 6.6634	4.3914 – 4.3957	3.3234 – 3.3267	2.9941 – 2.9970	1022	11111111 10
>15.9843	>6.6634	>4.3957	>3.3267	>2.9970	1023	11111111 11

*The V_{CC} output codes listed assume that V_{CC} is 3.3 V. If V_{CC} input is reconfigured for 5 V operation (by setting Bit 7 of Configuration Register 1), then the V_{CC} output codes are the same as for the 5 V_{IN} column.

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VID CODE MONITORING

The ADM1027 has five dedicated voltage ID (VID code) inputs. These are digital inputs that can be read back through the VID register (Reg. 0x43) to determine the processor voltage required/being used in the system. Five VID code inputs support VRM9.x solutions.

VID CODE REGISTER – Register 0x43

<0> = VID0 (reflects logic state of Pin 5)

<1> = VID1 (reflects logic state of Pin 6)

<2> = VID2 (reflects logic state of Pin 7)

<3> = VID3 (reflects logic state of Pin 8)

<4> = VID4 (reflects logic state of Pin 19)

ADDITIONAL ADC FUNCTIONS

A number of other functions are available on the ADM1027 to offer the systems designer increased flexibility:

Turn Off Averaging

For each voltage measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. There may be an instance where the user would like to speed up conversions. Setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off. This effectively gives a reading 16× faster than 711 μs, but the reading may be noisier.

Bypass Voltage Input Attenuators

Setting Bit 5 of Configuration Register 2 (Reg. 0x73) removes the attenuation circuitry from the 2.5 V, V_{CCP}, V_{CC}, 5 V, and 12 V inputs. This allows the user to directly connect external sensors or rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single-Channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADM1027 into single-channel ADC conversion mode. In this mode, the ADM1027 can be made to read a single voltage channel only. If the internal ADM1027 clock is used, the selected input will be read every 711 μs. The appropriate ADC channel is selected by writing to Bits <7:5> of TACH1 minimum high byte register (0x55).

Bits <7:5> Reg. 0x55	Channel Selected
000	2.5 V
001	V_{CCP}
010	V_{CC}
011	5 V
100	12 V

Configuration Register 2 (Reg. 0x73)

<4> = 1 Averaging off
<5> = 1 Bypass input attenuators
<6> = 1 Single-channel convert mode

TACH1 Minimum High Byte (Reg. 0x55)

<7:5> Selects ADC channel for single-channel convert mode

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TEMPERATURE MEASUREMENT SYSTEM

Local Temperature Measurement

The ADM1027 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip 10-bit ADC. The 8-bit MSB temperature data is stored in the local temp register (Address 0x26). As both positive and negative temperatures can be measured, the temperature data is stored in twos complement format, as shown in Table III. Theoretically, the temperature sensor and ADC can measure temperatures from –128°C to +127°C with a resolution of 0.25°C. However, this exceeds the operating temperature range of the device (0°C to 105°C), so local temperature measurements outside this range are not possible. Temperature measurement from –127°C to +127°C is possible using a remote sensor.

Remote Temperature Measurement

The ADM1027 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pins 15 and 16, or 17 and 18.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, the absolute value of V_{be} varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass production. The technique used in the ADM1027 is to measure the change in V_{be} when the device is operated at two different currents. This is given by

$$\Delta V_{be} = KT/q \times \ln(N)$$

where:

K is Boltzmann's constant.

q is charge on the carrier.

T is absolute temperature in kelvins.

N is the ratio of the two currents.

Figure 13 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors. It could equally well be a discrete transistor such as a 2N3904/06.

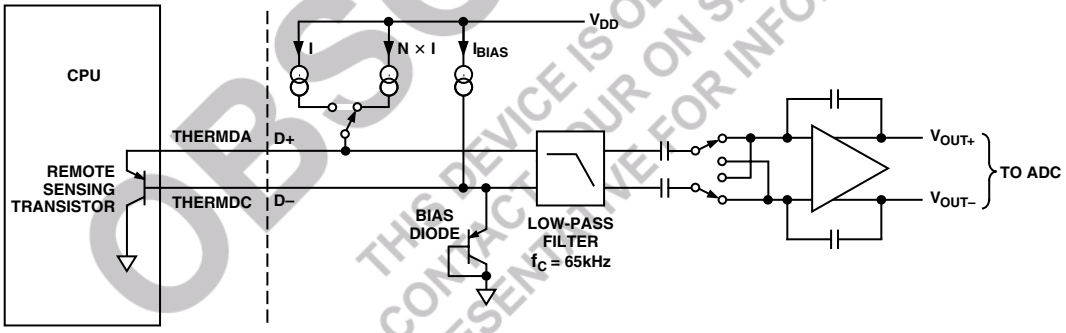

Figure 13. Signal Conditioning for Remote Diode Temperature Sensors

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If a discrete transistor is used, the collector will not be grounded, and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input. Figure 14 shows how to connect the ADM1027 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D– input.

To measure ΔV_{be}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low-pass filter to remove noise, and to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{be}. This voltage is measured by the ADC to give a temperature output in 10-bit, twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles. A remote temperature measurement takes nominally 25.5 ms. The results of remote temperature measurements are stored in 10-bit, twos complement format, as illustrated in Table III. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (Reg. 0x77). This gives temperature readings with a resolution of 0.25°C.

Table III. Temperature Data Format*

Temperature	Digital Output (10-Bit)
–128°C	1000 0000 **00**
–125°C	1000 0011 **00**
–100°C	1001 1100 **00**
–75°C	1011 0101 **00**
–50°C	1100 1110 **00**
–25°C	1110 0111 **00**
–10°C	1111 0110 **00**
0°C	0000 0000 **00**
+10.25°C	0000 1010 **01**
+25.5°C	0001 1001 **10**
+50.75°C	0011 0010 **11**
+75°C	0100 1011 **00**
+100°C	0110 0100 **00**
+125°C	0111 1101 **00**
+127°C	0111 1111 **00**

*Bold denotes 2 LSBs of measurement in Extended Resolution Register 2 (Reg. 0x77) with 0.25°C resolution.

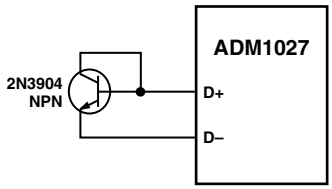

Figure 14a. Measuring Temperature Using an NPN Transistor

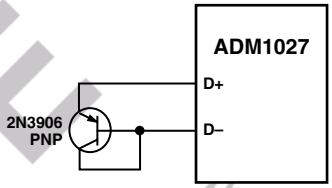

Figure 14b. Measuring Temperature Using a PNP Transistor

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NULLING OUT TEMPERATURE ERRORS

As CPUs run faster, it is getting more difficult to avoid high frequency clocks when routing the D–/D+ traces around a system board. Even when recommended layout guidelines are followed, there may still be temperature errors attributed to noise being coupled onto the D+/D– lines. High frequency noise generally has the effect of giving temperature measurements that are too high by a constant amount. The ADM1027 has temperature offset registers at addresses 0x70, 0x71, and 0x72 for the Remote 1, Local, and Remote 2 temperature channels. By doing a one-time calibration of the system, you can determine the offset caused by system board noise and null it out using the offset registers. The offset registers automatically add a twos complement 8-bit reading to every temperature measurement. The LSB adds a 1°C offset to the temperature reading so the 8-bit register effectively allows temperature offsets of up to ±127°C with a resolution of 1°C. This ensures that the readings in the temperature measurement registers are as accurate as possible.

TEMPERATURE OFFSET REGISTERS

Reg. 0x70 **Remote 1 Temperature Offset** = 0x00 (0°C default)
Reg. 0x71 **Local Temperature Offset** = 0x00 (0°C default)
Reg. 0x72 **Remote 2 Temperature Offset** = 0x00 (0°C default)

TEMPERATURE MEASUREMENT REGISTERS

Reg. 0x25 **Remote 1 Temperature** = 0x80 default
Reg. 0x26 **Local Temperature** = 0x80 default
Reg. 0x27 **Remote 2 Temperature** = 0x80 default

Reg. 0x77 **Extended Resolution 2** = 0x00 default
<7:6> TDM2 = Remote 2 Temperature LSBs
<5:4> LTMP = Local Temperature LSBs
<3:2> TDM1 = Remote 1 Temperature LSBs

TEMPERATURE MEASUREMENT LIMIT REGISTERS

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Reg. 0x4E **Remote 1 Temperature Low Limit** = 0x81 default
Reg. 0x4F **Remote 1 Temperature High Limit** = 0x7F default
Reg. 0x50 **Local Temperature Low Limit** = 0x81 default
Reg. 0x51 **Local Temperature High Limit** = 0x7F default
Reg. 0x52 **Remote 2 Temperature Low Limit** = 0x81 default
Reg. 0x53 **Remote 2 Temperature High Limit** = 0x7F default

READING TEMPERATURE FROM THE ADM1027

It is important to note that temperature can be read from the ADM1027 as an 8-bit value (with 1°C resolution), or as a 10-bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order.

If the 10-bit measurement is required, this involves a 2-register read for each measurement. The extended resolution register (Reg. 0x77) should be read first. This causes all temperature reading registers to be frozen until all temperature reading registers have been read from. This prevents an MSB reading from being updated while its two LSBs are being read, and vice versa.

ADDITIONAL ADC FUNCTIONS

A number of other functions are available on the ADM1027 to offer the systems designer increased flexibility:

Turn Off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. There may be an instance where the user would like to take a very fast measurement, e.g., of CPU temperature. Setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off. This takes a reading every 13 ms. The measurement itself takes 4 ms.

Single-Channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADM1027 into single-channel ADC conversion mode. In this mode, the ADM1027 can be made to read a single temperature channel only. If the internal ADM1027 clock is used, the selected input will be read every 1.4 ms. The appropriate ADC channel is selected by writing to Bits <7:5> of TACH1 minimum high byte register (Reg. 0x55).

Bits <7:5> Reg 0x55	Channel Selected
101	Remote 1 Temp
110	Local Temp
111	Remote 2 Temp

Configuration Register 2 (Reg. 0x73)

<4> = 1 Averaging off
<6> = 1 Single-channel convert mode

TACH1 Minimum High Byte (Reg. 0x55)

<7:5> Selects ADC channel for single-channel convert mode

OVERTEMPERATURE EVENTS

Overtemperature events on any of the temperature channels can be detected and dealt with automatically. Registers 0x6A to 0x6C are the THERM limits. When a temperature exceeds its THERM limit, all fans will run at 100% duty cycle. The fans will stay running at 100% until the temperature drops below THERM – 4°C.

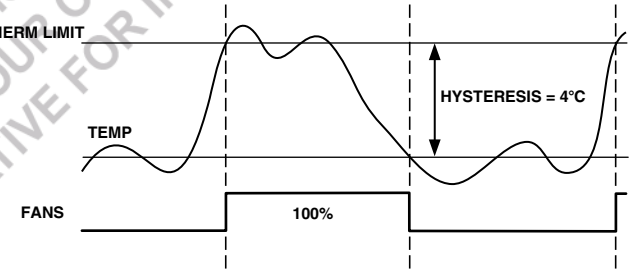

Figure 15. THERM Limit Operation

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SMBALERT, STATUS, AND MASK REGISTERS

SMBALERT CONFIGURATION

Pin 10 of the ADM1027 can be configured as either PWM2 or as an SMBALERT output. The SMBALERT output may be used to signal out-of-limit conditions as explained below. The default state of Pin 10 is PWM2. To configure Pin 10 as SMBALERT:

Configuration Reg. 3 (Addr = 0x78), Bit 0 = 1 = SMBALERT

Configuration Reg. 3 (Addr = 0x78), Bit 0 = 0 = PWM2 = default

LIMIT VALUES

Associated with each measurement channel on the ADM1027 are high and low limits. These can form the basis of system status monitoring; a status bit can be set for any out-of-limit condition and detected by polling the device. Alternatively, SMBALERT interrupts can be generated to flag a processor or microcontroller of out-of-limit conditions.

8-BIT LIMITS

The following is a list of 8-bit limits on the ADM1027:

Voltage Limit Registers

Reg. 0x44 **2.5 V Low Limit** = 0x00 default
Reg. 0x45 **2.5 V High Limit** = 0xFF default
Reg. 0x46 **V_{CCP} Low Limit** = 0x00 default
Reg. 0x47 **V_{CCP} High Limit** = 0xFF default
Reg. 0x48 **V_{CC} Low Limit** = 0x00 default
Reg. 0x49 **V_{CC} High Limit** = 0xFF default
Reg. 0x4A **5 V Low Limit** = 0x00 default
Reg. 0x4B **5 V High Limit** = 0xFF default
Reg. 0x4C **12 V Low Limit** = 0x00 default
Reg. 0x4D **12 V High Limit** = 0xFF default

Temperature Limit Registers

Reg. 0x4E **Remote 1 Temp Low Limit** = 0x81 default
Reg. 0x4F **Remote 1 Temp High Limit** = 0x7F default
Reg. 0x6A **Remote 1 THERM Limit** = 0x64 default
Reg. 0x50 **Local Temp Low Limit** = 0x81 default
Reg. 0x51 **Local Temp High Limit** = 0x7F default
Reg. 0x6B **Local THERM Limit** = 0x64 default
Reg. 0x52 **Remote 2 Temp Low Limit** = 0x81 default
Reg. 0x53 **Remote 2 Temp High Limit** = 0x7F default
Reg. 0x6C **Remote 2 THERM Limit** = 0x64 default

16-Bit Limits

The fan TACH measurements are 16-bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Since fans running underspeed or stalled are normally the only conditions of interest, only high limits exist for fan TACHs. Since fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Fan Limit Registers

Reg. 0x54 **TACH1 Minimum Low Byte** = 0xFF default
Reg. 0x55 **TACH1 Minimum High Byte** = 0xFF default
Reg. 0x56 **TACH2 Minimum Low Byte** = 0xFF default
Reg. 0x57 **TACH2 Minimum High Byte** = 0xFF default
Reg. 0x58 **TACH3 Minimum Low Byte** = 0xFF default
Reg. 0x59 **TACH3 Minimum High Byte** = 0xFF default
Reg. 0x5A **TACH4 Minimum Low Byte** = 0xFF default
Reg. 0x5B **TACH4 Minimum High Byte** = 0xFF default

OUT-OF-LIMIT COMPARISONS

The ADM1027 will measure all parameters in round-robin format and set the appropriate status bit for out-of-limit conditions. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

HIGH LIMIT: > COMPARISON PERFORMED

LOW LIMIT: < OR = COMPARISON PERFORMED

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ANALOG MONITORING CYCLE TIME

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1(Reg. 0x40). The ADC measures each analog input in turn and as each measurement is completed, the result is automatically stored in the appropriate value register. This round-robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

Since the ADC will normally be left to free-run in this manner, the time taken to monitor all the analog inputs will normally not be of interest as the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can easily be calculated.

The total number of channels measured is

- Four dedicated supply voltage inputs
- 3.3 V_{STBY} or 5 V supply (V_{CC} pin)
- Local temperature
- Two remote temperatures

As mentioned previously, the ADC performs round-robin conversions and takes 11.38 ms for each voltage measurement, 12 ms for a local temperature reading, and 25.5 ms for a remote temperature reading.

The total monitoring cycle time for averaged voltage and temperature monitoring is therefore nominally

$(5 \times 11.38) + 12 + (2 \times 25.5) = 120$ ms

Fan TACH measurements are made in parallel and are not synchronized with the analog measurements in any way.

STATUS REGISTERS

The results of limit comparisons are stored in Status Registers 1 and 2. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding status register bit will be cleared to 0. If the measurement is out-of-limits, the corresponding status register bit will be set to 1.

The state of the various measurement channels may be polled by reading the status registers over the serial bus. When 1, Bit 7 (OOL) of Status Register 1 (Reg. 0x41) means that an out-of-limit event has been flagged in Status Register 2. This means that the user need read only Status Register 2 when this bit is set. Alternatively, Pin 10 can be configured as an $\overline{\text{SMBALERT}}$ output. This will automatically notify the system supervisor of an out-of-limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared. Status register bits are “sticky.” Whenever a status bit gets set, indicating an out-of-limit condition, it will remain set even if the event that caused it has gone away (until read). The only way to clear the status bit is to read the status register after the event has gone away. Interrupt status mask registers (Reg. 0x74, 0x75) allow individual interrupt sources to be masked from causing an $\overline{\text{SMBALERT}}$. However, if one of these masked interrupt sources goes out-of-limit, its associated status bit will get set in the interrupt status registers.

STATUS REGISTER 1 (REG. 0x41)

Bit 7 (OOL) = 1, denotes a bit in Status Register 2 is set and Status Register 2 should be read.

Bit 6 (R2T) = 1, Remote 2 temp high or low limit has been exceeded.

Bit 5 (LT) = 1, Local temp high or low limit has been exceeded.

Bit 4 (R1T) = 1, Remote 1 temp high or low limit has been exceeded.

Bit 3 (5 V) = 1, 5 V high or low limit has been exceeded.

Bit 2 (V_{CC}) = 1, V_{CC} high or low limit has been exceeded.

Bit 1 (V_{CCP}) = 1, V_{CCP} high or low limit has been exceeded.

Bit 0 (2.5 V) = 1, 2.5 V high or low limit has been exceeded.

STATUS REGISTER 2 (REG. 0x42)

Bit 7 (D2) = 1, indicates an open or short on D2+/D2– inputs.

Bit 6 (D1) = 1, indicates an open or short on D2+/D2– inputs.

Bit 5 (FAN4) = 1, indicates Fan 4 has dropped below minimum speed.

Bit 4 (FAN3) = 1, indicates Fan 3 has dropped below minimum speed.

Bit 3 (FAN2) = 1, indicates Fan 2 has dropped below minimum speed.

Bit 2 (FAN1) = 1, indicates Fan 1 has dropped below minimum speed.

Bit 1 (OVT) = 1, indicates that a THERM overtemperature limit has been exceeded.

Bit 0 (12 V) = 1, 12 V high or low limit has been exceeded.

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SMBALERT INTERRUPT BEHAVIOR

The ADM1027 can be polled for status, or an SMBALERT interrupt can be generated for out-of-limit conditions. It is important to note how the SMBALERT output and status bits behave when writing interrupt handler software.

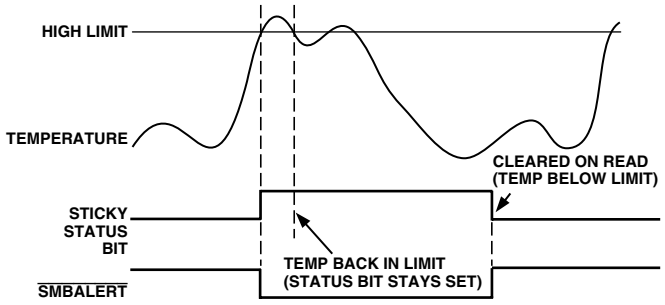

Figure 16. SMBALERT and Status Bit Behavior

Figure 16 shows how the SMBALERT output and sticky status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition subsides and the status register is read. The status bits are referred to as sticky since they remain set until read by software. This ensures that an out-of-limit event cannot be missed if software is polling the device periodically. Note that the SMBALERT output remains low for the entire duration that a reading is out-of-limit and until the status register has been read. This has implications on how software handles the interrupt.

HANDLING SMBALERT INTERRUPTS

To prevent the system from being tied up servicing interrupts, it is recommend to handle the SMBALERT interrupt as follows:

1. Detect the SMBALERT assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (Reg. 0x74, 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This will cause the SMBALERT output and status bits to behave as shown in Figure 17.

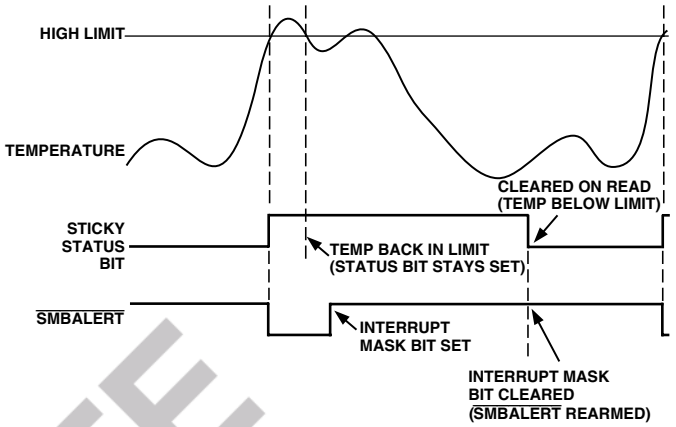

Figure 17. How Masking the Interrupt Source Affects SMBALERT Output

MASKING INTERRUPT SOURCES

Interrupt Mask Registers 1 and 2 are located at Addresses 0x74 and 0x75. These allow individual interrupt sources to be masked out to prevent SMBALERT interrupts. Note that masking an interrupt source prevents only the SMBALERT output from being asserted; the appropriate status bit will be set as normal.

INTERRUPT MASK REGISTER 1 (REG. 0x74)

Bit 7 (OOL) = 1, set this bit to 1 to allow masking of interrupts by Status Register 2. If this bit = 0, then setting a bit in Mask Register 2 to 1 will have no effect.

Bit 6 (R2T) = 1, masks SMBALERT for Remote 2 temperature.

Bit 5 (LT) = 1, masks SMBALERT for local temperature.

Bit 4 (R1T) = 1, masks SMBALERT for Remote 1 temperature.

Bit 3 (5 V) = 1, masks SMBALERT for 5 V channel.

Bit 2 (V_{CC}) = 1, masks SMBALERT for V_{CC} channel.

Bit 1 (V_{CCP}) = 1, masks SMBALERT for V_{CCP} channel.

Bit 0 (2.5 V) = 1, masks SMBALERT for 2.5 V channel.

INTERRUPT MASK REGISTER 2 (REG. 0x75)

Bit 7 (D2) = 1, masks SMBALERT for Diode 2 errors.

Bit 6 (D1) = 1, masks SMBALERT for Diode 1 errors.

Bit 5 (FAN4) = 1, masks SMBALERT for Fan 4.

Bit 4 (FAN3) = 1, masks SMBALERT for Fan 3.

Bit 3 (FAN2) = 1, masks SMBALERT for Fan 2.

Bit 2 (FAN1) = 1, masks SMBALERT for Fan 1.

Bit 1 (OVT) = 1, masks SMBALERT for overtemperature (exceeding THERM limits).

Bit 0 (12 V) = 1, masks SMBALERT for 12 V channel.

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FAN DRIVE CIRCUITRY

Fan Drive Using PWM Control

The ADM1027 uses Pulsewidth Modulation (PWM) to control fan speed. This relies on varying the duty cycle (or on/off ratio) of a square wave applied to the fan to vary the fan speed. The external circuitry required to drive a fan using PWM control is extremely simple. A single NMOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan being driven. Typical notebook fans draw a nominal 170 mA, so SOT devices can be used where board space is a concern. In desktops, fans can typically draw 250 mA to 300 mA each. If you drive several fans in parallel from a single PWM output or drive larger server fans, the MOSFET will need to handle the higher current requirements. The only other stipulation is that the MOSFET should have a gate voltage drive, V_{GS} < 3.3 V for direct interfacing to the PWM_OUT pin. V_{GS} can be greater than 3.3 V as long as the pull-up on the gate is tied to 5 V. The MOSFET should also have a low on resistance to ensure that there is not significant voltage drop across the FET. This would reduce the voltage applied across the fan and thus the maximum operating speed of the fan.

Figure 18 shows how a 3-wire fan may be driven using PWM control.

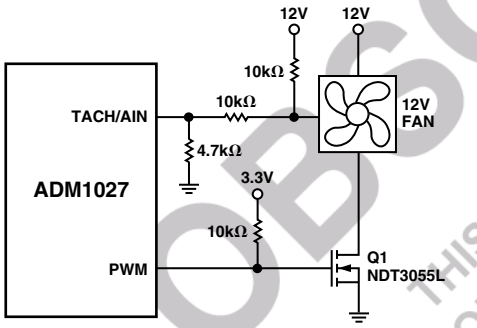

Figure 18. Driving a 3-Wire Fan Using an N-Channel MOSFET

Figure 18 uses a 10 kΩ pull-up resistor for the TACH signal. This assumes that the TACH signal is open-collector from the fan. In all cases, the TACH signal from the fan *must* be kept below 5 V maximum to prevent damaging the ADM1027. If in doubt as to whether the fan used has an open-collector or totem pole TACH output, use one of the input signal conditioning circuits shown in the Fan Speed Measurement section.

Figure 19 shows a fan drive circuit using an NPN transistor such as a general-purpose MMBT2222. While these devices are inexpensive, they tend to have much lower current handling capabilities and higher on resistance than MOSFETs. When choosing a transistor, care should be taken to ensure that it meets the fan's current requirements. Ensure that the base resistor is chosen such that the transistor is saturated when the fan is powered on.

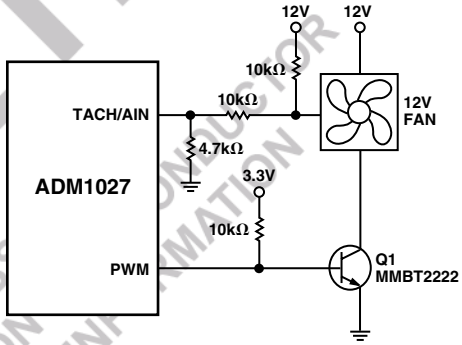

Figure 19. Driving a 3-Wire Fan Using an NPN Transistor

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Driving 2 Fans From PWM3

Note that the ADM1027 has four TACH inputs available for fan speed measurement, but only three PWM drive outputs. If a fourth fan is being used in the system, it should be driven from the PWM3 output in parallel with the third fan. Figure 20 shows how to drive two fans in parallel using low cost NPN transistors. Figure 21 is the equivalent circuit using the NDT3055L MOSFET. Note that since the MOSFET can handle up to 3.5 A, it is simply a matter of connecting another fan directly in parallel with the first.

Care should be taken in designing drive circuits with transistors and FETs to ensure that the PWM pins are not required to source current, and that they sink less than the 8 mA max current specified on the data sheet.

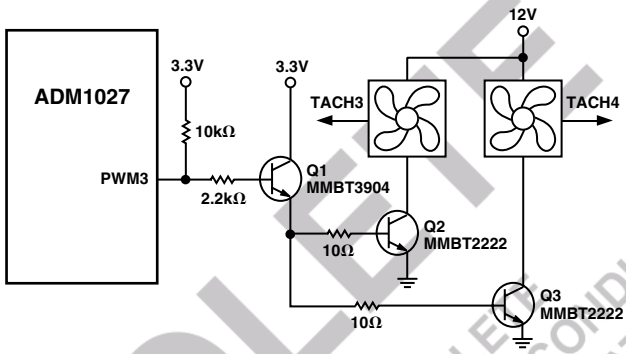

Figure 20. Interfacing Two Fans in Parallel to the PWM3 Output Using Low Cost NPN Transistors

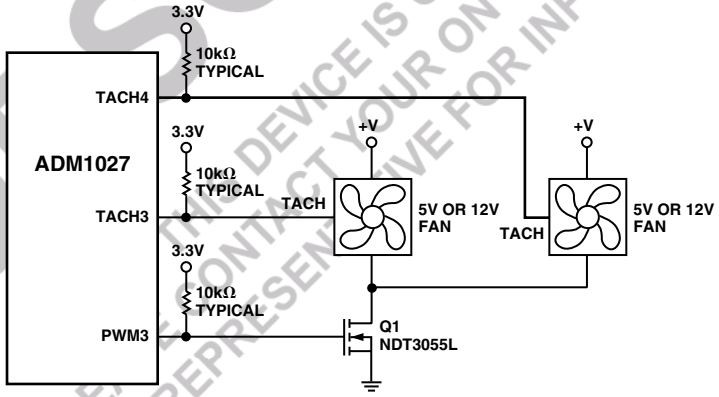

Figure 21. Interfacing Two Fans in Parallel to the PWM3 Output Using a Single N-Channel MOSFET

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Driving 2-Wire Fans

Figure 22 shows how a 2-wire fan may be connected to the ADM1027. This circuit allows the speed of a 2-wire fan to be measured even though the fan has no dedicated TACH signal. A series resistor, R_{SENSE}, in the fan circuit converts the fan commutation pulses into a voltage. This is ac-coupled into the ADM1027 through the 0.01 μF capacitor. On-chip signal conditioning allows accurate monitoring of fan speed. For fans drawing approximately 200 mA, a 2 Ω R_{SENSE} value is suitable. For fans that draw more current, such as larger desktop or server fans, R_{SENSE} may be reduced. The smaller R_{SENSE} is the better, since more voltage will be developed across the fan, and the fan will spin faster. Figure 23 shows a typical plot of the sensing waveform at a TACH/AIN pin. The most important thing is that the negative going spikes are more than 250 mV in amplitude. This allows fan speed to be reliably determined.

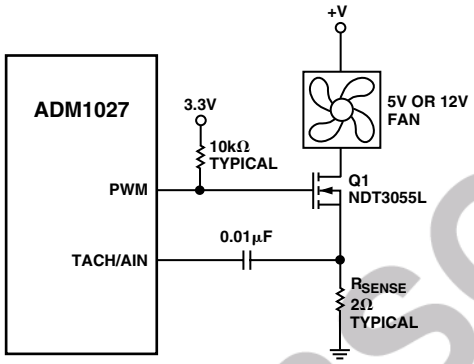

Figure 22. Driving a 2-Wire Fan

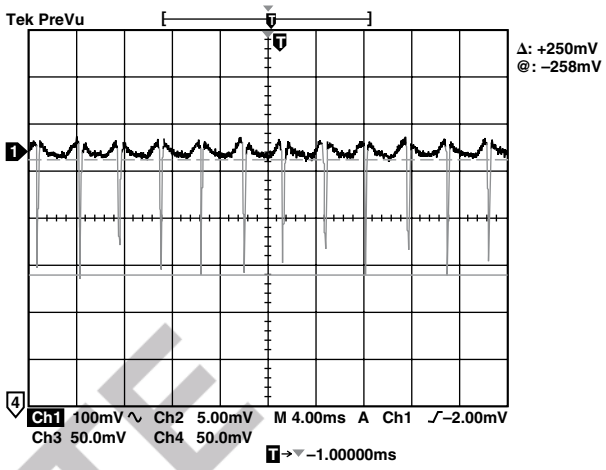

Figure 23. Fan Speed Sensing Waveform at TACH/AIN Pin

Laying Out for 2-Wire and 3-Wire Fans

Figure 24 shows how to lay out a common circuit arrangement for 2-wire and 3-wire fans. Some components will not be populated depending on whether a 2-wire or 3-wire fan is being used.

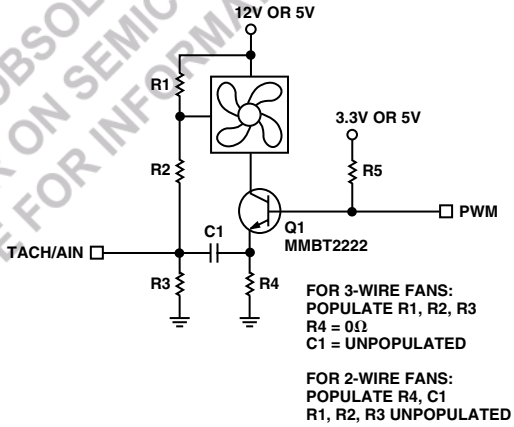

Figure 24. Planning for 2-Wire or 3-Wire Fans on a PCB

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FAN SPEED MEASUREMENTS

TACH Inputs

Pins 11, 12, 9, and 14 are open-drain TACH inputs intended for fan speed measurement.

Signal conditioning in the ADM1027 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 V to 5 V, even where V_{CC} is less than 5 V. In the event that these inputs are supplied from fan outputs that exceed 0 V to 5 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figures 25a to 25d show circuits for most common fan TACH outputs. If the fan TACH output has a resistive pull-up to V_{CC}, it can be connected directly to the fan input, as shown in Figure 25a.

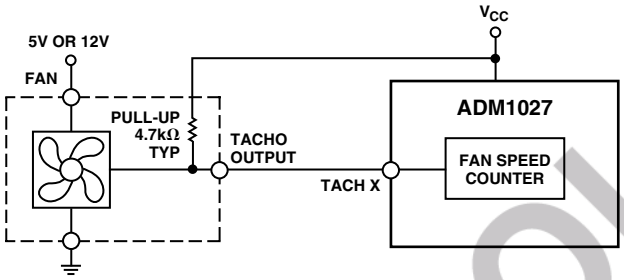

Figure 25a. Fan With TACH Pull-Up to +V_{CC}

If the fan output has a resistive pull-up to 12 V (or other voltage greater than 5 V), then the fan output can be clamped with a Zener diode, as shown in Figure 25b. The Zener diode voltage should be chosen so that it is greater than V_{IH} of the TACH input but less than 5 V, allowing for the voltage tolerance of the Zener. A value of between 3 V and 5 V is suitable.

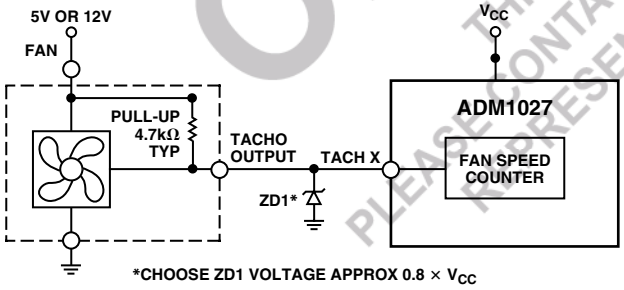

Figure 25b. Fan with TACH Pull-Up to Voltage > 5 V (e.g., 12 V) Clamped with Zener Diode

If the fan has a strong pull-up (less than 1 kΩ) to 12 V, or a totem-pole output, then a series resistor can be added to limit the Zener current, as shown in Figure 25c. Alternatively, a resistive attenuator may be used, as shown in Figure 25d.

R1 and R2 should be chosen such that

$$2\,V < V_{PULLUP} \times R2 / \left(R_{PULLUP} + R1 + R2\right) > 5\,V$$

The fan inputs have an input resistance of nominally 160 kΩ to ground; this should be taken into account when calculating resistor values.

With a pull-up voltage of 12 V and pull-up resistor less than 1 kΩ, suitable values for R1 and R2 would be 100 kΩ and 47 kΩ. This will give a high input voltage of 3.83 V.

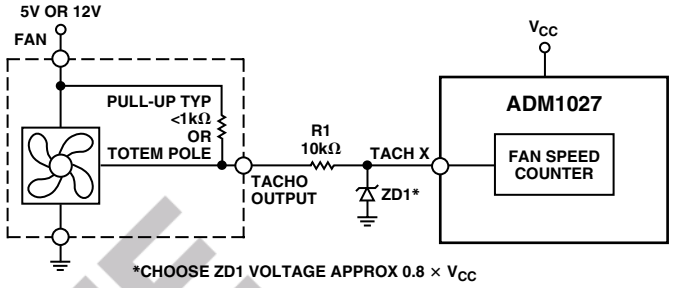

Figure 25c. Fan with Strong TACH Pull-Up to > V_{CC} or Totem-Pole Output, Clamped with Zener and Resistor

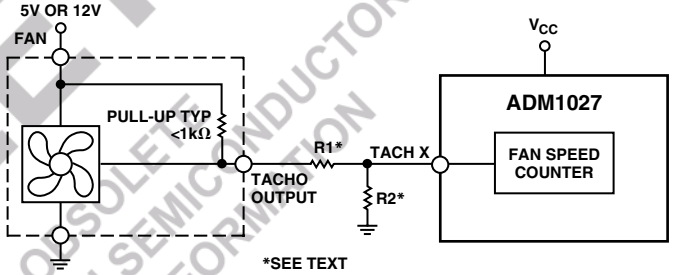

Figure 25d. Fan with Strong TACH Pull-Up to > V_{CC} or Totem-Pole Output, Attenuated with R1/R2

Fan Speed Measurement

The fan counter does not count the fan TACH output pulses directly because the fan speed may be less than 1000 RPM and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 90 kHz oscillator into the input of a 16-bit counter for N periods of the fan TACHO output (Figure 26), so the accumulated count is actually proportional to the fan tachometer period and inversely proportional to the fan speed.

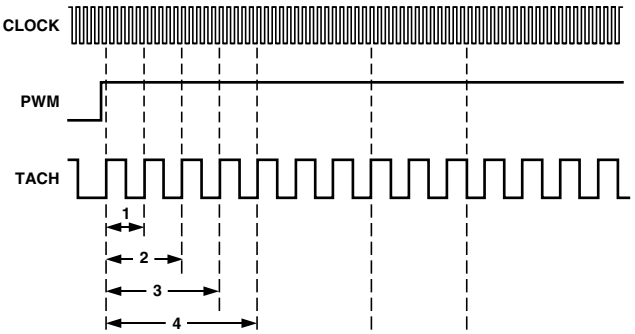

Figure 26. Fan Speed Measurement

N, the number of pulses counted, is determined by the settings of Register 0x7B (fan pulses per revolution register). This register contains two bits for each fan, allowing 1, 2 (default), 3, or 4 TACH pulses to be counted.

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Fan Speed Measurement Registers
The fan tachometer readings are 16-bit values consisting of a 2-byte read from the ADM1027.

Reg. 0x28 **TACH1 Low Byte** = 0x00 default

Reg. 0x29 **TACH1 High Byte** = 0x00 default

Reg. 0x2A **TACH2 Low Byte** = 0x00 default

Reg. 0x2B **TACH2 High Byte** = 0x00 default

Reg. 0x2C **TACH3 Low Byte** = 0x00 default

Reg. 0x2D **TACH3 High Byte** = 0x00 default

Reg. 0x2E **TACH4 Low Byte** = 0x00 default

Reg. 0x2F **TACH4 High Byte** = 0x00 default

Reading Fan Speed From the ADM1027
If fan speeds are being measured, this involves a 2-register read for each measurement. The low byte should be read first. This causes the high byte to be frozen until both high and low byte registers have been read from. This prevents erroneous TACH readings.

The fan tachometer reading registers report back the number of 11.11 μs period clocks (90 kHz oscillator) gated to the fan speed counter, from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse (assuming two pulses per revolution are being counted). Since the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan is actually running. A 16-bit fan tachometer reading of 0xFFFF indicates that the fan either has stalled or is running very slowly (< 100 RPM).

HIGH LIMIT: > COMPARISON PERFORMED

Since actual fan TACH period is being measured, exceeding a fan TACH limit by 1 will set the appropriate status bit and can be used to generate an $\overline{\text{SMBALERT}}$.

Fan Tach Limit Registers
The fan TACH limit registers are 16-bit values consisting of two bytes.

Reg. 0x54 **TACH1 Minimum Low Byte** = 0xFF default

Reg. 0x55 **TACH1 Minimum High Byte** = 0xFF default

Reg. 0x56 **TACH2 Minimum Low Byte** = 0xFF default

Reg. 0x57 **TACH2 Minimum High Byte** = 0xFF default

Reg. 0x58 **TACH3 Minimum Low Byte** = 0xFF default

Reg. 0x59 **TACH3 Minimum High Byte** = 0xFF default

Reg. 0x5A **TACH4 Minimum Low Byte** = 0xFF default

Reg. 0x5B **TACH4 Minimum High Byte** = 0xFF default

Fan Speed Measurement Rate
The fan TACH readings are normally updated once every second.

The fast bit (Bit 3) of Configuration Register 3 (Reg. 0x78), when set, updates the fan TACH readings every 250 ms.

If any of the fans are not being driven by a PWM channel but are powered directly from 5 V or 12 V, their associated dc bit in Configuration Register 3 should be set. This allows TACH readings to be taken on a continuous basis for fans connected directly to a dc source.

Calculating Fan Speed
Assuming a fan with 2 pulses/revolution (and 2 pulses/rev being measured), fan speed is calculated by:

$$Fan\ Speed\ (RPM) = (90{,}000 \times 60)/Fan\ Tach\ Reading$$

where *Fan Tach Reading* = 16-bit fan tachometer reading.

Example:
TACH1 high byte (Reg. 0x29) = 0x17
TACH1 low byte (Reg. 0x28) = 0xFF
What is Fan 1 speed in RPM?

Fan 1 TACH reading = 0x17FF = 6143 decimal
RPM = (f × 60)/fan 1 TACH reading
RPM = (90000 × 60)/6143
Fan Speed = 879 RPM

FAN PULSES PER REVOLUTION
Different fan models can output either 1, 2, 3, or 4 TACH pulses per revolution. Once the number of fan TACH pulses has been determined, it can be programmed into the fan pulses per revolution register (Reg. 0x7B) for each fan. Alternatively, this register can be used to determine the number or pulses/revolution output by a given fan. By plotting fan speed measurements at 100% speed with different pulses/rev setting, the smoothest graph with the lowest ripple determines the correct pulses/rev value.

Fan Pulses Per Revolution Register

<1:0> FAN1 default = 2 pulses/rev

<3:2> FAN2 default = 2 pulses/rev

<5:4> FAN3 default = 2 pulses/rev

<7:6> FAN4 default = 2 pulses/rev

00 = 1 pulse/rev

01 = 2 pulses/rev

10 = 3 pulses/rev

11 = 4 pulses/rev

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2-Wire Fan Speed Measurements
The ADM1027 is capable of measuring the speed of 2-wire fans, i.e., fans without TACH outputs. To do this, the fan must be interfaced as shown in the Fan Drive Circuitry section of the data sheet. In this case, the TACH inputs need to be reprogrammed as analog inputs, AIN.

CONFIGURATION REGISTER 2 (REG. 0x73)
Bit 3 (AIN4) = 1, Pin 14 is reconfigured to measure the speed of a 2-wire fan using an external sensing resistor and coupling capacitor.

Bit 2 (AIN3) = 1, Pin 9 is reconfigured to measure the speed of a 2-wire fan using an external sensing resistor and coupling capacitor.

Bit 1 (AIN2) = 1, Pin 12 is reconfigured to measure the speed of a 2-wire fan using an external sensing resistor and coupling capacitor.

Bit 0 (AIN1) = 1, Pin 11 is reconfigured to measure the speed of a 2-wire fan using an external sensing resistor and coupling capacitor.

FAN SPIN-UP
The ADM1027 has a unique fan spin-up function. It will spin the fan at 100% PWM duty cycle until two TACH pulses are detected on the TACH input. Once two pulses have been detected, the PWM duty cycle will go to the expected running value, e.g., 33%. The advantage of this is that fans have different spin-up characteristics and will take different times to overcome inertia. The ADM1027 just runs the fans fast enough to overcome inertia and will be quieter on spin-up than fans programmed to spin up for a given spin-up time.

FAN START-UP TIMEOUT
To prevent false interrupts being generated as a fan spins up (since it is below running speed), the ADM1027 includes a fan start-up timeout function. This is the time limit allowed for two TACH pulses to be detected on spin-up. For example, if 2 seconds fan start-up timeout is chosen, and no TACH pulses occur within 2 seconds of the start of spin-up, a fan fault is detected and flagged in the interrupt status registers.

PWM1 CONFIGURATION (REG. 0x5C)
<2:0> SPIN These bits control the start-up timeout for PWM1.
000 = No startup timeout
001 = 100 ms
010 = 250 ms (default)
011 = 400 ms
101 = 1 sec
110 = 2 sec
111 = 4 sec

PWM2 CONFIGURATION (REG. 0x5D)
<2:0> SPIN These bits control the start-up timeout for PWM2.
000 = No startup timeout
001 = 100 ms
010 = 250 ms (default)
011 = 400 ms
101 = 1 sec
110 = 2 sec
111 = 4 sec

PWM3 CONFIGURATION (REG. 0x5E)
<2:0> SPIN These bits control the start-up timeout for PWM3.
000 = No startup timeout
001 = 100 ms
010 = 250 ms (default)
011 = 400 ms
101 = 1 sec
110 = 2 sec
111 = 4 sec

Disabling Fan Start-Up Timeout
Although fan start-up makes fan spin-ups much quieter than fixed-time spin-ups, the option is there to use fixed spin-up times. Bit 5 (FSPDIS) = 1 in Configuration Register 1 (Reg. 0x40) disables the spin-up for two TACH pulses. Instead, the fan will spin up for the fixed time as selected in registers 0x5C to 0x5E.

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MANUAL FAN SPEED CONTROL MODE

PWM Logic State
The PWM outputs can be programmed to be high for 100% duty cycle (noninverted) or low for 100% duty cycle (inverted).

PWM1 Configuration (Reg. 0x5C)
<4> INV 0 = logic high for 100% PWM duty cycle
1 = logic low for 100% PWM duty cycle

PWM2 Configuration (Reg. 0x5D)
<4> INV 0 = logic high for 100% PWM duty cycle
1 = logic low for 100% PWM duty cycle

PWM3 Configuration (Reg. 0x5E)
<4> INV 0 = logic high for 100% PWM duty cycle
1 = logic low for 100% PWM duty cycle

PWM Drive Frequency
The PWM drive frequency can be adjusted for the application. Registers 0x5F to 0x61 configure the PWM frequency for PWM1 to PWM3, respectively.

PWM1 FREQUENCY REGISTERS (REG. 0x5F to 0x61)

<2:0> FREQ
000 = 11.0 Hz
001 = 14.7 Hz
010 = 22.1 Hz
011 = 29.4 Hz
100 = 35.3 Hz (default)
101 = 44.1 Hz
110 = 58.8 Hz
111 = 88.2 Hz

Manual Fan Speed Control
The ADM1027 allows the duty cycle of any PWM output to be manually adjusted. This can be useful if you want to change fan speed in software or want to adjust PWM duty cycle output for test purposes. Bits <7:5> of Registers 0x5C to 0x5E (PWM configuration) control the behavior of each PWM output.

PWM CONFIGURATION (REG. 0x5C to 0x5E)
<7:5> BHVR 111 = Manual Mode

Once under manual control, each PWM output may be manually updated by writing to Registers 0x30 to 0x32 (PWMx current duty cycle registers).

Programming the PWM Current Duty Cycle Registers
The PWM current duty cycle registers are 8-bit registers that allow the PWM duty cycle for each output to be set anywhere from 0% to 100%. This allows the PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by

$$Value\,(decimal) = PWM_{MIN} / 0.39$$

Example 1: for a PWM duty cycle of 50%,
Value (decimal) = 50/0.39 = 128 *decimal*
Value = 128 decimal or 80 hex.

Example 2: for a PWM duty cycle of 33%,
Value (decimal) = 33/0.39 = 85 *decimal*
Value = 85 decimal or 54 hex.

PWM Duty Cycle Registers
Reg. 0x30 **PWM1 Duty Cycle** = 0xFF (100% default)
Reg. 0x31 **PWM2 Duty Cycle** = 0xFF (100% default)
Reg. 0x32 **PWM3 Duty Cycle** = 0xFF (100% default)

By reading the PWMx current duty cycle registers, you can keep track of the current duty cycle on each PWM output, even when the fans are running in automatic fan speed control mode or acoustic enhancement mode.

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AUTOMATIC FAN SPEED CONTROL MODE

The ADM1027 has a local temperature sensor and two remote temperature channels that may be connected to an on-chip diode-connected transistor on a CPU. These three temperature channels may be used as the basis for automatic fan speed control to drive fans using pulsewidth modulation (PWM). In general, the greater the number of fans in a system, the better the cooling, but to the detriment of system acoustics. Automatic fan speed control reduces acoustic noise by optimizing fan speed according to measured temperature. Reducing fan speed can also decrease system current consumption. The automatic fan speed control mode is very flexible, owing to the number of programmable parameters, including T_{MIN} and T_{RANGE}, as discussed in detail later. The T_{MIN} and T_{RANGE} values chosen for a given fan are critical, since these define the thermal characteristics of the system. The thermal validation of the system is one of the most important steps of the design process, so these values should be carefully selected.

The aim of this section is not only to provide the system designer with an understanding of the automatic fan control loop, but also to provide step-by-step guidance as to how to most effectively evaluate and select the critical system parameters. To optimize the system characteristics, the designer needs to give some forethought to how the system will be configured, e.g., the number of fans, where they are located, and what temperatures are being measured in the particular system. The mechanical or thermal engineer who is tasked with the actual system evaluation should also be involved at the beginning of the process.

Automatic Fan Control Overview

Figure 27 gives a top-level overview of the automatic fan control circuitry on the ADM1027. From a systems-level perspective, up to three system temperatures can be monitored and used to control three PWM outputs. The three PWM outputs can be used to control up to four fans. The ADM1027 allows the speed of four fans to be monitored. The right side of the block diagram shows controls that are fan-specific. The designer has control over individual parameters such as minimum PWM duty cycle, fan speed failure thresholds, and even ramp control of the PWM outputs. This ultimately allows graceful fan speed changes that are less perceptible to the system user.

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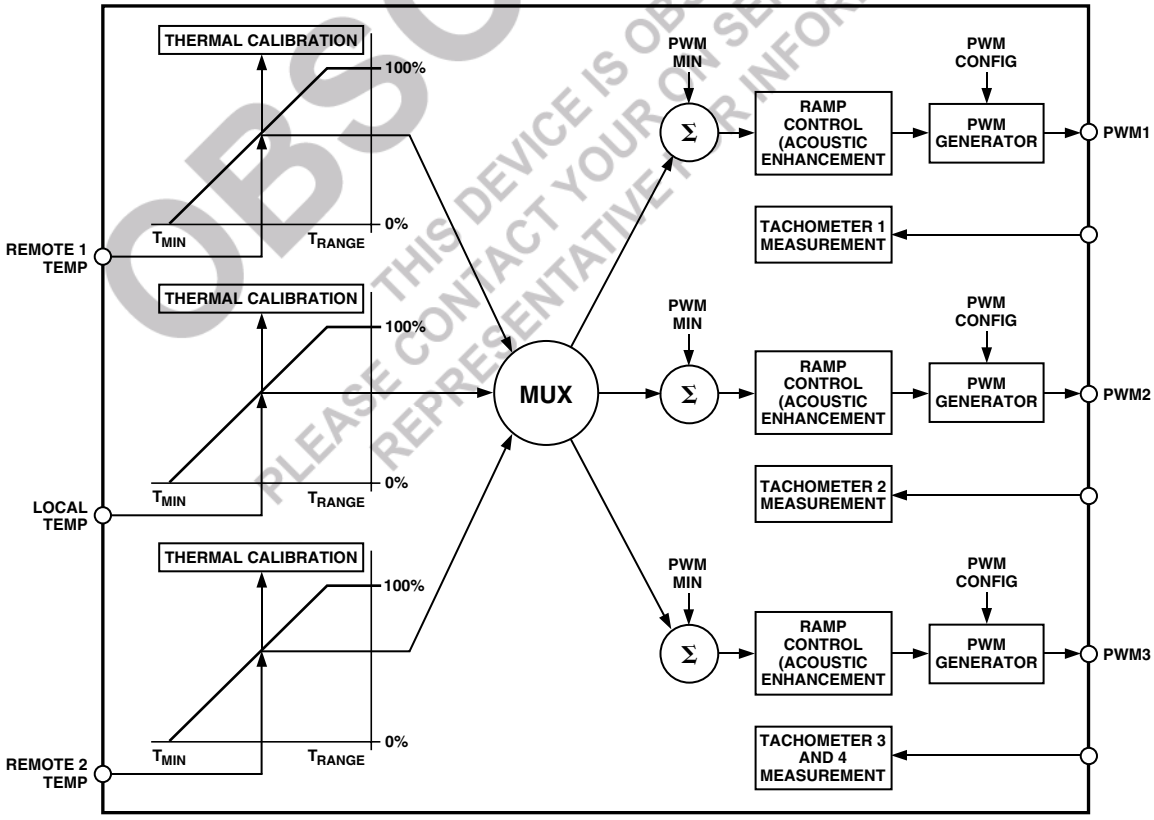

Figure 27. Automatic Fan Control Block Diagram

Step 1

Determine the Hardware Configuration

Essentially this means choosing whether to use Pin 10 as a PWM2 output or as an $\overline{\text{SMBALERT}}$ output and deciding which SMBus address is to be used. To set Pin 10 as $\overline{\text{SMBALERT}}$, set Bit 0 of Configuration Register 3 (Addr = 0x78) equal to 1. The default state is PWM2, where this bit equals 0.

It also refers to the layout recommendations of the ADM1027 on a motherboard, for example.

ADM1027 Placement Considerations

Motherboards are electrically noisy environments, and care must be taken to protect the analog inputs from noise, particularly the D+/D– lines of a remote diode sensor. The following precautions should be taken:

1. Place the ADM1027 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clocks and data/address buses are avoided, this distance can be 4 inches to 8 inches.
2. Route the D+ and D– tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible. Do NOT run the D+/D– lines in different directions.
3. Use wide tracks to minimize inductance and reduce noise pickup. A 10 mil track minimum width and spacing is recommended.
4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D– path and at the same temperature. Avoid routing D+/D– on multiple layers or through vias if possible. These increase series resistance that will cause temperature error.
5. Place a 0.1 μF supply bypass capacitor close to the ADM1027.
6. If the distance to the remote sensor is more than 8 inches, the use of shielded twisted pair cable is recommended. This will work up to 100 feet. Connect the twisted pair to D+/D– and the shield to GND close to the ADM1027. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable (adds resistance) and/or filter capacitance can affect the measurement. A 1 Ω series resistance introduces about 0.8°C error.

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Step 2

Configuring the Mux: Which Temperature Controls Which Fan?
Having decided on the system hardware configuration, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels, but how a fan behaves is configurable. For example, fans can run under automatic fan control, manually (software control), or can run at the fastest speed calculated by multiple temperature channels. The MUX is the bridge between temperature measurement channels and the three PWM outputs.

Bits <7:5> (BHVR bits) of Registers 0x5C, 0x5D, and 0x5E (PWM configuration registers) control the behavior of the fans connected to the PWM1, PWM2, and PWM3 outputs. The values selected for these bits determine how the MUX connects a temperature measurement channel to a PWM output.

Automatic Fan Control Mux Options

<7:5> (BHVR) REGISTERS 0x5C, 0x5D, 0x5E

000 = Remote 1 temp controls PWMx

001 = Local temp controls PWMx

010 = Remote 2 temp controls PWMx

101 = Fastest speed calculated by local and remote 2 temp controls PWMx

110 = Fastest speed calculated by all three temperature channels controls PWMx

The fastest speed calculated options refer to the ability to control one PWM output based on multiple temperature channels. While the thermal characteristics of the three temperature zones can be set up differently, they can drive a single fan. An example would be if the fan turns on when Remote 1 temp exceeds 60°C or local temp exceeds 45°C.

Other Mux Options

<7:5> (BHVR) REGISTERS 0x5C, 0x5D, 0x5E

011 = PWMx runs full-speed (default).

100 = PWMx disabled.

111 = Manual Mode. PWMx is run under software control. In this mode, PWM duty cycle registers (Reg. 0x30 to 0x32) are writable and control the PWM outputs.

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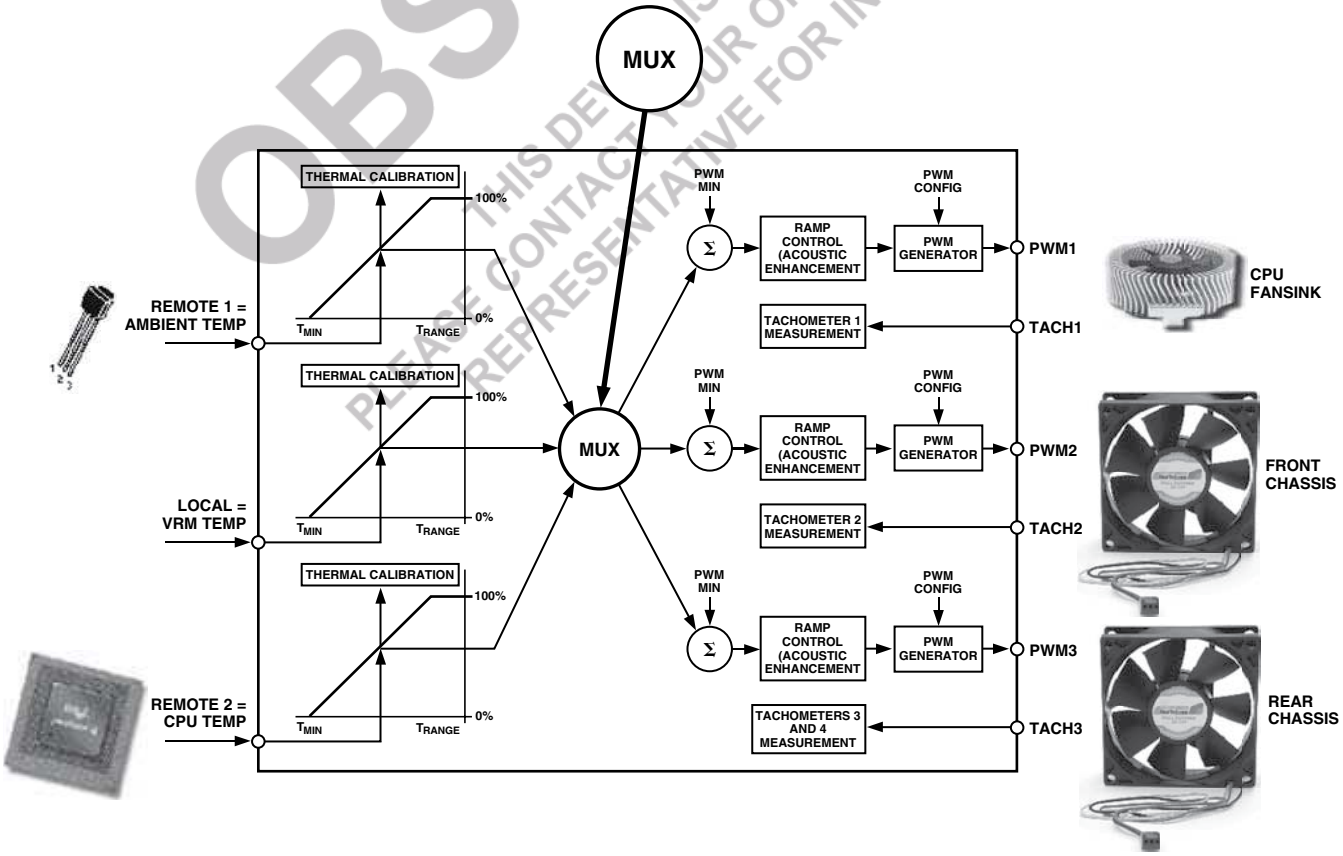

Figure 28. Assigning Temperature Channels to Fan Channels

Step 3

Determine T_{MIN} Setting for Each Thermal Channel

T_{MIN} is the temperature at which the fans will start to turn on under automatic fan control. The speed at which the fan runs at T_{MIN} is programmed later. The T_{MIN} values chosen will be temperature channel specific, e.g., 25°C for ambient channel, 30°C for VRM temperature, and 40°C for processor temperature.

T_{MIN} is an 8-bit twos complement value that can be programmed in 1°C increments. There is a T_{MIN} register associated with each temperature measurement channel, Remote 1, Local and Remote 2 Temp. Once the T_{MIN} value is exceeded, the fan turns on and runs at minimum PWM duty cycle. The fan will turn off once temperature has dropped below $T_{MIN} - T_{HYST}$ (detailed later).

To overcome fan inertia, the fan is spun up until two valid TACH rising edges are counted. See the Fan Start-Up Timeout section for more details. In some cases, primarily for psycho-acoustic reasons, it is desirable that the fan never switches off below T_{MIN}. Bits <7:5> of Enhance Acoustics Register 1 (Reg. 0x62), when set, keep the fans running at PWM minimum duty cycle should the temperature be below T_{MIN}.

T_{MIN} Registers

Reg. 0x67 **Remote 1 Temperature T_{MIN}** = 0x5A (90°C default)

Reg. 0x68 **Local Temperature T_{MIN}** = 0x5A (90°C default)

Reg. 0x69 **Remote 2 Temperature T_{MIN}** = 0x5A (90°C default)

Enhance Acoustics Reg 1 (Reg. 0x62)

Bit 7 (MIN3) = 0, PWM3 is OFF (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is OFF (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is OFF (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

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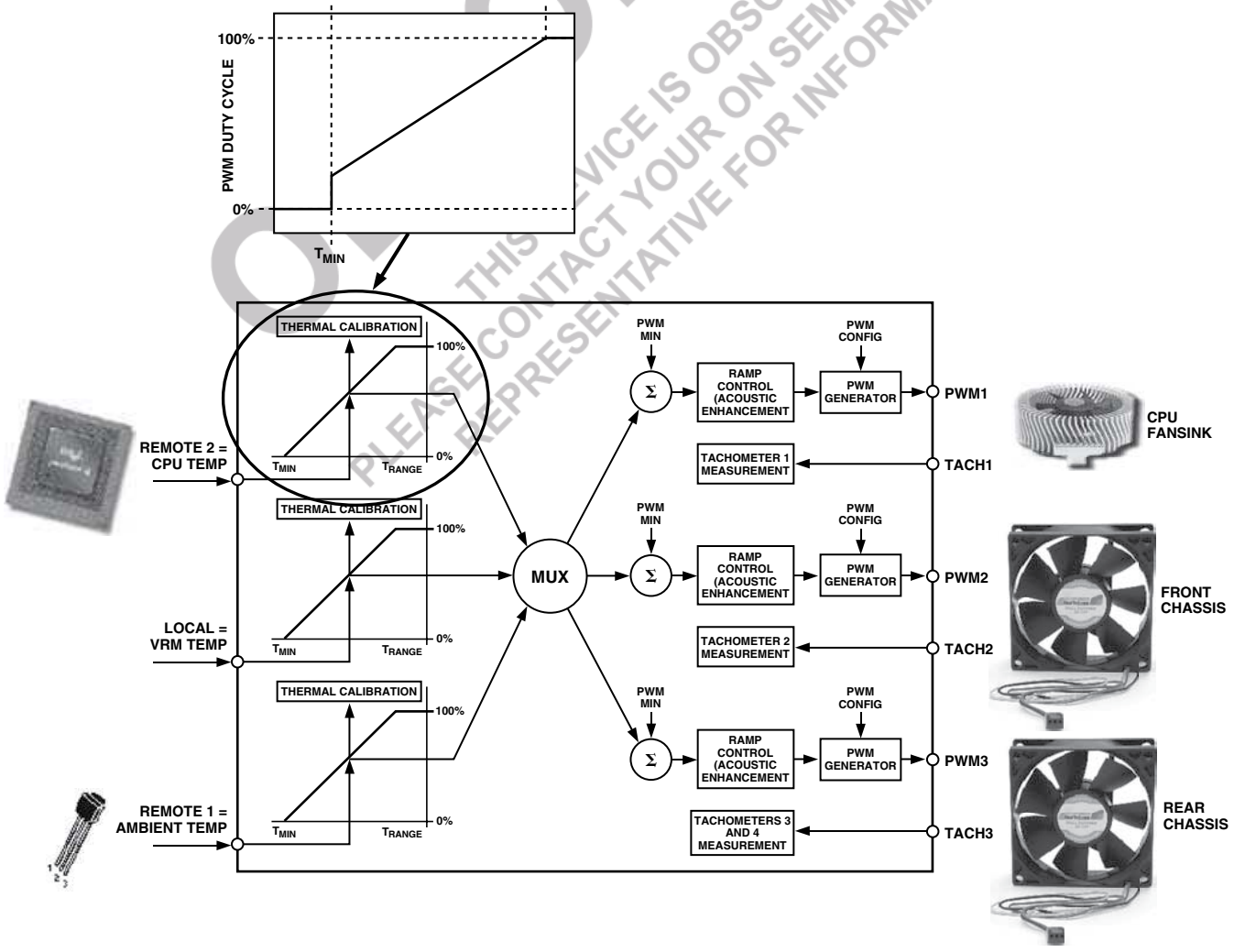

Figure 29. Understanding T_{MIN} Parameter

Step 4

Determine PWM_{MIN} for Each PWM (Fan) Output

PWM_{MIN} is the minimum PWM duty cycle that each fan in the system will run at. It is also the start speed for each fan under automatic fan control once the temperature rises above T_{MIN}. For maximum system acoustic benefit, PWM_{MIN} should be as low as possible. Starting the fans at higher speeds than necessary will merely make the system louder than needed. Depending on the fan used, the PWM_{MIN} setting should be in the range 20% to 33% duty cycle. This value can be found through fan validation.

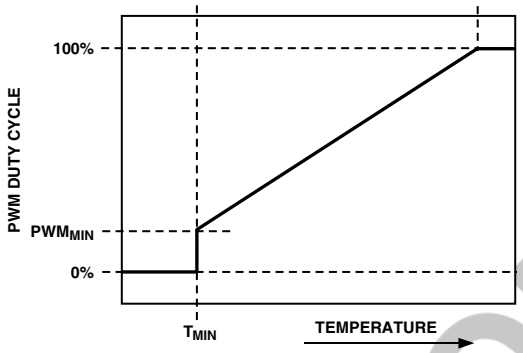

Figure 30. PWM_{MIN} Determines Minimum PWM Duty Cycle

It is important to note that more than one PWM output can be controlled from a single temperature measurement channel. For example, Remote 1 temperature can control PWM1 and PWM2 outputs. If two different fans are used on PWM1 and PWM2, then the fan characteristics can be set up differently. So Fan 1 driven by PWM1 can have a different PWM_{MIN} value than that of Fan 2 connected to PWM2. Figure 31 illustrates this as $PWM1_{MIN}$ (front fan) is turned on at a minimum duty cycle of 20%, whereas $PWM2_{MIN}$ (rear fan) turns on at a minimum of 40% duty cycle. Note however, that both fans turn on at the exact same temperature, defined by T_{MIN}.

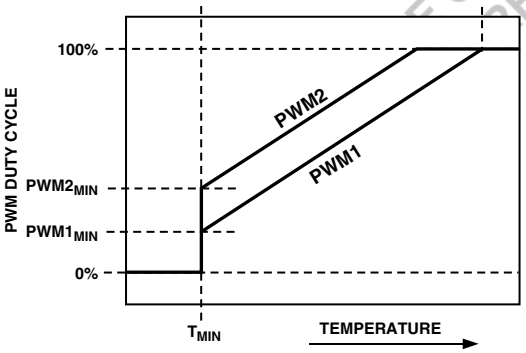

Figure 31. Operating Two Different Fans from a Single-Temperature Channel

Programming the PWM_{MIN} Registers

The PWM_{MIN} registers are 8-bit registers that allow the minimum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows minimum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by

$$Value\ (decimal) = PWM_{MIN}\ /0.39$$

Example 1: For a minimum PWM Duty Cycle of 50%,

Value (decimal) = 50/0.39 = 128 *decimal*

Value = 128 *decimal* or 80 *hex*

Example 2: For a minimum PWM duty cycle of 33%,

Value (decimal) = 33/0.39 = 85 *decimal*

Value = 85 *decimal* or 54 *hex*

PWM_{MIN} Registers

Reg. 0x64 **PWM1 Minimum Duty Cycle** = 0x80 (50% default)

Reg. 0x65 **PWM2 Minimum Duty Cycle** = 0x80 (50% default)

Reg. 0x66 **PWM3 Minimum Duty Cycle** = 0x80 (50% default)

Fan Speed and PWM Duty Cycle

Note that PWM duty cycle does not directly correlate to fan speed in rpm. Running a fan at 33% PWM duty cycle does not equate to running the fan at 33% speed. Driving a fan at 33% PWM duty cycle actually runs the fan at closer to 50% of its full speed. This is because fan speed in %rpm relates to the square root of PWM duty cycle. Given a PWM square wave as the drive signal, fan speed in RPM equates to

$$\%\ fan\ speed = \sqrt{PWM\ duty\ cycle} \times 10$$

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Step 5

Determine T_{RANGE} for Each Temperature Channel

T_{RANGE} is the range of temperature over which automatic fan control occurs once the programmed T_{MIN} temperature has been exceeded. T_{RANGE} is actually a temperature slope and not an arbitrary value, i.e., a T_{RANGE} of 40°C only holds true for PWM_{MIN} = 33%. If PWM_{MIN} is increased or decreased, the effective T_{RANGE} is changed, as described later.

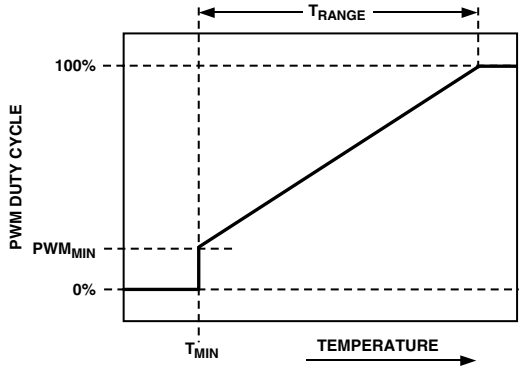

Figure 32. T_{RANGE} Parameter Affects Cooling Slope

The T_{RANGE} or fan control slope is determined by the following procedure:

1. Determine the maximum operating temperature for that channel, e.g., 70°C.
2. Determine experimentally the fan speed (PWM duty cycle value) will not exceed that temperature at the worst-case operating points, e.g., 70°C is reached when the fans are running at 50% PWM duty cycle.
3. Determine the slope of the required control loop to meet these requirements.
4. Use best fit approximation to determine the most suitable T_{RANGE} value. There is ADM1027 evaluation software available to calculate the best fit value; ask your local Analog Devices representative for more details.

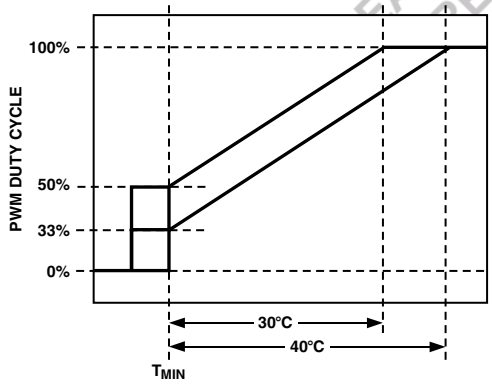

Figure 33. Adjusting PWM_{MIN} Affects T_{RANGE}

T_{RANGE} is implemented as a slope, which means as PWM_{MIN} is changed, T_{RANGE} changes, but the actual slope remains the same. The higher the PWM_{MIN} value, the smaller the effective T_{RANGE} will be, i.e., the fan will reach full speed (100%) at a lower temperature.

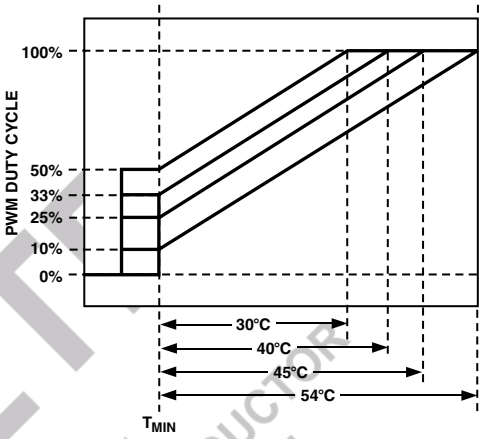

Figure 34. Increasing PWM_{MIN} Changes Effective T_{RANGE}

For a given T_{RANGE} value, the temperature at which the fan will run full-speed for different PWM_{MIN} values can easily be calculated:

$$T_{MAX} = T_{MIN} + (MaxD.C. - MinD.C.) \times T_{RANGE}/170$$

where:

T_{MAX} = Temperature at which the fan runs full-speed

T_{MIN} = Temperature at which the fan will turn on

MaxD.C. = Maximum duty cycle (100%) = 255 decimal

MinD.C. = PWM_{MIN}

T_{RANGE} = PWM duty cycle versus temperature slope

Example: Calculate T_{MAX}, given T_{MIN} = 30°C, T_{RANGE} = 40°C, and PWM_{MIN} = 10% duty cycle = 26 decimal

$$T_{MAX} = T_{MIN} + (MaxD.C. - MinD.C.) \times T_{RANGE}/170$$
$$T_{MAX} = 30°C + (100\% - 10\%) \times 40°C/170$$
$$T_{MAX} = 30°C + (255 - 26) \times 40°C/170$$

T_{MAX} = 84°C (*effective* T_{RANGE} = 54°C)

Example: Calculate T_{MAX}, given T_{MIN} = 30°C, T_{RANGE} = 40°C and PWM_{MIN} = 25% duty cycle = 64 decimal

$$T_{MAX} = T_{MIN} + (MaxD.C. - MinD.C.) \times T_{RANGE}/170$$
$$T_{MAX} = 30°C + (100\% - 25\%) \times 40°C/170$$
$$T_{MAX} = 30°C + (255 - 64) \times 40°C/170$$

T_{MAX} = 75°C (*effective* T_{RANGE} = 45°C)

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Example: Calculate T_{MAX}, given T_{MIN} = 30°C, T_{RANGE} = 40°C, and PWM_{MIN} = 33% duty cycle = 85 decimal

$$T_{MAX} = T_{MIN} + (MaxD.C. - MinD.C.) \times T_{RANGE}/170$$
$$T_{MAX} = 30°C + (100\% - 33\%) \times 40°C/170$$
$$T_{MAX} = 30°C + (255 - 85) \times 40°C/170$$

T_{MAX} = 70°C (effective T_{RANGE} = 40°C)

Example: Calculate T_{MAX}, given T_{MIN} = 30°C, T_{RANGE} = 40°C, and PWM_{MIN} = 50% duty cycle = 128 decimal

$$T_{MAX} = T_{MIN} + (MaxD.C. - MinD.C.) \times T_{RANGE}/170$$
$$T_{MAX} = 30°C + (100\% - 50\%) \times 40°C/170$$
$$T_{MAX} = 30°C + (255 - 128) \times 40°C/170$$

T_{MAX} = 60°C (effective T_{RANGE} = 30°C)

Selecting a T_{RANGE} Slope

The T_{RANGE} value can be selected for each temperature channel: Remote 1, Local and Remote 2 Temp. Bits <7:4> (TRANGE) of Registers 0x5F to 0x61 define the T_{RANGE} value for each temperature channel.

Bits <7:4>*	T_{RANGE} (°C)
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32 (default)
1101	40
1110	53.33
1111	80

* Register 0x5F configures remote 1 T_{RANGE}.
Register 0x60 configures local T_{RANGE}.
Register 0x61 configures remote 2 T_{RANGE}.

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Step 6

Determine T_{THERM} for Each Temperature Channel

T_{THERM} is the absolute maximum temperature allowed on a temperature channel. Above this temperature, a component such as the CPU or VRM may be operating beyond its safe operating limit. When the measured temperature exceeds T_{THERM}, all fans are driven at 100% PWM duty cycle (full speed) to provide critical system cooling. The fans remain running at 100% until the temperature drops below T_{THERM} – hysteresis. The hysteresis value is 4°C.

The T_{THERM} limit should be considered the maximum worst-case operating temperature of the system. Since exceeding any T_{THERM} limit runs all fans at 100%, it has very negative acoustic effects. Ultimately, this limit should be set up as a fail-safe, and the user should ensure that it is not exceeded under normal system operating conditions.

Note that the T_{THERM} limits are nonmaskable and affect the fan speed no matter what automatic fan control settings are configured. This allows some flexibility since a T_{RANGE} value can be selected based on its slope, while a hard limit, e.g., 70°C, can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting T_{THERM} to 70°C.

THERM hysteresis is 4°C.

THERM Registers

Reg. 0x6A **Remote 1 THERM Limit =** 0x64 (100°C default)

Reg. 0x6B **Local Temperature THERM Limit =** 0x64 (100°C default)

Reg. 0x6C **Remote 2 THERM Limit =** 0x64 (100°C default)

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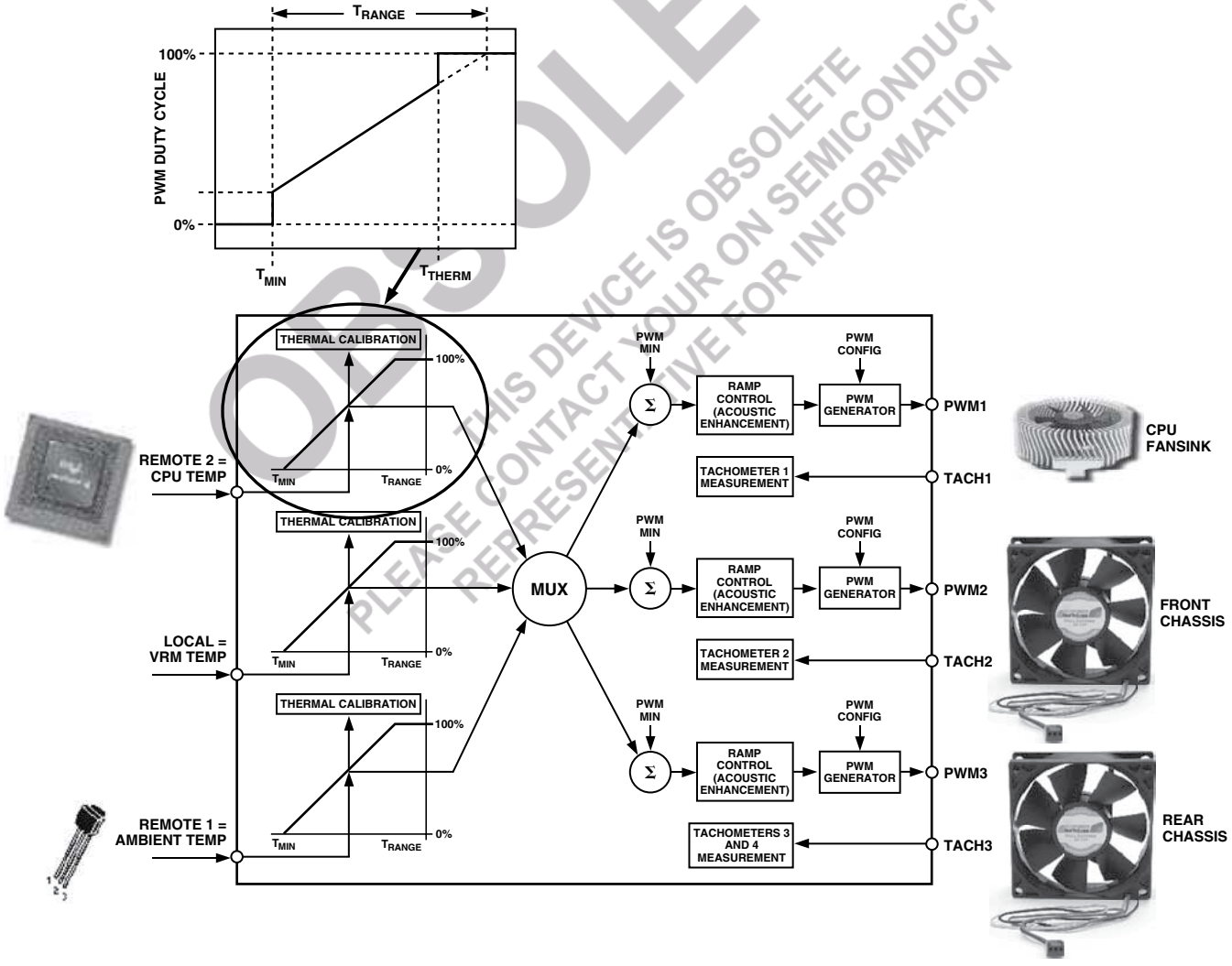

Figure 35. Understanding How T_{THERM} Relates to Automatic Fan Control

Step 7

Determine T_{HYST} for Each Temperature Channel

T_{HYST} is the amount of extra cooling a fan provides after the measured temperature has dropped back below T_{MIN} before the fan turns off. The premise for temperature hysteresis (T_{HYST}) is that without it, the fan would merely chatter, or cycle on and off regularly, whenever the temperature is hovering about the T_{MIN} setting.

The T_{HYST} value chosen will determine the amount of time needed for the system to cool down or heat up, as the fan is turning on and off. Values of hysteresis are programmable in the range 1°C to 15°C. Larger values of T_{HYST} prevent the fans chattering on and off as previously described. The T_{HYST} default value is 4°C.

Hysteresis Registers

Reg. 0x6D Remote 1, Local Hysteresis Register

<7:4> = Remote 1 temperature hysteresis (default = 4°C)

<3:0> = Local temperature hysteresis (default = 4°C)

Reg. 0x6E Remote 2 Temperature Hysteresis Register

<7:4> = Remote 2 temperature hysteresis (default = 4°C)

Note that in some applications it is required that the fans not turn off below T_{MIN}, but remain running at PWM_{MIN}. Bits <7:5> of Enhance Acoustics Register 1 (Reg. 0x62) allow the fans to be turned off or kept spinning below T_{MIN}. If the fans are always on, the T_{HYST} value has no effect on the fan when the temperature drops below T_{MIN}.

Enhance Acoustics Register 1 (Reg. 0x62)

Bit 7 (MIN3) = 0, PWM3 is OFF (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is OFF (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is OFF (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

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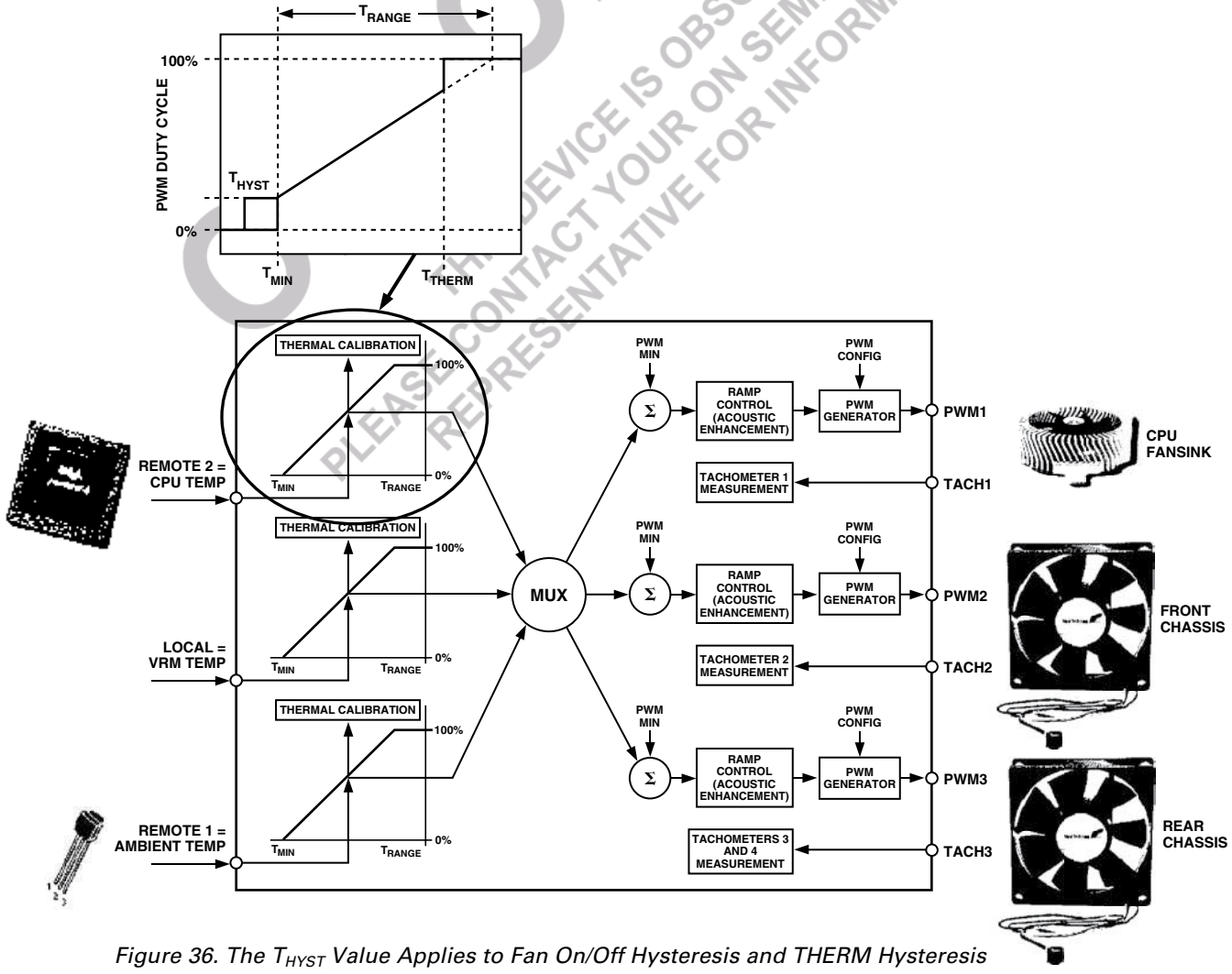

Figure 36. The T_{HYST} Value Applies to Fan On/Off Hysteresis and THERM Hysteresis

ENHANCING SYSTEM ACOUSTICS

Automatic fan speed control mode reacts instantaneously to changes in temperature, i.e., the PWM duty cycle will respond immediately to temperature change. Any impulses in temperature can cause an impulse in fan noise. For psycho-acoustic reasons, the ADM1027 can prevent the PWM output from reacting instantaneously to temperature changes. Enhanced acoustic mode will control the maximum change in PWM duty cycle in a given time. The objective is to prevent the fan cycling up and down and annoying the system user.

Acoustic Enhancement Mode Overview

Figure 37 gives a top-level overview of the automatic fan control circuitry on the ADM1027 and where acoustic enhancement fits in. Acoustic enhancement is intended as a post-design tweak when a system or mechanical engineer is evaluating best settings for the system. Having determined the optimal settings for the thermal solution, the engineer can adjust the system acoustics. The goal is to implement a system that is acoustically pleasing without causing the user annoyance due to fan cycling. It is important to realize that although a system may pass an acoustic noise requirement specification, e.g., 36 dB, if the fan is annoying, it will fail the consumer test.

The Approach

There are two different approaches to implementing system acoustic enhancement. The first method is temperature-centric. This involves smoothing transient temperatures as they are measured by a temperature source, e.g., Remote 1 temperature.

The temperature values used to calculate PWM duty cycle values would be smoothed, reducing fan speed variation. However, this approach causes an inherent delay in updating fan speed and causes the thermal characteristics of the system to change. It also causes the system fans to stay on longer than necessary, since the fan reaction is merely delayed. The user also has no control over noise from different fans driven by the same temperature source. Consider controlling a CPU cooler fan (on PWM1) and a chassis fan (on PWM2) using Remote 1 temperature. Because the Remote 1 temperature is smoothed, both fans will be updated at exactly the same rate. If the chassis fan is much louder than the CPU fan, there is no way to improve its acoustics without changing the thermal solution of the CPU cooling fan.

The second approach is fan-centric. The idea is to control the PWM duty cycle driving the fan at a fixed rate, e.g., 6%. Each time the PWM duty cycle is updated, it is incremented by a fixed 6%. So the fan ramps smoothly to its newly calculated speed. If the temperature starts to drop, the PWM duty cycle immediately decreases by 6% every update. So the fan ramps smoothly up or down without inherent system delay. Consider controlling the same CPU cooler fan (on PWM1) and chassis fan (on PWM2) using Remote 1 temperature. The T_{MIN} and T_{RANGE} settings have already been defined in automatic fan speed control mode, i.e., thermal characterization of the control loop has been optimized. Now the chassis fan is noisier than the CPU cooling fan. So PWM2 can be placed into acoustic enhancement mode independent of PWM1. The acoustics of the chassis fan can therefore be adjusted without affecting the acoustic behavior of the CPU cooling fan, even though both fans are being controlled by Remote 1 temperature. This is exactly how acoustic enhancement works on the ADM1027.

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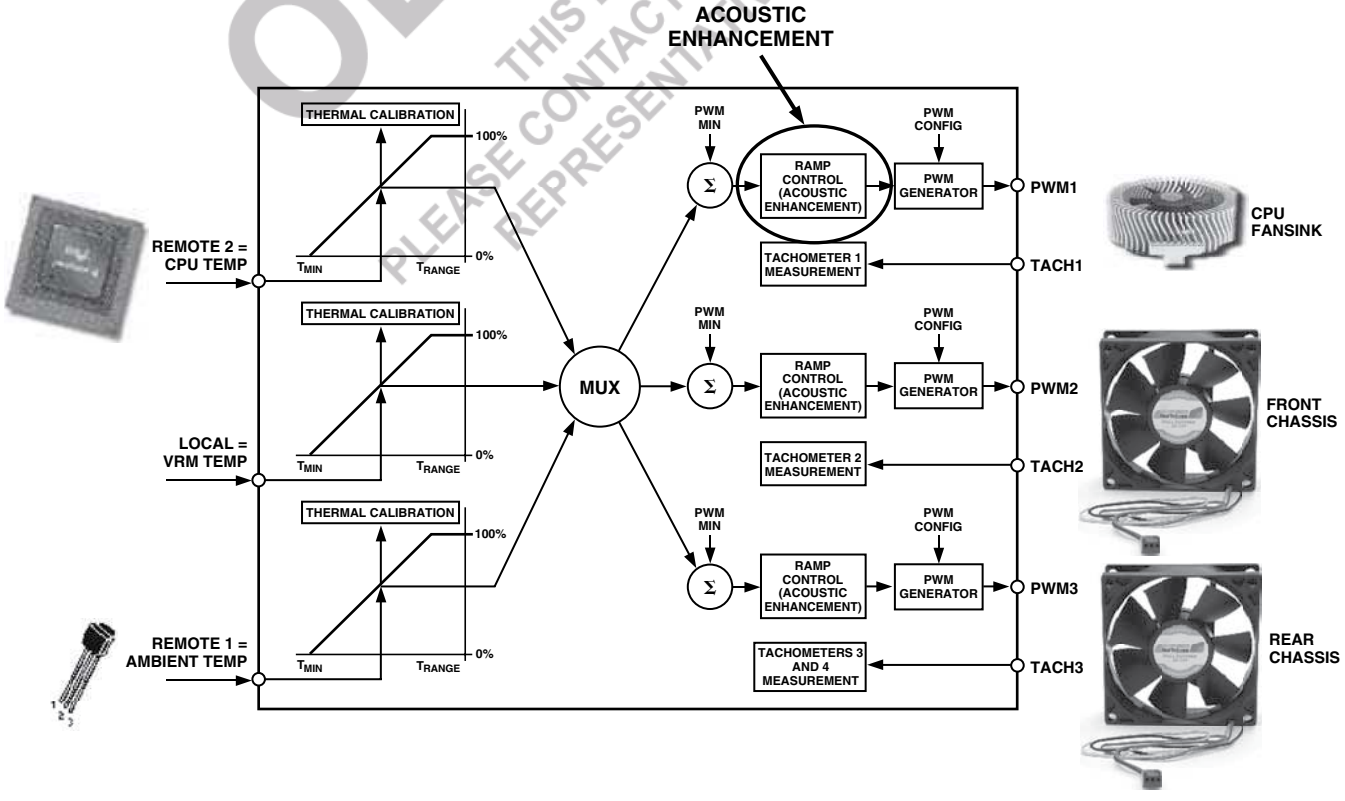

Figure 37. Acoustic Enhancement Smooths Fan Speed Variations Under Automatic Fan Speed Control

Enabling Acoustic Enhancement for Each PWM Output

ENHANCED ACOUSTICS REGISTER 1 (Reg. 0x62)

<3> = 1 enables acoustic enhancement on PWM1 output.

ENHANCED ACOUSTICS REGISTER 2 (Reg. 0x63)

<7> = 1 enables acoustic enhancement on PWM2 output.

<3> = 1 enables acoustic enhancement on PWM3 output.

Effect of Ramp Rate on Enhanced Acoustics Mode

The PWM signal driving the fan will have a period, T, given by the PWM drive frequency, f, since T = 1/f. For a given PWM period, T, the PWM period is subdivided into 255 equal time slots. One time slot corresponds to the smallest possible increment in PWM duty cycle. A PWM signal of 33% duty cycle will thus be high for 1/3 × 255 time slots and low for 2/3 × 255 time slots. Therefore, 33% PWM duty cycle corresponds to a signal that is high for 85 time slots and low for 170 time slots.

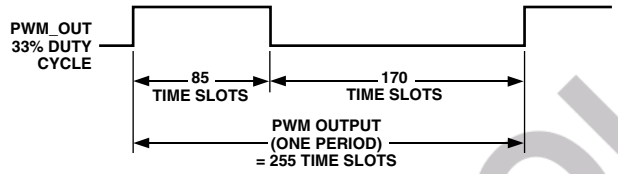

Figure 38. 33% PWM Duty Cycle Represented in Time Slots

The ramp rates in enhanced acoustics mode are selectable between 1, 2, 3, 5, 8, 12, 24, and 48. The ramp rates are actually discrete time slots. For example, if the ramp rate = 8, then eight time slots will be added to the PWM high duty cycle each time the PWM duty cycle needs to be increased. If the PWM duty cycle value needs to be decreased, it will be decreased by eight time slots. Figure 39 shows how the enhanced acoustics mode algorithm operates.

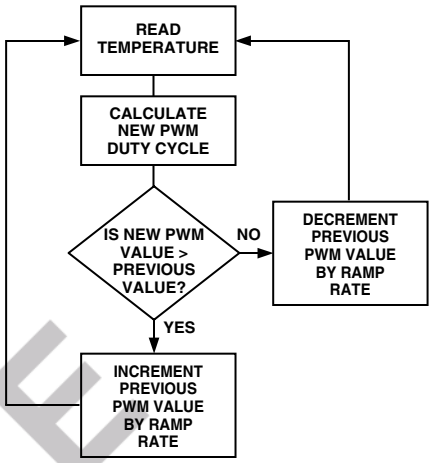

Figure 39. Enhanced Acoustics Algorithm

The enhanced acoustics mode algorithm calculates a new PWM duty cycle based on the temperature measured. If the new PWM duty cycle value is greater than the previous PWM value, then the previous PWM duty cycle value is incremented by either 1, 2, 3, 5, 8, 12, 24, or 48 time slots (depending on the settings of the enhanced acoustics registers). If the new PWM duty cycle value is less than the previous PWM value, then the previous PWM duty cycle is decremented by 1, 2, 3, 5, 8, 12, 24, or 48 time slots. Each time the PWM duty cycle is incremented or decremented, it is stored as the previous PWM duty cycle for the next comparison.

A ramp rate of 1 corresponds to one time slot, which is 1/255 of the PWM period. In enhanced acoustics mode, incrementing or decrementing by 1 changes the PWM output by 1/255 × 100%.

It is important to note that when using the enhanced acoustics mode, the fan spin-up should be disabled.

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CHOOSING RAMP RATE FOR ACOUSTIC ENHANCEMENT

The optimal ramp rate for acoustic enhancement can be found through system characterization after the thermal optimization has been finished. Each ramp rate's effects should be logged, if possible, to determine the best setting for a given solution.

Enhanced Acoustics Register 1 (Reg. 0x62)

<2:0> ACOU Select the ramp rate for PWM1.

000 = 1 time slot = 35 sec
001 = 2 time slots = 17.6 sec
010 = 3 time slots = 11.8 sec
011 = 5 time slots = 7 sec
100 = 8 time slots = 4.4 sec
101 = 12 time slots = 3 sec
110 = 24 time slots = 1.6 sec
111 = 48 time slots = 0.8 sec

Enhanced Acoustics Register 2 (Reg. 0x63)

<2:0> ACOU3 Select the ramp rate for PWM3.

000 = 1 time slot = 35 sec
001 = 2 time slots = 17.6 sec
010 = 3 time slots = 11.8 sec
011 = 5 time slots = 7 sec
100 = 8 time slots = 4.4 sec
101 = 12 time slots = 3 sec
110 = 24 time slots = 1.6 sec
111 = 48 time slots = 0.8 sec

<6:4> ACOU2 Select the ramp rate for PWM2.

000 = 1 time slot = 35 sec
001 = 2 time slots = 17.6 sec
010 = 3 time slots = 11.8 sec
011 = 5 time slots = 7 sec
100 = 8 time slots = 4.4 sec
101 = 12 time slots = 3 sec
110 = 24 time slots = 1.6 sec
111 = 48 time slots = 0.8 sec

Another way to view the ramp rates is as the time it takes for the PWM output to ramp from 0% to 100% duty cycle for an instantaneous change in temperature. This can be tested by putting the ADM1027 into manual mode and changing the PWM output from 0% to 100% PWM duty cycle. The PWM output takes 35 sec to reach 100% with a ramp rate of 1 time slot selected.

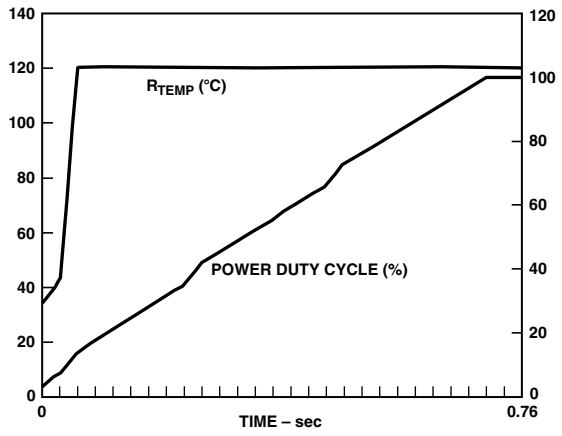

Figure 40. Enhanced Acoustics Mode with Ramp Rate = 48

Figure 40 shows remote temperature plotted against PWM duty cycle for enhanced acoustics mode. The ramp rate is set to 48, which corresponds to the fastest ramp rate. Assume that a new temperature reading is available every 115 ms. With these settings, it took approximately 0.76 seconds to go from 33% duty cycle to 100% duty cycle (full speed). It can be seen that even though the temperature increased very rapidly, the fan ramps up to full speed gradually.

Figure 41 shows how changing the ramp rate from 48 to 8 affects the control loop. The overall response of the fan is slower. Since the ramp rate is reduced, it takes longer for the fan to achieve full running speed. In this case, it took approximately 4.4 sec for the fan to reach full speed.

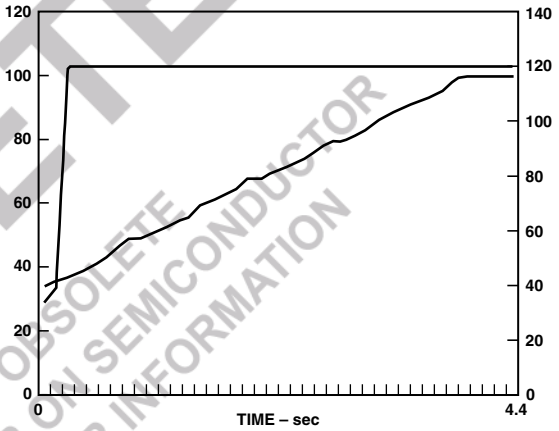

Figure 41. Enhanced Acoustics Mode with Ramp Rate = 8

As can be seen from the preceding examples, the rate at which the fan will react to temperature change is dependent on the ramp rate selected in the enhance acoustics registers. The higher the ramp rate, the faster the fan will reach the newly calculated fan speed.

Figure 42 shows the behavior of the PWM output as temperature varies. As the temperature rises, the fan speed ramps up. Small drops in temperature will not affect the ramp-up function since the newly calculated fan speed will still be higher than the previous PWM value. The enhanced acoustics mode allows the PWM output to be made less sensitive to temperature variations. This will be dependent on the ramp rate selected and programmed into the enhanced acoustics.

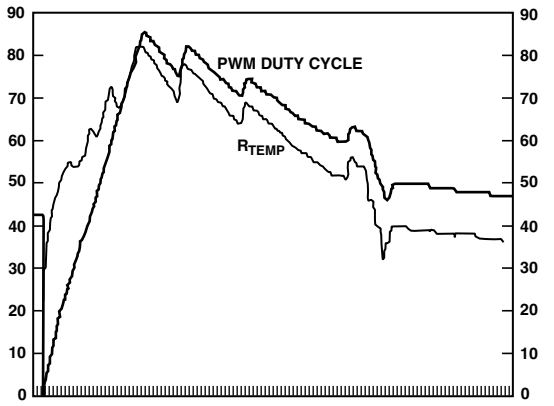

Figure 42. How Fan Reacts to Temperature Variation in Enhanced Acoustics Mode

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OPERATING FROM 3.3 V STANDBY

The ADM1027 has been specifically designed to operate from a 3.3 V STBY supply. In computers that support S3 and S5 states, the core voltage of the processor will be lowered in these states.

Note that since other voltages can drop or be turned off during a low power state, these voltage channels will set status bits or generate $\overline{\text{SMBALERT}}$s. It is still necessary to mask out these channels prior to entering a low power state by using the interrupt mask registers. When exiting the low power state, the mask bits can be cleared. This prevents the device from generating unwanted $\overline{\text{SMBALERT}}$s during the low power state.

XOR TREE TEST MODE

The ADM1027 includes an XOR tree test mode. This mode is useful for in-circuit test equipment at board-level testing. By applying stimulus to the pins included in the XOR tree, it is possible to detect opens or shorts on the system board. Figure 43 shows the signals that are exercised in the XOR tree test mode.

The XOR tree test is invoked by setting Bit 0 (XEN) of the XOR tree test enable register (Reg. 0x6F).

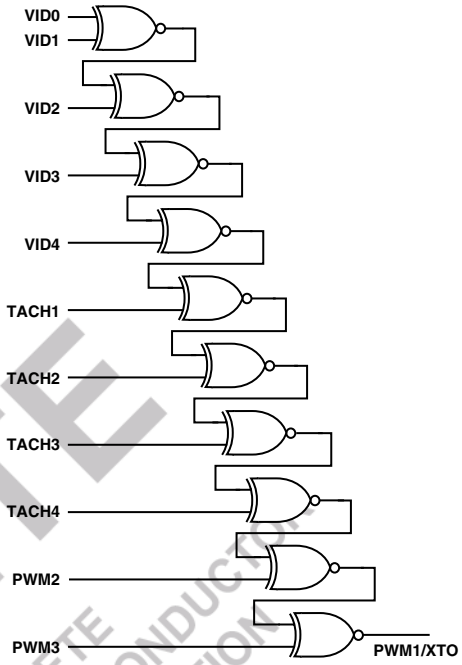

Figure 43. XOR Tree Test

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Table IV. ADM1027 Registers

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable?
0x20	R	2.5 V Reading	9	8	7	6	5	4	3	2	0x00	
0x21	R	V_{CCP} Reading	9	8	7	6	5	4	3	2	0x00	
0x22	R	V_{CC} Reading	9	8	7	6	5	4	3	2	0x00	
0x23	R	5 V Reading	9	8	7	6	5	4	3	2	0x00	
0x24	R	12 V Reading	9	8	7	6	5	4	3	2	0x00	
0x25	R	Remote 1 Temperature	9	8	7	6	5	4	3	2	0x80	
0x26	R	Local Temperature	9	8	7	6	5	4	3	2	0x80	
0x27	R	Remote 2 Temperature	9	8	7	6	5	4	3	2	0x80	
0x28	R	TACH1 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x29	R	TACH1 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2A	R	TACH2 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2B	R	TACH2 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2C	R	TACH3 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2D	R	TACH3 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2E	R	TACH4 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2F	R	TACH4 High Byte	15	14	13	12	11	10	9	8	0x00	
0x30	R/W	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x31	R/W	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x32	R/W	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x3D	R	Device ID Register	7	6	5	4	3	2	1	0	0x27	
0x3E	R	Company ID Number	7	6	5	4	3	2	1	0	0x41	
0x3F	R	Revision Number	VER	VER	VER	VER	STP	STP	STP	STP	0x60	
0x40	R/W	Configuration Register 1	V_{CC}	TODIS	FSPDIS	V × I	FSPD	RDY	LOCK	STRT	0x00	Yes
0x41	R	Interrupt Status Register 1	OOL	R2T	LT	R1T	5 V	V_{CC}	V_{CCP}	2.5 V	0x00	
0x42	R	Interrupt Status Register 2	D2	D1	5	FAN3	FAN2	FAN1	OVT	12 V	0x00	
0x43	R/W	VID Register	7	6	5	VID4	VID3	VID2	VID1	VID0	0xFF	
0x44	R/W	2.5 V Low Limit	7	6	5	4	3	2	1	0	0x00	
0x45	R/W	2.5 V High Limit	7	6	5	4	3	2	1	0	0xFF	
0x46	R/W	V_{CCP} Low Limit	7	6	5	4	3	2	1	0	0x00	
0x47	R/W	V_{CCP} High Limit	7	6	5	4	3	2	1	0	0xFF	
0x48	R/W	V_{CC} Low Limit	7	6	5	4	3	2	1	0	0x00	
0x49	R/W	V_{CC} High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4A	R/W	5 V Low Limit	7	6	5	4	3	2	1	0	0x00	
0x4B	R/W	5 V High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4C	R/W	12 V Low Limit	7	6	5	4	3	2	1	0	0x00	
0x4D	R/W	12 V High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4E	R/W	Remote 1 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	
0x4F	R/W	Remote 1 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x50	R/W	Local Temp Low Limit	7	6	5	4	3	2	1	0	0x81	
0x51	R/W	Local Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x52	R/W	Remote 2 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	
0x53	R/W	Remote 2 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x54	R/W	TACH1 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x55	R/W	TACH1 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x56	R/W	TACH2 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x57	R/W	TACH2 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x58	R/W	TACH3 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x59	R/W	TACH3 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5A	R/W	TACH4 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x5B	R/W	TACH4 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	

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Table IV. ADM1027 Registers (continued)

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable?
0x5C	R/W	PWM1 Configuration Register	BHVR	BHVR	BHVR	INV	3	SPIN	SPIN	SPIN	0x62	Yes
0x5D	R/W	PWM2 Configuration Register	BHVR	BHVR	BHVR	INV	3	SPIN	SPIN	SPIN	0x62	Yes
0x5E	R/W	PWM3 Configuration Register	BHVR	BHVR	BHVR	INV	3	SPIN	SPIN	SPIN	0x62	Yes
0x5F	R/W	Remote 1 T_{RANGE}/PWM 1 Freq	RANGE	RANGE	RANGE	RANGE	3	FREQ	FREQ	FREQ	0xC4	Yes
0x60	R/W	Local T_{RANGE}/PWM 2 Freq	RANGE	RANGE	RANGE	RANGE	3	FREQ	FREQ	FREQ	0xC4	Yes
0x61	R/W	Remote 2 T_{RANGE}/PWM 3 Freq	RANGE	RANGE	RANGE	RANGE	3	FREQ	FREQ	FREQ	0xC4	Yes
0x62	R/W	Enhance Acoustics Reg 1	MIN3	MIN2	MIN1	4	EN1	ACOU	ACOU	ACOU	0x00	Yes
0x63	R/W	Enhance Acoustics Reg 2	EN2	ACOU2	ACOU2	ACOU2	EN3	ACOU3	ACOU3	ACOU3	0x00	Yes
0x64	R/W	PWM1 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x65	R/W	PWM2 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x66	R/W	PWM3 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x67	R/W	Remote 1 Temp T_{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x68	R/W	Local Temp T_{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x69	R/W	Remote 2 Temp T_{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x6A	R/W	Remote 1 THERM Limit	7	6	5	4	3	2	1	0	0x64	Yes
0x6B	R/W	Local THERM Limit	7	6	5	4	3	2	1	0	0x64	Yes
0x6C	R/W	Remote 2 THERM Limit	7	6	5	4	3	2	1	0	0x64	Yes
0x6D	R/W	Remote 1, Local Hysteresis	HYSR1	HYSR1	HYSR1	HYSR1	HYSL	HYSL	HYSL	HYSL	0x44	Yes
0x6E	R/W	Remote 2 Temp Hysteresis	HYSR2	HYSR2	HYSR2	HYSR2	RES	RES	RES	RES	0x40	Yes
0x6F	R/W	XOR Tree Test Enable	RES	RES	RES	RES	RES	RES	RES	XEN	0x00	Yes
0x70	R/W	Remote 1 Temperature Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x71	R/W	Local Temperature Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x72	R/W	Remote 2 Temperature Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x73	R/W	Configuration Register 2	7	CONV	ATTN	AVG	AIN4	AIN3	AIN2	AIN1	0x00	Yes
0x74	R/W	Interrupt Mask 1 Register	OOL	R2T	LT	R1T	5 V	V_{CC}	V_{CCP}	2.5 V	0x00	
0x75	R/W	Interrupt Mask 2 Register	D2	D1	5	FAN3	FAN2	FAN1	OVT	12 V	0x00	
0x76	R/W	Extended Resolution 1	5 V	5 V	V_{CC}	V_{CC}	V_{CCP}	V_{CCP}	2.5 V	2.5 V	0x00	
0x77	R/W	Extended Resolution 2	TDM2	TDM2	LTMP	LTMP	TDM1	TDM1	12 V	12 V	0x00	
0x78	R/W	Configuration Register 3	DC4	DC3	DC2	DC1	FAST	BOOST	1	ALERT	0x00	Yes
0x7B	R/W	Fan Pulses per Revolution	FAN4	FAN4	FAN3	FAN3	FAN2	FAN2	FAN1	FAN1	0x55	

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Table V. Voltage Reading Registers (Power-On Default = 0x00)

Register Address	R/W	Description
0x20	Read-Only	2.5 V Reading (8 MSBs of reading).
0x21	Read-Only	V_{CCP} Reading. Holds processor core voltage measurement (8 MSBs of reading).
0x22	Read-Only	V_{CC} Reading. Measures V_{CC} through the V_{CC} pin (8 MSBs of reading).
0x23	Read-Only	5 V Reading (8 MSBs of reading).
0x24	Read-Only	12 V Reading (8 MSBs of reading).

If the extended resolution bits of these readings are also being read, the extended resolution registers (Reg. 0x76, 0x77) should be read first. Once the extended resolution register is read, the associated MSB reading registers are frozen until read. Both the extended resolution register and the MSB registers are frozen.

Table VI. Temperature Reading Registers (Power-On Default = 0x80)

Register Address	R/W	Description
0x25	Read-Only	Remote 1 Temperature Reading* (8 MSBs of reading).
0x26	Read-Only	Local Temperature Reading (8 MSBs of reading).
0x27	Read-Only	Remote 2 Temperature Reading* (8 MSBs of reading).

These temperature readings are in twos complement format.

*Note that a reading of 0x80 in a temperature reading register indicates a diode fault (open or short) on that channel. If the extended resolution bits of these readings are also being read, the extended resolution registers (Reg. 0x76, 0x77) should be read first. Once the extended resolution register is read, all associated MSB reading registers are frozen until read. Both the extended resolution register and the MSB registers are frozen.

Table VII. Fan Tachometer Reading Registers (Power-On Default = 0x00)

Register Address	R/W	Description
0x28	Read-Only	TACH1 Low Byte
0x29	Read-Only	TACH1 High Byte
0x2A	Read-Only	TACH2 Low Byte
0x2B	Read-Only	TACH2 High Byte
0x2C	Read-Only	TACH3 Low Byte
0x2D	Read-Only	TACH3 High Byte
0x2E	Read-Only	TACH4 Low Byte
0x2F	Read-Only	TACH4 High Byte

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These registers count the number of 11.11 μs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan tach pulses (default = 2). The number of tach pulses used to count can be changed using the fan pulses per revolution register (Reg. 0x7B). This allows the fan speed to be accurately measured. Since a valid fan tachometer reading requires that two bytes are read; the low byte MUST be read first. Both the low and high bytes are then frozen until read. At power-on, these registers contain 0x0000 until such time as the first valid fan tach measurement is read in to these registers. This prevents false interrupts from occurring while the fans are spinning up.

A count of 0xFFFF indicates that a fan is:

1. **Stalled or Blocked** (object jamming the fan)
2. **Failed** (internal circuitry destroyed)
3. **Not Populated** (The ADM1027 expects to see a fan connected to each TACH. If a fan is not connected to that TACH, its TACH minimum high and low bytes should be set to 0xFFFF.)
4. **2-Wire Instead of 3-Wire Fan**

Table VIII. Current PWM Duty Cycle Registers (Power-On Default = 0xFF)

Register Address	R/W	Description
0x30	Read/Write	PWM1 Current Duty Cycle (0% to 100% duty cycle = 0x00 to 0xFF)
0x31	Read/Write	PWM2 Current Duty Cycle (0% to 100% duty cycle = 0x00 to 0xFF)
0x32	Read/Write	PWM3 Current Duty Cycle (0% to 100% duty cycle = 0x00 to 0xFF)

These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the ADM1027 reports the PWM duty cycles back through these registers. The PWM duty cycle values will vary according to temperature in automatic fan speed control mode. During fan startup, these registers report back 0x00. In software mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

Table IX. Register 0x40 – Configuration Register 1 (Power-On Default = 0x00)

Bit	Name	R/W	Description
<0>	STRT	Read/Write	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control based on the default power-up limit settings. Note that the limit values programmed are preserved even if a LOGIC 0 is written to this bit and the default settings are enabled. This bit becomes read-only and cannot be changed once Bit 1 (lock bit) has been written. All limit registers should be programmed by BIOS before setting this bit to 1 (lockable).
<1>	LOCK	Write Once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read-only and cannot be modified until the ADM1027 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings (lockable).
<2>	RDY	Read-Only	This bit gets set to 1 by the ADM1027 to indicate that the device is fully powered up and ready to begin systems monitoring.
<3>	FSPD	Read/Write	When set to 1, this runs all fans at full speed. Power-on default = 0. This bit does not get locked at any time.
<4>	$V \times I$	Read/Write	BIOS should set this bit to 1 when the ADM1027 is configured to measure current from an ADI ADOPT® VRM controller and measure the CPU's core voltage. This will allow monitoring software to display CPU watts usage (lockable).
<5>	FSPDIS	Read/Write	Logic 1 disables fan spin-up for two TACH pulses. Instead, the PWM outputs will go high for the entire fan spin-up timeout selected.
<6>	TODIS	Read/Write	When this bit is set to 1, the SMBus timeout feature is disabled. This allows the ADM1027 to be used with SMBus controllers that cannot handle SMBus timeouts (lockable).
<7>	V_{CC}	Read/Write	When this bit is set to 1, the ADM1027 rescales its V_{CC} pin to measure a 5 V supply. If this bit is 0, the ADM1027 measures V_{CC} as a 3.3 V supply (lockable).

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Table X. Register 0x41 – Interrupt Status Register 1 (Power-On Default = 0x00)

Bit	Name	Read/Write	Description
<0>	2.5 V	Read-Only	A 1 indicates the 2.5 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<1>	V_{CCP}	Read-Only	A 1 indicates the V_{CCP} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<2>	V_{CC}	Read-Only	A 1 indicates the V_{CC} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<3>	5 V	Read-Only	A 1 indicates the 5 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<4>	R1T	Read-Only	A 1 indicates the Remote 1 low or high temp limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<5>	LT	Read-Only	A 1 indicates the local low or high temp limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<6>	R2T	Read-Only	A 1 indicates the Remote 2 low or high temperature limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<7>	OOL	Read-Only	A 1 indicates that an out-of-limit event has been latched in Status Register 2. This bit is a logical OR of all status bits in Status Register 2. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Status Register 2 are out-of-limit. This saves the need to read Status Register 2 every interrupt or polling cycle.

Table XI. Register 0x42 – Interrupt Status Register 2 (Power-On Default = 0x00)

Bit	Name	Read/Write	Description
<0>	12 V	Read-Only	A 1 indicates the 12 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<1>	OVT	Read-Only	A 1 indicates that one of the THERM overtemperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below THERM – 4°C
<2>	FAN1	Read-Only	A 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is NOT set when the PWM 1 output is off.
<3>	FAN2	Read-Only	A 1 indicates that Fan 2 has dropped below minimum speed or has stalled. This bit is NOT set when the PWM 2 output is off.
<4>	FAN3	Read-Only	A 1 indicates that Fan 3 has dropped below minimum speed or has stalled. This bit is NOT set when the PWM 3 output is off.
<5>	FAN4	Read-Only	A 1 indicates that Fan 4 has dropped below minimum speed or has stalled. This bit is NOT set when the PWM 3 output is off.
<6>	D1	Read-Only	A 1 indicates either an open or short circuit on the Thermal Diode 1 inputs.
<7>	D2	Read-Only	A 1 indicates either an open or short circuit on the Thermal Diode 2 inputs.

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Table XII. Register 0x43 – VID Register (Power-On Default = 0x00)

Bit	Name	R/W	Description
<4:0>	VID[4:0]	Read-Only	The VID[4:0] inputs from the CPU to indicate the expected processor core voltage. On power-up, these bits reflect the state of the VID pins, even if monitoring is not enabled.
<7:5>	Reserved	Read-Only	Reserved for future use.

Table XIII. Voltage Limit Registers

Register Address	R/W	Description	Power-On Default
0x44	Read/Write	2.5 V Low Limit	0x00
0x45	Read/Write	2.5 V High Limit	0xFF
0x46	Read/Write	V_{CCP} Low Limit	0x00
0x47	Read/Write	V_{CCP} High Limit	0xFF
0x48	Read/Write	V_{CC} Low Limit	0x00
0x49	Read/Write	V_{CC} High Limit	0xFF
0x4A	Read/Write	5 V Low Limit	0x00
0x4B	Read/Write	5 V High Limit	0xFF
0x4C	Read/Write	12 V Low Limit	0x00
0x4D	Read/Write	12 V High Limit	0xFF

Setting the Configuration Register 1 lock bit has no effect on these registers.

High Limits: An interrupt is generated when a value exceeds its high limit (> comparison).
Low Limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table XIV. Temperature Limit Registers

Register Address	R/W	Description	Power-On Default
0x4E	Read/Write	Remote 1 Temperature Low Limit	0x81
0x4F	Read/Write	Remote 1 Temperature High Limit	0x7F
0x50	Read/Write	Local Temperature Low Limit	0x81
0x51	Read/Write	Local Temperature High Limit	0x7F
0x52	Read/Write	Remote 2 Temperature Low Limit	0x81
0x53	Read/Write	Remote 2 Temperature High Limit	0x7F

Exceeding any of these temperature limits by 1°C will cause the appropriate status bit to be set in the interrupt status register. Setting the Configuration Register 1 lock bit has no effect on these registers.

High Limits: An interrupt is generated when a value exceeds its high limit (> comparison).
Low Limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

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Table XV. Fan Tachometer Limit Registers

Register Address	R/W	Description	Power-On Default
0x54	Read/Write	TACH 1 Minimum Low Byte	0xFF
0x55	Read/Write	TACH 1 Minimum High Byte	0xFF
0x56	Read/Write	TACH 2 Minimum Low Byte	0xFF
0x57	Read/Write	TACH 2 Minimum High Byte	0xFF
0x58	Read/Write	TACH 3 Minimum Low Byte	0xFF
0x59	Read/Write	TACH 3 Minimum High Byte	0xFF
0x5A	Read/Write	TACH 4 Minimum Low Byte	0xFF
0x5B	Read/Write	TACH 4 Minimum High Byte	0xFF

Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit will be set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 lock bit has no effect on these registers.

Table XVI. PWM Configuration Registers

Register Address	R/W	Description	Power-On Default
0x5C	Read/Write	PWM1 Configuration	0x62
0x5D	Read/Write	PWM2 Configuration	0x62
0x5E	Read/Write	PWM3 Configuration	0x62

Bit	Name	Read/Write	Description
<2:0> (Fan Startup Timeout)	SPIN	Read/Write	These bits control the startup timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement directly after the fan startup timeout period, then the TACH measurement will read 0xFFFF and Status Register 2 will reflect the fan fault. If the TACH minimum high and low byte contains 0xFFFF or 0x0000, then the Status Register 2 bit will not be set, even if the fan has not started. 000 = No startup timeout 001 = 100 ms 010 = 250 ms (default) 011 = 400 ms 101 = 1 sec 110 = 2 sec 111 = 4 sec Note: Do not program 100.
<3>	Reserved	Read-Only	Reserved for future use.
<4>	INV	Read/Write	This bit inverts the PWM output. The default is 0, which corresponds to a logic high output for 100% duty cycle. Setting this bit to 1, inverts the PWM output, so 100% duty cycle corresponds to a logic low output.
<7:5>	BHVR	Read/Write	These bits assign each fan to a particular temperature sensor for localized cooling. 000 = Remote 1 temperature controls PWMx (automatic fan control mode). 001 = Local temperature controls PWMx (automatic fan control mode). 010 = Remote 2 temperature controls PWMx (automatic fan control mode). 011 = PWMx runs full speed (default). 100 = PWMx disabled. 101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx. 110 = Fastest speed calculated by all three temperatures controls PWMx. 111 = Manual mode. PWM duty cycle registers (Reg. 0x30 to 0x32) become writable.

These registers become read-only when the configuration register 1 lock bit is set to 1. Any subsequent attempts to write to these registers will fail.

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Table XVII. TEMP T_{RANGE}/PWM Frequency Registers

Register Address	R/W	Description	Power-On Default
0x5F	Read/Write	Remote 1 T_{RANGE}/PWM 1 Frequency	0xC4
0x60	Read/Write	Local Temperature T_{RANGE}/PWM 2 Frequency	0xC4
0x61	Read/Write	Remote 2 T_{RANGE}/PWM 3 Frequency	0xC4

Bit	Name	Read/Write	Description
<2:0>	FREQ	Read/Write	These bits control the PWMx frequency. 000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz
<3>	Reserved	Read/Write	Reserved for future use.
<7:4>	RANGE	Read/Write	These bits determine the PWM duty cycle versus temperature slope for automatic fan control. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C 1000 = 13.33°C 1001 = 16°C 1010 = 20°C 1011 = 26.67°C 1100 = 32°C (default) 1101 = 40°C 1110 = 53.33°C 1111 = 80°C

These registers become read-only when the Configuration Register 1 lock bit is set. Any further attempts to write to these registers will have no effect.

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Table XVIII. Register 0x62 – Enhance Acoustics Register 1 (Power-On Default = 0x00)

Bit	Name	R/W	Description
<2:0>	ACOU	Read-Only	These bits select the ramp rate applied to the PWM1 output. Instead of PWM1 jumping instantaneously to its newly calculated speed, PWM1 will ramp gracefully at the rate determined by these bits. This feature enhances the acoustics of the fan being driven by the PWM1 output. **Time slot increase** — **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 1.8 sec 011 = 5 — 7 sec 100 = 8 — 4.4 sec 101 = 12 — 3 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
<3>	EN1	Read/Write	When this bit is 1, acoustic enhancement is enabled on PWM1 output. When acoustic enhancement is enabled, fan spin-up time should be disabled.
<4>	Reserved	Read-Only	Reserved for future use.
<5>	MIN1	Read/Write	When the ADM1027 is in automatic fan control mode, this bit defines whether PWM 1 is off (0% duty cycle) or at PWM 1 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis 1 = PWM 1 minimum duty cycle below T_{MIN} – hysteresis
<6>	MIN2	Read/Write	When the ADM1027 is in automatic fan speed control mode, this bit defines whether PWM 2 is off (0% duty cycle) or at PWM 2 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis 1 = PWM 2 minimum duty cycle below T_{MIN} – hysteresis
<7>	MIN3	Read/Write	When the ADM1027 is in automatic fan speed control mode, this bit defines whether PWM 3 is off (0% duty cycle) or at PWM 3 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis 1 = PWM 3 minimum duty cycle below T_{MIN} – hysteresis

This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register will have no effect.

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Table XIX. Register 0x63 – Enhance Acoustics Register 2 (Power-On Default = 0x00)

Bit	Name	R/W	Description
<2:0>	ACOU3	Read/Write	These bits select the ramp rate applied to the PWM3 output. Instead of PWM3 jumping instantaneously to its newly calculated speed, PWM3 will ramp gracefully at the rate determined by these bits. This effect enhances the acoustics of the fan being driven by the PWM3 output. **Time slot increase** — **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 5 — 7 sec 100 = 8 — 4.4 sec 101 = 12 — 3 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
<3>	EN3	Read/Write	When this bit is 1, acoustic enhancement is enabled on PWM3 output. When acoustic enhancement is enabled, fan spin-up time should be disabled.
<6:4>	ACOU2	Read/Write	These bits select the ramp rate applied to the PWM2 output. Instead of PWM2 jumping instantaneously to its newly calculated speed, PWM2 will ramp gracefully at the rate determined by these bits. This effect enhances the acoustics of the fans being driven by the PWM2 output. **Time slot increase** — **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 5 — 7 sec 100 = 8 — 4.4 sec 101 = 12 — 3 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
<7>	EN2	Read/Write	When this bit is 1, acoustic enhancement is enabled on PWM2 output. When acoustic enhancement is enabled, fan spin-up time should be disabled.

This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register will have no effect.

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Table XX. PWM Minimum Duty Cycle Registers

Register Address	R/W	Description	Power-On Default
0x64	Read/Write	PWM1 Minimum Duty Cycle	0x80 (50% duty cycle)
0x65	Read/Write	PWM2 Minimum Duty Cycle	0x80 (50% duty cycle)
0x66	Read/Write	PWM3 Minimum Duty Cycle	0x80 (50% duty cycle)

Bit	Name	Read/Write	Description
<7:0>	PWM Duty	Read/Write	These bits define the PWM_{MIN} duty cycle for the PWMx output. 0x00 = 0% duty cycle (fan off) 0x40 = 25% duty cycle 0x80 = 50% duty cycle 0xFF = 100% duty cycle (fan full speed)

These registers become read-only when the ADM1027 is in automatic fan control mode.

Table XXI. T_{MIN} Registers

Register Address	R/W	Description	Power-On Default
0x67	Read/Write	Remote 1 Temperature T_{MIN}	0x5A (90°C)
0x68	Read/Write	Local Temperature T_{MIN}	0x5A (90°C)
0x69	Read/Write	Remote 2 Temperature T_{MIN}	0x5A (90°C)

These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan will run at minimum speed and increase with temperature according to T_{RANGE}.

These registers become read-only when the Configuration Register 1 lock bit is set. Any further attempts to write to these registers will have no effect.

Table XXII. Therm Limit Registers

Register Address	R/W	Description	Power-On Default
0x6A	Read/Write	Remote 1 THERM Limit	0x64 (100°C)
0x6B	Read/Write	Local THERM Limit	0x64 (100°C)
0x6C	Read/Write	Remote 2 THERM Limit	0x64 (100°C)

If any temperature measured exceeds its THERM limit, all PWM outputs will drive their fans at 100% duty cycle. This is a fail-safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output will remain at 100% until the temperature drops below THERM limit – 4°C.

These registers become read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to these registers will have no effect.

Table XXIII. Temperature Hysteresis Registers

Register Address	R/W	Description	Power-On Default
0x6D	Read/Write	Remote 1, Local Temperature Hysteresis	0x44
0x6E	Read/Write	Remote 2 Temperature Hysteresis	0x40

Each 4-bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan will remain running at PWM_{MIN} duty cycle until the temperature = T_{MIN} – hysteresis. Up to 15°C of hysteresis may be assigned to any temperature channel. Setting the hysteresis value lower than 4°C will cause the fan to switch on and off regularly when the temperature is close to T_{MIN}.

These registers become read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to these registers will have no effect.

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Table XXIV. XOR Tree Test Enable

Register Address	R/W	Description	Power-On Default
0x6F	Read/Write	XOR Tree Test Enable Register	0x00
<0>	XEN	If the XEN bit is set to 1, the device enters the XOR tree test mode. Clearing the bit removes the device from the XOR tree test mode.	
<7:1>	Reserved	Unused. Do not write to these bits.	

This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register will have no effect.

Table XXV. Remote 1 Temperature Offset

Register Address	R/W	Description	Power-On Default
0x70	Read/Write	Remote 1 Temperature Offset	0x00
<7:0>	Read/Write	Allows a twos complement offset value to be automatically added to or subtracted from the Remote 1 temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 1°C.	

This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register will have no effect.

Table XXVI. Local Temperature Offset

Register Address	R/W	Description	Power-On Default
0x71	Read/Write	Local Temperature Offset	0x00
<7:0>	Read/Write	Allows a twos complement offset value to be automatically added to or subtracted from the local temperature reading. LSB value = 1°C.	

This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register will have no effect.

Table XXVII. Remote 2 Temperature Offset

Register Address	R/W	Description	Power-On Default
0x72	Read/Write	Remote 2 Temperature Offset	0x00
<7:0>	Read/Write	Allows a twos complement offset value to be automatically added to or subtracted from the Remote 2 temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 1°C.	

This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register will have no effect.

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Table XXVIII. Register 0x73 – Configuration Register 2 (Power-On Default = 0x00)

Bit	Name	R/W	Description
0	AIN1	Read/Write	AIN1 = 0, speed of 3-wire fans measured using the TACH output from the fan. AIN1 = 1, Pin 11 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor.
1	AIN2	Read/Write	AIN2 = 0, speed of 3-wire fans measured using the TACH output from the fan. AIN2 = 1, Pin 12 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor.
2	AIN3	Read/Write	AIN3 = 0, speed of 3-wire fans measured using the TACH output from the fan. AIN3 = 1, Pin 9 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor.
3	AIN4	Read/Write	AIN4 = 0, speed of 3-wire fans measured using the TACH output from the fan. AIN4 = 1, Pin 14 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor.
4	AVG	Read/Write	AVG = 1, averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster.
5	ATTN	Read/Write	ATTN = 1, the ADM1027 removes the attenuators from the 2.5 V, V_{CCP}, 5 V, and 12 V inputs. The inputs can be used for other functions such as connecting up external sensors.
6	CONV	Read/Write	CONV = 1, the ADM1027 is put into a single-channel ADC conversion mode. In this mode, the ADM1027 can be made to read continuously from one input only, e.g., Remote 1 temperature. It is also possible to start ADC conversions using an external clock on Pin 11 by setting Bit 2 of Test Register 2 (Reg. 0x7F). This mode could be useful if, for example, the user wanted to characterize/profile CPU temperature quickly. The appropriate ADC channel is selected by writing to Bits <7:5> of TACH1 minimum high byte register (0x55). **Bits <7:5> Reg. 0x55 — Channel Selected** 000 — 2.5 V 001 — V_{CCP} 010 — V_{CC} (3.3 V) 011 — 5 V 100 — 12 V 101 — Remote 1 Temp 110 — Local Temp 111 — Remote 2 Temp
7	Reserved	Read/Write	Reserved for future use

This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register will have no effect.

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Table XXIX. Register 0x74 – Interrupt Mask Register 1 (Power-On Default <7:0> = 0x00)

Bit	Name	R/W	Description
0	2.5 V	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the 2.5 V channel.
1	V_{CCP}	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the V_{CCP} channel.
2	V_{CC}	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the V_{CC} channel.
3	5 V	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the 5 V channel.
4	R1T	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the Remote 1 temperature channel.
5	LT	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the local temperature channel.
6	R2T	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the Remote 2 temperature channel.
7	OOL	Read/Write	This bit needs to be set to 1 to allow masking in the Interrupt Mask Register 2. If this bit is not set to 1, then setting a bit in Mask Register 2 will have no effect.

Table XXX. Register 0x75 – Interrupt Mask Register 2 (Power-On Default <7:0> = 0x00)

Bit	Name	R/W	Description
0	12 V	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the 12 V channel.
1	OVT	Read-Only	A 1 masks $\overline{\text{SMBALERT}}$ for overtemperature $\overline{\text{THERM}}$ conditions.
2	FAN1	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for a Fan 1 fault.
3	FAN2	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for a Fan 2 fault.
4	FAN3	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for a Fan 3 fault.
5	FAN4	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for a Fan 4 fault.
6	D1	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on Remote 1 channel.
7	D2	Read/Write	A 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on Remote 2 channel.

Table XXXI. Register 0x76 – Extended Resolution Register 1

Bit	Name	R/W	Description
<1:0>	2.5 V	Read-Only	2.5 V LSBs. Holds the 2 LSBs of the 10-bit 2.5 V measurement.
<3:2>	V_{CCP}	Read-Only	V_{CCP} LSBs. Holds the 2 LSBs of the 10-bit V_{CCP} measurement.
<5:4>	V_{CC}	Read-Only	V_{CC} LSBs. Holds the 2 LSBs of the 10-bit V_{CC} measurement.
<7:6>	5 V	Read-Only	5 V LSBs. Holds the 2 LSBs of the 10-bit 5 V measurement.

If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table XXXII. Register 0x77 – Extended Resolution Register 2

Bit	Name	R/W	Description
<1:0>	12 V	Read-Only	12 V LSBs. Holds the 2 LSBs of the 10-bit 12 V measurement.
<3:2>	TDM1	Read-Only	Remote 1 temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 1 temperature measurement.
<5:4>	LTMP	Read-Only	Local temperature LSBs. Holds the 2 LSBs of the 10-bit local temperature measurement.
<7:6>	TDM2	Read-Only	Remote 2 temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 2 temperature measurement.

If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

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Table XXXIII. Register 0x78 – Configuration Register 3 (Power-On Default = 0x00)

Bit	Name	R/W	Description
<0>	ALERT	Read/Write	ALERT = 1, Pin 10 (PWM2/$\overline{\text{SMBALERT}}$) is configured as an $\overline{\text{SMBALERT}}$ interrupt output to indicate out-of-limit error conditions. Default = 0 = PWM2.
<1>	Reserved	Read/Write	Reserved for future use.
<2>	Reserved	Read/Write	Reserved for future use.
<3>	FAST	Read/Write	FAST = 1 enables fast TACH measurements on all channels. This increases the TACH measurement rate from once per second, to once per 250 ms (4×).
<4>	DC1	Read/Write	DC1 = 1 enables TACH measurements to be continuously made on TACH1.
<5>	DC2	Read/Write	DC2 = 2 enables TACH measurements to be continuously made on TACH2.
<6>	DC3	Read/Write	DC3 = 1 enables TACH measurements to be continuously made on TACH3.
<7>	DC4	Read/Write	DC4 = 1 enables TACH measurements to be continuously made on TACH4.

This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register will have no effect.

Table XXXIV. Register 0x7B – Fan Pulses Per Revolution Register (Power On Default = 0x55)

Bit	Name	R/W	Description
<1:0>	FAN1	Read/Write	Sets number of pulses to be counted when measuring FAN1 speed. Can be used to determine fan's pulses per revolution number for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (default) 10 = 3 11 = 4
<3:2>	FAN2	Read/Write	Sets number of pulses to be counted when measuring FAN2 speed. Can be used to determine fan's pulses per revolution number for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (default) 10 = 3 11 = 4
<5:4>	FAN3	Read/Write	Sets number of pulses to be counted when measuring FAN3 speed. Can be used to determine fan's pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (default) 10 = 3 11 = 4
<7:6>	FAN4	Read/Write	Sets number of pulses to be counted when measuring FAN4 speed. Can be used to determine fan's pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (default) 10 = 3 11 = 4

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Table XXXV. Register 0x7E – Manufacturer's Test Register 1 (Power-On Default = 0x00)

Bit	Name	Read/Write	Description
<7:0>	Reserved	Read-Only	Manufacturer's Test Register. These bits are reserved for the manufacturer's test purposes and should NOT be written to under normal operation.

This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register will have no effect.

Table XXXVI. Register 0x7F – Manufacturer's Test Register 2 (Power-On Default = 0x00)

Bit	Name	Read/Write	Description
<7:0>	Reserved	Read-Only	Manufacturer's Test Register. These bits are reserved for the manufacturer's test purposes and should NOT be written to under normal operation.

This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register will have no effect.

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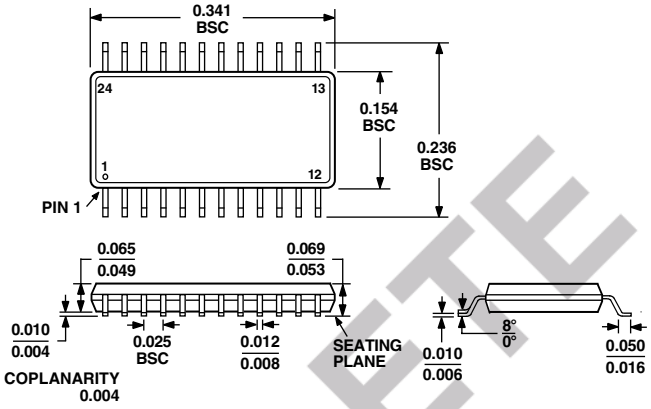
OUTLINE DIMENSIONS

24-Lead Shrink Small Outline Package [QSOP]
(RQ-24)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-137AE

Model	Temperature Range	Package Description	Package Option
ADM1027ARQ	0°C to 105°C	24-Lead QSOP	RQ-24
ADM1027ARQ-REEL	0°C to 105°C	24-Lead QSOP	RQ-24
ADM1027ARQ-REEL7	0°C to 105°C	24-Lead QSOP	RQ-24
ADM1027ARQZ	0°C to 105°C	24-Lead QSOP	RQ-24
ADM1027ARQZ-REEL	0°C to 105°C	24-Lead QSOP	RQ-24
ADM1027ARQZ-RL7[1]	0°C to 105°C	24-Lead QSOP	RQ-24

[1]Z = Pb-Free part

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