THE DATASHEET OF

A3944KLPTR-T

Automotive, Low-Side FET Pre-Driver

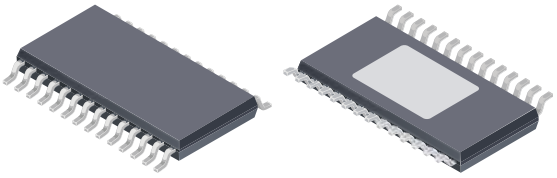
Features and Benefits

- 6 channels
- Drives logic-level N-channel MOSFETs
- 40 mA gate drive current
- Short and open detection
- High voltage (50 V) drain feedback inputs
- Programmable fault timers and thresholds per channel
- UVLO and thermal warning circuitry
- Serial or parallel gate drive control
- Highly configurable, through SPI compatible interface
- Compact TSSOP package

Applications:

- Automotive ECU
- Automotive high-side actuators

Package: 28-pin TSSOP with exposed thermal pad (suffix LP)



Not to scale

Description

The A3944 is a programmable 6 channel low-side MOSFET pre-driver suitable for use in automotive applications. Each channel is controllable by a combination of parallel and serial inputs and provides sufficient gate drive current to allow PWM control up to 10 kHz, depending on the MOSFET gate charge.

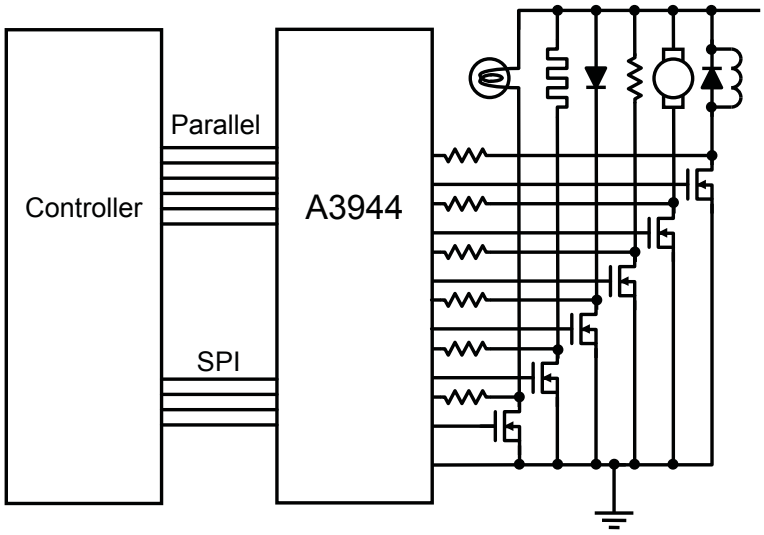
Each channel provides independent fault diagnostics for short to ground and open load when in the off-state, and short to battery when in the on-state. A short to battery can disable the output until reset or for a programmable retry time. Each channel provides independently programmable fault thresholds and blanking times.

In addition to channel state control, channel fault masking, fault thresholds and fault timers are programmed through the SPI compatible serial interface. The serial interface also provides read back of the fault status for each channel.

Digital inputs and outputs are compatible with 3.3 V and 5 V supplies.

The A3944 is supplied in a 28 lead TSSOP package (suffix LP) with an exposed thermal pad. The package is lead (Pb) free with 100% matte-tin leadframe plating.

Typical Application Diagram



Selection Guide

Part Number	Packing*
A3944KLPTR-T	4000 pieces per reel

*Contact Allegro™ for additional packing options

Absolute Maximum Ratings with respect to ground at T_A = 25°C

Characteristic	Symbol	Notes	Rating	Unit
Analog Supply Voltage	V_{BB}		–0.3 to 40	V
Logic Supply Voltage	V_{DD}		–0.3 to 6.5	V
Gate Drive Supply Voltage	V_{DR}		–0.3 to 6.5	V
Terminal VREG	V_{REG}		–0.3 to 20	V
Terminals GATx			–0.3 to 6.5	V
Terminals DRNx			–0.3 to 50	V
Terminals INx			–0.3 to 6.5	V
Terminals SI, SCK, CSN			–0.3 to 6.5	V
Terminal SO			–0.3 to 6.5	V
Terminal RESETN			–0.3 to 6.5	V
Drain Feedback Clamp Energy*	E_{DRNC}	Single pulse less than 2 ms	10	µJ
Drain Feedback Clamp Current*	I_{DRNC}	Single pulse not exceeding E_{DRN} or P_{DRN}	100	mA
Drain Feedback Clamp Power*	P_{DRNC}	Average power over any 2 ms period	100	mW
Junction Temperature	T_J(max)		150	°C
Transient Junction Temperature*	T_{tJ}	Overtemperature event not exceeding 10 s, lifetime duration not exceeding 10 hours	175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Temperature Range	T_A	Range K	–40 to 150	°C

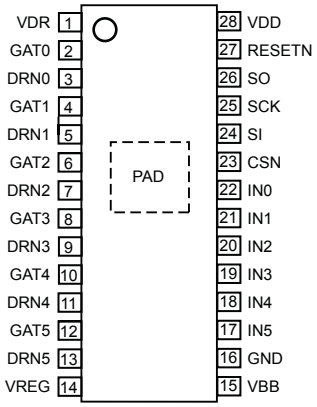
*Guaranteed by design characterization.

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	28	ºC/W
		2-layer PCB with 3.8 in.^{2} of copper area each side	32	ºC/W
Package Thermal Resistance, Junction to Pad	$R_{\theta JP}$		2	ºC/W

*Additional thermal information available on the Allegro website

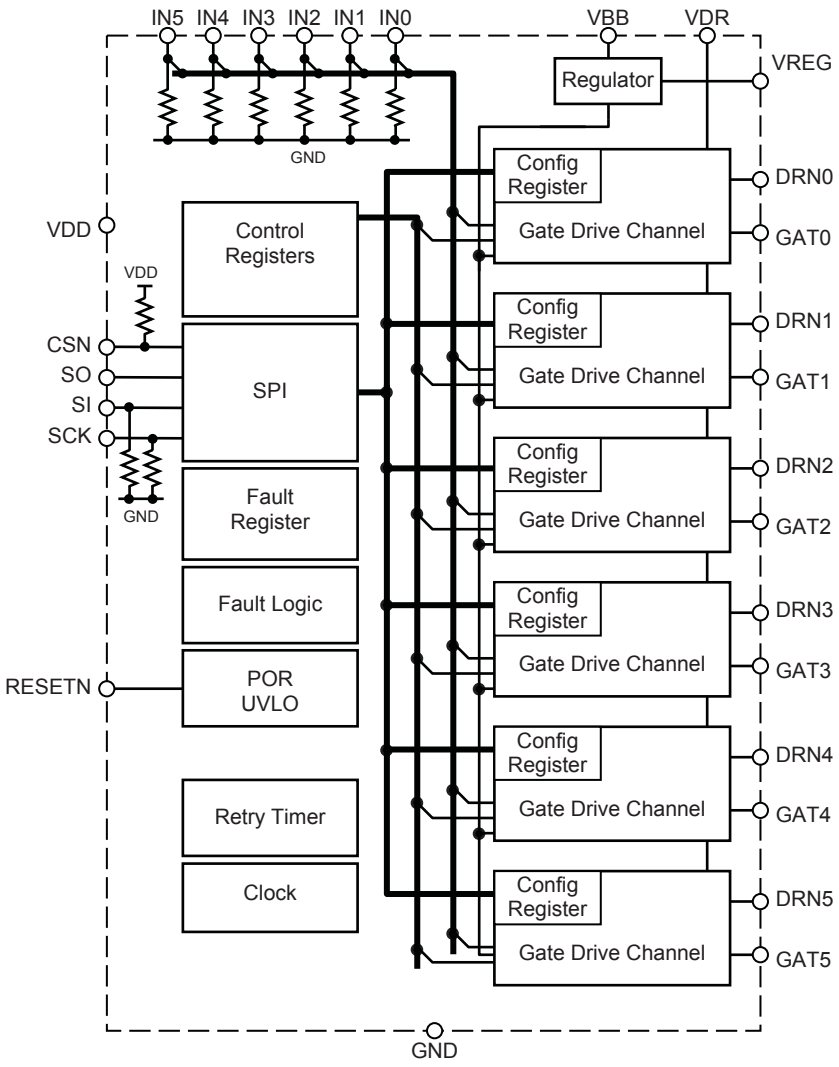
Pin-out Diagram



Terminal List Table

Name	Number	Function	Name	Number	Function
CSN	23	Serial interface chip select	IN1	21	Gate drive 1 control input
DRN0	3	Gate drive 0 drain sense input	IN2	20	Gate drive 2 control input
DRN1	5	Gate drive 1 drain sense input	IN3	19	Gate drive 3 control input
DRN2	7	Gate drive 2 drain sense input	IN4	18	Gate drive 4 control input
DRN3	9	Gate drive 3 drain sense input	IN5	17	Gate drive 5 control input
DRN4	11	Gate drive 4 drain sense input	PAD	–	Exposed thermal pad, connect to ground
DRN5	13	Gate drive 5 drain sense input	RESETN	27	Chip reset input
GAT0	2	Gate drive 0 output	SCK	25	Serial clock
GAT1	4	Gate drive 1 output	SI	24	Serial data input
GAT2	6	Gate drive 2 output	SO	26	Serial data output
GAT3	8	Gate drive 3 output	VBB	15	Analog supply (Battery)
GAT4	10	Gate drive 4 output	VDD	28	Logic Supply
GAT5	12	Gate drive 5 output	VDR	1	Gate drive supply
GND	16	Power ground	VREG	14	Voltage regulator
IN0	22	Gate drive 0 control input			

Functional Block Diagram



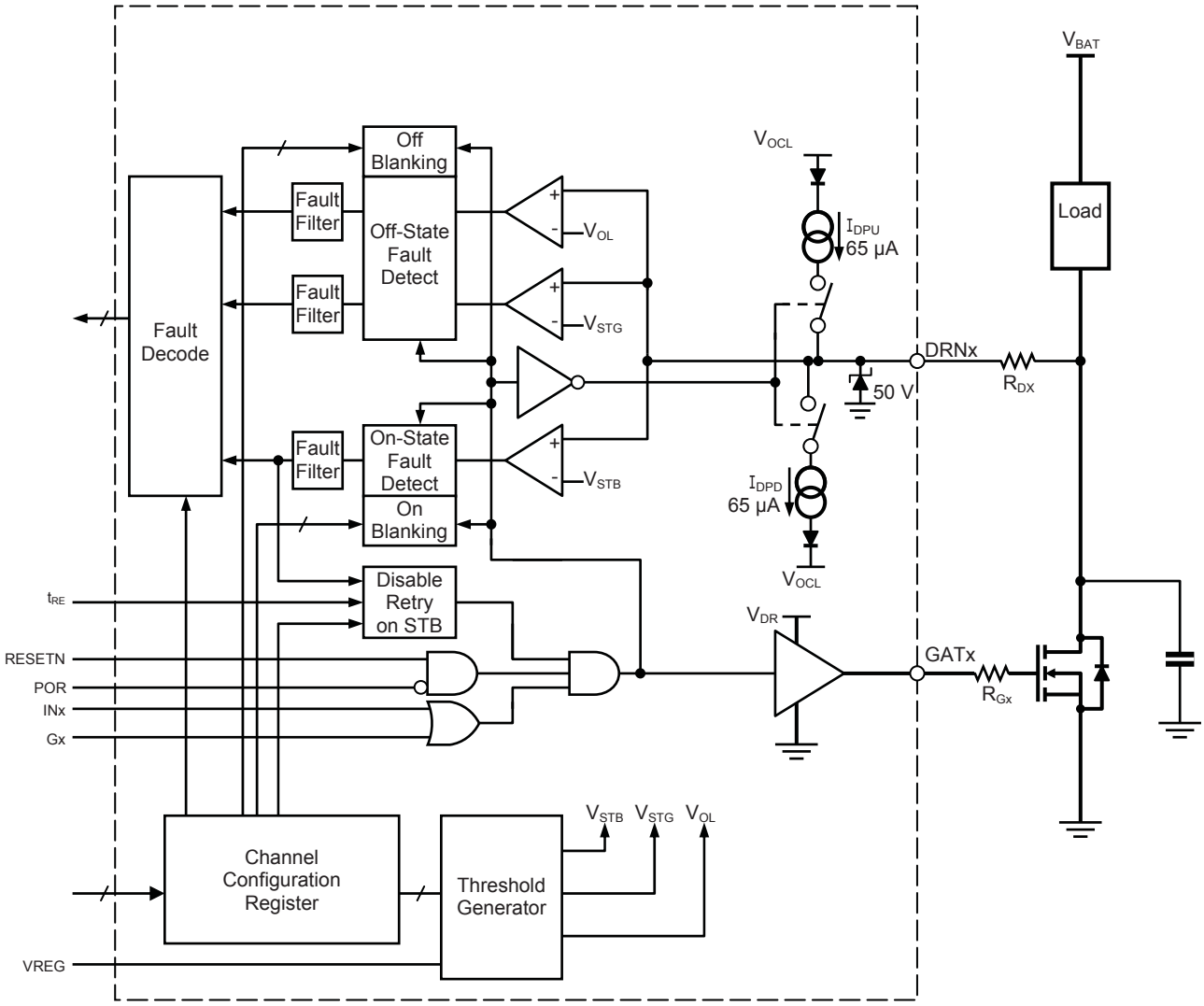


Figure 1. Gate Drive Channel functional block diagram (shows 1 channel of 6)

ELECTRICAL CHARACTERISTICS Valid at T_J = –40°C to 150°C, V_{DD} = 3.3 V, V_{DR} = 5 V, V_{BB} = 6 to 40 V; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply and Reference						
Logic Supply Voltage	V_{DD}		3.0	–	5.5	V
Analog Supply Voltage	V_{BB}		6	–	40	V
Gate Drive Supply Voltage	V_{DR}		3.0	–	6.0	V
VDD Quiescent Current	I_{DDQ}		–	–	3	mA
VBB Quiescent Current	I_{BBQ}		–	–	4	mA
		V_{DD} = 0, V_{BB} ≤ 30 V	–	–	10	µA
VDR Quiescent current	I_{DRQ}		–	–	4	mA
Regulator Voltage	V_{REG}	V_{BB} > 19.5 V	17.5	–	18.5	V
Regulator Dropout	V_{DO}		0	–	0.6	V
RESETN Pulse Width	t_{RST}		1	–	–	µs
RESETN Glitch Filter	t_{RGF}		–	–	200	ns
Oscillator Frequency	f_{OSC}		1.4	2	2.6	MHz
Digital Inputs and Outputs						
Input High Voltage	V_{IH}		70	–	–	%V_{DD}
Input Low Voltage	V_{IL}		–	–	30	%V_{DD}
Input Hysteresis	V_{Ihys}		300	500	–	mV
Input Pull-Up Resistor	R_{PU}	CSN to VDD	–	50	–	kΩ
Input Pull-Down Resistor	R_{PD}	INx, SI, SCK to GND	–	50	–	kΩ
SO Output High Voltage*	V_{OH}	SO, I_{OH} = –2 mA	V_{DD} - 0.4	V_{DD} - 0.2	–	V
SO Output Low Voltage	V_{OL}	SO, I_{OL} = 2 mA	–	0.2	0.4	V
SO Output Leakage*	I_L	CSN = VDD	–1	–	1	µA
Gate Output Drive						
Pull-Up On-Resistance*	$R_{DS(on)UP}$	T_J = 25°C, I_{GHx} = –20 mA	25	50	70	Ω
		T_J = 150°C, I_{GHx} = –20 mA	50	75	125	Ω
Pull-Down On-Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GLx} = 20 mA	25	50	70	Ω
		T_J = 150°C, I_{GLx} = 20 mA	50	75	125	Ω
Output Sink Current	I_{GL}	GATx off, V_{GATx} = V_{DR}	20	–	–	mA
Output Source Current*	I_{GH}	GATx on, V_{GATx} = 0 V	–	–	–40	mA
Output Rise Time	t_r	C_{LOAD} = 400 pF, 20% to 80% V_{DR}	–	180	–	ns
Output Fall Time	t_f	C_{LOAD} = 400 pF, 80% to 20% V_{DR}	–	180	–	ns
Minimum On-Time	t_{on}	At INx input	–	–	1	µs
Minimum Off-Time	t_{off}	At INx input	–	–	1	µs
Turn-On Propagation Delay	$t_{P(on)}$	INx to GATx	–	200	–	ns
Turn-Off Propagation Delay	$t_{P(off)}$	INx to GATx	–	200	–	ns
		RESETN to GATx	–	0.5	1	µs

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ELECTRICAL CHARACTERISTICS (continued) Valid at T_J = –40°C to 150°C, V_{DD} = 3.3 V, V_{DR} = 5 V, V_{BB} = 6 to 40 V; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Fault Detection (On-State)						
Drain Clamp Voltage	V_{DCL}	I_{DRNx} = 10 µA	45	–	–	V
		I_{DRNx} = 10 mA	–	54	–	V
Drain Clamp Leakage	I_{DC}	V_{DRNx} < 32 V	–	–	1	µA
Short to Battery Threshold	V_{STB}	GATx driven high, SB[2:0] = 111	30	31	32	%V_{REG}
		GATx driven high, SB[2:0] = 110	17	18	19	%V_{REG}
		GATx driven high, SB[2:0] = 101	15	16	17	%V_{REG}
		GATx driven high, SB[2:0] = 100	13	14	15	%V_{REG}
		GATx driven high, SB[2:0] = 011	11	12	13	%V_{REG}
		GATx driven high, SB[2:0] = 010	9	10	11	%V_{REG}
		GATx driven high, SB[2:0] = 001	7	8	9	%V_{REG}
		GATx driven high, SB[2:0] = 000	5	6	7	%V_{REG}
Retry Timer	t_{RE}	RT0 = 1	40	55	72	ms
		RT0 = 0	7	10	13	ms
Fault Filter Time	$t_{FF(on)}$		1.25	2	2.75	µs
Fault Blank Timer	$t_{BL(on)}$	GATx driven high, TON[1:0] = 11	40	56	72	µs
		GATx driven high, TON[1:0] = 10	20	28	36	µs
		GATx driven high, TON[1:0] = 01	10	14	18	µs
		GATx driven high, TON[1:0] = 00	4	5	7	µs
Fault Detection (Off-State)						
DRNx Pull-Up Diagnostic Current*	I_{DPU}	GATx low, V_{DRNx} < (V_{OCL} – 200 mV)	–80	–65	–50	µA
DRNx Pull-Down Diagnostic Current	I_{DPD}	GATx low, NPD = 0, V_{DRNx} >(V_{OCL} + 200 mV)	50	65	80	µA
Short to Ground Threshold	V_{STG}	GATx driven low, SG = 1	65	66	67	%V_{REG}
		GATx driven low, SG = 0	44	45	46	%V_{REG}
Open Load Threshold	V_{OL}	GATx driven low	75	76	77	%V_{REG}
Open Load Clamp Voltage	V_{OCL}		70	71	72	%V_{REG}
Fault Filter Time	$t_{FF(off)}$		1.25	2	2.75	µs
Fault Blank Timer	$t_{BL(off)}$	GATx driven low, TOF[1:0] = 11	3000	4000	5000	µs
		GATx driven low, TOF[1:0] = 10	200	280	360	µs
		GATx driven low, TOF[1:0] = 01	100	140	180	µs
		GATx driven low, TOF[1:0] = 00	60	80	100	µs

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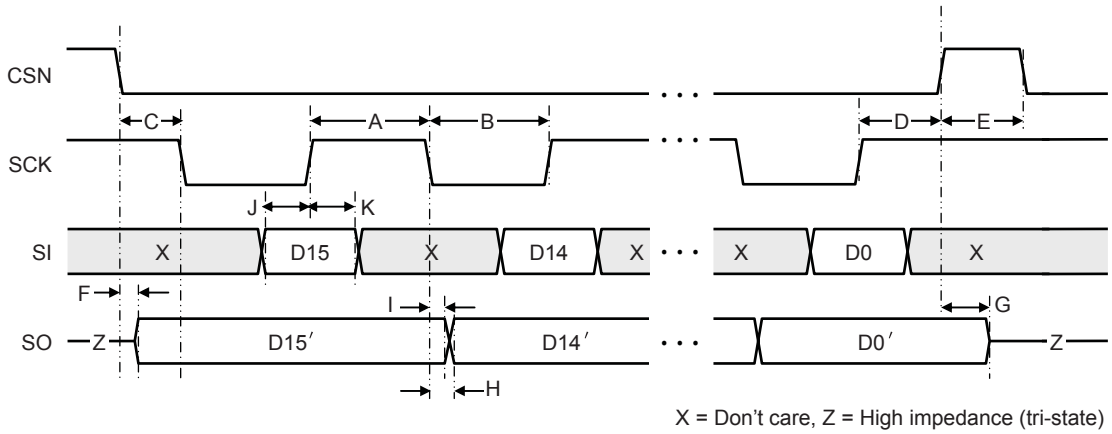
ELECTRICAL CHARACTERISTICS (continued) Valid at T_J = –40°C to 150°C, V_{DD} = 3.3 V, V_{DR} = 5 V, V_{BB} = 6 to 40 V; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Serial Interface Timing						
Clock High Time	t_{SCKH}	A in figure 2	50	–	–	ns
Clock Low Time	t_{SCKL}	B in figure 2	50	–	–	ns
CSN Set-up to SCK Low	t_{CSS}	C in figure 2	30	–	–	ns
CSN Hold after SCK High	t_{CSHD}	D in figure 2	30	–	–	ns
CSN High Time	t_{CSH}	E in figure 2	300	–	–	ns
Data Out Enable Time	t_{SOE}	F in figure 2	–	–	40	ns
Data Out Disable Time	t_{SOD}	G in figure 2	–	–	30	ns
Data Out Valid Time from Clock Falling	t_{SOV}	H in figure 2	–	–	40	ns
Data Out Hold Time from Clock Falling	t_{SOH}	I in figure 2	5	–	–	ns
Data In Set-up Time to Clock Rising	t_{SIS}	J in figure 2	15	–	–	ns
Data In Hold Time from Clock Rising	t_{SIH}	K in figure 2	10	–	–	ns
CSN High to Output Change	t_{PCS}		–	200	–	ns
Chip Diagnostics Protection						
VDD Undervoltage Lockout	V_{DDUV}	Decreasing V_{DD}	2.6	2.75	2.9	V
VDD Undervoltage Lockout Hysteresis	$V_{DDUVhys}$		50	100	150	mV
VREG Undervoltage Lockout	V_{REGUV}	Decreasing V_{REG}	4.5	4.8	5.1	V
VREG Undervoltage Lockout Hysteresis	$V_{REGUVhys}$		100	200	300	mV
Overtemperature Warning Threshold	T_{JW}	Temperature increasing	145	160	175	ºC
Overtemperature Hysteresis	T_{JWhys}	Recovery = $T_{JW} - T_{JWhys}$	–	15	–	ºC

*For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.



X = Don't care, Z = High impedance (tri-state)

Figure 2. Serial Interface Timing Diagram. Letter keys refer to the Serial Interface Timing section of the Electrical Characteristics table.

Functional Description

The A3944 provides a programmable interface between an ECU and 6 low-side MOSFET switches in automotive applications. Each channel provides all the features necessary to drive and monitor the external FET and load.

The gate of the external FET is driven by a 50 Ω (typ) push-pull driver capable of sourcing and sinking at least 40 mA under all conditions. This is sufficient to allow most typically used FETs to be switched with a PWM input at up to 10 kHz. The state of each channel is determined by a combination of parallel and serial inputs.

When the FET is active its drain is monitored for a short to battery. When the FET is inactive, internal current sources are activated and the drain voltage is monitored to check for shorts to ground or open loads.

The serial, SPI compatible interface provides access to control and configuration registers. Each channel has a dedicated fault configuration register that allows independent fault thresholds, fault timing, and fault configuration for each channel.

The output state of each channel is determined by the logic control input for the channel and a dedicated bit in the single output control register. Channels can therefore be controlled by parallel input, by serial input, or by a combination of the two. All channels can be switched at the same time with a single serial write.

A single fault mask register can be used to ignore the fault detect output for any channel combination.

The serial interface also provides read back of the fault status for each channel.

Digital inputs and outputs are compatible with 3.3 V and 5 V supplies.

Terminal Functions

VDD: Positive supply for digital input, output, and logic.

VBB: Positive supply for voltage regulator. Can be connected to battery voltage through reverse polarity protection.

VREG: Regulated voltage for analog and reference functions.

VDR: Positive supply for gate drive outputs.

GND: Ground return. Connect to common return point for all external MOSFET source connections.

RESETN: Active low digital input. When held low for longer than the minimum reset pulse width: forces outputs low, resets the configuration, sets the LR bit, and resets all other channel faults.

SI: Active high digital input with pull-down resistor. Data on SI is clocked into the serial register on the rising edge of SCK.

SO: Push-pull digital output. Data from the fault register is output on SO, changing on the falling edge of SCK.

SCK: Digital clock input with pull-down resistor. See SI and SO for action.

CSN: Active low digital input with pull-up resistor. When CSN is low SO becomes active and data is accepted on SI. Data is latched in the serial register when CSN goes high. When CSN is high SO is high impedance and SI and SCK are ignored.

INx: Active high digital inputs with pull-down resistors. When INx is high GATx is allowed to go high, depending the contents of the serial control register and any active faults. When INx is low GATx is held off.

GATx: Gate drive outputs. Drive between GND and VDR. Connected through a resistor or directly to the gate of the external MOSFETs.

DRNx: Analog, high-voltage inputs. Drain monitor connection used to determine the status of the drive to the load.

Gate Drive Channels

Each gate drive channel has independent control logic, gate drive output, fault detection circuitry, fault threshold generators, fault timers, and fault configuration register. The fault configuration register and reference generation provides two short to ground thresholds and eight short to battery thresholds, plus four turn-on blank times and four turn-off blank times independently selectable per channel.

The gate drive channel block diagram (figure 1) shows the functional circuit for one gate drive channel, which is duplicated in each gate drive channel. A retry timer, common to all channels, allows automatic retry for short to battery faults.

Control and Enable

A gate drive output, GATx, is turned-on when: RESETN is high, no short to battery fault is present, and either the direct digital input, INx, or the relevant bit in the serial control register, Gx, is

high, in other words the logical OR of the INx input and the Gx bit for each channel x. If the GATx output is to be controlled by the serial interface, then the corresponding INx logic input should be held low. Internal pull-down resistors from each INx terminal to GND ensure that any unconnected input will be pulled low. Conversely, if the GATx output is to be controlled by the INx logic input, then the corresponding Gx bit in the control register should be set to 0, which is its default power-on and reset state.

Gate Drive Output

Each gate drive output is designed to provide symmetrical charge current from the VDR supply terminal and discharge current to the GND return terminal. The maximum source and sink impedance provides peak charge and discharge currents of at least 50 mA when connected directly to the gate of the external FET. This current can be limited, in order to limit the FET turn-on switching speed, by using a resistor between the GATx output and the gate of the FET. Although the GATx drive is designed to be symmetrical, the actual drive performance will be affected by the FET parameters and the resistance between the GATx output and the gate of the FET.

The VDR supply is used only to supply the GATx output. The voltage at VDR can therefore be varied to provide voltage limited drive to the FET gate. Undervoltage detection is not provided for this supply.

Reset Function

If RESETN is held low for more than the minimum reset pulse width, then all registers are reset to their power-on state, and all GATx outputs are held low. Any latched channel faults and corresponding bits in the fault register are reset, the logic reset (LR) bit is set, and the UV and OT bits reflect the status of the undervoltage and overtemperature detectors.

The RESETN input uses a glitch filter to reduce the susceptibility to transients and noise on the RESETN input. This glitch filter is guaranteed to ignore any pulses shorter than the minimum RESETN glitch filter time, t_{RGF}.

Channel Fault Diagnostics

All channel faults are determined by monitoring the voltage at the drain of the external FET through the DRNx terminal. Each channel has independent bias current generators, programmable fault comparators, fault decode logic, and programmable fault timers. The serial interface provides a dedicated fault configuration register for each channel to select these features and thresholds per channel. A single fault mask register provides a fault mask bit for each channel. Fault detection is disabled when RESETN is low or when the fault mask bit is set. Fault reporting through the serial interface is fully described in the Serial Interface section below.

A short to battery (short across the load to the load supply) can be detected when the channel is active, GATx is high, and the FET is on (on-state). A short to battery fault always attempts to protect the FET by pulling GATx low.

A short to ground or open load can be detected when GATx is low and the FET is off (off-state). A short to ground fault or open load fault does not interfere with the operation of the GATx output.

Each channel fault detected is latched as a fault state, and remains latched until the diagnostic circuits can determine that the fault has been removed for that channel. This determination can only occur at the end of a fault blank time. For short to battery this is at the end of the on-state fault blank time following a transition from off to on. For a short to ground or open load this is at the end of the off-state fault blank time following a transition from on to off.

When a fault is detected, a dedicated bit in one of the two fault registers is set for each fault on each channel. This requires 3 bits per channel over 6 channels or 18 fault bits in total. The fault bits in the fault registers remain latched until the first serial transfer after the associated fault state has been reset. All latched fault states and all latched channel fault bits can also be cleared either by a power-on reset or by taking the RESETN terminal low.

Practical limits for load resistance, and voltage conditions to provide effective determination of the load status, are discussed in the Applications Information section below.

Note that each DRNx terminal has an internal Zener clamp which limits the voltage at the terminal to V_{DCL}. If the voltage at the drain of the FET is likely to be higher than V_{DCL}, even during a transient, then a current limit resistor, R_{Dx}, must be added

between the drain connection to the FET and the DRNx terminal. This resistor should be selected such that the energy dissipated by the clamp diode is less than the absolute maximum drain clamp energy, E_{DRN}. This is necessary to avoid excessive heat generation in the silicon; otherwise permanent damage to the chip is likely. Selecting a value for R_{Dx} is described in the Applications Information section, below.

On-State Diagnostics: Short to Battery

When a channel is in the on-state the voltage at the drain monitor terminal, V_{DRNx}, is compared to a threshold level derived from the voltage at the REF terminal. A short to battery fault is present if V_{DRNx} is higher than V_{STB} (see figure 3). Note that an open FET also would be detected as a short to battery.

The threshold voltage, V_{STB}, is selected per channel as a percentage of the voltage at the REF terminal. The voltage selection is determined by the SB0, SB1, and SB2 bits (bits1, 2, and 3 of the fault configuration register for the channel).

When a FET is switched-on there is a finite time before the drain voltage reaches a steady state. To avoid false fault detection at switch-on, the output from the short to battery comparator is ignored during the on-state fault blank time, $t_{BL(on)}$, after the GATx output is commanded to drive high. One of four possible on-state fault blank times is selected, per channel, through the TON0 and TON1 bits (bits 4 and 5 of the fault configuration register for the channel).

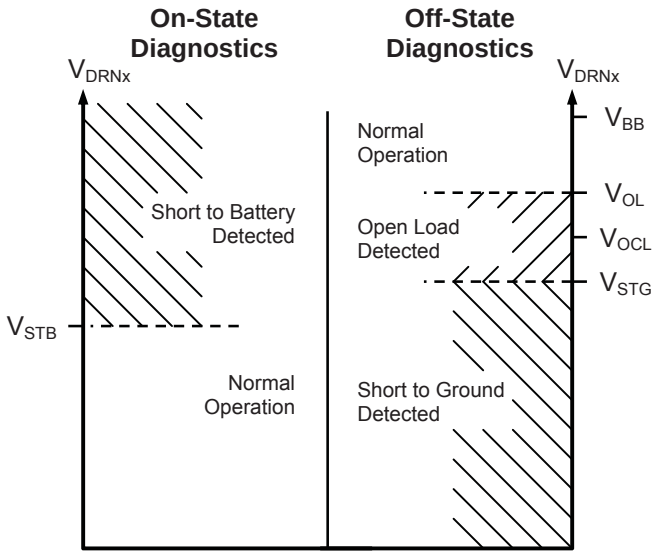


Figure 3. Diagnostic Threshold Voltages

To avoid false fault detection during supply transients, when the FET is active an additional fault filter will mask faults that are present for less than the on-state fault filter time, $t_{FF(on)}$. This fault filter is only active after the fault blank time.

The result is that directly after switch-on, a short to battery fault will not be detected until $t_{BL(on)}$ after the GATx output is commanded to drive high. If a short occurs after $t_{BL(on)}$ from switch-on, then it must be present for at least $t_{FF(on)}$ before it is detected.

When a short to battery is detected the GATx output is automatically commanded to drive low and to switch-off the FET. Two alternative modes are then available depending on the status of the RT0 and RT1 bits (bits 10 and 11 of the fault configuration register for the channel).

If RT1 is 0, the FET will be held off until the fault is reset by pulsing RESETN low for longer than t_{RST} or by toggling the channel off then on, through the serial interface. In this mode, toggling the input terminal for the channel has no effect until after a reset.

If RT1 is 1, the channel will be held off until one of the two common retry timers completes a time-out. The timer selection is made by the state of the RT0 bit. The channel control bits, both serial and logic input, are ignored during this time. At the end of the retry time-out the channel will be switched-on again if the state of the control logic commands the channel to be on. In the retry mode the fault can be reset also by pulsing RESETN low for longer than t_{RST} or by toggling the channel off then on, through the serial interface. This resets the channel fault and re-enables the channel from the control logic.

Note that, if the common retry timer has already been activated by another channel, then the first retry time-out for the second channel may be shorter that the full time. Subsequent retry sequences will run for the full time-out period minus the short detection time.

Off-State Diagnostics: Open Load and Short to Ground

Two current generators and two comparators per channel provide off-state diagnostic capability. If the voltage at the DRNx terminal, V_{DRNx}, is greater than the open load clamp voltage, V_{OCL}, then one of the current generators sinks current to V_{OCL} through the DRNx terminal. If V_{DRNx} is less than V_{OCL}, then one of the current generators sources current from V_{OCL} through the DRNx

terminal. The voltage output capability of the current sources is limited such that they cannot source current when the output voltage is greater than V_{OCL} or sink current when the output voltage is less than V_{OCL}. The equivalent circuit is shown in figure 4a. The typical sink and source currents are shown graphically in figure 4b.

When a channel is in the off-state the current generators source or sink current through the DRNx terminal in an attempt to pull the voltage at the terminal to the open load clamp voltage, V_{OCL}. The resulting voltage at the DRNx terminal, V_{DRNx}, is measured to test for a short to ground or an open load.

Normal Operation

If a load is present, the load supply is active, and there are no shorts to ground, then the load will pull V_{DRNx} above V_{OCL}.

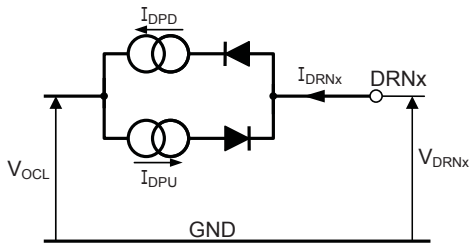


Figure 4a. Diagnostic Current Source Circuit

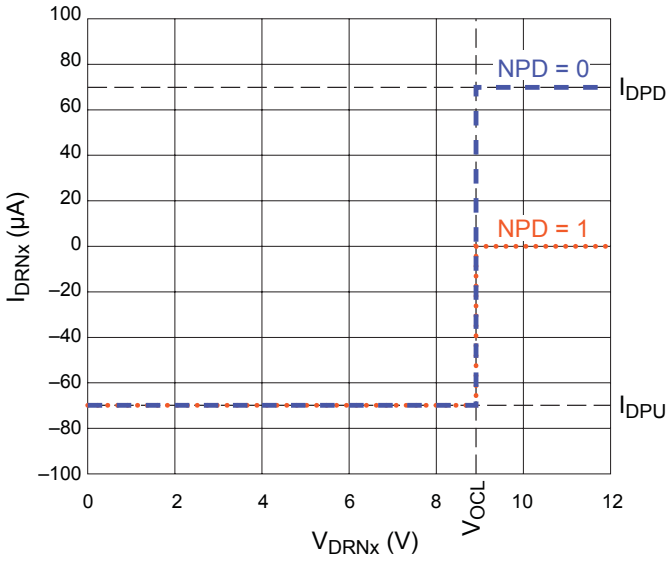


Figure 4b. Diagnostic Currents

V_{DRNx} will then be greater than the open load threshold, V_{OL}, and no fault is detected (see figure 3). If the NPD bit is zero then the current sink will pull I_{DPD} from the supply through the load, through the DRNx terminal, to V_{OCL}

The open load threshold, V_{OL}, and the open load clamp voltage, V_{OCL}, are a both a fixed percentage of the voltage at the VREG terminal and are common to all channels.

Short to Ground

If a short to ground is present, then V_{DRNx} will be pulled low by the short circuit. V_{DRNx} will be less than the short detect threshold, V_{STG}, and a short to ground fault is reported (see figure 3).

The short detect threshold voltage, V_{STG}, is selected, per channel, as a percentage of the voltage at the VREG terminal. The voltage selection is determined by the SG bit (bit 0 of the fault configuration register for the channel).

Open Load

If there is no short to ground or to supply, and the load is not connected, then the current sources will pull V_{DRNx} towards the open load clamp voltage, V_{OCL}. V_{DRNx} will then be greater than V_{STG} but less than V_{OL} and an open load is reported (see figure 3).

The time taken for V_{DRNx} to reach the correct value for an open fault condition depends on the current sourced from the DRNx terminal and on the capacitance connected to the drain of the FET. To avoid false fault detection at switch-off, the outputs from the short to ground and open load comparators are ignored during the off-state fault blank time, $t_{BL(off)}$, after the GATx output drives low. One of four possible off-state fault blank times is selected, per channel, through the TOF0 and TOF1 bits (bits 6 and 7 of the fault configuration register for the channel).

To avoid false fault detection during supply transients, an additional fault filter masks faults that are present for less than the off-state fault filter time, $t_{FF(off)}$. This fault filter is only active after the fault blank time.

The result is that directly after switch-off, a short to ground or open load fault will not be detected until $t_{BL(off)}$ after the GATx output is commanded to drive low. If a fault occurs after $t_{BL(off)}$ from switch-off then it must be present for at least $t_{FF(off)}$ before it is detected.

In some applications, for example when driving high efficiency LEDs, the load may be sensitive to the pull down current used to

ensure open load detection. In these cases this pull-down current can be disabled by setting the NPD bit (bit 8 in the fault configuration register for the channel). If the NPD bit is set then it is possible that V_{DRNx} will reach the correct value for an open fault condition when the load is connected, resulting in a false open load detection.

If this is likely, there are two options:

- Set the fault mask bit for the channel. This will mask all faults on that channel and may not be a suitable option.
- Set the open load fault mask bit, OLM (bit 6 in the fault mask register). This will disable open load detection on any channel where NPD is set to 1.

Chip Diagnostics

The chip temperature and the supply voltage levels at VDD and VREG are monitored to ensure correct and safe operation of the circuit.

VDD is monitored to ensure that power-up and power-down does not cause incorrect operation. All outputs will be switched to high impedance, the VREG regulator will be disabled and all faults reset when the voltage at VDD, V_{DD}, falls below the undervoltage level, V_{DDUV}. The outputs will be reactivated when V_{DD} rises above the undervoltage turn-on level plus the hysteresis voltage, defined as $V_{DDUV} + V_{DDUVhys}$. When V_{DD} rises above this threshold, all registers will be reset to their power-on state, and all GATx outputs will be low. In the fault register any latched channel faults will be reset, the logic reset (LR) and undervoltage (UV) bits will be set, and the OT bit will reflect the status of the overtemperature monitor.

VREG is monitored to ensure correct operation of the fault detection and control circuits. All channel faults will be reset when the voltage at VREG, V_{REG}, falls below the undervoltage level, V_{REGUV}. They will be held reset until V_{REG} rises above the undervoltage lockout level plus the hysteresis voltage, $V_{REGUV} + V_{REGUVhys}$. The outputs will remain active irrespective of the value of V_{REG}.

The chip temperature is monitored by the thermal warning circuit. An overtemperature fault will be indicated but no action will be taken when the chip temperature exceeds the overtemperature warning level T_{JW}. It is incumbent upon the user to take any necessary action to limit dissipation to reduce the temperature.

Serial Interface

The inputs CSN, SCK, and SI provide a three wire synchronous serial interface, compatible with SPI, that can be used to control all features of the A3944. The output, SO, can be used to provide a fourth interface connection for detailed diagnostic feedback.

The serial interface timing requirements are specified in the Electrical Characteristics table, and illustrated in the Serial Interface Timing diagram, figure 2. Data is received on the SI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. CSN is normally held high, and is only brought low to initiate a serial transfer. No data is clocked through the shift register when CSN is high, allowing multiple slave units to use common SI, SCK, and SO connections. Each slave then requires an independent CSN connection.

When 16 data bits have been clocked into the shift register, CSN must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the fault register is reset.

If there is either: more than 16 rising edges on SCK, or at least one but fewer than 16 rising edges on SCK and CSN goes high, then the write will be cancelled without writing data to the registers or resetting the diagnostic registers. The FF bit will be set to indicate a data transfer error.

Configuration and Control Registers

The serial data word is 16 bits, input MSB first. The first four bits are defined as the register address. This provides sixteen writeable registers:

Address 1: Gate Select Register

The six least significant bits of this register are the control bits for each of the six channels. G0 corresponds to channel 0, G1 to channel 1, and so forth. If RESETN is high and no faults are present on the channel, then when the Gx bit for a channel is set to 1 the GATx output will be high.

Address 5: Fault Mask Register

The six least significant bits of this register are the fault mask bits for each of the six channels. K0 corresponds to channel 0, K1 to channel 1, and so forth. When the K bit for a channel is set to 1 all faults on that channel are ignored and no faults are reported for that channel. Bit 6 is an open load fault mask bit, OLM, that disables the open load detection on any channel where NPD is set to 1.

Addresses 8 to 13: Channel Fault Configuration Registers

These six registers, one per channel, determine the fault threshold levels, fault blank times, and fault features for each channel. The MSB is always set to 1. The next three bits, bits 12,13, and 14, are the channel address bits.

The remaining register addresses are unused. Writing to these addresses will have no effect on the operation but will still report the fault register on SO.

Fault Register

In addition to the writable registers there are two fault registers, Fault0 and Fault1. The register being output is identified by bit 11, which contains a zero for Fault0 and a one for Fault1. Each time any register is written through the serial interface, one of the fault registers can be read, MSB first, on the serial output terminal, SO (see the Serial Interface Timing diagram, figure 2). Fault0 is output: on the first write after a power-on-reset, after a RESETN low input, or after a serial fault poll (described in the next paragraph). Fault1 is then read on the next write. The two registers then alternate on each successful serial write sequence.

The first, most significant, bit in both fault registers is the fault register flag, FF (bit 15). This bit is set to one, if any faults have been detected since the last fault reset. The state of FF appears on SDO as soon as CSN goes low, allowing the fault status to be determined without a change in the level of SCK. A serial transfer may be terminated when CSN goes low then high, without generating a serial read fault, by ensuring that SCK remains high while CSN is low. This allows the main controller to poll the A3944 through the serial interface to determine if a fault has been detected. When this occurs the fault register pointer is reset to the Fault0 register, so the next full write sequence outputs the Fault0 register. The fault status can also be read, without disturbing any settings, by writing to one of the unused register addresses. In this case the fault registers will continue to alternate between Fault0 and Fault1.

The next three most significant bits, after FF, in each fault register are the system diagnostic bits: UV (bit 14), LR (bit 13), and OT (bit 12). These provide an indication of undervoltage, logic reset, and overtemperature faults.

Bit 11 (FR) indicates which of the two fault registers is being output on SO. This bit is a zero for the Fault0 register and a one for the Fault1 register.

The least significant 9 bits in each fault register provide three bits per channel, one bit for each of the three possible fault states: short to battery, short to ground, and open load. Fault0 contains the fault data for channels 0, 1, and 2. Fault1 contains the fault data for channels 3, 4, and 5. The bits naming convention indicates the channel and fault allocation. The format is “ccff,” where “cc” is C0, C1, C2, C3, C4, or C5 (indicating the channel) and “ff” is SG, SB, or OL (indicating the faults: short-to-ground, short-to-battery and open-load respectively).

The contents of the fault register that is being read cannot change when CSN is low and a serial read is in progress. Any faults detected during a serial read do affect the read in progress but the fault will be latched in the fault register when CSN goes high at the end of a serial read. The fault bits can only be cleared after: either the diagnostic circuits have confirmed that the fault that has been reported is no longer present, or there is a low level on the RESETN input.

In the case of undervoltage or overtemperature faults, which are not latched, the fault bits will be reset at the end of a serial read if the fault is not detected at that time.

For channel faults, which are latched, the fault bits will be reset at the end of a serial read if the diagnostic circuits have previously determined that the fault that has been reported is no longer present. This determination can only occur at the end of a fault blank time and therefore requires: either an on-to-off transition (for short to ground and open load faults), or an off-to-on transition (for short to battery faults) on the faulty channel before the start of a serial read. Any changes to the fault state when a read is in progress are ignored until the end of the serial read. If a fault is cleared when a serial read is in progress, then the fault bits will be cleared when CSN goes high.

Figures 5 through 10 are channel fault timing diagrams, which show fault conditions applied to a channel and the results of the fault latches and the state of the fault register after serial reads and channel state changes. Each diagram shows the state of the channel control signal, INx, and the state of the gate drive output, GATx, for the channel, as well as an approximation of the relative voltage, DRNx, at the drain of the external MOSFET. Beneath this is the latched fault state and the contents of the fault register bits for the channel. The sequence of serial reads are shown at the bottom of each figure as the state of the CSN input and the resulting data bits read for the channel.

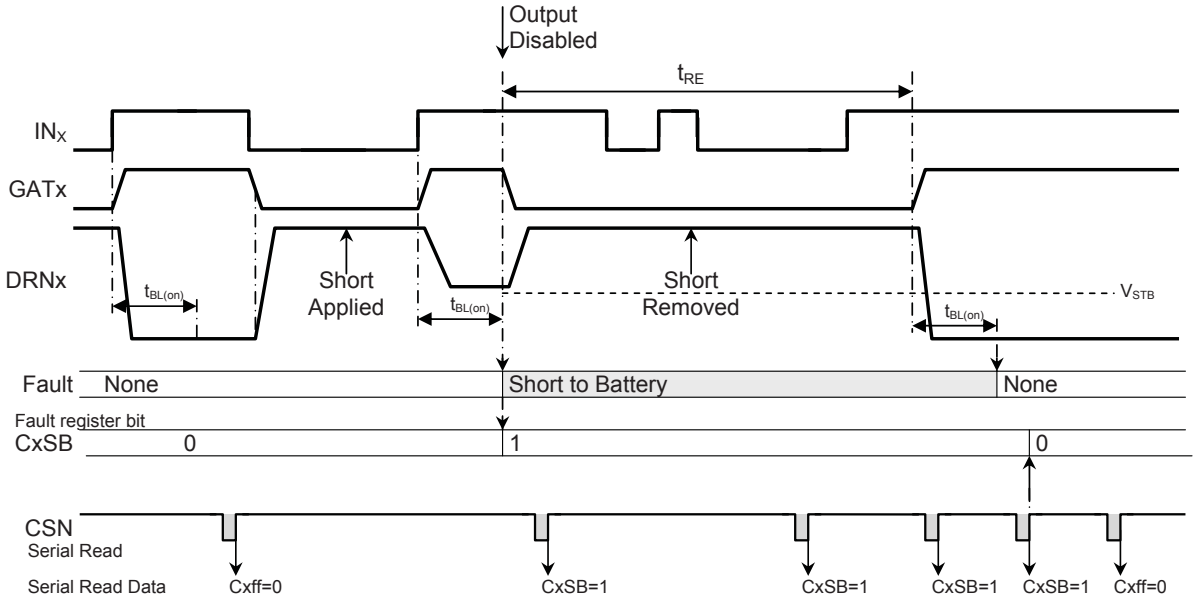


Figure 5. Fault Sequence: Short to battery during off-state (RT1=1)

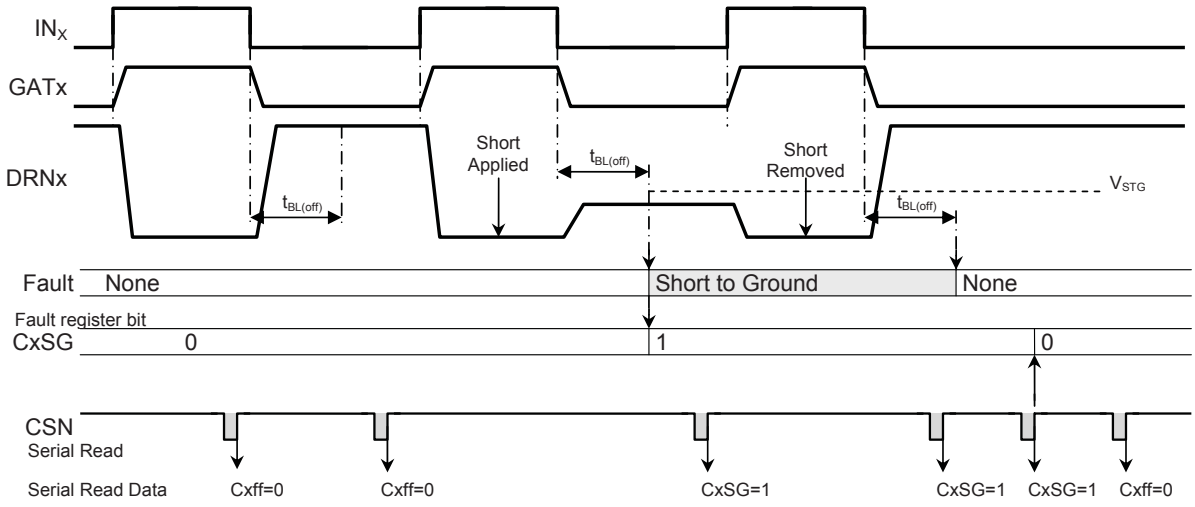


Figure 6. Fault Sequence: Short to ground during on-state

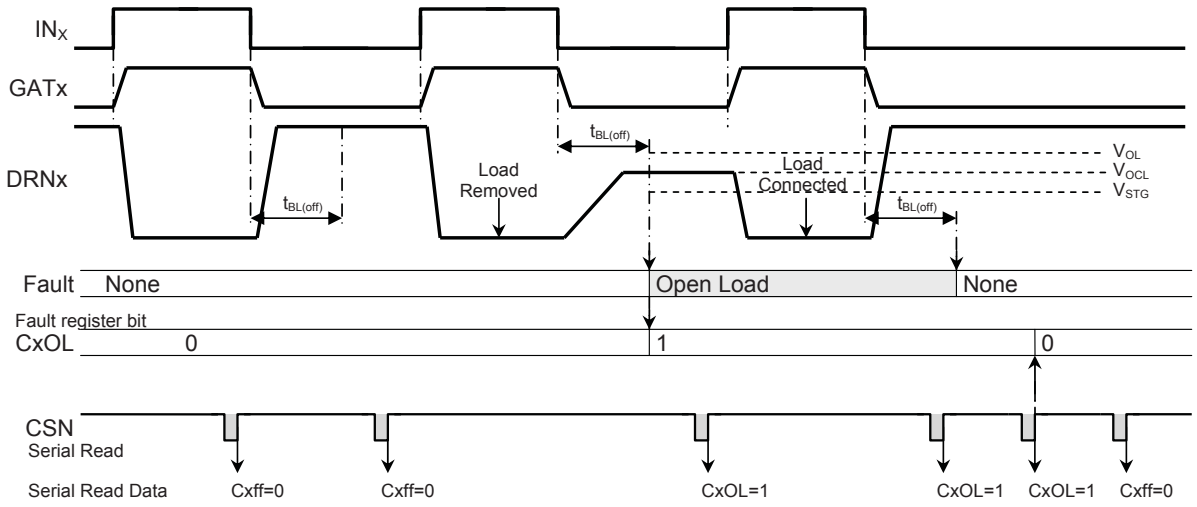


Figure 7. Fault Sequence: Open load during on-state

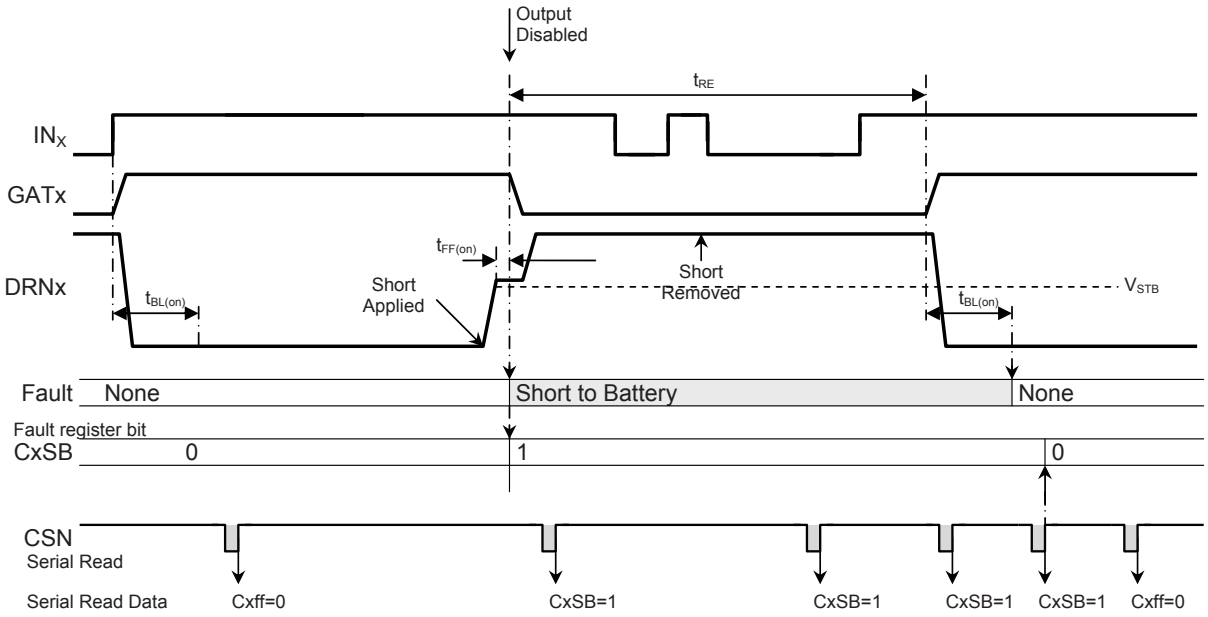


Figure 8. Fault Sequence : Short to battery during on-state (RT1=1)

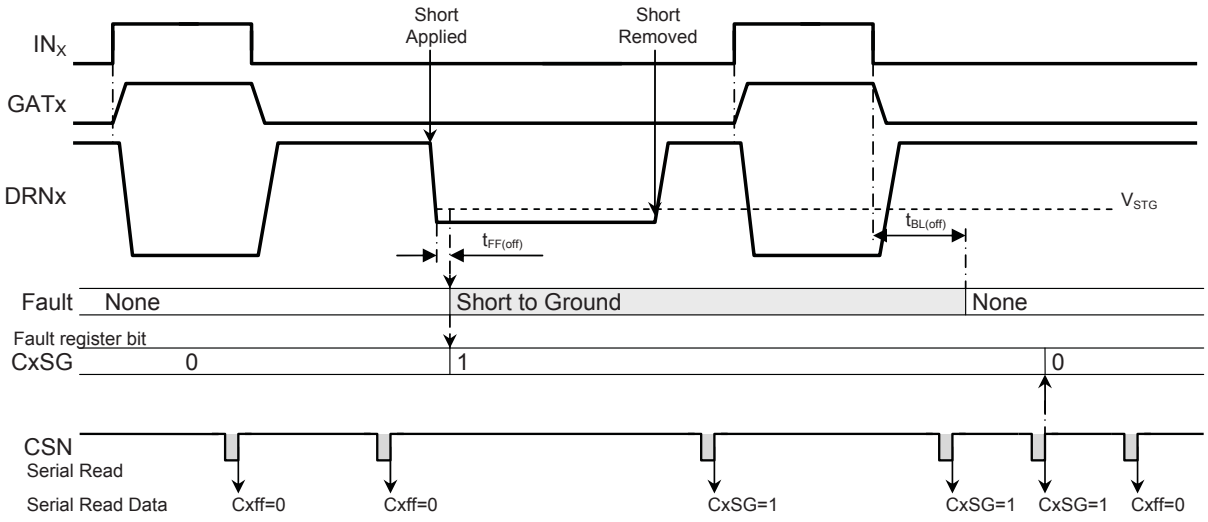


Figure 9. Fault Sequence: Short to ground during off-state

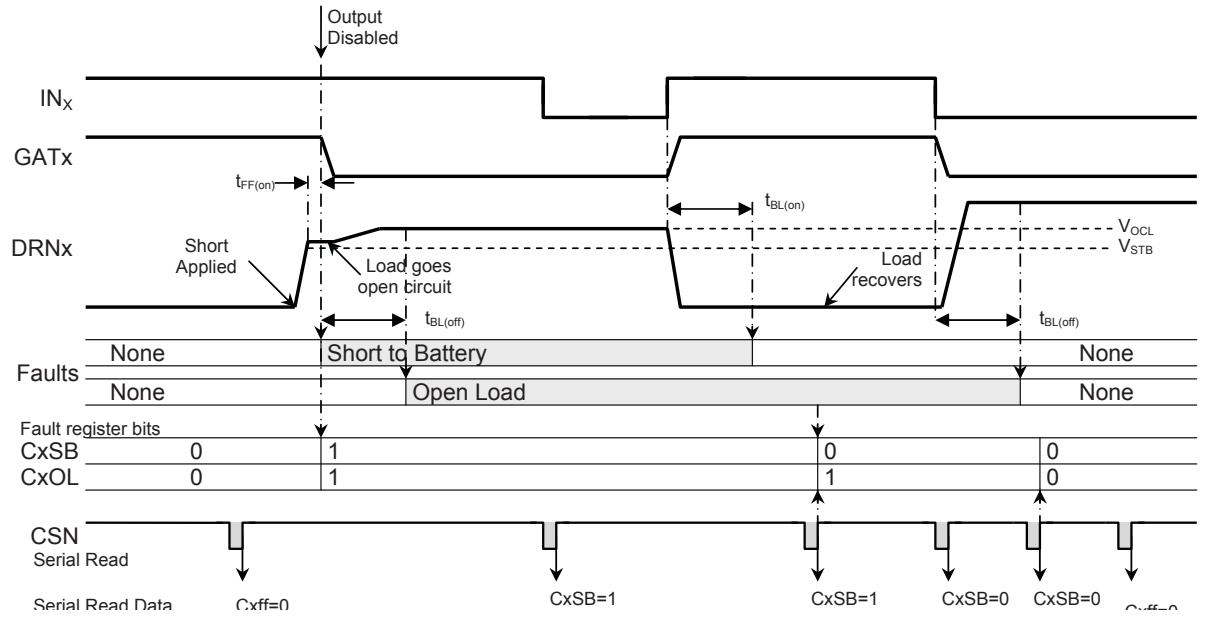


Figure 10. Fault Sequence: Short to battery during on-state followed immediately by open load (RT1=0)

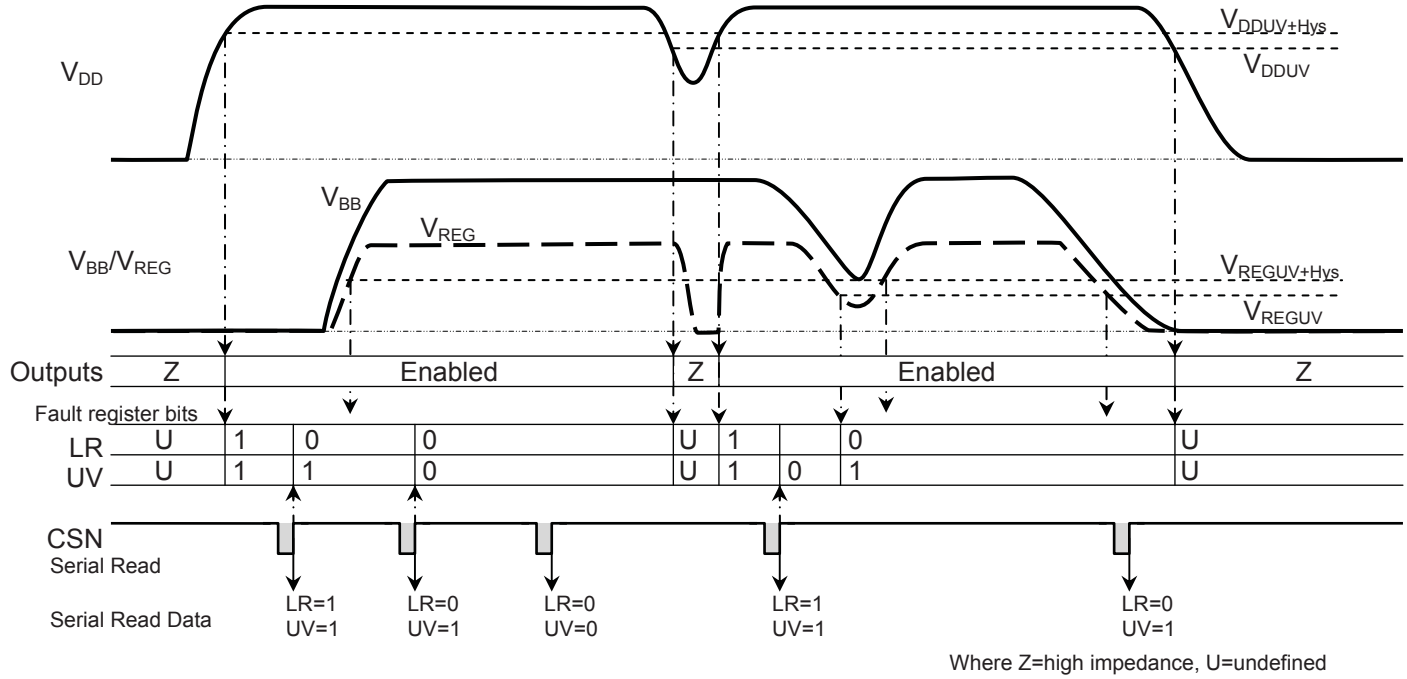


Figure 11. Power Sequence Timing- V_{DD} before V_{BB}

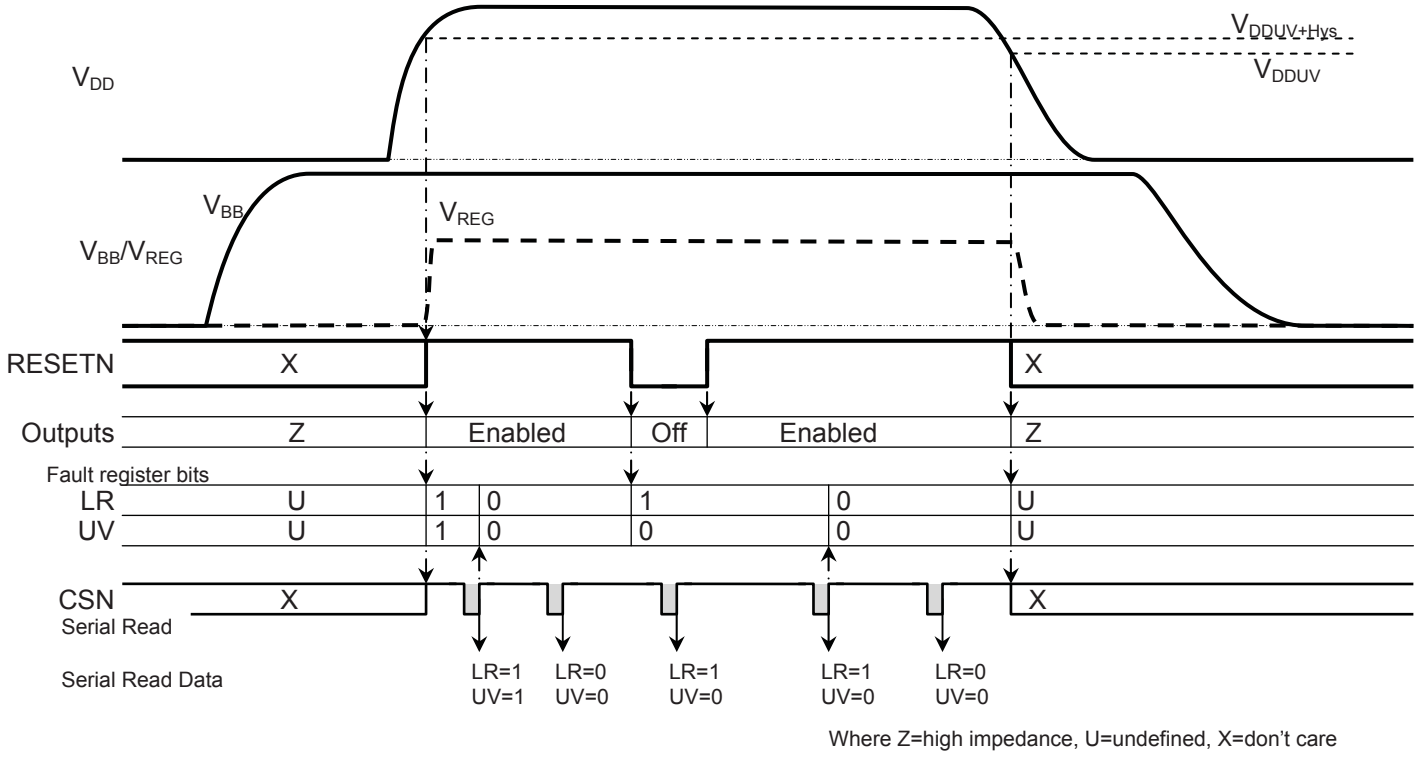


Figure 12. Power Sequence Timing- V_{DD} after V_{BB} - with RESET

Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Gate Select	0	0	0	1							G5	G4	G3	G2	G1	G0
					0	0	0	0	0	0	0	0	0	0	0	0
Fault Mask	0	1	0	1						OLM	K5	K4	K3	K2	K1	K0
					0	0	0	0	0	0	0	0	0	0	0	0
Channel Fault Config	1	ADR2	ADR1	ADR0	RT1	RT0		NPD	TOF1	TOF0	TON1	TON0	SB2	SB1	SB0	SG
					0	0	0	0	0	0	0	0	0	0	0	0
Fault0	FF	UV	LR	OT	FR	0	0	C2SG	C2SB	C2OL	C1SG	C1SB	C1OL	C0SG	C0SB	C0OL
	1	UV	1	OT	0	0	0	0	0	0	0	0	0	0	0	0
Fault1	FF	UV	LR	OT	FR	0	0	C5SG	C5SB	C5OL	C4SG	C4SB	C4OL	C3SG	C3SB	C3OL
	1	UV	1	OT	1	0	0	0	0	0	0	0	0	0	0	0

*Power on reset value shown below each input register bit.

Gate Select Register

G[5..0] Control bits for each of the six channels. G0 corresponds to channel 0, G1 to channel 1 etc. If RESETN is high and no faults are present on the channel then when the Gx bit for a channel is set to 1 the GATx output will be high

Fault Mask Register

K[5..0] Fault mask bits for each of the six channels. K0 corresponds to channel 0, K1 to channel 1 etc. When the Kx bit for a channel is set to 1 all faults on that channel are ignored and no faults are reported for that channel.

OLM Open load fault mask for all channels where NPD=1. If the NPD bit is set to 1 on a channel and OLM is set to 1 then the open load diagnostic is disabled for that channel.

Fault0/Fault1 Registers

FF Logic 1 if any faults have been detected since the last fault reset.

UV Logic 1 if any VDD or VREG undervoltage faults have been detected since the last fault reset.

LR Logic 1 if a logic reset has occurred since the last register read. A logic reset is caused by a power-on-reset or by taking the RESETN input low.

OT Logic 1 if an overtemperature fault has been detected since the last fault reset.

FR Fault register identifier. Logic 0 for Fault0 register, logic 1 for Fault1 register.

CxSG Logic 1 if channel short to ground detected. Where x is channel number.

CxSB Logic 1 if channel short to battery detected. Where x is channel number.

CxOL Logic 1 if channel open load detected. Where x is channel number.

Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel Fault Config	1	ADR2	ADR1	ADR0	RT1	RT0		NPD	TOF1	TOF0	TON1	TON0	SB2	SB1	SB0	SG
					0	0	0	0	0	0	0	0	0	0	0	0

*Power on reset value shown below each input register bit.

Channel Fault Config Register

ADDR[2..0] Channel address

ADR2	ADR1	ADR0	Address
0	0	0	Channel 0
0	0	1	Channel 1
0	1	0	Channel 2
0	1	1	Channel 3
1	0	0	Channel 4
1	0	1	Channel 5

RT[1..0] Retry select

RT1	RT0	Fault
0	X	Lockout until reset
1	0	Short retry timer. Nominally 10ms
1	1	Long retry timer. Nominally 55ms

NPD Disable diagnostic pull-down

NPD	Action
0	Enable diagnostic pull-down
1	Disable diagnostic pull-down

TOF[1..0] Turn-off blank time select.

TOF1	TOF0	Turn-off blank time (nominal)
0	0	80µs
0	1	140µs
1	0	280µs
1	1	4ms

TON[1..0] Turn-on blank time select.

TON1	TON0	Turn-on blank time (nominal)
0	0	5µs
0	1	14µs
1	0	28µs
1	1	56µs

SB[2..0] Short to battery threshold select

SB2	SB1	SB0	Threshold (nominal)
0	0	0	6% V_{REG}
0	0	1	8% V_{REG}
0	1	0	10% V_{REG}
0	1	1	12% V_{REG}
1	0	0	14% V_{REG}
1	0	1	16% V_{REG}
1	1	0	18% V_{REG}
1	1	1	31% V_{REG}

SG Short to ground threshold select.

SG	Threshold (nominal)
0	45% V_{REG}
1	66% V_{REG}

For tolerances on selected parameters refer to the Electrical Characteristics Table.

Applications Information

Drain Feedback Clamp Resistor Selection

The drain feedback input, DRNx, for each channel is clamped internally with a 50 V (nominal) Zener diode. If the voltage applied to this terminal is likely to exceed 50 V then an external current limit resistor will be required to limit the current, power, and energy to less than the Absolute Maximum specifications in this document.

Note that the internal drain clamp in the A3944 is not intended to dissipate the energy from any external load. The internal clamp is provided to protect the internal circuits of the A3944 from any high voltage that would otherwise cause permanent damage.

If the voltage at DRNx, V_{DRNx}, will never exceed the minimum drain clamp voltage, V_{DCL}, then no external resistor is required and DRNx can be connected directly to the drain of the external MOSFET switch.

Three Absolute Maximum specifications apply to the A3944, none of which may be exceeded:

- The maximum clamp current, I_{DRNC}, applies to very short pulses, typically less than 1.85 µs. Any current pulse less than 1.85 µs and less than I_{DRNC}, will never exceed the maximum power or energy limits.
- The maximum clamp energy, E_{DRNC}, applies to pulses between 1.85 µs and 2 ms. Above 2 ms the heat produced by the clamp energy dissipates through the silicon and the package; in that case, the maximum clamp power applies. Note that for pulse lengths between about 500 µs and 2 ms the energy starts to dissipate during the pulse, so the maximum current that is possible will actually be higher than that calculated using the maximum energy limit.
- The maximum clamp power, P_{DRNC}, applies to pulses lasting longer than 2 ms up to continuous operation.

Maximum current example:

- Load resistance: 26 Ω
- Load inductance: 130 µH
- Load current: 0.5 A
- Load supply voltage: 13 V
- FET clamp voltage: 80 V

These values would typically apply to a remote load which is primarily resistive. The load inductance will be due to a combination of the wiring and any parasitic inductance in the load. In this example, the DC on-state current will be 13 V / 26 Ω = 0.5 A.

When the load is switched off, the inductance attempts to keep the current flowing by increasing the voltage at the end connect to the FET switch. This voltage increases up to the breakdown voltage of the FET. At that point, the voltage across the load amounts to the difference between the FET breakdown voltage and the supply voltage, and it acts to reduce the current. With the parameters in this example, the current would decay to zero in less than 1 µs. This is less than the 1.85 µs limit for maximum current, so the drain resistor will be based only on the maximum current. The value of the drain resistor, R_{Dx}, in this case is simply the voltage across the resistor divided by the maximum current:

$$R_{Dx} = \frac{V_{FET} - V_{DCL}}{I_{DRNC}} \quad (1)$$

where

V_{FET} is the FET breakdown voltage,

V_{DCL} is the A3944 drain clamp voltage, and

I_{DRNC} is the A3944 drain clamp max current.

Substituting into equation 1:

$$R_{Dx} = \frac{80\text{ V} - 54\text{ V}}{100\text{ mA}} = 260\ \Omega$$

The energy injected into the A3944 drain clamp is:

$$E_{DRNC} = V_{DCL} \times I_{DRNC} \times t_{PULSE} \quad (2)$$

where t_{PULSE} is the duration of the current pulse.

Substituting into equation 2:

$$E_{DRNC} = 54\text{ V} \times 100\text{ mA} \times 0.9\ \mu\text{s} = 4.86\ \mu\text{J (per pulse)}$$

As expected, based on the pulse length, this is less than half the clamp energy limit, given in the Absolute Maximum table.

The maximum repetition rate of this pulse is derived from the maximum average clamp power dissipation limit. The minimum time between pulses, t_{REP} , is:

$$t_{REP} = \frac{E_{DRNC}}{P_{DRNC}} \quad (3)$$

where P_{DRNC} is the A3944 drain clamp maximum power.

Substituting into equation 3:

$$t_{REP} = \frac{4.86\ \mu J}{100\ mW} = 48.6\ \mu s$$

resulting in a repetition rate of just over 20 kHz.

Maximum energy example:

- Load resistance: 18 Ω
- Load inductance: 1 mH
- Load current: 0.72 A
- Load supply voltage: 13 V
- FET clamp voltage: 80 V

These values would typically apply to a small inductive load such as a solenoid or relay. When the load is switched off, the inductance attempts to keep the current flowing by increasing the voltage at the end connected to the FET switch. This voltage increases up to the breakdown voltage of the FET. At that point, the voltage across the load amounts to the difference between the FET breakdown voltage and the supply voltage, and it acts to reduce the current. With the parameters in this example, the current would decay to zero in about 10 µs. This is greater than the 1.85 µs pulse time defining the maximum current but less than the 2 ms time constant for maximum average clamp power, so the drain resistor will be selected to limit the energy injected into the drain clamp in the A3944. The maximum current, the A3944 drain clamp maximum current, I_{DRNC} , will be:

$$I_{DRNC} = \frac{E_{DRNC}}{V_{DCL} \times t_{PULSE}} \quad (4)$$

where

E_{DRNC} is the A3944 drain clamp maximum energy,
V_{DCL} is the A3944 drain clamp voltage, and
t_{PULSE} is the duration of the current pulse.

Substituting into equation 4:

$$I_{DRNC} = \frac{10\ \mu J}{54\ V \times 10\ \mu s} = 18.5\ mA$$

As given in equation 1, the value of the drain resistor is the voltage across the resistor divided by the maximum current:

$$R_{Dx} = \frac{V_{FET} - V_{DCL}}{I_{DRNC}}$$

$$R_{Dx} = \frac{80\ V - 54\ V}{18.5\ mA} = 1.4\ k\Omega$$

As given in equation 3, the maximum repetition rate of this pulse is derived from the maximum average clamp power dissipation limit as:

$$t_{REP} = \frac{E_{DRNC}}{P_{DRNC}}$$

$$t_{REP} = \frac{10\ \mu J}{100\ mW} = 100\ \mu s$$

:

resulting in a repetition rate of 10 kHz.

Maximum power example:

- Load resistance: 5 Ω
- Load inductance: 80 mH
- Load current: 2.6 A
- Load supply voltage: 13 V
- FET clamp voltage: 60 V

These values would typically apply to a large inductive load such as a coil or actuator. When the load is switched off, the inductance attempts to keep the current flowing by increasing the voltage at the end connected to the FET switch. This voltage increases up to the breakdown voltage of the FET. At that point, the voltage across the load amounts to the difference between the FET breakdown voltage and the supply voltage, and it acts to reduce the current. With the parameters in this example, the current would decay to zero in about 4 ms. This is greater than the 2 ms time constant for maximum average clamp power, so the drain resistor will be selected to limit the power dissipated by

the drain clamp in the A3944. The maximum current, the A3944 drain clamp maximum current, I_{DRNC} , will be:

$$I_{DRNC} = \frac{P_{DRNC}}{V_{DCL}} \quad (5)$$

where

P_{DRNC} is the A3944 drain clamp maximum power and

V_{DCL} is the A3944 drain clamp voltage.

Substituting into equation 5:

$$I_{DRNC} = \frac{100\ \text{mW}}{54\ \text{V}} = 1.8\ \text{mA}$$

As given in equation 1, the value of the drain resistor is the voltage across the resistor divided by the maximum current:

$$R_{Dx} = \frac{V_{FET} - V_{DCL}}{I_{DRNC}}$$

$$R_{Dx} = \frac{60\ \text{V} - 54\ \text{V}}{1.8\ \text{mA}} = 3.3\ \text{k}\Omega$$

The maximum repetition rate is irrelevant in this case because the A3944 will sustain the maximum clamp dissipation indefinitely.

Practical Open Load Limits

An open load is detected, when the external FET is off, if the voltage at the DRNx terminal is less than the open load threshold, V_{OL}, but greater than the short to ground threshold, V_{STG} . The voltage at the DRNx terminal in the off-state is defined as (referring to figure 13):

$$V_{DRNx} = V_L - I_{DPD}(R_L + R_D) \quad (6)$$

where

V_{DRNx} is the voltage at the DRNx terminal,

V_L is the load supply voltage,

I_{DPD} is the diagnostic pull-down current,

R_L is the load resistance, and

R_D is the DRNx current limit resistor.

Note that this equation is only valid for normal load and open load conditions when:

$$V_{DRNx} > V_{OCL}$$

where V_{OCL} is the open load clamp voltage.

Ideally an open load would mean an infinite or at least a very large (>1 MΩ) resistance. In practice this is not necessarily the case, and the limit of open-load resistance values for correct detection will be determined by: the threshold voltages, the diagnostic currents, and the load voltage.

An open load is detected when:

$$V_{DRNx} < V_{OL}$$

where V_{OL} is the open load detect voltage, then:

$$\Rightarrow V_{OL} > V_{DRNx},$$

$$\Rightarrow V_{OL} > V_L - I_{DPD}(R_L + R_D), \quad \text{(from 6)}$$

$$\therefore \quad R_L > [(V_L - V_{OL}) / I_{DPD}] + R_D . \quad (7)$$

There are two open-load resistance values to consider. The first is the minimum resistance at which an open load detection is always guaranteed. The second is the maximum resistance that a load can present without ever causing an open load to be detected. Both cases, described below, assume that the load is connected to the load supply and that the load supply is higher than the open load clamp voltage, V_{OCL}.

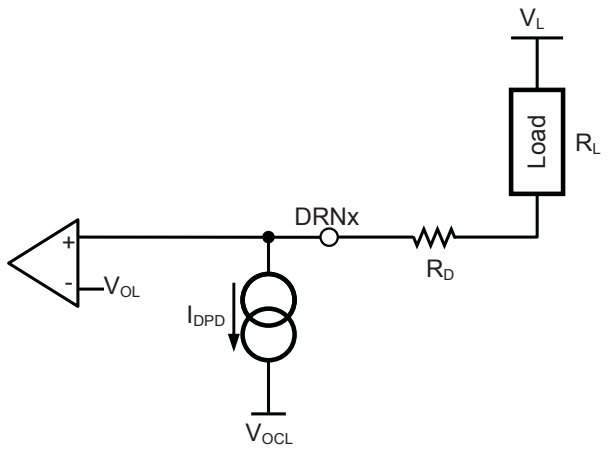


Figure 13. Open load detection condition

Minimum guaranteed open load resistance

The minimum value of R_L that will always be detected as an open is given by the maximum value of R_L that could be detected as a load, R_{Lmax}. This is defined by:

$$R_{Lmax} = \frac{V_{Lmax} - V_{OLmax}}{I_{DPDmin}} - R_{Dmin} \quad (8)$$

For an 18 V supply this gives a minimum guaranteed open load resistance value of 79 kΩ. This means that under all conditions, with a load voltage of up to 18 V, a load resistance greater than 79 kΩ will always be detected as an open load. For a 36 V supply the minimum guaranteed open load resistance value increases to 379 kΩ.

Maximum load resistance

The maximum value of R_L that will always be detected as a load is given by the minimum value of R_L that could be detected as a open, R_{Lmin}. This is defined by:

$$R_{Lmax} = \frac{V_{Lmax} - V_{OLmax}}{I_{DPDmin}} - R_{Dmin} \quad (9)$$

For a 6 V supply this gives a maximum value of 19 kΩ for the sum of the open load resistance and the DRNx current limit resistor. This means, for example, that under all conditions, with a DRNx current limit resistor of up to 7 kΩ, a load resistance less than 12 kΩ will never cause an open load detection.

The two limiting values are shown in figure 14 for load voltages from 6 to 36 V. Note that the load resistance value includes the DRNx current limit resistor. In this figure, a load resistance greater than the upper line is guaranteed to be detected as an open load and a load resistance less than the lower line is guaranteed not to be detected as an open load.

Practical Short to Ground Limits

A short to ground is detected, when the external FET is off, if the voltage at the DRNx terminal is less than the short to ground threshold, V_{STG}. Under ideal conditions a short circuit would be zero resistance and the short would be to ground at zero volts. However in practical systems the short will have a finite resistance and the power ground voltage may be higher than the reference ground of the detection circuit. The equivalent circuit during a short to ground is shown in figure 15.

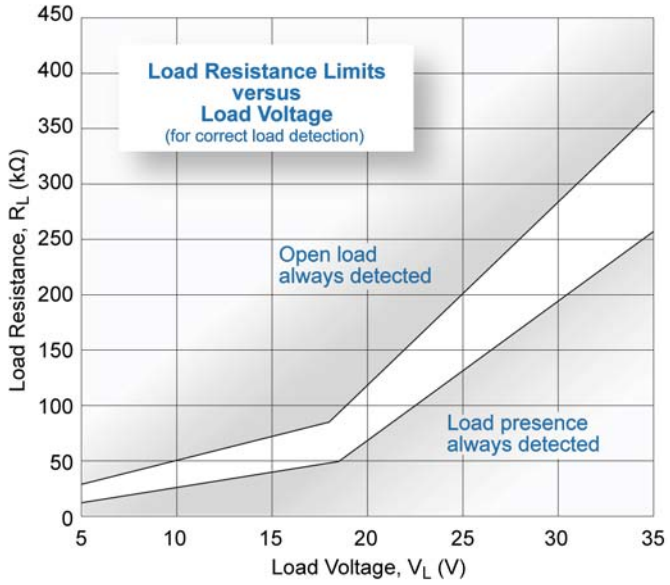


Figure 14. Open load detection limits

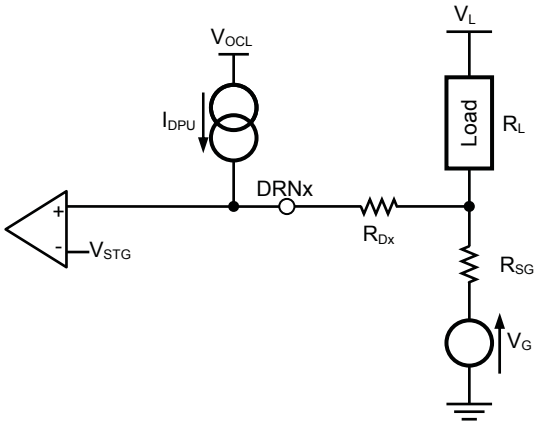


Figure 15. Short to ground detection condition

The voltage at the DRNx terminal, V_{DRNx}, in the off-state when a short to ground is present is defined as:

$$V_{DRNx} = \frac{(V_L - V_G)\,R_{SG}}{R_L + R_{SG}} + V_G + I_{DPU}R_D \qquad (10)$$

where

V_L is the load supply voltage,

V_G is the ground (offset) voltage,

R_{SG} is the resistance of the short to ground (offset),

R_L is the load resistance,

I_{DPU} is the diagnostic pull-up current, and

R_D is the DRNx current limit resistor.

Note that this equation is only valid for short to ground conditions when:

$$V_{DRNx} < V_{OCL}$$

where V_{OCL} is the open load clamp voltage.

A short to ground is detected when:

$$V_D < V_{STG}$$

where V_{STG} is the short to ground detect voltage, then:

$$\Rightarrow \frac{(V_L - V_G)\,R_{SG}}{R_L + R_{SG}} + V_G + I_{DPU}R_D < V_{STG}$$

Note that R_D must be less than:

$$\frac{(V_{STG} - V_G)}{I_{DPU}}$$

$$\Rightarrow \frac{(V_L - V_G)\,R_{SG}}{R_L + R_{SG}} < V_{STG} - V_G - I_{DPU}R_D$$

$$\therefore \quad R_L > \left(\frac{V_L - V_G}{V_{STG} - V_G - I_{DPU}R_D} - 1\right) R_{SG} \qquad (11)$$

Minimum load resistance

The minimum value of R_L that will always allow a short to be detected is given by the maximum value of R_L that satisfies the short detection criterion, R_{Lmax}., defined by:

$$R_{Lmax} = \left(\frac{V_L - V_{Gmax}}{V_{STGmin} - V_{Gmax} - I_{DPUmax}R_{Dmax}} - 1\right) R_{SGmax} \qquad (12)$$

Assuming worst case conditions of a maximum ground voltage offset of +1 V and a maximum short resistance of 0.5 Ω allows the minimum load resistance to be calculated for different load voltages. This will be maximum at either V_{Lmax} or V_{Lmin} depending on the relative values of R_{Dmax} and V_L.

For example, at a load voltage of 6 V and R_D set to 5 kΩ, a short will be detected with a load resistance greater than 0.75 Ω when SG = 0, or at 2.63 Ω when SG = 1. At a load voltage of 18 V the same conditions give 0.9 Ω for SG = 0 and 0.34 Ω for SG = 1.

The limiting values for SG = 0 and SG = 1 are shown in figure 16 for load voltage from 6 to 36 V and with a DRNx current limit resistor (R_{Dmax}) of 7 kΩ. In this figure, a load resistance above the line is guaranteed to allow detection of a 0.5 Ω short to a +1 V offset ground. An increase in R_D raises the line.

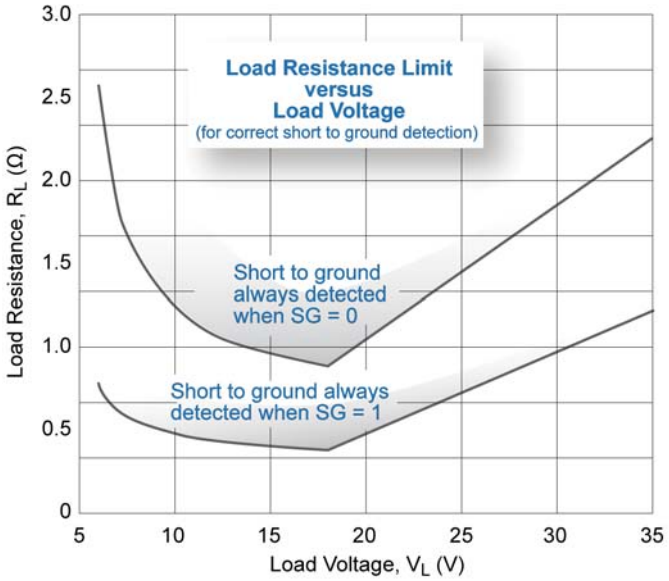


Figure 16. Short to ground detection limits

Practical Short to Battery Limits

A short to battery is detected, when the external FET is on, if the voltage at the DRNx terminal is greater than the short to battery threshold, V_{STB}. Under ideal conditions a short circuit would be zero resistance. However in practical systems the short will have a finite resistance. The equivalent circuit during a short to battery is shown in figure 17.

The voltage at the DRNx terminal in the on-state when a short to battery is present is defined as:

$$V_{DRNx} = \frac{V_L R_{ON}}{\frac{R_L R_{SB}}{R_L + R_{SB}} + R_{ON}} \quad (13)$$

where

V_{DRNx} is the voltage at the DRNx terminal,

V_L is the load supply voltage,

R_{ON} is the FET switch on-resistance,

R_L is the load resistance, and

R_{SB} is the resistance of the short across the load.

A short to ground is detected when:

$$V_{DRNx} > V_{STB}$$

where V_{STB} is the short to ground detect voltage, then:a

$$\Rightarrow \frac{V_L R_{ON}}{\frac{R_L R_{SB}}{R_L + R_{SB}} + R_{ON}} > V_{STB} \quad (14)$$

For short to battery diagnostics there are two limiting resistance values to consider. The first is the maximum value of R_{SB} that will always cause a short to be detected. The second is the minimum value of R_L that will not cause a short to battery detection under normal operating conditions.

Maximum short resistance

The maximum value of the short resistance, R_{SB}, that will always cause a short to be detected is given by the minimum value of R_{SB} that satisfies the short detection criterion defined by:

$$R_{SB} < \frac{(V_L - V_{STB}) R_{ON} R_L}{V_{STB}(R_L + R_{ON}) - V_L R_{ON}} \quad (15)$$

This will be at a minimum when

$$\frac{(V_L - V_{STB})}{V_{STB} R_L - (V_L - V_{STB}) R_{ON}}$$

is at its minimum. This occurs when $V_L - V_{STB}$ is at its minimum and V_{STB} is at its maximum. This is the condition that is present when V_L is just high enough to provide the minimum drop-out voltage above the maximum value of V_{REG}, (that is, when $V_L = V_{REGmax} + V_{DOmin}$) and V_{STB} is at the maximum tolerance value.

Placing these limits into the expression for R_{SB} gives the expression for the minimum short resistance, defined by:

$$R_{SBmax(min)} = \frac{(V_{REGmax} + V_{DOmin} + V_{STBmax}) R_{ON} R_L}{V_{STBmax}(R_L + R_{ON}) - (V_{REGmax} + V_{DOmin}) R_{ON}} \quad (16)$$

The maximum short resistance at any load voltage is given by:

$$R_{SBmax} = \frac{(V_L - V_{STBmax}) R_{ON} R_L}{V_{STBmax}(R_L + R_{ON}) - V_L R_{ON}} \quad (17)$$

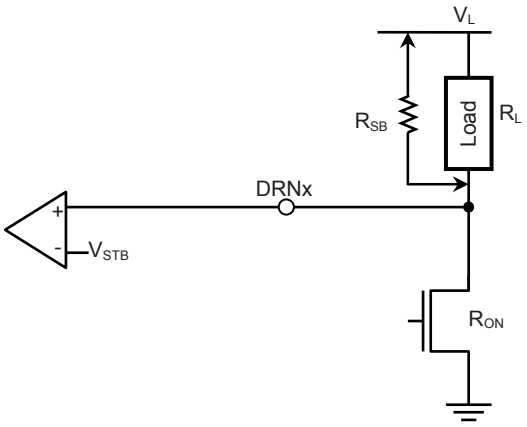


Figure 17. Short to battery detection condition

The variation of R_{SBmax} with load voltage is shown as the lower line (Maximum Short Resistance) in figure 18. This example shows the maximum possible resistance of a short to battery that will always be detected as a short with a 2.8 Ω load and a 100 mΩ MOSFET using short to battery threshold level 5.

As R_L increases, R_{SB} becomes the dominant resistance and:

$$V_D = \frac{V_L R_{ON}}{\frac{R_L R_{SB}}{R_L + R_{SB}} + R_{ON}}$$

$$V_D = \frac{V_L R_{ON}}{R_{SB} + R_{ON}} \quad (18)$$

The expression for R_{SB} (from equation 15) becomes:

$$R_{SB} < \frac{(V_L - V_{STB})R_{ON}}{V_{STB}} \quad (19)$$

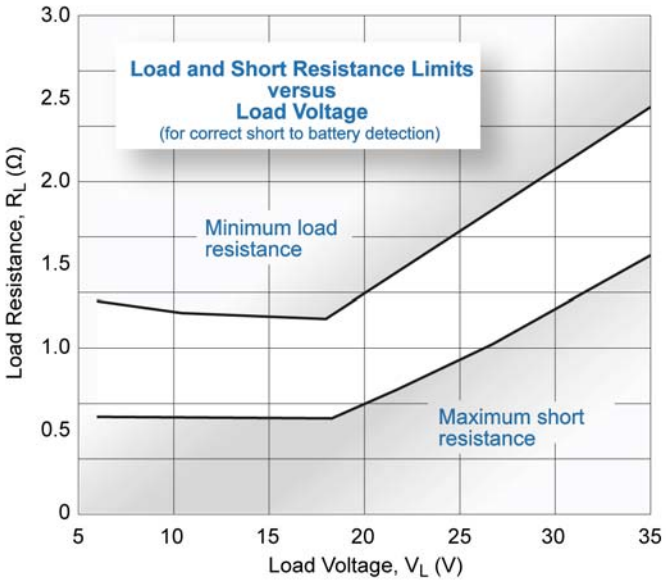


Figure 18. Short to battery detection limits

This allows a lower threshold to be used for V_{STB}, resulting in a faster short to battery detection and a lower short circuit current.

Minimum load resistance

For normal operation:

$$V_{DRNx} = \frac{V_L R_{ON}}{R_L + R_{ON}} \quad (20)$$

and:

$$V_{DRNx} < V_{STB}$$

Rearranging gives:

$$R_L > \frac{(V_L - V_{STB})R_{ON}}{V_{STB}} \quad (21)$$

The minimum value of the load resistance, R_L, that will not cause a short to battery detection under normal operating conditions is given by:

$$R_{Lmin} = \frac{(V_{Lmax} - V_{STBmin})R_{ONmax}}{V_{STBmin}} \quad (22)$$

The variation of R_{Lmin} with load voltage is shown as the upper line (Minimum Load Resistance) in figure 18. This example shows the minimum possible load resistance that will always allow a short to battery to be detected with a 0.5 Ω short and a 100 mΩ MOSFET using short to battery threshold level 5.

Power Dissipation Estimation

The A3944 supply currents have very little dependency on the state of the internal circuits. In addition, the internal operation is essentially low speed so the power dissipation has almost no dependency on operating frequency other than dissipation due to channel switching and diagnostics that are proportional to PWM frequency. It is therefore possible to estimate the maximum power dissipated within the A3944 by summing the contribution from the three quiescent supply currents with the dissipation due to channel switching and diagnostics associated with turning each external MOSFET on and off.

Quiescent Dissipation

The quiescent dissipation for each supply is the simply product of the supply current and the supply voltage:

$$P_{DD} = V_{DD} \times I_{DDQ}$$

$$P_{BB} = V_{BB} \times I_{BBQ}$$

$$P_{BR} = V_{DR} \times I_{DRQ}$$

From the Electrical Characteristics table specification this gives the total maximum quiescent dissipation of 131 mW when V_{DD} and V_{DR} are 5 V and V_{BB} is 24 V. At 12 V this drops to 83 mW.

Channel Switching Dissipation

The dissipation produced by switching each channel on or off is calculated by summing the energy passing through the gate drive output to and from the gate of the external MOSFET over time. The energy transferred to the gate is given by:

$$E_{SW} = \frac{Q_g V_G}{2} \quad (23)$$

where

Q_g is the total MOSFET gate charge and

V_G is the MOSFET gate voltage when on.

This is the energy transferred through the gate drive each time a MOSFET is switched on or off. The total power due to this energy transfer is calculated by multiplying the energy by the number of switching events per second. The number of switching events per second is twice the PWM frequency, so the dissipation due to switching losses becomes:

$$P_{SW} = Q_g V_G f_{PWM} \quad (24)$$

where f_{PWM} is the PWM frequency for the channel.

If there is no gate resistor then this is the total dissipation that will occur inside the A3944. If a gate resistor is used then the dissipation will be shared proportionally by the gate resistor and by the on-resistance of the A3944 gate drive. This gives the equation for internal dissipation as:

$$P_{SW} = Q_g V_G f_{PWM} \frac{R_{ON}}{R_{ON} + R_G} \quad (25)$$

where

R_{ON} is the on-resistance of the gate drive and

R_G is the gate resistor value.

As an example, the maximum likely switching losses can be estimated by using a reasonably large MOSFET total charge of 100 nC and a PWM frequency of 10 kHz. With no gate resistor the dissipation in the A3944 due to switching losses for a single channel will be approximately 5 mW.

Channel Diagnostic Dissipation

Each channel has three current generators that are used to determine the state of the load during the off-state for the channel. Under normal load conditions the power dissipated is limited to the product of the pull-down current source and the difference between the load supply and the open load clamp voltage. For example, with a 24 V load supply, this would contribute a maximum of 80 µA × 9.2 V = 0.8 mW. At 12 V this drops to 0.2 mW.

However, the worst case dissipation will occur when the load is not connected and a capacitor is attached to the diagnostic feedback terminal for the channel, DRNx. As for the switching losses, the dissipation can be calculated by summing the energy transferred to the capacitor over time. In this case the energy transferred is:

$$E_D = \frac{C_D V^2_{OCL}}{2} \quad (26)$$

where

C_D is the value of the DRNx capacitor and

V_{OCL} is the offset clamp voltage.

This is the energy transferred through the current source each time a MOSFET is switched off. The total power due to this energy transfer is calculated by multiplying this energy by the number of switching events per second. The number of switching events per second is the PWM frequency, so the dissipation due to switching losses becomes:

$$P_D = \frac{C_D V^2_{OCL} f_{PWM}}{2} \quad (27)$$

where f_{PWM} is the PWM frequency for the channel.

As an example, a 10 nF capacitor and a PWM frequency of 10 kHz will produce a dissipation in the A3944 for a single channel of approximately 4.3 mW. This is the worst case dissipation. It will not be present if a load is attached and will be reduced by any DRNx current limit resistor.

Total Dissipation Example

The total dissipation is the sum of the quiescent dissipation and the dissipation due to switching and diagnostic currents in each of the six channels:

$$P_{max} = P_{DD} + P_{BB} + P_{DR} + 6\,(P_{SW} + P_{diag}) \qquad (28)$$

The worst case maximum dissipation occurs at maximum supply voltage and all loads open circuit. Assuming: a channel PWM frequency of 10 kHz on each channel, a 10 nF capacitor attached to each DRNx terminal, 10 nC MOSFETs, no DRNx resistors, and no gate resistors, then the maximum dissipation will be 275 mW. This is a conservative maximum dissipation showing that the A3944 can easily be used in high ambient temperatures without requiring derating.

This worst case dissipation will drop to 227 mW with a 24 V supply and to 139 mW with a 12 V supply.

The maximum typical dissipation, with all loads connected and the same conditions, will be 219 mW at 36 V, 165 mW at 24 V ,and 114 mW at 12 V (see figure 19).

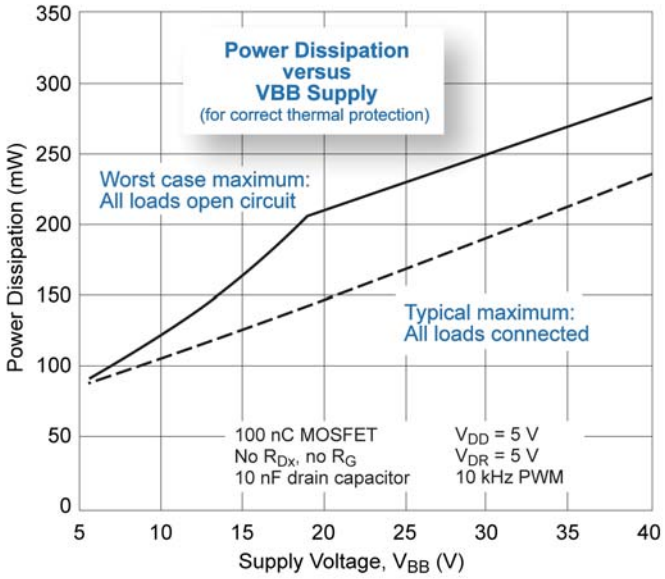
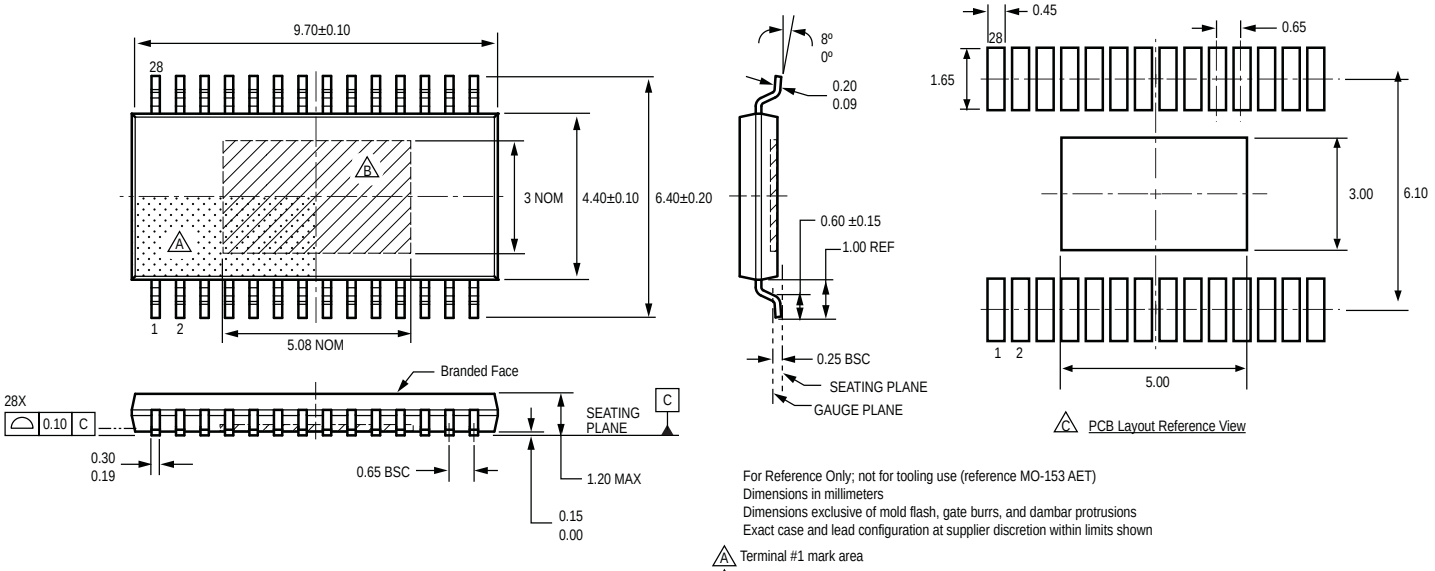


Figure 19. Power dissipation all loads connected

Package LP, 28-Pin TSSOP with Exposed Thermal Pad



For Reference Only; not for tooling use (reference MO-153 AET)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Revision History

Revision	Revision Date	Description of Revision
Rev. 1	May 18, 2012	Update $R_{DS(on)}$, I_{BBQ}, and I_{GL}

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