



**THE DATASHEET OF
ADG704BRMZ-REEL7**



FEATURES

+1.8 V to +5.5 V Single Supply
2.5 Ω (Typ) On Resistance
Low On-Resistance Flatness
-3 dB Bandwidth >200 MHz
Rail-to-Rail Operation
10-Lead μ SOIC Package
Fast Switching Times
 t_{ON} 20 ns
 t_{OFF} 13 ns
Typical Power Consumption (<0.01 μ W)
TTL/CMOS Compatible

APPLICATIONS

Battery Powered Systems
Communication Systems
Sample-and-Hold Systems
Audio Signal Routing
Data Acquisition System
Video Switching

GENERAL DESCRIPTION

The ADG704 is a CMOS analog multiplexer, comprising four single channels. This multiplexer is designed on an advanced submicron process that provides low power dissipation yet gives high switching speed, low on resistance, low leakage currents and high bandwidths.

The on resistance profile is very flat over the full analog signal range. This ensures excellent linearity and low distortion when switching audio signals. Fast switching speed also makes the part suitable for video signal switching.

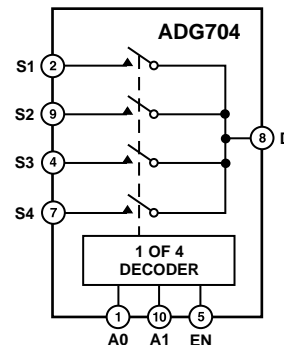
The ADG704 can operate from a single supply range of +1.8 V to +5.5 V, making it ideal for use in battery powered instruments and with the new generation of DACs and ADCs from Analog Devices.

The ADG704 switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1 and EN. A Logic "0" on the EN pin disables the device.

Each switch of the ADG704 conducts equally well in both directions when ON. The ADG704 exhibits break-before-make switching action.

The ADG704 is available in 10-lead μ SOIC package.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

- +1.8 V to +5.5 V Single Supply Operation.
The ADG704 offers high performance and is fully specified and guaranteed with +3 V and +5 V supply rails.
- Very Low R_{ON} (4.5 Ω Max at 5 V, 8 Ω Max at 3 V).
At supply voltage of +1.8 V, R_{ON} is typically 35 Ω over the temperature range.
- Low On-Resistance Flatness.
- 3 dB Bandwidth Greater than 200 MHz.
- Low Power Dissipation.
CMOS construction ensures low power dissipation.
- Fast t_{ON}/t_{OFF} .
- Break-Before-Make Switching Action.
- 10-Lead μ SOIC Package.

REV. A

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ADG704—SPECIFICATIONS¹ ($V_{DD} = +5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All Specifications -40°C to $+85^{\circ}\text{C}$, unless otherwise noted.)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	2.5		Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = -10\text{ mA}$; Test Circuit 1
	4	4.5	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})		0.1	Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = -10\text{ mA}$
		0.4	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.75		Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = -10\text{ mA}$
		1.2	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.01		nA typ	$V_{DD} = +5.5\text{ V}$ $V_S = 4.5\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/4.5\text{ V}$; Test Circuit 2
	± 0.1	± 0.3	nA max	
Drain OFF Leakage I_D (OFF)	± 0.01		nA typ	$V_S = 4.5\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/4.5\text{ V}$; Test Circuit 2
	± 0.1	± 0.3	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.01		nA typ	$V_S = V_D = 4.5\text{ V}$ or 1 V ; Test Circuit 3
	± 0.1	± 0.3	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
DYNAMIC CHARACTERISTICS²				
t_{ON}	14		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 4
		20	ns max	
t_{OFF}	6		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 4
		13	ns max	
Break-Before-Make Time Delay, t_D	8		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 3\text{ V}$, Test Circuit 5
		1	ns min	
Charge Injection	3		pC typ	$V_S = 2\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test Circuit 6
Off Isolation	-60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$
	-80		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 7
Channel-to-Channel Crosstalk	-62		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$
	-82		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 8
Bandwidth -3 dB	200		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Test Circuit 9
C_S (OFF)	9		pF typ	
C_D (OFF)	37		pF typ	
C_D , C_S (ON)	54		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.001		μA typ	$V_{DD} = +5.5\text{ V}$ Digital Inputs = 0 V or 5 V
		1.0	μA max	

NOTES

¹Temperature ranges are as follows: B Version: -40°C to $+85^{\circ}\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS¹ ($V_{DD} = +3\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All Specifications -40°C to $+85^\circ\text{C}$, unless otherwise noted.)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	4.5	5 8	Ω typ Ω max	$V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = -10\text{ mA}$; Test Circuit 1
On-Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ Ω max	$V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = -10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)		0.4 2.5	Ω max Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = -10\text{ mA}$
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.01		nA typ nA max	$V_{DD} = +3.3\text{ V}$ $V_S = 3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3\text{ V}$; Test Circuit 2
Drain OFF Leakage I_D (OFF)	± 0.01	± 0.3	nA typ nA max	$V_S = 3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3\text{ V}$; Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.01	± 0.3	nA typ nA max	$V_S = V_D = 3\text{ V}$ or 1 V ; Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current I_{INL} or I_{INH}	0.005	± 0.1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
DYNAMIC CHARACTERISTICS²				
t_{ON}	16	24	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$, Test Circuit 4
t_{OFF}	8	16	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$, Test Circuit 4
Break-Before-Make Time Delay, t_D	9	1	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 2\text{ V}$, Test Circuit 5
Charge Injection	3		pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test Circuit 6
Off Isolation	-60 -80		dB typ dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 7
Channel-to-Channel Crosstalk	-62 -82		dB typ dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 8
Bandwidth -3 dB	200		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Test Circuit 9
C_S (OFF)	9		pF typ	
C_D (OFF)	37		pF typ	
C_D , C_S (ON)	54		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.001	1.0	μA typ μA max	$V_{DD} = +3.3\text{ V}$ Digital Inputs = 0 V or 3 V

NOTES

¹Temperature ranges are as follows: B Version: -40°C to $+85^\circ\text{C}$.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG704

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

V _{DD} to GND	-0.3 V to +6 V
Analog, Digital Inputs ²	-0.3 V to V _{DD} +0.3 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range		
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
μSOIC Package, Power Dissipation	315 mW
θ _{JA} Thermal Impedance	206°C/W
Lead Temperature, Soldering		
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C
ESD	2 kV

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

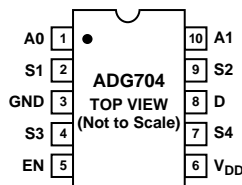
Model	Temperature Range	Brand ¹	Package Option ²
ADG704BRM	-40°C to +85°C	S9B	RM-10

NOTES

¹Brand = Due to small package size, these three characters represent the part number.

²RM = μSOIC.

PIN CONFIGURATION (10-Lead μSOIC)



TERMINOLOGY

V _{DD}	Most positive power supply potential.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
A0, A1	Logic control inputs.
EN	Logic control input.
R _{ON}	Ohmic resistance between D and S.
ΔR _{ON}	On resistance match between any two channels i.e., R _{ONmax} -R _{ONmin} .
R _{FLAT(ON)}	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I _D (OFF)	Drain leakage current with the switch "OFF."
I _S (OFF)	Source leakage current with the switch "OFF."
I _D , I _S (ON)	Channel leakage current with the switch "ON."
V _D (V _S)	Analog voltage on terminals D, S.
C _S (OFF)	"OFF" switch source capacitance.
C _D (OFF)	"OFF" switch drain capacitance.
C _D , C _S (ON)	"ON" switch capacitance.
t _{ON}	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
t _{OFF}	Delay between applying the digital control input and the output switching off.
t _D	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another. See Test Circuit 5.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Bandwidth	The frequency at which the output is attenuated by -3 dBs.
On Response	The frequency response of the "ON" switch.
On Loss	The voltage drop across the "ON" switch, seen on the On Response vs. Frequency plot as how many dBs the signal is away from 0 dB at very low frequencies.

Table I. Truth Table

A1	A0	EN	ON Switch
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG704 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Typical Performance Characteristics—ADG704

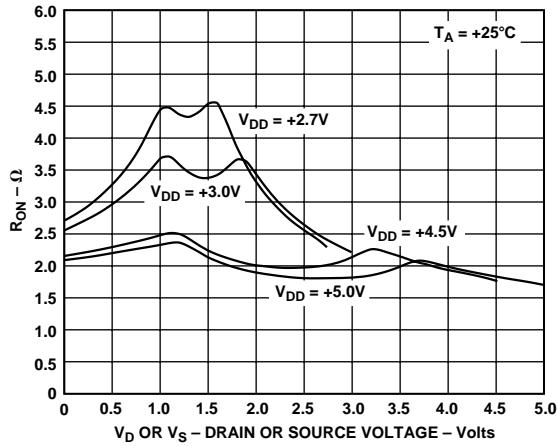


Figure 1. On Resistance as a Function of V_D (V_S) Single Supplies

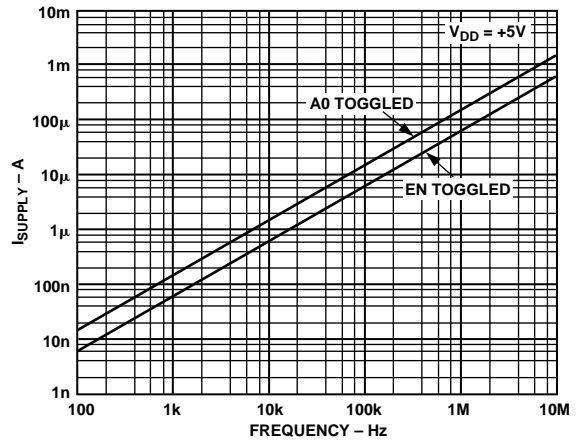


Figure 4. Supply Current vs. Input Switching Frequency

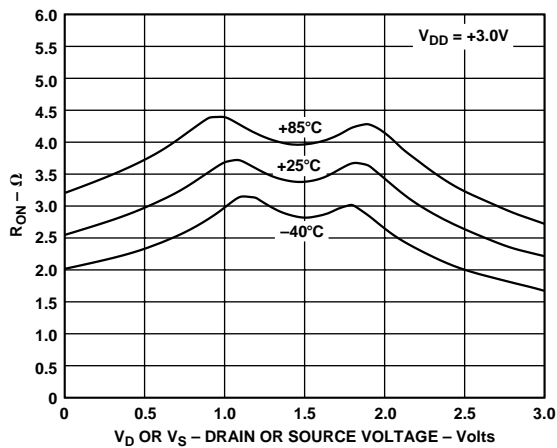


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures; $V_{DD} = 3\text{ V}$

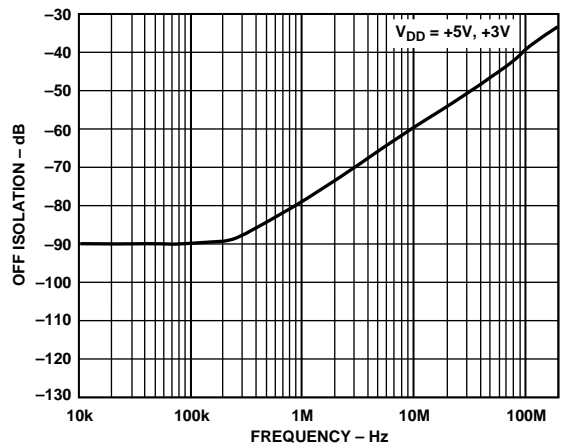


Figure 5. Off Isolation vs. Frequency

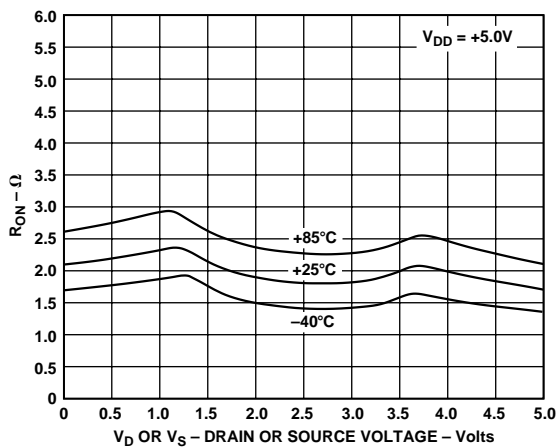


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures; $V_{DD} = 5\text{ V}$

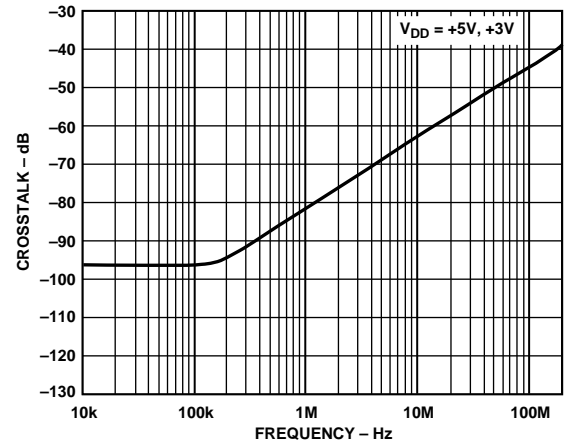


Figure 6. Crosstalk vs. Frequency

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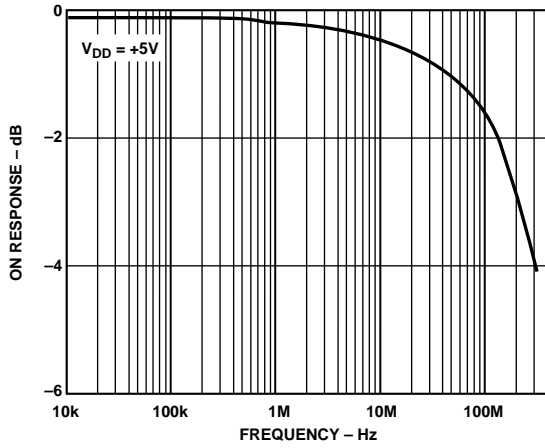


Figure 7. On Response vs. Frequency

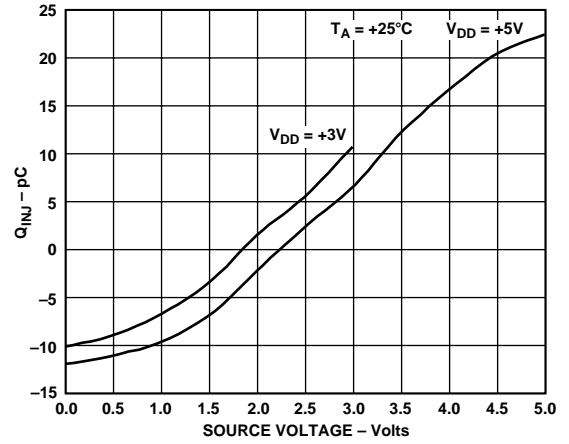


Figure 8. Charge Injection vs. Source Voltage

APPLICATIONS

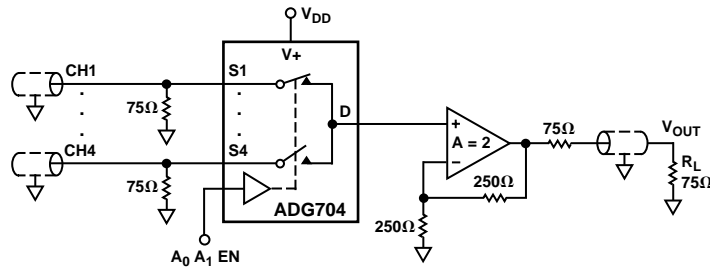
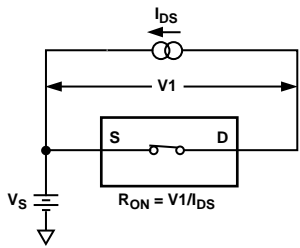
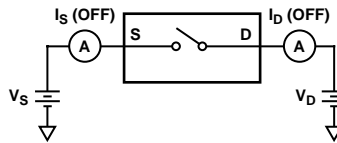


Figure 9. 4-Channel Video Multiplexing

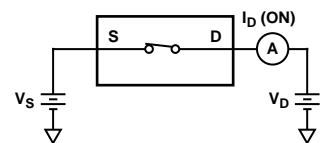
Test Circuits



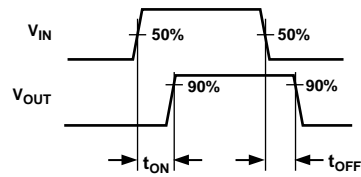
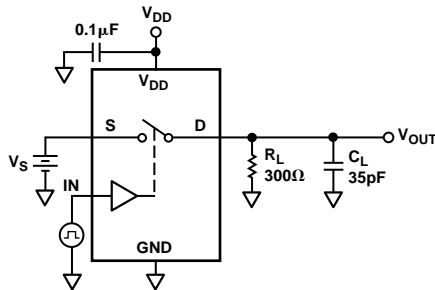
Test Circuit 1. On Resistance



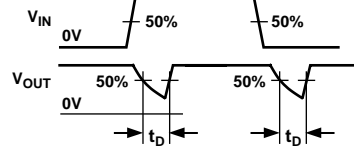
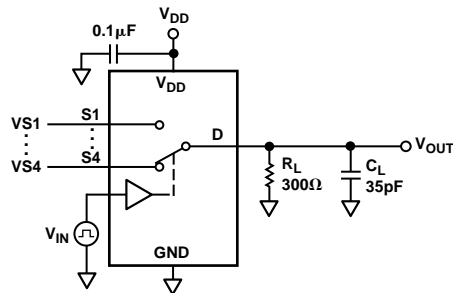
Test Circuit 2. Off Leakage



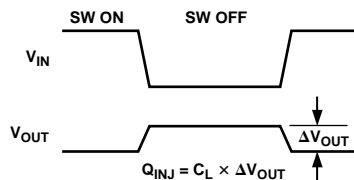
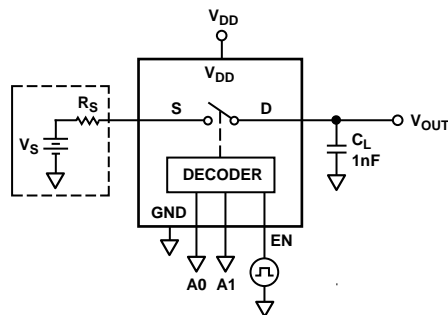
Test Circuit 3. On Leakage



Test Circuit 4. Switching Times

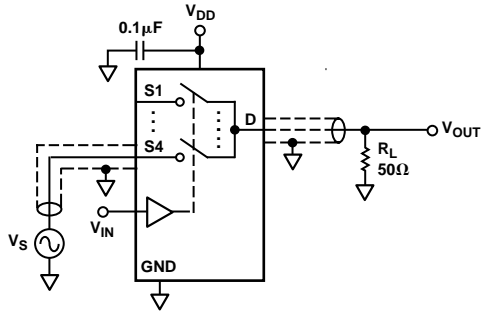


Test Circuit 5. Break-Before-Make Time Delay, t_D

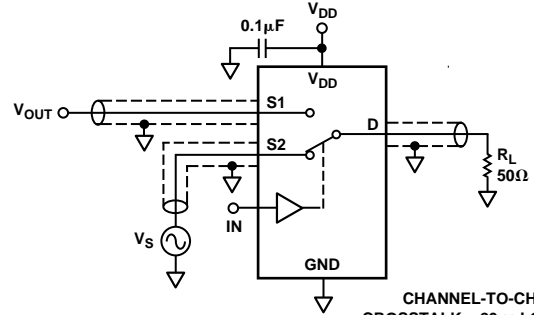


Test Circuit 6. Charge Injection

ADG704

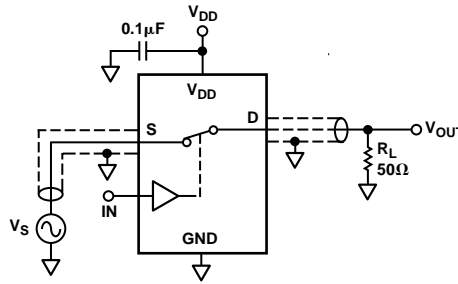


Test Circuit 7. Off Isolation



CHANNEL-TO-CHANNEL
CROSSTALK = $20 \times \text{LOG} |V_S/V_{OUT}|$

Test Circuit 8. Channel-to-Channel Crosstalk

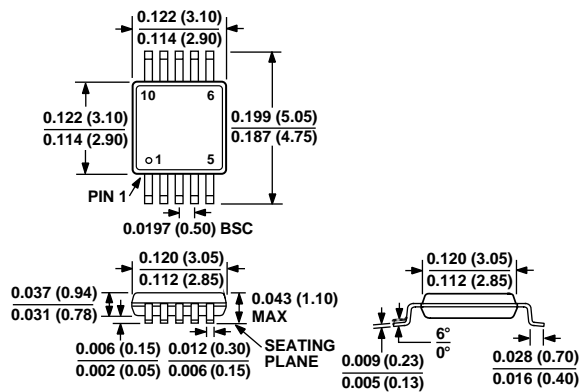


Test Circuit 9. Bandwidth

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

10-Lead μ SOIC (RM-10)



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