

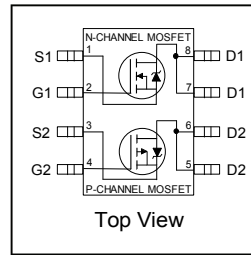


**THE DATASHEET OF
AUIRF7379Q**

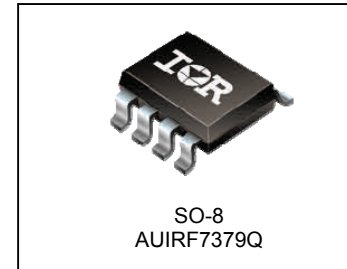


Features

- Advanced Planar Technology
- Low On-Resistance
- Logic Level Gate Drive
- Dual N and P Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- 150°C Operating Temperature
- Lead-Free, RoHS Compliant
- Automotive Qualified *



	N-CH	P-CH
V_{DSS}	30V	-30V
$R_{DS(on)}$ typ.	0.038Ω	0.070Ω
	max.	0.045Ω
I_D	5.8A	-4.3A



SO-8
AUIRF7379Q

G	D	S
Gate	Drain	Source

Description

Specifically designed for Automotive applications, these HEXFET® Power MOSFET's in a Dual SO-8 package utilize the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of these Automotive qualified HEXFET Power MOSFET's are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

The efficient SO-8 package provides enhanced thermal characteristics and dual MOSFET die capability making it ideal in a variety of power applications. This dual, surface mount SO-8 can dramatically reduce board space and is also available in Tape & Reel.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF7379Q	SO-8	Tape and Reel	4000	AUIRF7379QTR

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	30	-30	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	5.8	-4.3	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	4.6	-3.4	
I_{DM}	Pulsed Drain Current ①	46	-34	
$P_D @ T_A = 25^\circ C$	Maximum Power Dissipation	2.5		W
	Linear Derating Factor	0.02		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ④	—	50	°C/W

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*Qualification standards can be found at www.infineon.com

Static @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	N-Ch	30	—	—	V	V _{GS} = 0V, I _D = 250μA
		P-Ch	-30	—	—		V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.032	—	V/°C	Reference to 25°C, I _D = 1mA
		P-Ch	—	-0.037	—		Reference to 25°C, I _D = -1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	N-Ch	—	0.038	0.045	Ω	V _{GS} = 10V, I _D = 5.8A ③
			—	0.055	0.075		V _{GS} = 4.5V, I _D = 4.9A ③
		P-Ch	—	0.070	0.090		V _{GS} = -10V, I _D = -4.3A ③
			—	0.130	0.180		V _{GS} = -4.5V, I _D = -3.7A ③
V _{GS(th)}	Gate Threshold Voltage	N-Ch	1.0	—	3.0	V	V _{DS} = V _{GS} , I _D = 250μA
		P-Ch	-1.0	—	-3.0		V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Trans conductance	N-Ch	5.2	—	—	S	V _{DS} = 15V, I _D = 2.4A ③
		P-Ch	2.5	—	—		V _{DS} = -24V, I _D = -1.8A ③
I _{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V
		P-Ch	—	—	-1.0		V _{DS} = -24V, V _{GS} = 0V
		N-Ch	—	—	25		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
		P-Ch	—	—	-25		V _{DS} = -24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	± 100	nA	V _{GS} = ± 20V
	Gate-to-Source Reverse Leakage	N-P	—	—	± 100		V _{GS} = ± 20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Q _g	Total Gate Charge	N-Ch	—	—	25	nC	N-Channel I _D = 2.4A, V _{DS} = 24V, V _{GS} = 10V ③
		P-Ch	—	—	25		
Q _{gs}	Gate-to-Source Charge	N-Ch	—	—	2.9	nC	P-Channel I _D = -1.8A, V _{DS} = -24V, V _{GS} = -10V ③
		P-Ch	—	—	2.9		
Q _{gd}	Gate-to-Drain Charge	N-Ch	—	—	7.9	nC	P-Channel I _D = -1.8A, V _{DS} = -24V, V _{GS} = -10V ③
		P-Ch	—	—	9.0		
t _{d(on)}	Turn-On Delay Time	N-Ch	—	6.8	—	ns	N-Channel V _{DD} = 15V, I _D = 2.4A, R _G = 6.0Ω, R _D = 6.2Ω ③
		P-Ch	—	11	—		
t _r	Rise Time	N-Ch	—	21	—	ns	P-Channel V _{DD} = -15V, I _D = -1.8A, R _G = 6.0Ω, R _D = 8.2Ω ③
		P-Ch	—	17	—		
t _{d(off)}	Turn-Off Delay Time	N-Ch	—	22	—	ns	P-Channel V _{DD} = -15V, I _D = -1.8A, R _G = 6.0Ω, R _D = 8.2Ω ③
		P-Ch	—	25	—		
t _f	Fall Time	N-Ch	—	7.7	—	ns	P-Channel V _{DD} = -15V, I _D = -1.8A, R _G = 6.0Ω, R _D = 8.2Ω ③
		P-Ch	—	18	—		
L _D	Internal Drain Inductance	N-P	—	4.0	—	nH	Between lead, 6mm (0.25in.) from Package and center of die contact
L _S	Internal Source Inductance	N-P	—	6.0	—		
C _{iss}	Input Capacitance	N-Ch	—	520	—	pF	N-Channel V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz
		P-Ch	—	440	—		
C _{oss}	Output Capacitance	N-Ch	—	180	—	pF	P-Channel V _{GS} = 0V, V _{DS} = -25V, f = 1.0MHz
		P-Ch	—	200	—		
C _{rss}	Reverse Transfer Capacitance	N-Ch	—	72	—	pF	P-Channel V _{GS} = 0V, V _{DS} = -25V, f = 1.0MHz
		P-Ch	—	93	—		

Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	N-Ch	—	—	3.1	A	
		P-Ch	—	—	-3.1		
I _{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	46	A	
		P-Ch	—	—	-34		
V _{SD}	Diode Forward Voltage	N-Ch	—	—	1.0	V	T _J = 25°C, I _S = 1.8A, V _{GS} = 0V ③
		P-Ch	—	—	-1.0		T _J = 25°C, I _S = -1.8A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	N-Ch	—	47	71	ns	N-Channel T _J = 25°C, I _F = 2.4A, di/dt = 100A/μs
		P-Ch	—	53	80		
Q _{rr}	Reverse Recovery Charge	N-Ch	—	56	84	nC	P-Channel T _J = 25°C, I _F = -1.8A, di/dt = 100A/μs ③
		P-Ch	—	66	99		

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② N-Channel I_{SD} ≤ 2.4A, di/dt ≤ 73A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C.
P-Channel I_{SD} ≤ -1.8A, di/dt ≤ 90A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C.
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ④ Surface mounted on FR-4 board, t ≤ 10sec.

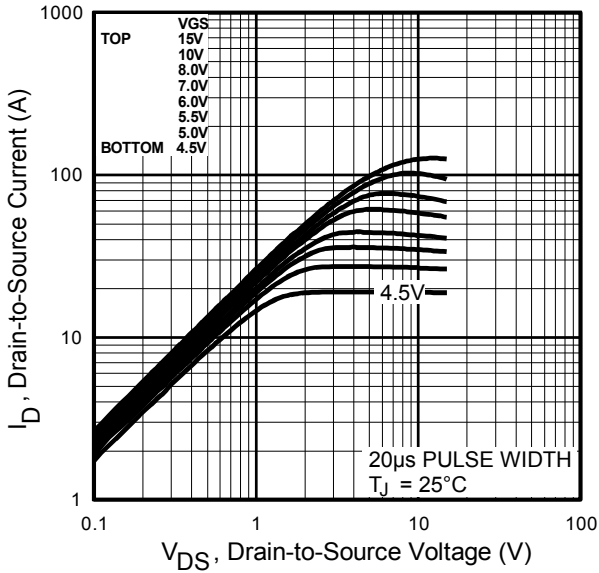


Fig. 1 Typical Output Characteristics

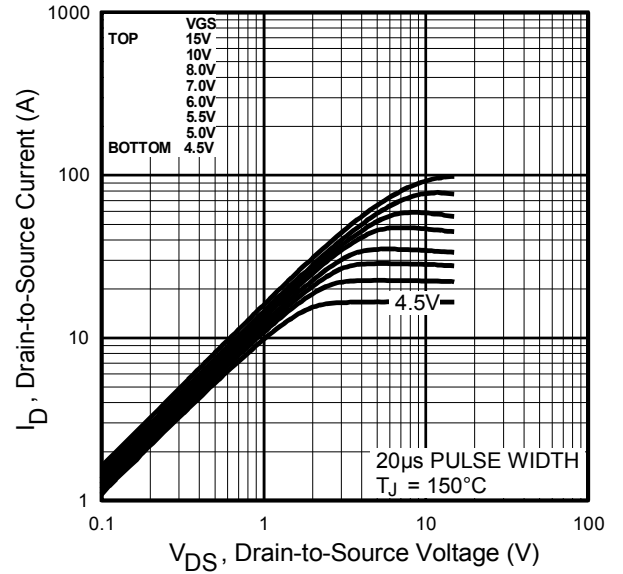


Fig. 2 Typical Output Characteristics

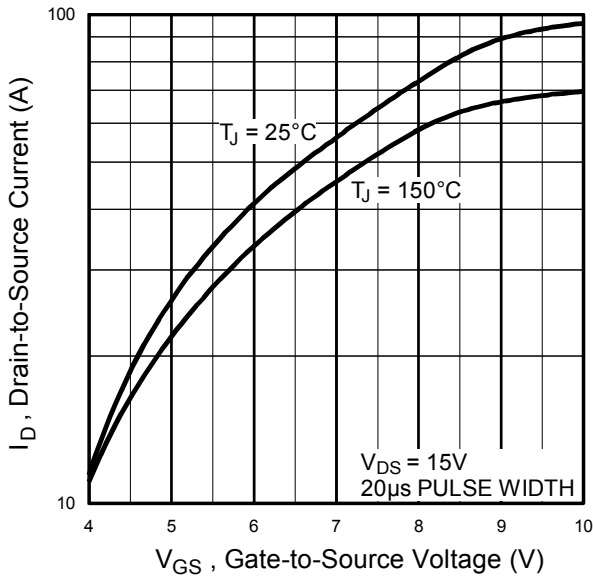


Fig. 3 Typical Transfer Characteristics

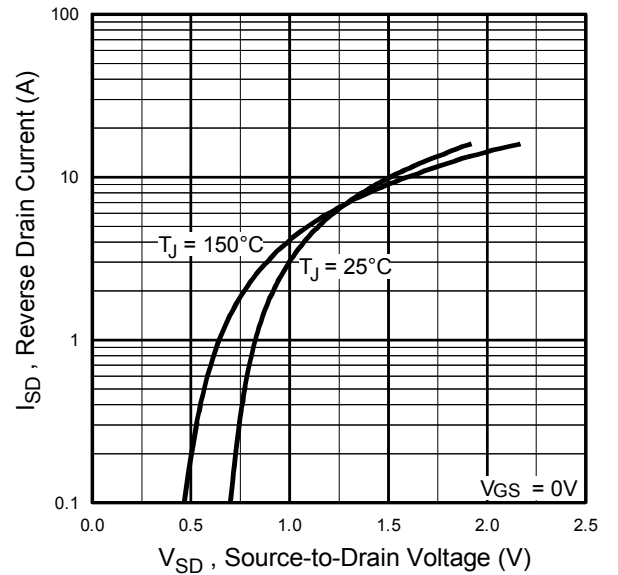


Fig. 4 Typical Source-Drain Diode Forward Voltage

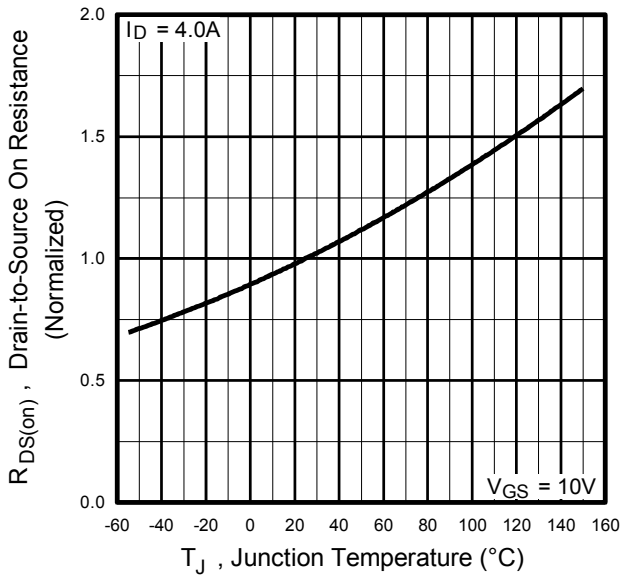


Fig 5. Normalized On-Resistance Vs. Temperature

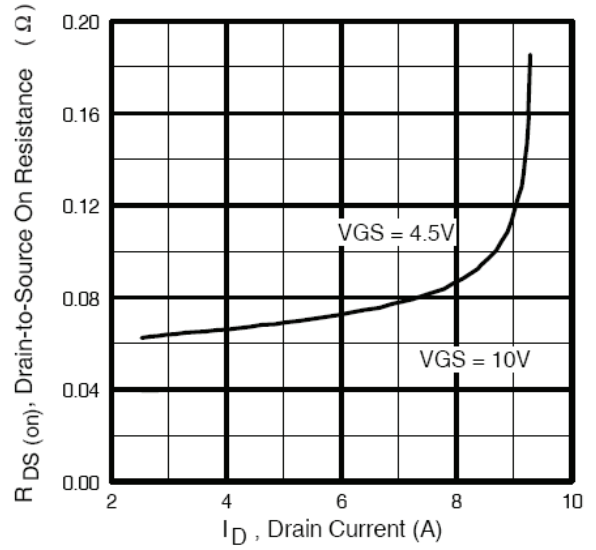


Fig 6. Typical On-Resistance Vs. Drain Current

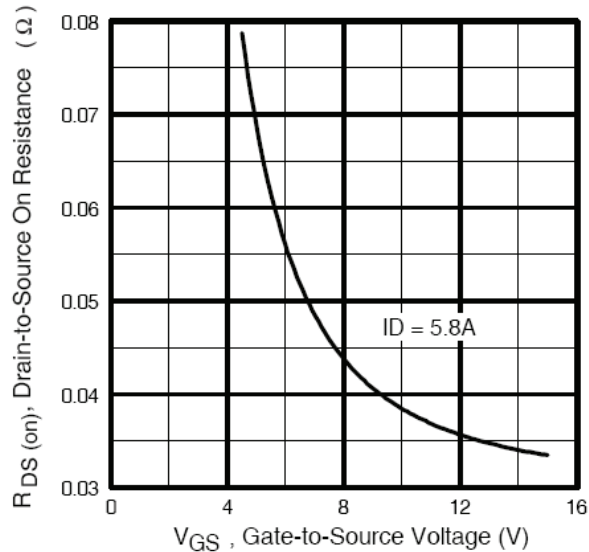


Fig. 7 Typical On-Resistance Vs. Gate Voltage

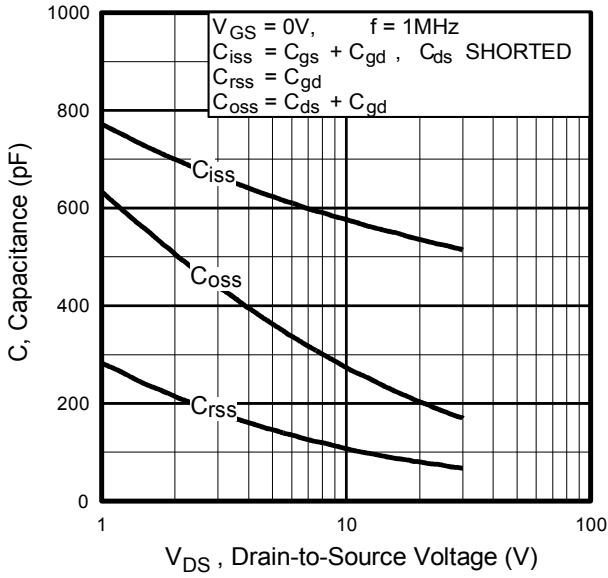


Fig 8. Typical Capacitance Vs. Drain-to-Source Voltage

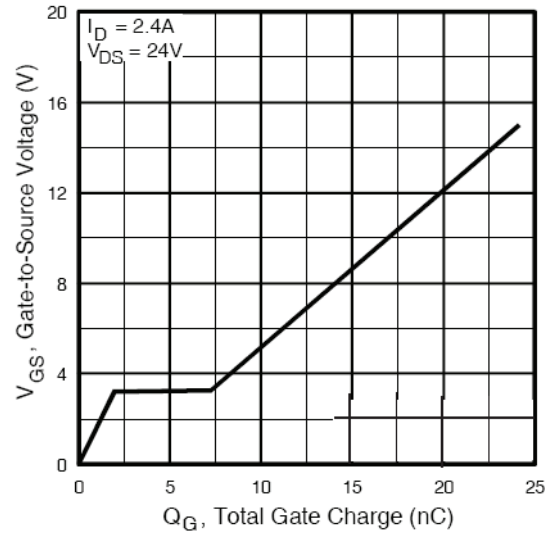


Fig 9. Typical Gate Charge Vs. Gate-to-Source Voltage

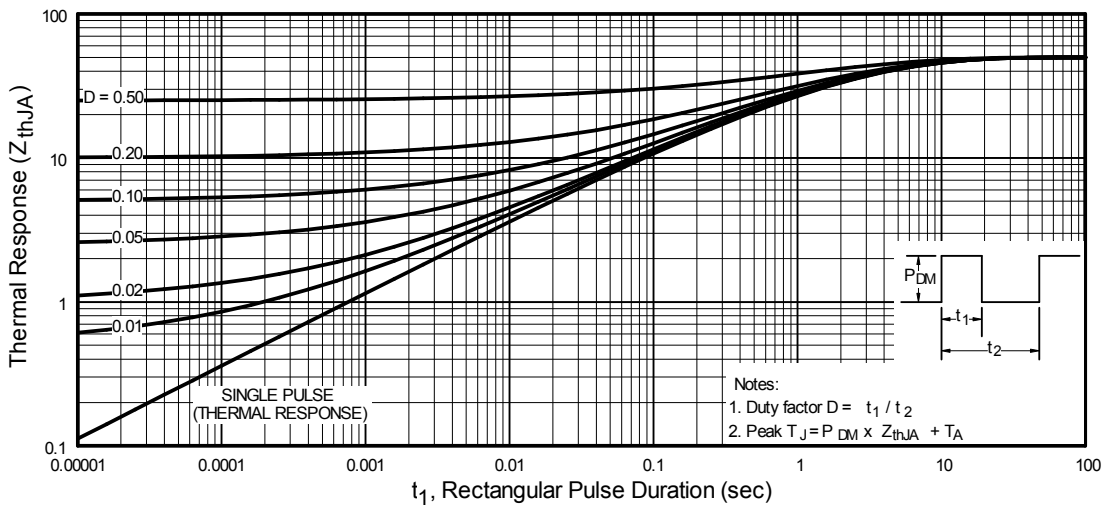


Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

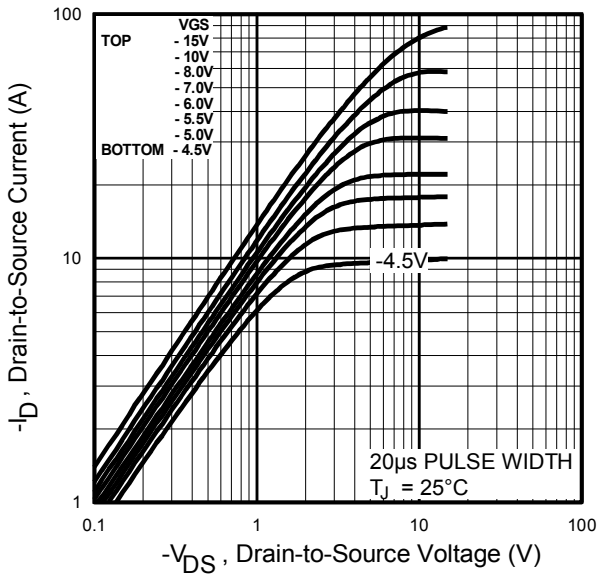


Fig. 11 Typical Output Characteristics

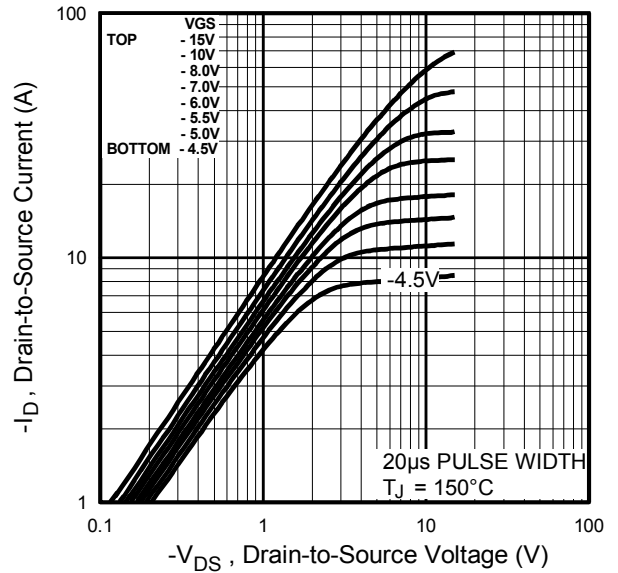


Fig. 12 Typical Output Characteristics

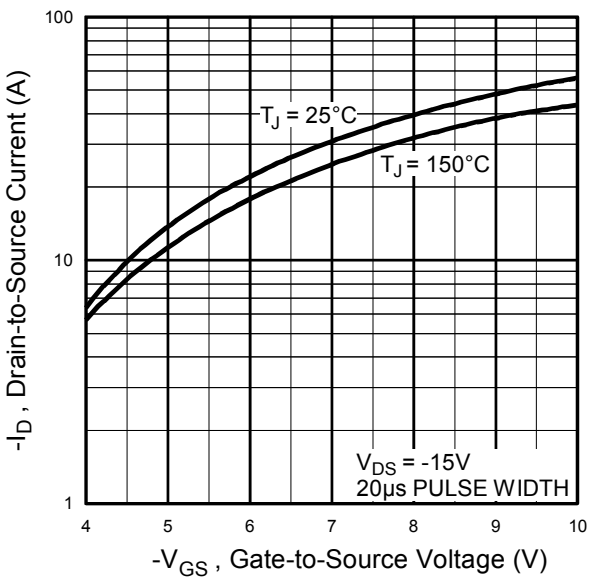


Fig. 13 Typical Transfer Characteristics

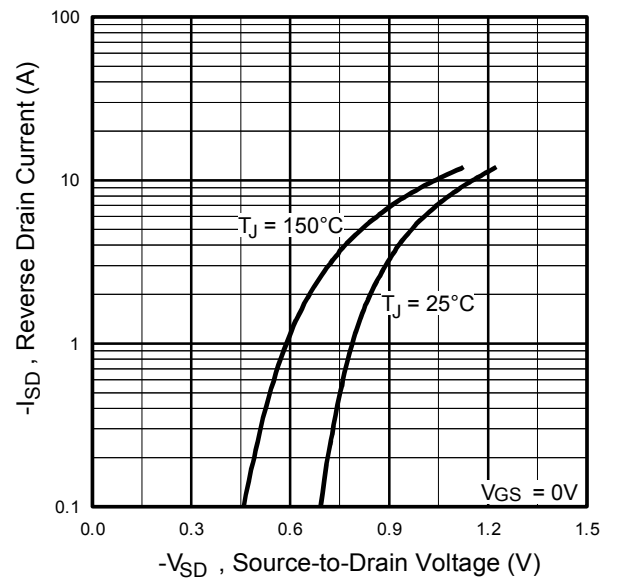


Fig. 14 Typical Source-Drain Diode Forward Voltage

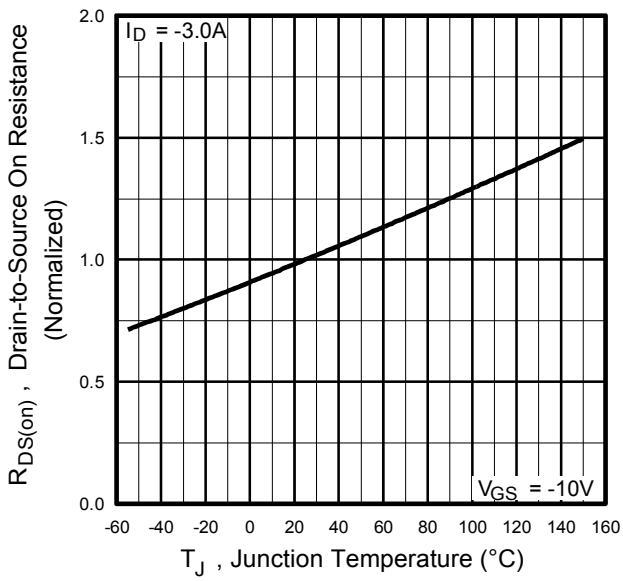


Fig 15. Normalized On-Resistance Vs. Temperature

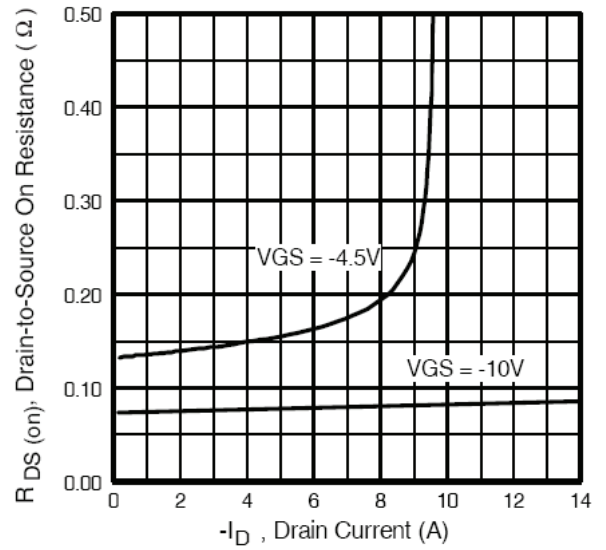


Fig 16. Typical On-Resistance Vs. Drain Current

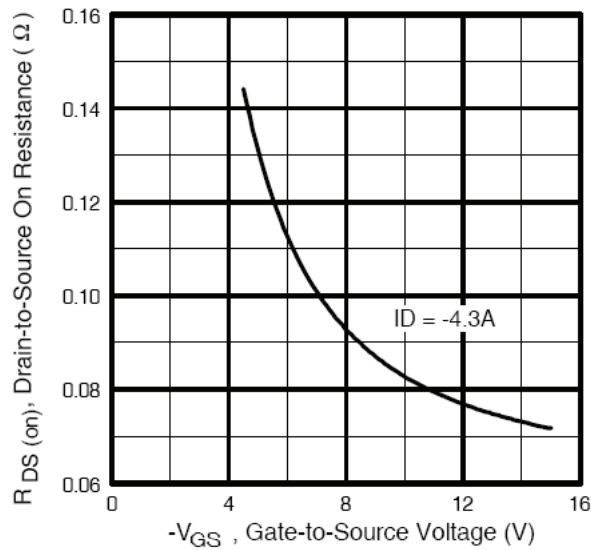


Fig. 17 Typical On-Resistance Vs. Gate Voltage

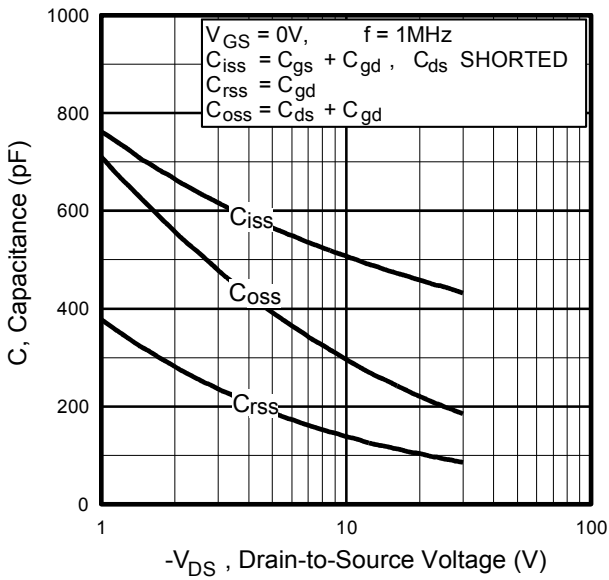


Fig 18. Typical Capacitance Vs. Drain-to-Source Voltage

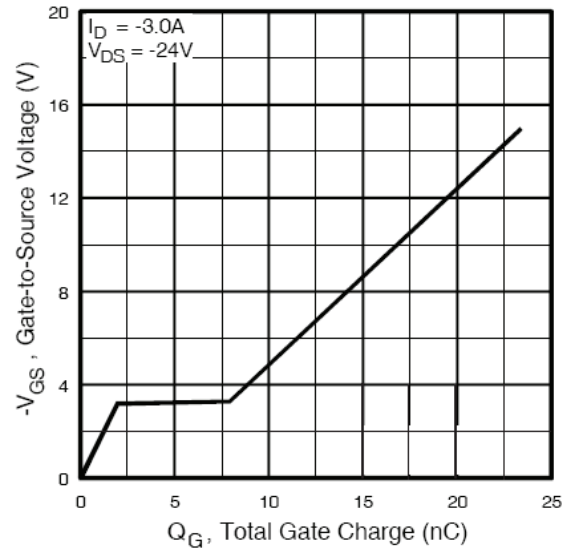


Fig 19. Typical Gate Charge Vs. Gate-to-Source Voltage

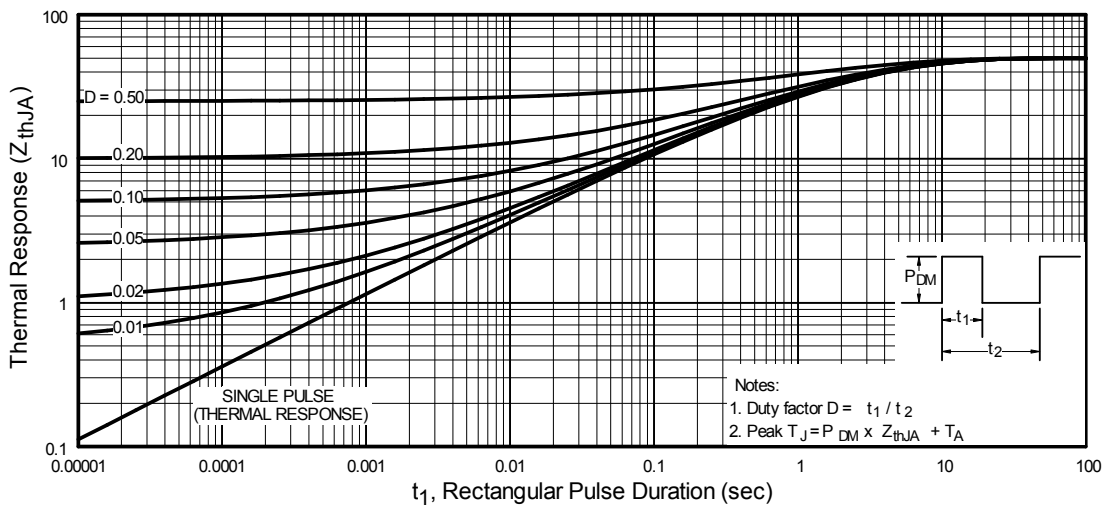
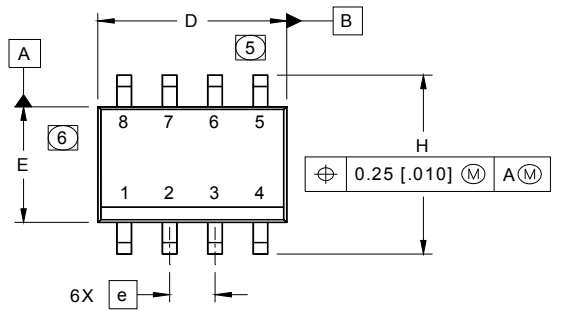
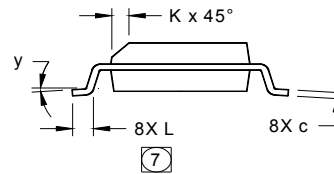
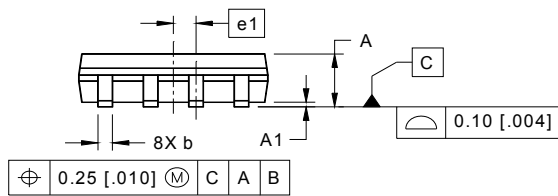


Fig 20. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

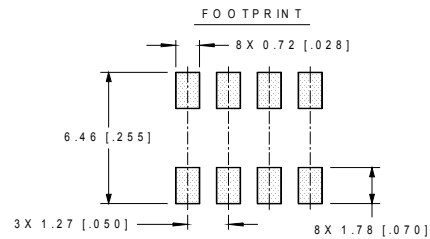
SO-8 Package Outline (Dimensions are shown in millimeters (inches))



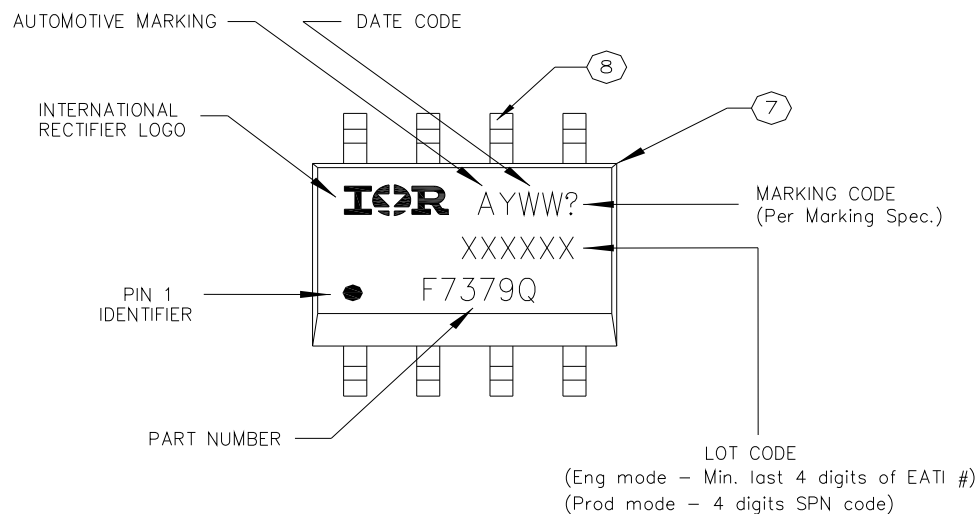
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

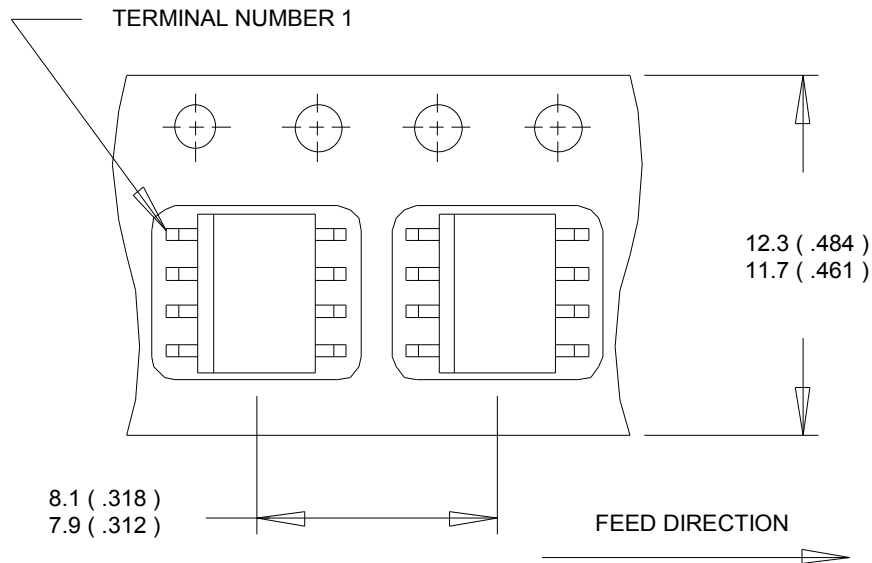


- NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M -1994.
 2. CONTROLLING DIMENSION: MILLIMETER
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
 5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
 6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
 7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

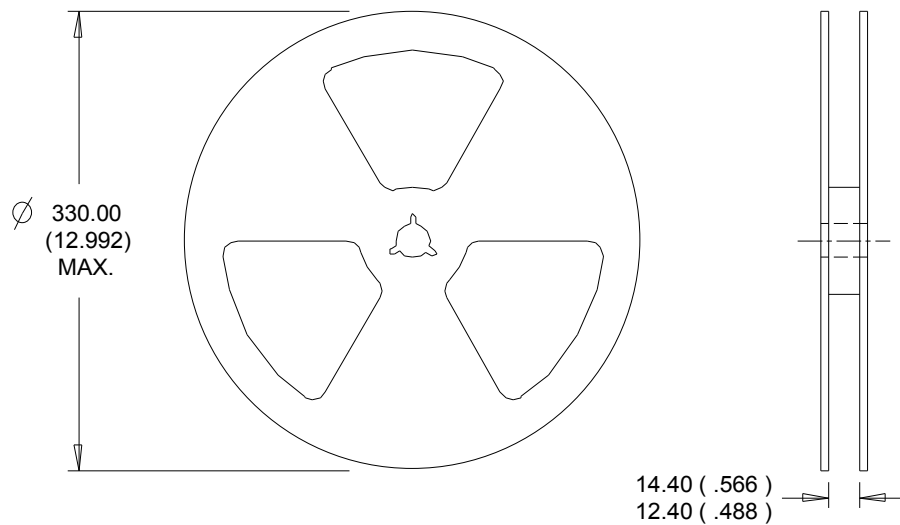


SO-8 Part Marking Information



SO-8 Tape and Reel (Dimensions are shown in millimeters (inches))

NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SO-8	MSL1
ESD	Machine Model	N Ch: Class M2 (+/- 150V) [†] P Ch: Class M2 (+/- 150V) [†] AEC-Q101-002	
	Human Body Model	N Ch: Class H1A (+/- 500V) [†] P Ch: Class H0 (+/- 250V) [†] AEC-Q101-001	
	Charged Device Model	N Ch: Class C5 (+/- 2000V) [†] P Ch: Class C5 (+/- 2000V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
3/10/2014	<ul style="list-style-type: none"> Added "Logic Level Gate Drive" bullet in the features section on page 1 Updated data sheet with new IR corporate template
9/30/2015	<ul style="list-style-type: none"> Updated datasheet with corporate template Corrected ordering table on page 1.

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