



**THE DATASHEET OF  
ADG1612BRUZ**



## FEATURES

- 1  $\Omega$  typical on resistance
- 0.2  $\Omega$  on resistance flatness
- $\pm 3.3$  V to  $\pm 8$  V dual-supply operation
- 3.3 V to 16 V single-supply operation
- No  $V_L$  supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- Continuous current per channel
  - LFCSP package: 280 mA
  - TSSOP package: 175 mA
- 16-lead TSSOP and 16-lead, 4 mm  $\times$  4 mm LFCSP

## APPLICATIONS

- Communication systems
- Medical systems
- Audio signal routing
- Video signal routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Relay replacements

## GENERAL DESCRIPTION

The **ADG1611/ADG1612/ADG1613** contain four independent single-pole/single-throw (SPST) switches. The **ADG1611** and **ADG1612** differ only in that the digital control logic is inverted. The **ADG1611** switches are turned on with Logic 0 on the appropriate control input, while Logic 1 is required for the **ADG1612** switches. The **ADG1613** has two switches with digital control logic similar to that of the **ADG1611**; the logic is inverted on the other two switches. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The **ADG1613** exhibits break-before-make switching action for use in multiplexer applications. Inherent in the design is the low charge injection for minimum transients when switching the digital inputs.

The ultralow on resistance of these switches make them ideal solutions for data acquisition and gain switching applications where low on resistance and distortion is critical. The on resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals.

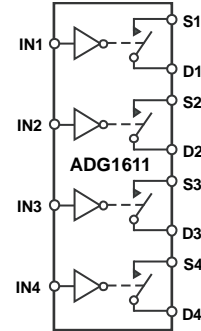
The CMOS construction ensures ultralow power dissipation, making them ideally suited for portable and battery-powered instruments.

Rev. C

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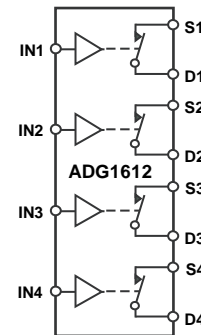
## FUNCTIONAL BLOCK DIAGRAMS



NOTES  
1. SWITCHES SHOWN FOR A LOGIC 1 INPUT.

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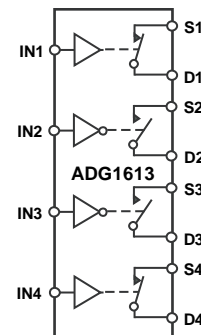
Figure 1.



NOTES  
1. SWITCHES SHOWN FOR A LOGIC 1 INPUT.

07981-033

Figure 2.



NOTES  
1. SWITCHES SHOWN FOR A LOGIC 1 INPUT.

07981-034

Figure 3.

## PRODUCT HIGHLIGHTS

1. 1.6  $\Omega$  maximum on resistance over temperature.
2. Minimum distortion: THD + N = 0.007%.
3. 3 V logic-compatible digital inputs:  $V_{INH} = 2.0$  V,  $V_{INL} = 0.8$  V.
4. No  $V_L$  logic power supply required.
5. Ultralow power dissipation: <16 nW.
6. 16-lead TSSOP and 16-lead, 4 mm  $\times$  4 mm LFCSP.

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**REVISION HISTORY**

**5/15—Rev. B to Rev. C**

Changed NC Pin to NIC Pin.....	Throughout
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**3/12—Rev. A to Rev. B**

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**8/09—Rev. 0 to Rev. A**

Changes to On Resistance ( $R_{ON}$ ) Parameter, On Resistance Match Between Channels ( $\Delta R_{ON}$ ) Parameter, and On Resistance Flatness ( $R_{FLATON}$ ) Parameter, Table 4 .....	6
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**1/09—Revision 0: Initial Version**

## SPECIFICATIONS

## ±5 V DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance ( $R_{ON}$ )	1			$\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 24
	1.2	1.4	1.6	$\Omega$ max	$V_{DD} = \pm 4.5\text{ V}$ , $V_{SS} = \pm 4.5\text{ V}$
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.04	0.09	0.1	$\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.08	0.09	0.1	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.2			$\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.25	0.29	0.34	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ $V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ ; see Figure 25
	$\pm 0.3$	$\pm 1$	$\pm 6$	nA max	
Drain Off Leakage, $I_D$ (Off)	$\pm 0.1$			nA typ	$V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ ; see Figure 25
	$\pm 0.3$	$\pm 1$	$\pm 6$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.2$			nA typ	$V_S = V_D = \pm 4.5\text{ V}$ ; see Figure 26
	$\pm 0.4$	$\pm 1.5$	$\pm 10$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	+0.005		$\pm 0.1$	$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	165			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	212	253	285	ns max	$V_S = 2.5\text{ V}$ ; see Figure 31
$t_{OFF}$	105			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	137	150	159	ns max	$V_S = 2.5\text{ V}$ ; see Figure 31
Break-Before-Make Time Delay, $t_D$ (ADG1613 Only)	25			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			20	ns min	$V_{S1} = V_{S2} = 2.5\text{ V}$ ; see Figure 32
Charge Injection	140			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 33
Off Isolation	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 27
Channel-to-Channel Crosstalk	110			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 28
Total Harmonic Distortion + Noise (THD + N)	0.007			% typ	$R_L = 110\ \Omega$ , 5 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 30
-3 dB Bandwidth	42			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 29
$C_S$ (Off)	63			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	63			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	154			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ Digital inputs = 0 V or $V_{DD}$
			1.0	$\mu\text{A}$ max	
$V_{DD}/V_{SS}$			$\pm 3.3/\pm 8$	V min/max	

<sup>1</sup> Guaranteed by design, not subject to production test.

## 12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 2.**

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.95			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 24
	1.1	1.25	1.45	$\Omega$ max	$V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.03			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
	0.06	0.7	0.08	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.2			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
	0.23	0.27	0.32	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$
	$\pm 0.3$	$\pm 1$	$\pm 6$	nA max	$V_S = 1\text{ V}/10\text{ V}$ , $V_S = 10\text{ V}/1\text{ V}$ , see Figure 25
Drain Off Leakage, $I_D$ (Off)	$\pm 0.1$			nA typ	$V_S = 1\text{ V}/10\text{ V}$ , $V_S = 10\text{ V}/1\text{ V}$ see Figure 25
	$\pm 0.3$	$\pm 1$	$\pm 6$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.2$			nA typ	$V_S = V_D = 1\text{ V or }10\text{ V}$ ; see Figure 26
	$\pm 0.4$	$\pm 1.5$	$\pm 10$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.001			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	125			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	156	190	215	ns max	$V_S = 8\text{ V}$ ; see Figure 31
$t_{OFF}$	75			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	87	93	99	ns max	$V_S = 8\text{ V}$ ; see Figure 31
Break-Before-Make Time Delay, $t_D$ (ADG1613 Only)	35			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			30	ns min	$V_{S1} = V_{S2} = 8\text{ V}$ ; see Figure 32
Charge Injection	170			pC typ	$V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 33
Off Isolation	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 27
Channel-to-Channel Crosstalk	110			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 28
Total Harmonic Distortion + Noise	0.012			% typ	$R_L = 110\ \Omega$ , 5 V p-p, $f = 20\text{ Hz to }20\text{ kHz}$ ; see Figure 30
-3 dB Bandwidth	38			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 29
$C_S$ (Off)	60			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	60			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	154			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 12\text{ V}$
			1	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$I_{DD}$	320			$\mu\text{A}$ typ	Digital inputs = 5 V
			480	$\mu\text{A}$ max	
$V_{DD}$			3.3/16	V min/max	

<sup>1</sup> Guaranteed by design, not subject to production test.

**5 V SINGLE SUPPLY**

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 3.**

Parameter	25°C	-40°C to +85°C	-40°C to 125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	1.7			$\Omega$ typ	$V_S = 0\text{ V to }4.5\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 24
	2.15	2.4	2.7	$\Omega$ max	$V_{DD} = 4.5\text{ V}$ , $V_{SS} = 0\text{ V}$
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.05			$\Omega$ typ	$V_S = 0\text{ V to }4.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.09	0.12	0.15	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.4			$\Omega$ typ	$V_S = 0\text{ V to }4.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.53	0.55	0.6	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.05$			nA typ	$V_{DD} = 5.5\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/4.5\text{ V}$ , $V_D = 4.5\text{ V}/1\text{ V}$ ; see Figure 25
	$\pm 0.3$	$\pm 1$	$\pm 6$	nA max	
Drain Off Leakage, $I_D$ (Off)	$\pm 0.05$			nA typ	$V_S = 1\text{ V}/4.5\text{ V}$ , $V_D = 4.5\text{ V}/1\text{ V}$ ; see Figure 25
	$\pm 0.3$	$\pm 1$	$\pm 6$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.15$			nA typ	$V_S = V_D = 1\text{ V or }4.5\text{ V}$ ; see Figure 26
	$\pm 0.4$	$\pm 1.5$	$\pm 10$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.001			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	215			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	279	334	376	ns max	$V_S = 2.5\text{ V}$ ; see Figure 31
$t_{OFF}$	115			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	150	169	180	ns max	$V_S = 2.5\text{ V}$ ; see Figure 31
Break-Before-Make Time Delay, $t_D$ (ADG1613 Only)	35			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			25	ns min	$V_{S1} = V_{S2} = 2.5\text{ V}$ ; see Figure 32
Charge Injection	80			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 33
Off Isolation	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 27
Channel-to-Channel Crosstalk	110			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 28
Total Harmonic Distortion + Noise	0.093			% typ	$R_L = 110\ \Omega$ , $f = 20\text{ Hz to }20\text{ kHz}$ , $V_S = 3.5\text{ V p-p}$ ; see Figure 30
-3 dB Bandwidth	42			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 29
$C_S$ (Off)	72			pF typ	$V_S = 2.5\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	72			pF typ	$V_S = 2.5\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	160			pF typ	$V_S = 2.5\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$ Digital inputs = 0 V or $V_{DD}$
			1	$\mu\text{A}$ max	
$V_{DD}$			3.3/16	V min/max	

<sup>1</sup> Guaranteed by design, not subject to production test.

**3.3 V SINGLE SUPPLY**

$V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 4.**

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	3.2	3.4	3.6	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = -10\text{ mA}$ , $V_{DD} = 3.3\text{ V}$ , $V_{SS} = 0\text{ V}$ ; see Figure 24
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.06	0.07	0.08	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = -10\text{ mA}$
On Resistance Flatness ( $R_{FLAT(ON)}$ )	1.2	1.3	1.4	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.02$			nA typ	$V_{DD} = 3.6\text{ V}$ , $V_{SS} = 0\text{ V}$
	$\pm 0.3$	$\pm 1$	$\pm 6$	nA max	$V_S = 0.6\text{ V}/3\text{ V}$ , $V_D = 3\text{ V}/0.6\text{ V}$ ; see Figure 25
Drain Off Leakage, $I_D$ (Off)	$\pm 0.02$			nA typ	$V_S = 0.6\text{ V}/3\text{ V}$ , $V_D = 3\text{ V}/0.6\text{ V}$ ; see Figure 25
	$\pm 0.3$	$\pm 1$	$\pm 6$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.1$			nA typ	$V_S = V_D = 0.6\text{ V or }3\text{ V}$ ; see Figure 26
	$\pm 0.4$	$\pm 1.5$	$\pm 10$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.001			$\mu\text{A typ}$	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A max}$	
Digital Input Capacitance, $C_{IN}$	3			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	350			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	493	556	603	ns max	$V_S = 1.5\text{ V}$ ; see Figure 31
$t_{OFF}$	190			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	263	286	300	ns max	$V_S = 1.5\text{ V}$ ; see Figure 31
Break-Before-Make Time Delay, $t_D$ (ADG1613 Only)	25			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			18	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$ ; see Figure 32
Charge Injection	50			pC typ	$V_S = 1.5\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 33
Off Isolation	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 27
Channel-to-Channel Crosstalk	110			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 28
Total Harmonic Distortion + Noise	0.18			% typ	$R_L = 110\ \Omega$ , $f = 20\text{ Hz to }20\text{ kHz}$ , $V_S = 2\text{ V p-p}$ ; see Figure 30
−3 dB Bandwidth	52			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 29
$C_S$ (Off)	76			pF typ	$V_S = 1.5\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	76			pF typ	$V_S = 1.5\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	160			pF typ	$V_S = 1.5\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A typ}$	$V_{DD} = 3.6\text{ V}$
		1.0	1.0	$\mu\text{A max}$	Digital inputs = 0 V or $V_{DD}$
$V_{DD}$			3.3/16	V min/max	

<sup>1</sup> Guaranteed by design, not subject to production test.

**CONTINUOUS CURRENT PER CHANNEL, S OR D**

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
$V_{DD} = +5\text{ V}, V_{SS} = -5\text{ V}$				
TSSOP ( $\theta_{JA} = 150.4^\circ\text{C/W}$ )	175	119	70	mA maximum
LFCSP ( $\theta_{JA} = 48.7^\circ\text{C/W}$ )	280	175	95	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ( $\theta_{JA} = 150.4^\circ\text{C/W}$ )	206	135	84	mA maximum
LFCSP ( $\theta_{JA} = 48.7^\circ\text{C/W}$ )	336	203	108	mA maximum
$V_{DD} = 5\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ( $\theta_{JA} = 150.4^\circ\text{C/W}$ )	140	91	63	mA maximum
LFCSP ( $\theta_{JA} = 48.7^\circ\text{C/W}$ )	220	140	84	mA maximum
$V_{DD} = 3.3\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ( $\theta_{JA} = 150.4^\circ\text{C/W}$ )	140	98	70	mA maximum
LFCSP ( $\theta_{JA} = 48.7^\circ\text{C/W}$ )	228	150	91	mA maximum

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 6.

Parameter	Rating
$V_{DD}$ to $V_{SS}$	18 V
$V_{DD}$ to GND	-0.3 V to +18 V
$V_{SS}$ to GND	+0.3 V to -18 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	630 mA (pulsed at 1 ms, 10% duty-cycle maximum)
Continuous Current, S or D <sup>2</sup>	Data + 15%
Operating Temperature Range Industrial (Y Version)	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, $\theta_{JA}$ Thermal Impedance (2-Layer Board)	150.4°C/W
16-Lead LFCSOP, $\theta_{JA}$ Thermal Impedance (4-Layer Board)	48.7°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

<sup>2</sup> See Table 5.

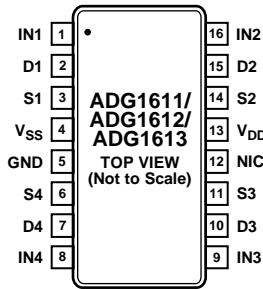
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



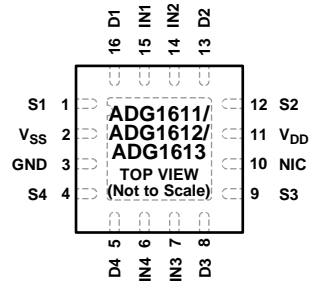
**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

### PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES  
1. NIC = NOT INTERNALLY CONNECTED.

Figure 4. 16-Lead TSSOP Pin Configuration



NOTES  
1. NIC = NOT INTERNALLY CONNECTED.  
2. EXPOSED PAD TIED TO SUBSTRATE, VSS.

Figure 5. 16-Lead LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.		Mnemonic	Description
16-Lead TSSOP	16-Lead LFCSP		
1	15	IN1	Logic Control Input.
2	16	D1	Drain Terminal. This pin can be an input or output.
3	1	S1	Source Terminal. This pin can be an input or output.
4	2	V <sub>SS</sub>	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Source Terminal. This pin can be an input or output.
7	5	D4	Drain Terminal. This pin can be an input or output.
8	6	IN4	Logic Control Input.
9	7	IN3	Logic Control Input.
10	8	D3	Drain Terminal. This pin can be an input or output.
11	9	S3	Source Terminal. This pin can be an input or output.
12	10	NIC	Not Internally Connected.
13	11	V <sub>DD</sub>	Most Positive Power Supply Potential.
14	12	S2	Source Terminal. This pin can be an input or output.
15	13	D2	Drain Terminal. This pin can be an input or output.
16	14	IN2	Logic Control Input.
Not applicable	17 (EPAD)	EP (EPAD)	Exposed Pad. Tied to substrate, V <sub>SS</sub> .

Table 8. ADG1611/ADG1612 Truth Table

ADG1611 INx	ADG1612 INx	Switch Condition
0	1	On
1	0	Off

Table 9. ADG1613 Truth Table

Logic (INx)	Switch 1, Switch 4	Switch 2, Switch 3
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

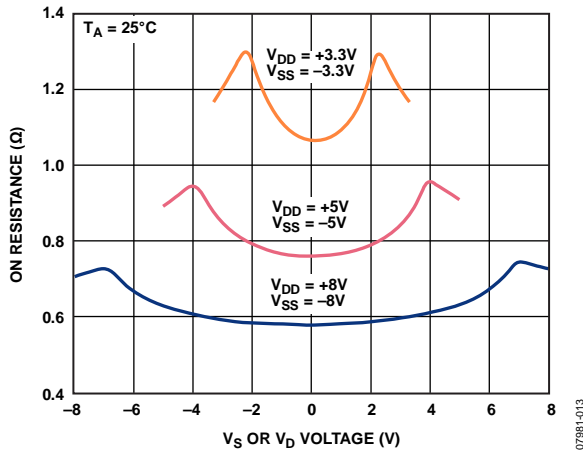


Figure 6. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply

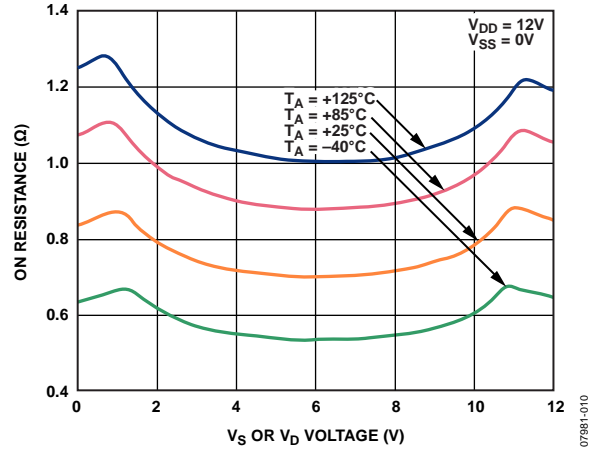


Figure 9. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, 12 V Single Supply

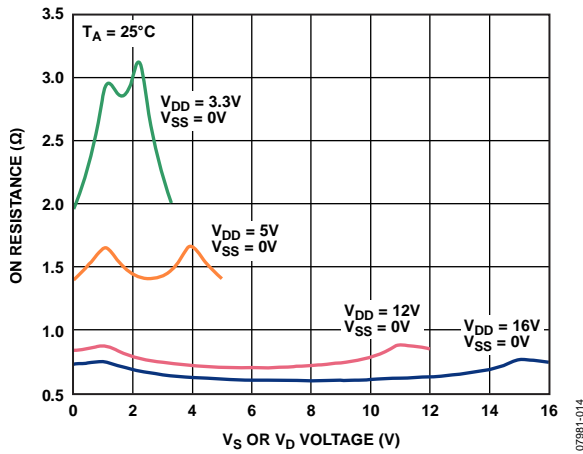


Figure 7. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Single Supply

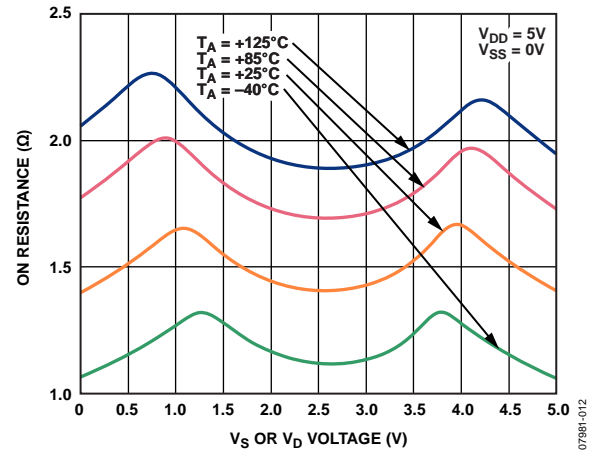


Figure 10. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, 5 V Single Supply

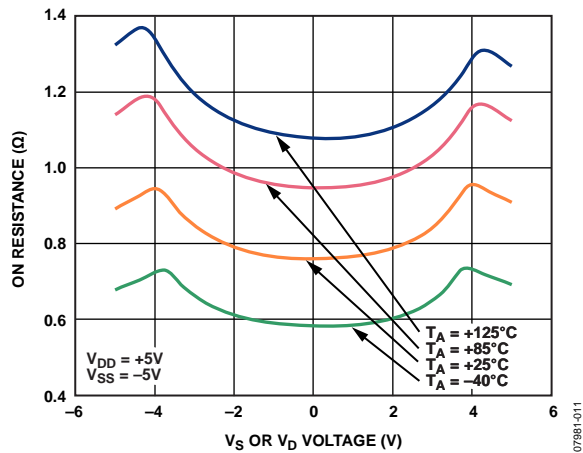


Figure 8. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures,  $\pm 5$  V Dual Supply

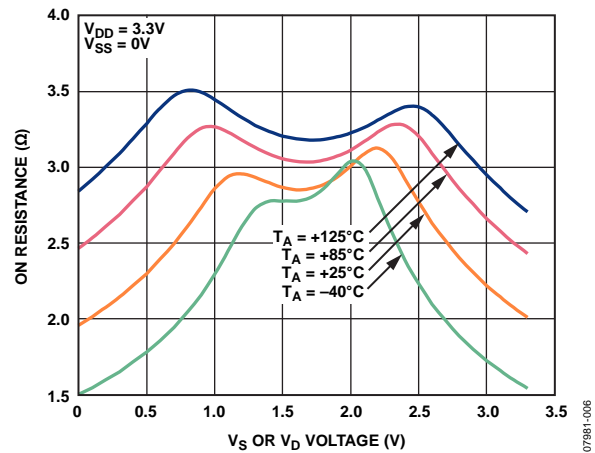


Figure 11. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, 3.3 V Single Supply

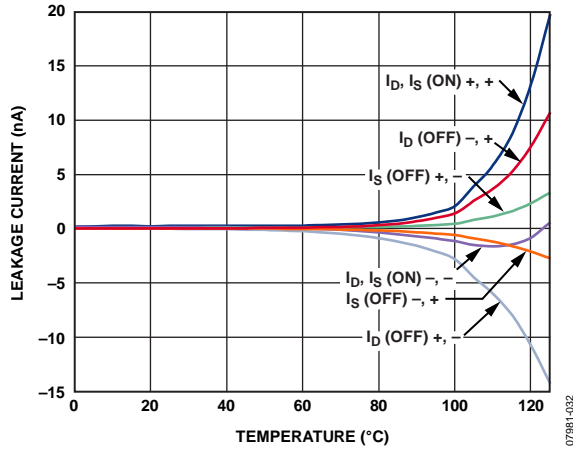


Figure 12. Leakage Currents as a Function of Temperature, ±5 V Dual Supply

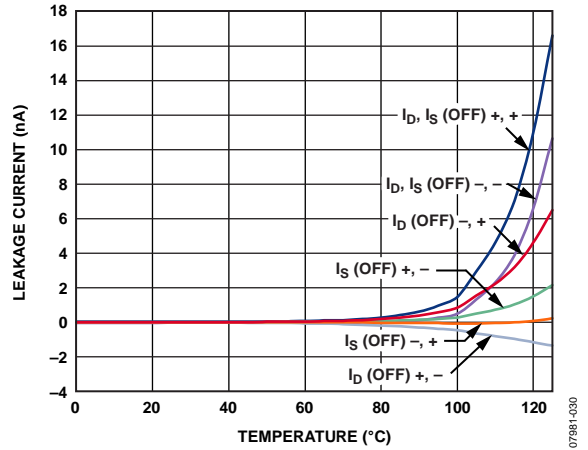


Figure 15. Leakage Currents as a Function of Temperature, 3.3 V Single Supply

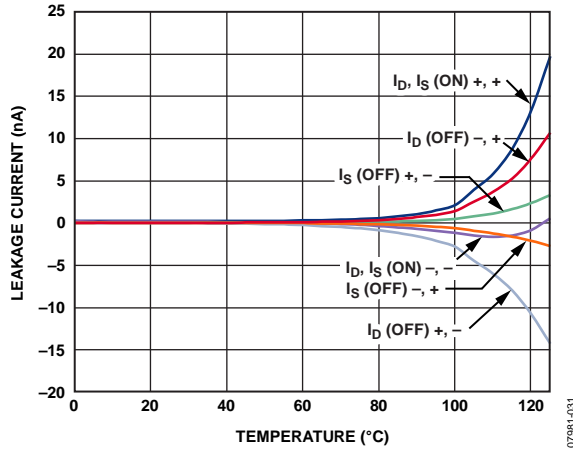


Figure 13. Leakage Currents as a Function of Temperature, 12 V Single Supply

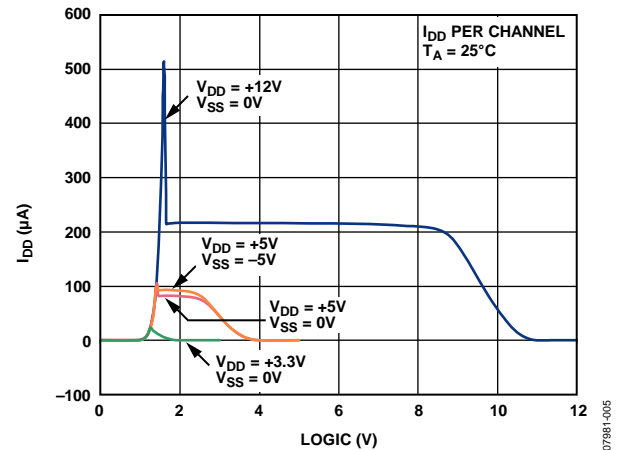


Figure 16.  $I_{DD}$  vs. Logic Level

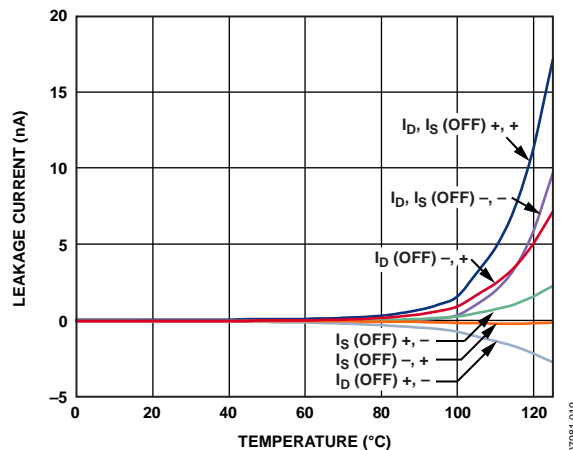


Figure 14. Leakage Currents as a Function of Temperature, 5 V Single Supply

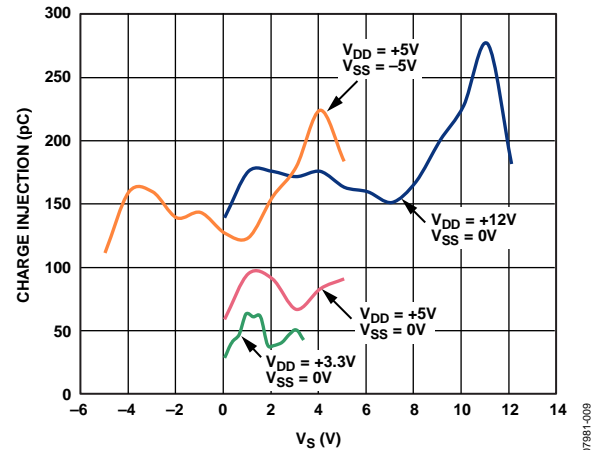


Figure 17. Charge Injection vs. Source Voltage ( $V_s$ )

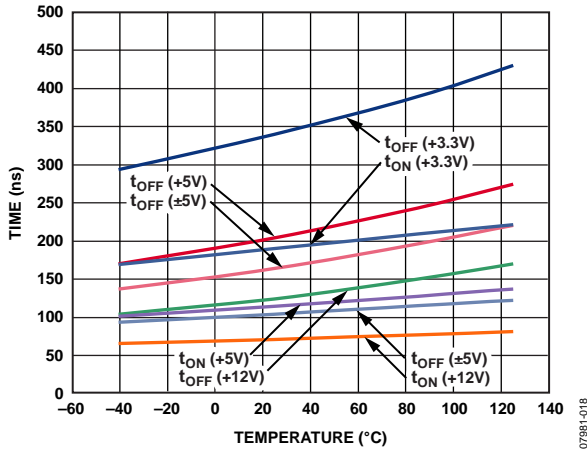


Figure 18.  $t_{ON}/t_{OFF}$  Times vs. Temperature

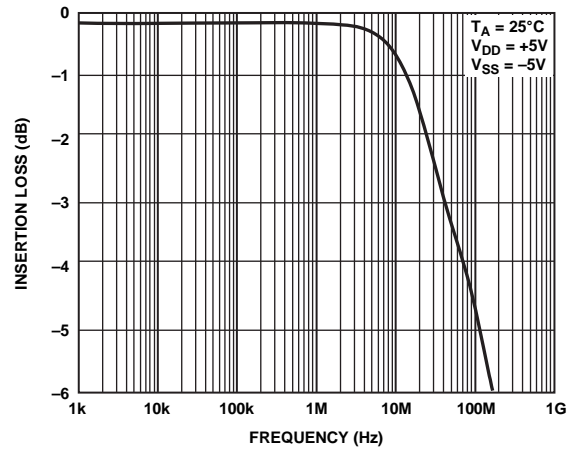


Figure 21. On Response vs. Frequency

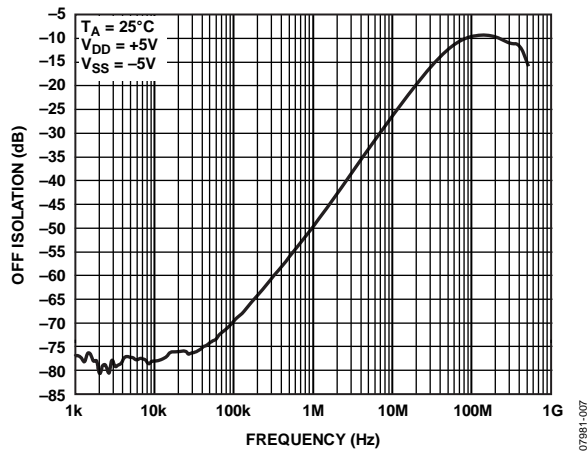


Figure 19. Off Isolation vs. Frequency

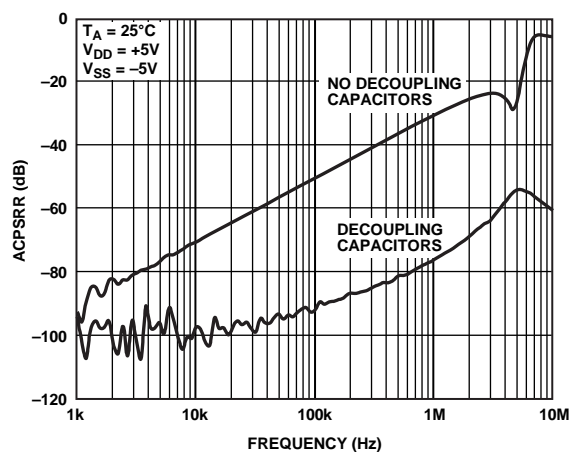


Figure 22. ACPSRR vs. Frequency

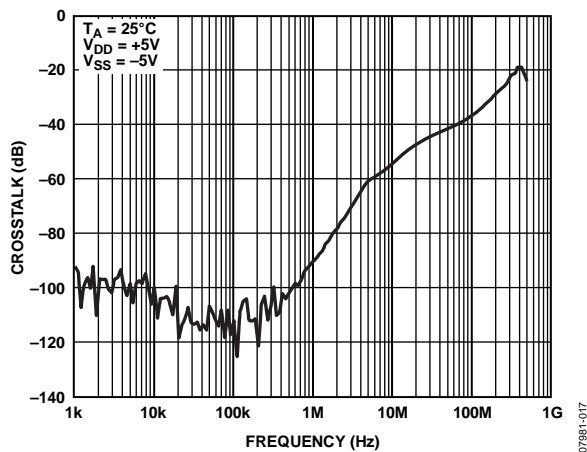


Figure 20. Crosstalk vs. Frequency

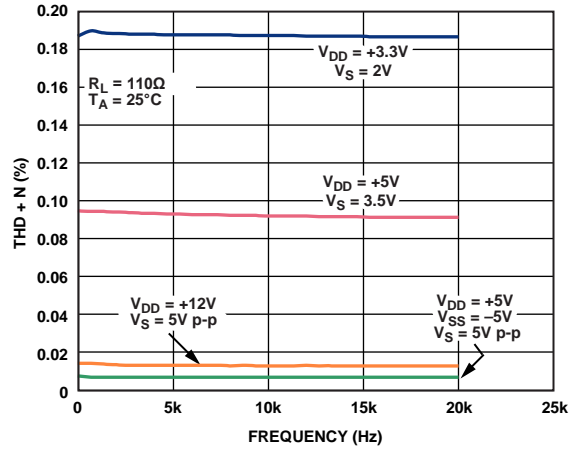


Figure 23. THD + N vs. Frequency

TEST CIRCUITS

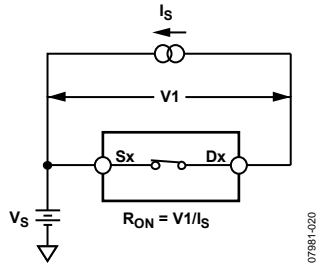


Figure 24. On Resistance

07981-020

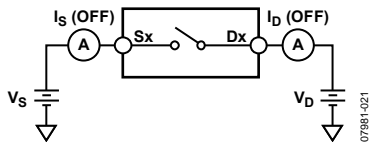


Figure 25. Off Leakage

07981-021

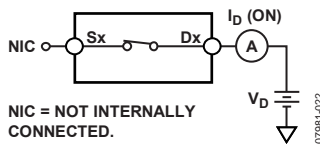


Figure 26. On Leakage

07981-022

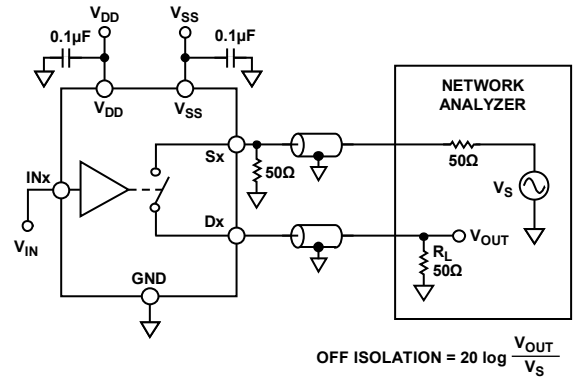


Figure 27. Off Isolation

07981-026

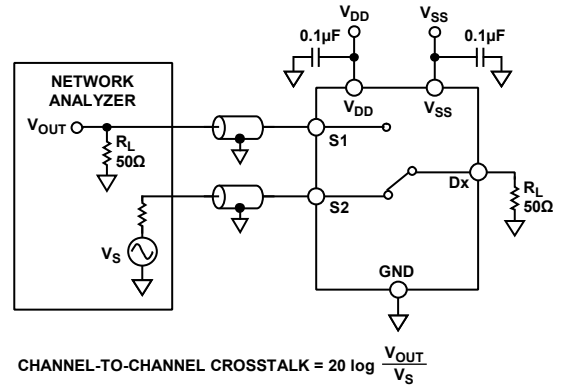


Figure 28. Channel-to-Channel Crosstalk

07981-027

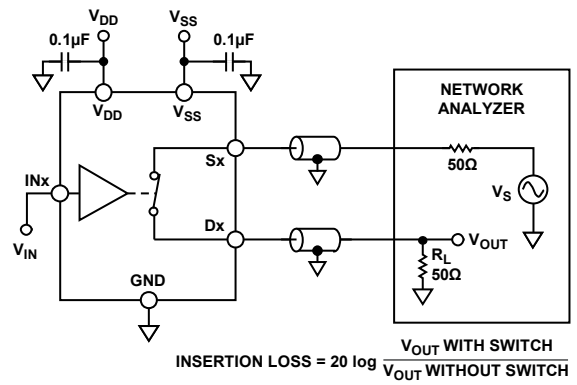


Figure 29. Bandwidth

07981-028

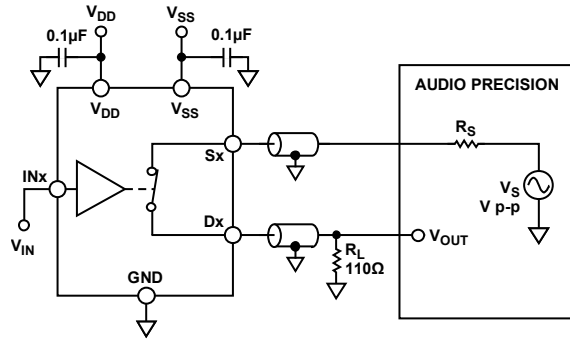


Figure 30. THD + Noise

07981-023

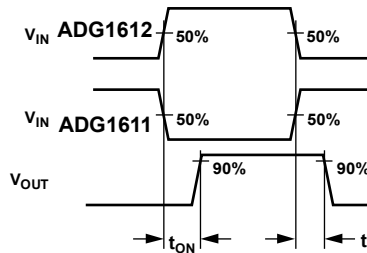
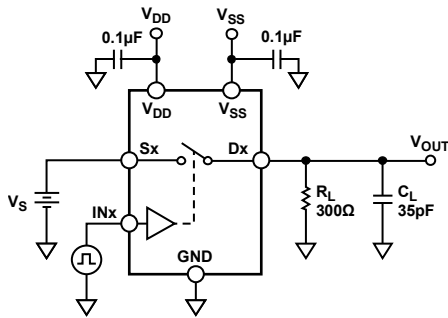


Figure 31. Switching Times

07981-023

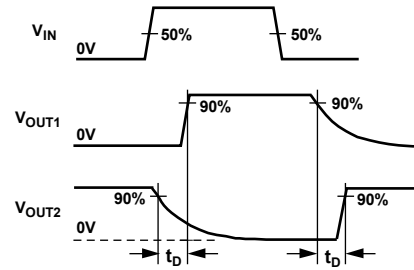
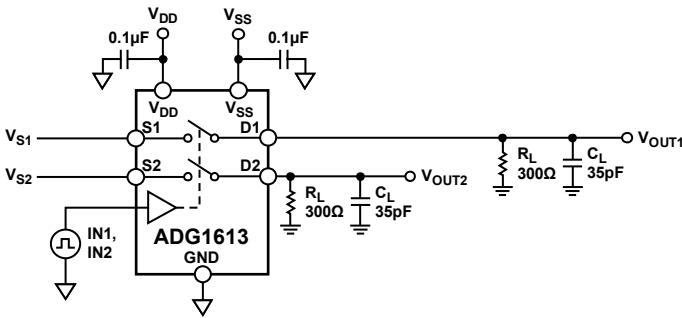


Figure 32. Break-Before-Make Time Delay

07981-024

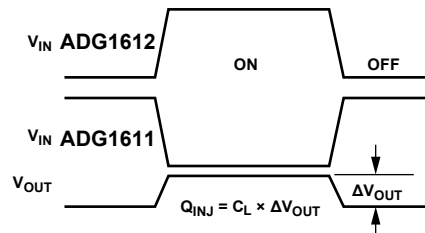
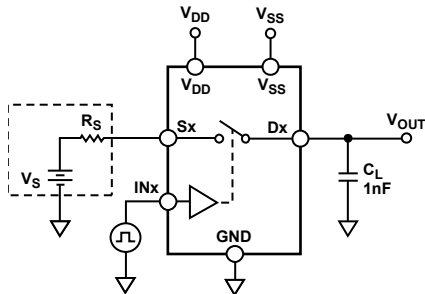


Figure 33. Charge Injection

07981-025

## TERMINOLOGY

### $I_{DD}$

The positive supply current.

### $I_{SS}$

The negative supply current.

### $V_D (V_S)$

The analog voltage on Terminal D and Terminal S.

### $R_{ON}$

The ohmic resistance between Terminal D and Terminal S.

### $R_{FLAT(ON)}$

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

### $I_S$ (Off)

The source leakage current with the switch off.

### $I_D$ (Off)

The drain leakage current with the switch off.

### $I_D, I_S$ (On)

The channel leakage current with the switch on.

### $V_{INL}$

The maximum input voltage for Logic 0.

### $V_{INH}$

The minimum input voltage for Logic 1.

### $I_{INL} (I_{INH})$

The input current of the digital input.

### $C_S$ (Off)

The off switch source capacitance, which is measured with reference to ground.

### $C_D$ (Off)

The off switch drain capacitance, which is measured with reference to ground.

### $C_D, C_S$ (On)

The on switch capacitance, which is measured with reference to ground.

### $C_{IN}$

The digital input capacitance.

### $t_{ON}$

The delay between applying the digital control input and the output switching on. See Figure 31.

### $t_{OFF}$

The delay between applying the digital control input and the output switching off. See Figure 31.

### Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching. See Figure 33.

### Off Isolation

A measure of unwanted signal coupling through an off switch. See Figure 27.

### Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. See Figure 28.

### Bandwidth

The frequency at which the output is attenuated by 3 dB. See Figure 29.

### On Response

The frequency response of the on switch.

### Insertion Loss

The loss due to the on resistance of the switch.

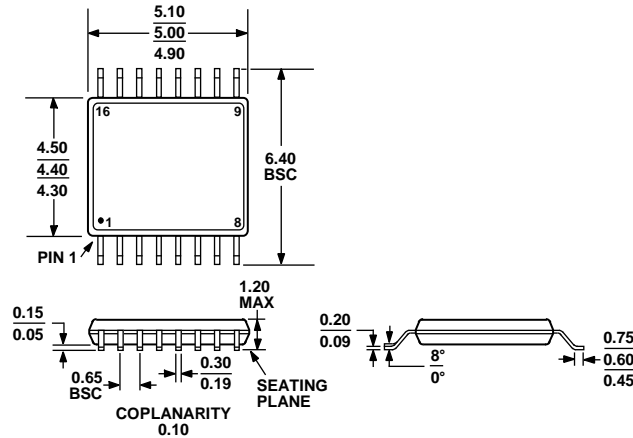
### Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental. See Figure 30.

### AC Power Supply Rejection Ratio (ACPSRR)

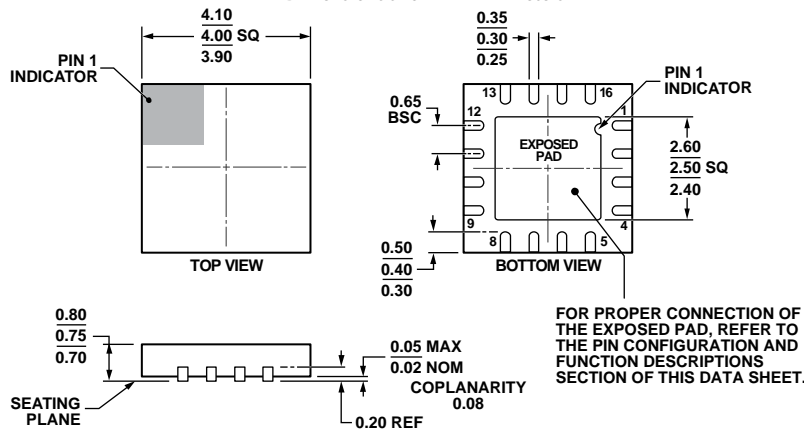
The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB  
 Figure 34. 16-Lead Thin Shrink Small Outline Package [TSSOP]  
 (RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.  
 Figure 35. 16-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
 4 mm x 4 mm Body, Very Very Thin Quad  
 (CP-16-26)

Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADG1611BRUZ	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1611BRUZ-REEL	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1611BRUZ-REEL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1611BCPZ-REEL	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-26
ADG1611BCPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-26
ADG1612BRUZ	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1612BRUZ-REEL	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1612BRUZ-REEL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1612BCPZ-REEL	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-26
ADG1612BCPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-26
ADG1613BRUZ	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1613BRUZ-REEL	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1613BRUZ-REEL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1613BCPZ-REEL	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-26
ADG1613BCPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-26

<sup>1</sup> Z = RoHS Compliant Part.

## Looking for pricing, stock, or lifecycle information?

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