THE DATASHEET OF

A8601KLPTR-T

Multiple-Output Regulator for Automotive LCD Displays

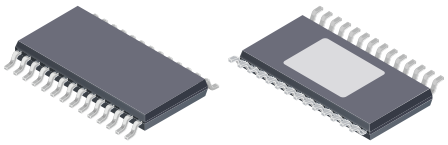
Features and Benefits

- Automotive-grade AEC-Q100 qualified
- Five individual output supplies
- Independent control of each output voltage
- 350 kHz to 2.25 MHz switching frequency with external synchronization capability
- <10 µA shutdown current
- Preprogrammed power-up and shutdown sequences
- Overcurrent, overvoltage, short circuit, and thermal overload protection

Applications:

- GPS
- Infotainment
- Medium LCDs

Package: 28-pin TSSOP with exposed thermal pad (suffix LP)



Not to scale

Description

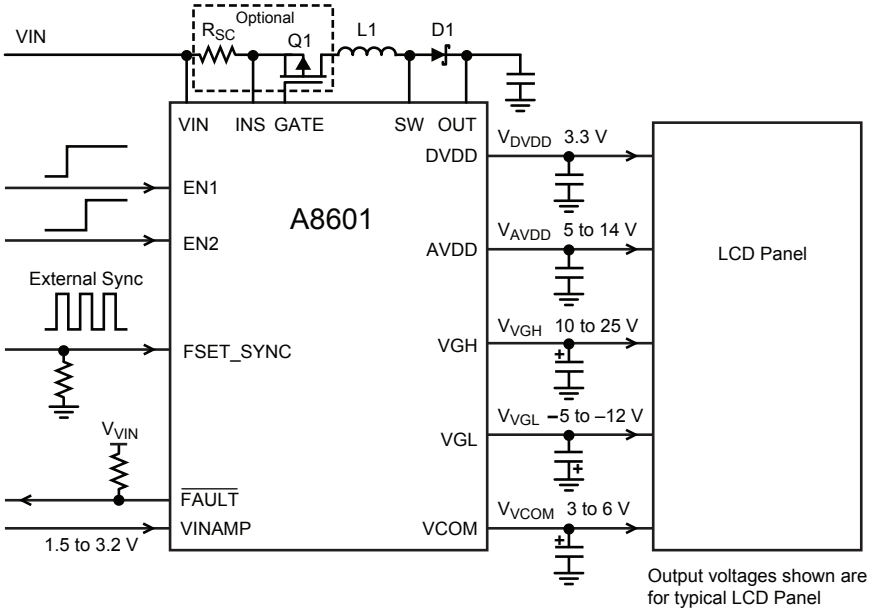
The A8601 is a fixed frequency, multiple-output supply for LCD bias. Its switching frequency can be either programmed or synchronized with an external clock signal between 350 kHz and 2.25 MHz, to minimize interference with AM and FM radio bands.

A total of five output voltages are provided, from three linear regulators and two charge-pump regulators. Each output voltage can be adjusted independently. During power-up and shutdown, the outputs are turned on and off in preprogrammed sequences, to meet the sequencing requirements for specific LCD panels.

Short-circuit protection is provided for all outputs. The boost switch is protected against overcurrent and overvoltage. Input disconnect protection is achieved by driving an external P-MOSFET.

28-pin exposed thermal pad TSSOP package allows operation at high ambient temperatures. It is lead (Pb) free with 100% matte-tin leadframe plating.

System Block Diagram



Selection Guide

Part Number	Packing*	Programming
A8601KLPTR-T	4000 pieces per 13-in. reel	Contact Allegro Sales for VCOM regulator factory trim option

*Contact Allegro™ for additional packing options.

Absolute Maximum Ratings[1,2]

Characteristic	Symbol	Notes	Rating	Unit
VIN and INS Pin Voltage	V_{VIN}, V_{INS}	All voltages measured with respect to GND	–0.3 to 6.5	V
SW Pin Voltage[3,4]	V_{SW}	Continuous	–0.6 to 22	V
		Voltage spikes (pulse width < 100 ns)	–1 to 40	V
OUT Pin Voltage	V_{OUT}		–0.3 to 22	V
AVDD and FB2 Pin Voltage	V_{AVDD}, V_{FB2}		–0.3 to V_{OUT} + 0.3	V
CP11 Pin Voltage	V_{CP11}	Positive charge pump	–0.3 to V_{CP12} + 0.3	V
CP12 Pin Voltage	V_{CP12}	Positive charge pump	–0.3 to 27	V
VGH Pin Voltage	V_{VGH}	Positive charge pump	–0.3 to 27	V
FB4 Pin Voltage	V_{FB4}	Positive charge pump	–0.3 to V_{VGH} + 0.3	V
CP21 Pin Voltage	V_{CP21}	Negative charge pump	–0.3 to 14	V
CP22, VGL and FB3 Pin Voltage	V_{CP22}, V_{VGL}, V_{FB3}	Negative charge pump	–14 to 0.3	V
EN1, EN2, and $\overline{\text{FAULT}}$ Pin Voltage	V_{EN1}, V_{EN2}, V_{FAULT}		–0.3 to 5.5	V
BIAS Pin Voltage	V_{BIAS}		–0.3 to lower of: 5.5 or V_{VIN} + 0.3	V
VCOM Pin Voltage	V_{VCOM}		–0.3 to lower of: 7 or V_{AVDD} + 0.3	V
PGND and GNDVCOM Pin Voltage	V_{PGND}, $V_{GNDVCOM}$		–0.3 to 0.3	V
All other pins[5]	–		–0.3 to 7	V
Operating Ambient Temperature	T_A	K temperature range	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.
[2] All voltages referenced to AGND.
[3] The SW pin has internal clamp diodes to GND. Applications that forward bias this diode should take care not to exceed the IC package power dissipation limits. Note: Exact energy specification to be determined.
[4] The switch DMOS is self-protected. If voltage spikes exceeding 40 V are applied, the device would conduct and absorb the energy safely.
[5] When V_{VIN} = 0 (no power), all inputs are limited by –0.3 to 5.5 V.

Thermal Characteristics: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	28	°C/W

*Additional thermal information available on the Allegro website.

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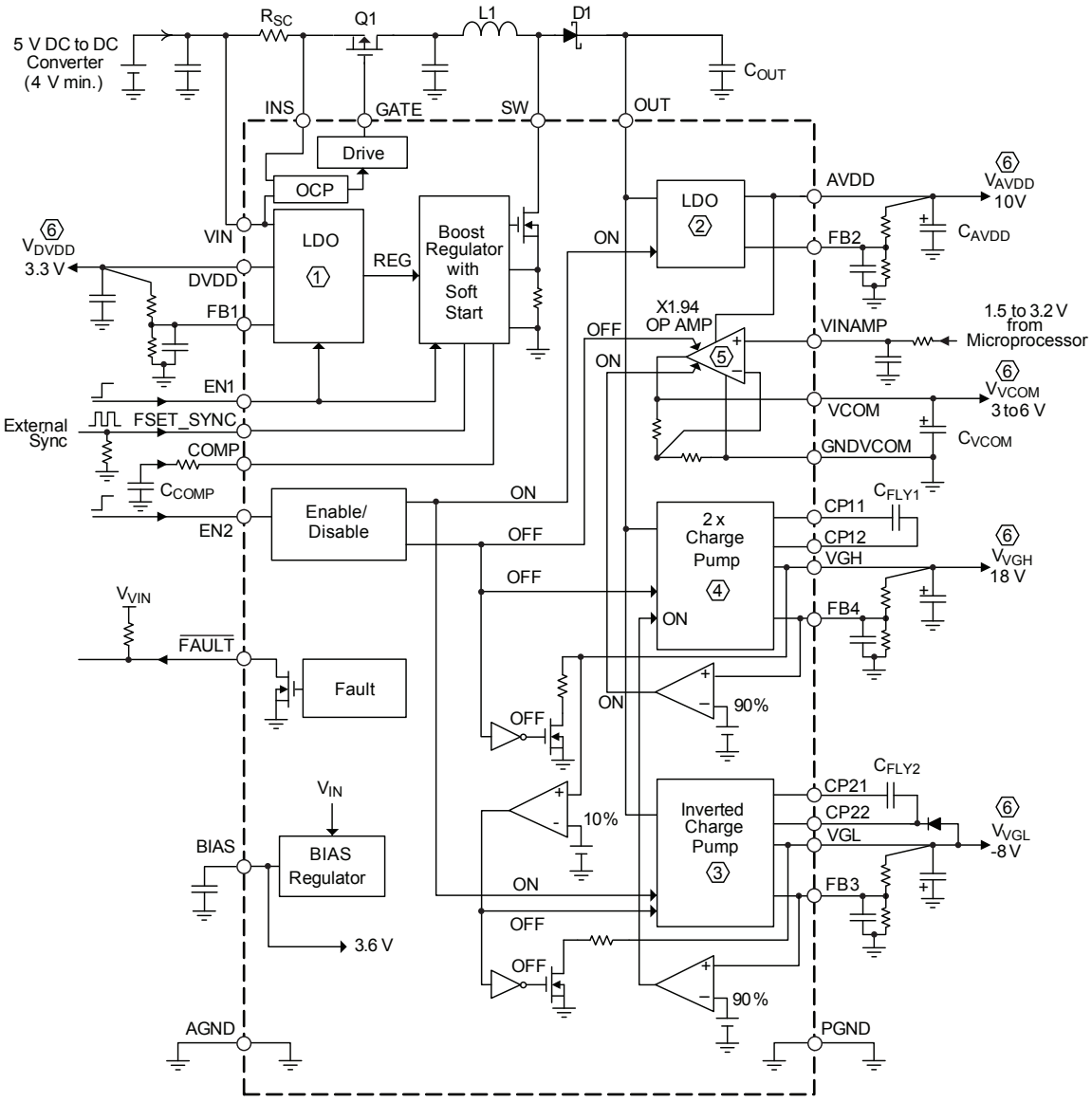
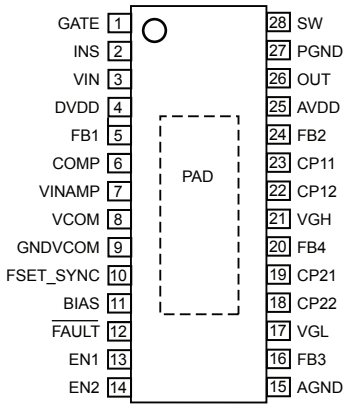
Functional Block Diagram



1 to 5 See Terminal List Table

6 Output voltages shown are for a typical LCD panel

Pin-Out Diagram



Terminal List Table

Number	Name	Function
1	GATE	Gate driver for input disconnect P-MOSFET
2	INS	High-side sense for input overcurrent detection
3	VIN	Input supply voltage (4.0 to 5.5 V) for the IC
4	DVDD	Output from internal LDO (item 1 in Functional Block Diagram) powered by VIN
5	FB1 (DVDD)	Connect to resistor divider network to set DVDD
6	COMP	Compensation pin, connect to external COMP capacitor
7	VINAMP	Control voltage from external microprocessor
8	VCOM	Output from operational amplifier (item 5 in Functional Block Diagram), controlled by VINAMP
9	GNDVCOM	Ground reference for VCOM
10	FSET_SYNC	Input for synchronizing boost and charge pump signals switching frequency to external clock signal; alternatively, it can be connected to an external resistor to set the switching frequency
11	BIAS	Output from internal 3.6 V bias regulator; connect to GND via 0.1 µF ceramic capacitor
12	$\overline{\text{FAULT}}$	Open-drain output, pulls low in error condition
13	EN1	Enable pin for DVDD output; system can only be enabled after V_{VIN} is above UVLO level (refer to Startup Timing Diagram)
14	EN2	Enable pin for the voltage outputs other than DVDD; it can be activated only after V_{VIN} is above UVLO and EN1 = high.
15	AGND	Analog GND reference for signals; connect to ground plane
16	FB3 (VGL)	Connect to resistor divider network to set V_{VGL}
17	VGL	Inverted charge pump output (item 3 in Functional Block Diagram)
18	CP22	Capacitor terminal for inverted charge pump (item 3 in Functional Block Diagram); refer to Negative Charge Pump section for usage
19	CP21	Capacitor terminal for inverted charge pump (item 3 in Functional Block Diagram)
20	FB4 (VGH)	Connect to resistor divider network to set V_{VGH}
21	VGH	2× charge pump (item 4 in Functional Block Diagram) output
22	CP12	Capacitor terminals for charge pump (item 4 in Functional Block Diagram)
23	CP11	
24	FB2 (AVDD)	Connect to external resistor network to set V_{AVDD}
25	AVDD	Output from internal LDO (item 2 in Functional Block Diagram) powered by V_{OUT}
26	OUT	Connect to boost output for internal LDO and charge pump regulators
27	PGND	Power ground for internal boost switch; connect this pin to ground terminal of output ceramic capacitor(s)
28	SW	Boost converter switch node
–	PAD	Exposed pad (substrate of IC); solder to GND plane for better thermal conduction

ELECTRICAL CHARACTERISTICS[1]: Valid at V_{VIN} = 5 V, EN1 = EN2 = high, f_{SW} = 2 MHz, V_{DVDD} = 3.3 V, V_{AVDD} = 10 V, V_{VGH} = 20 V, V_{VGL} = –8 V, T_J = T_A = 25°C, except • indicates specifications guaranteed for T_J = T_A = −40°C to 125°C, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Input Voltage and Current							
Input Voltage	V_{VIN}		•	4.0	–	5.5	V
VIN Pin Undervoltage Lockout (UVLO) Threshold	V_{UVLO}	V_{VIN} rising	•	3.6	–	4.0	V
VIN Pin UVLO Hysteresis	$V_{UVLO(HYS)}$			–	0.15	0.25	V
Shutdown Bias Current	$I_{VINBIAS(SD)}$	Current into VIN pin, EN1 = low	•	–	5	50	µA
Standby Bias Current	$I_{VINBIAS(STB)}$	EN1 = high, EN2 = low, no load at DVDD pin		–	2	–	mA
Operating Bias Current	$I_{VINBIAS(OP)}$	EN1 = high, EN2 = high		–	6.5	–	mA
Boost Switch							
Switch Peak Current Limit	$I_{SW(MAX)}$	Cycle-by-cycle current limit	•	1.3	–	2.0	A
Switch On-Resistance	$R_{DS(on)}$	I_{SW} = 0.5 A		–	0.5	–	Ω
Switch Minimum On-Time	$t_{ON(MIN)}$			50	72	95	ns
Switch Minimum Off-Time	$t_{OFF(MIN)}$			33	50	75	ns
SW Pin Leakage Current	$I_{SW(LKG)}$	V_{SW} = 5 V, EN1 = low		–	0.1	–	µA
OUT Pin Leakage Current	$I_{OUT(LKG)}$	V_{OUT} = 5 V, EN1 = low		–	0.1	–	µA
SW Pin Secondary Overvoltage Protection (OVP)	$V_{SW(OVP)}$		•	17.4	19.2	21.2	V
SW Pin Secondary OVP Minimum Pulse Width[4]	$t_{SW(OVP)}$	V_{SW} ≥ OVP level		–	40	–	ns
Switching Frequency / Synchronization							
FSET_SYNC Pin Voltage	$V_{FSETSYNC}$	Without using external synchronization signal		–	1.0	–	V
FSET_SYNC Pin Current	$I_{FSETSYNC}$			34	–	220	µA
Switching Frequency	f_{SW}	R_{FSET_SYNC} = 5.1 kΩ	•	1.81	2.0	2.17	MHz
Synchronization Frequency	f_{SYNC}	External logic signal connected to FSET_SYNC pin	•	0.35	–	2.25	MHz
Synchronization Minimum On-Time	$t_{SYNC(ON)}$		•	150	–	–	ns
Synchronization Minimum Off-Time	$t_{SYNC(OFF)}$		•	150	–	–	ns
Input Disconnect							
GATE Pin Sink Current	$I_{GATE(SNK)}$	V_{GATE} = V_{VIN}, no fault		–	100	–	µA
GATE Pin Source Current	$I_{GATE(SRC)}$	V_{GATE} = 0 V, fault tripped		–	130	–	mA
GATE Voltage at Off Condition	$V_{GATE(OFF)}$	EN1 = EN2 = low, or fault tripped		–	V_{VIN}	–	V
INS Trip Point	$V_{INS(TRIP)}$	Between VIN and INS pins	•	85	100	115	mV
INS Trip Blanking Time	$t_{INS(BLANK)}$	Sensed voltage = 2 × input current limit		1.5	–	3	µs

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ELECTRICAL CHARACTERISTICS[1] (continued): Valid at V_{VIN} = 5 V, EN1 = EN2 = high, f_{SW} = 2 MHz, V_{DVDD} = 3.3 V, V_{AVDD} = 10 V, V_{VGH} = 20 V, V_{VGL} = –8 V, T_J = T_A = 25°C, except • indicates specifications guaranteed for T_J = T_A = −40°C to 125°C, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Feedback Pins							
Feedback Sense Voltage	V_{FBx}	FB1, FB2, and FB4 pins		–	2.40	–	V
		FB3 pin		–	–1.8	–	V
Output Overvoltage Fault Threshold	$V_{FBx(OV)}$	FB1, FB2, and FB4 pins; V_{FBx} rising		–	2.88	–	V
		V_{FB3} falling		–	–2.16	–	V
Output Undervoltage Fault Threshold	$V_{FBx(UV)}$	FB1, FB2, and FB4 pins; V_{FBx} falling		–	1.92	–	V
		V_{FB3} rising		–	–1.44	–	V
Feedback Input Currents	I_{FBx}	FB1, FB2, and FB4 pins; V_{FBx} = 2.4 V		–	–0.5	–	µA
		V_{FB3} = –1.8 V		–	0.5	–	µA
Feedback Load Resistance[2]	R_{FBx}	FB1 pin		9	10	11	kΩ
		FB2 pin		24	25	26	kΩ
		FB3 and FB4 pins		47.5	50	52.5	kΩ
Output Regulators							
DVDD Output Voltage	V_{DVDD}	V_{VIN} = 4.0 to 5.5 V	•	2.4	–	V_{VIN} – 0.6	V
AVDD Output Voltage	V_{AVDD}	V_{VIN} = 4.0 to 5.5 V	•	4.4	–	14.8	V
VCOM Output Voltage	V_{VCOM}	V_{VIN} = 4.0 to 5.5 V, V_{AVDD} > V_{VCOM} + 1.5 V	•	2.9	–	6.8	V
VGH Output Voltage	V_{VGH}	V_{VIN} = 4.0 to 5.5 V	•	2.4	–	26	V
VGL Output Voltage	V_{VGL}	V_{VIN} = 4.0 to 5.5 V	•	–12.9	–	–5	V
Dropout for DVDD Regulator	$V_{DVDD(DO)}$	Between VIN and DVDD pins; V_{FB1} = 2.33 V, I_{OUT} = 50 mA	•	–	–	0.6	V
Boost Minimum Headroom for AVDD Regulator	$V_{AVDD(DO)}$	Defined as V_{OUT} – V_{AVDD}; V_{FB2} = 2.33 V, I_{OUT} = 100 mA		–	2	–	V
Boost Minimum Headroom for VGH Regulator	$V_{VGH(DO)}$	Defined as V_{OUT} – V_{VGH} / 2; V_{FB4} = 2.33 V, I_{OUT} = 8 mA		–	2.4	–	V
Boost Minimum Headroom for VGL Regulator	$V_{VGL(DO)}$	Defined as V_{OUT} – (–V_{VGL}); V_{FB3} = –1.75 V, I_{OUT} = –8 mA		–	3.6	–	V
Output Pull-Down Resistor During Shutdown (AVDD, VCOM, VGH, VGL)	R_{OUTPD}	EN1 = high, EN2 = low		–	250	–	Ω
Logic Inputs							
Input Logic High	V_{IH}	EN1, EN2, FSET_SYNC pins	•	1.8	–	–	V
Input Logic Low	V_{IL}	EN1, EN2, FSET_SYNC pins	•	–	–	0.8	V
Internal Pull-Down Resistance to AGND	$R_{ENx(PD)}$	EN1, EN2 pins		–	100	–	kΩ

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ELECTRICAL CHARACTERISTICS[1] (continued): Valid at V_{VIN} = 5 V, EN1 = EN2 = high, f_{SW} = 2 MHz, V_{DVDD} = 3.3 V, V_{AVDD} = 10 V, V_{VGH} = 20 V, V_{VGL} = –8 V, T_J = T_A = 25°C, except • indicates specifications guaranteed for T_J = T_A = −40°C to 125°C, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Output Current Capacity							
DVDD Overcurrent Protection (OCP) Trip Level	$I_{DVDD(OCP)}$			50	–	90	mA
AVDD OCP Trip Level	$I_{AVDD(OCP)}$	Includes i_{VCOM}		200	–	350	mA
VCOM OCP Trip Level	i_{VCOM}			60	–	110	mA
VGH OCP Trip Level	i_{VGH}			14	–	32	mA
VGL OCP Trip Level	i_{VGL}	Current into VGL pin		14	–	32	mA
Output Voltage Accuracy							
DVDD Load Regulation	$V_{DVDDreg}$	V_{DVDD} = 3.3 V, I_{LOAD} = 10 to 50 mA	•	–0.1	–	0.1	V
AVDD, VGL and VGH Load Regulation	V_{xreg}	I_{LOAD} = 10% to 100% of $I_{x(OCP)}$(min)	•	–0.1	–	0.1	V
DVDD Accuracy[3]	err_{DVDD}	V_{DVDD} = 3.30 V	•	–2.5	–	2.5	%
AVDD Accuracy[3]	err_{AVDD}	V_{AVDD} = 10.0 V	•	–2.1	–	2.1	%
VGH Accuracy[3]	err_{VGH}	V_{VGH} = 20.0 V	•	–2.5	–	2.5	%
VGL Accuracy[3]	err_{VGL}	V_{VGL} = –8.0 V	•	–2.5	–	2.5	%
VCOM Operational Amplifier							
VCOM Gain[4]	A_{VCOM}	Defined as V_{VCOM} / V_{VINAMP} ; 1.5 V < V_{VINAMP} < 3.21 V, –30°C < T_A < 85°C, I_{LOAD} = 25 mA	•	1.92	1.94	1.96	V/V
VCOM Load Regulation[4]	$V_{VCOMreg}$	I_{LOAD} = 5 to 50 mA	•	–5	–	5	mV
VCOM Temperature Coefficient[4]	TC_{VCOM}	–30°C < T_A < 85°C, I_{LOAD} = 25 mA	•	–50	–	50	µV/°C
Input Resistance to AGND	$R_{VINAMP(PD)}$	VINAMP pin		–	100	–	kΩ
Dropout for VCOM from AVDD	$V_{VCOM(DO)}$	V_{AVDD} = 7 V, I_{VCOM} = 60 mA		–	–	1.5	V
$\overline{\text{FAULT}}$ Pin							
$\overline{\text{FAULT}}$ Pull-Down Voltage	$V_{FAULT(PD)}$	Fault condition asserted, pull-up current = 1 mA		–	–	0.4	V
$\overline{\text{FAULT}}$ Pin Leakage Current	$I_{FAULT(LKG)}$	Fault condition cleared, pull-up to 5 V		–	–	1	µA

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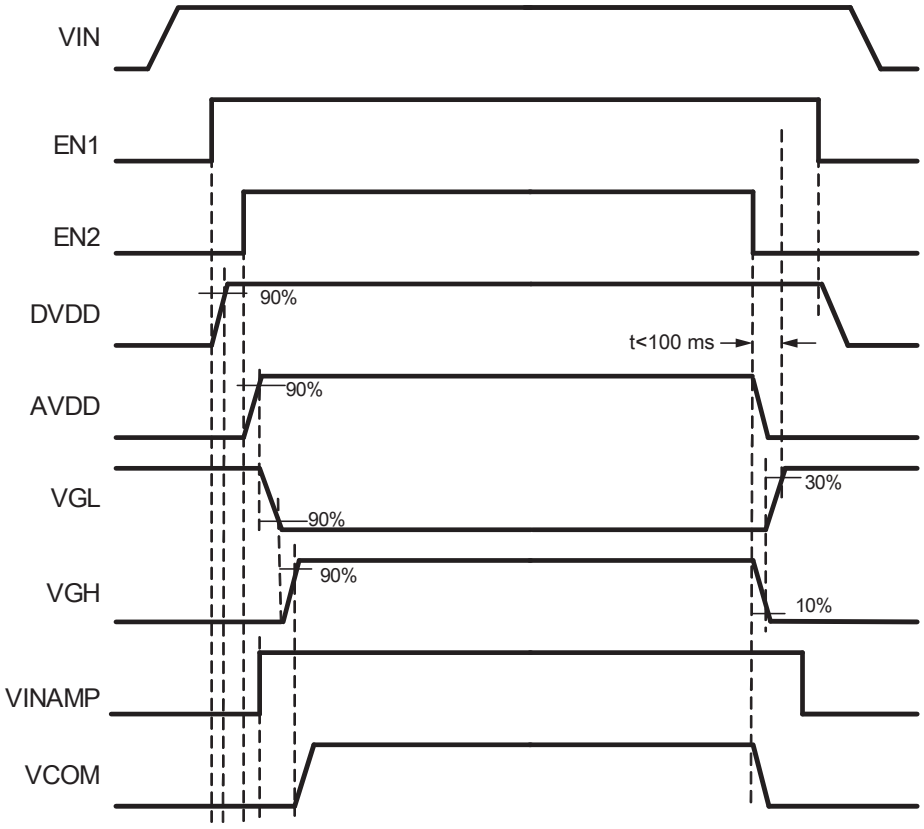
ELECTRICAL CHARACTERISTICS[1] (continued): Valid at V_{VIN} = 5 V, EN1 = EN2 = high, f_{SW} = 2 MHz, V_{DVDD} = 3.3 V, V_{AVDD} = 10 V, V_{VGH} = 20 V, V_{VGL} = –8 V, $T_J = T_A$ = 25°C, except • indicates specifications guaranteed for $T_J = T_A$ = −40°C to 125°C, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Fault Timers							
Soft-Start Time-Out	$t_{SS(TO)}$	Maximum time allowed for any output to reach 90% of its target		40	50	60	ms
Shutdown Time-Out	$t_{SDN(TO)}$	Maximum time allowed for VGH to fall to 10% and VGL to 30% of their respective targets; EN1 = high, EN2 = low		40	50	60	ms
Overcurrent Protection (OCP) Time-Out	$t_{OCP(TO)}$	Maximum time allowed for any output to stay in an overcurrent fault condition before shutdown		40	50	60	ms
Restart Delay	$t_{RESTART}$	Delay time after fault shutdown until the next retry (repeats until Fault counter = 8)		80	100	120	ms
Fault Counter Reset Time	t_{fault}	Time required after setting EN1 = low until Fault counter clears		1	–	–	µs
Thermal Shutdown (TSD) Protection							
TSD Threshold	T_{TSD}	Temperature rising		–	165	–	°C
TSD Hysteresis[4]	$T_{TSD(HYS)}$			–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Net parallel resistance required at FBx pin in order to meet accuracy.
[3] Output voltage is set to required nominal value using external sense resistor network. Output current at 50% of minimum OCP trip level. Accuracy does not include mismatch error caused by external sense resistor network.
[4] Ensured by design and characterization, not production tested.

Characteristic Performance

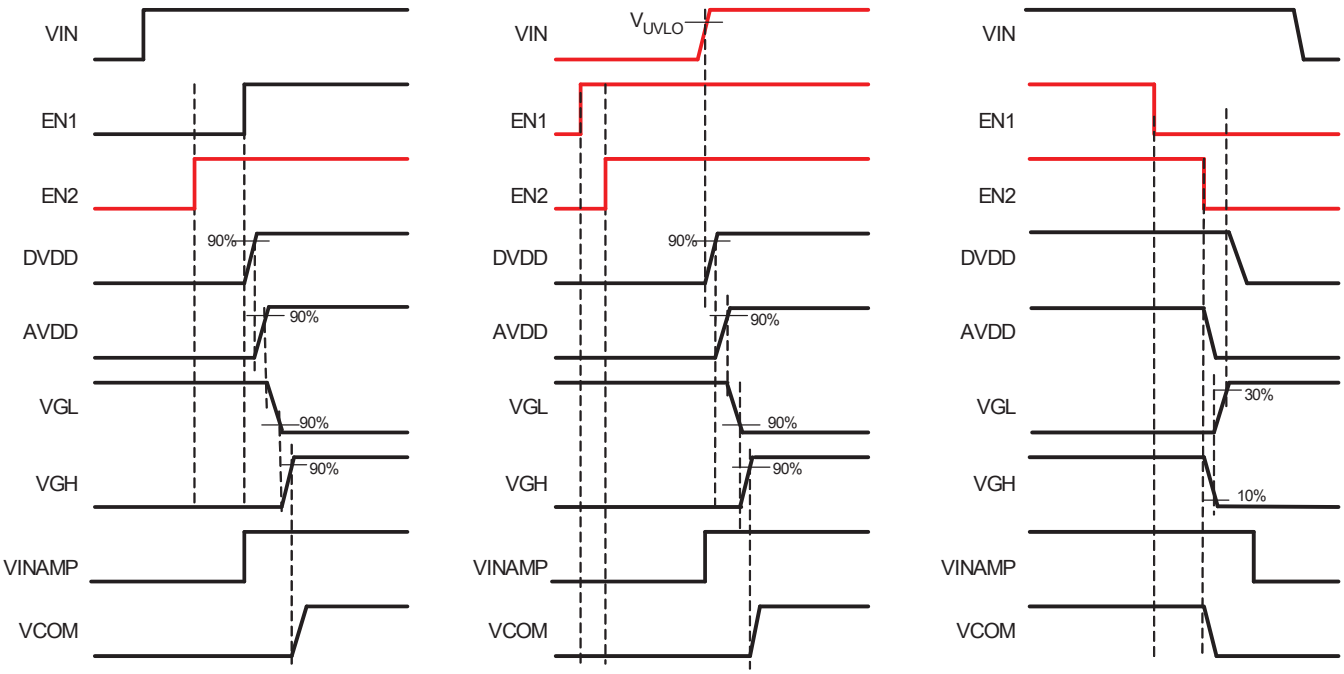
Startup and Shutdown Sequences (Normal Operation)



Notes:

- Normal system startup should follow the above sequence (VIN →EN1 →EN2).
- EN1 can only be asserted after VIN is above UVLO level, V_{UVLO}. If asserted before that, it is ignored until VIN rises above V_{UVLO}.
- EN2 can only be asserted when DVDD is >90% target voltage. If asserted before that, it is ignored until the condition is met.
- VGH is enabled only after the magnitude of VGL has reached >90% of its target voltage.
- VCOM output is enabled only after VGH has reached >90% of its target voltage. (A valid VINAMP must be asserted prior to this.)
- System shutdown should start with EN2 = low, followed by EN1 = low.
- VGL shutdown can only start after VGH has dropped to 10% its original target voltage, or the VGH shutdown time-out interval has expired.
- EN1 = low can only be asserted when VGL has fallen below 30% of its target voltage. If asserted before that, it is ignored until the condition is met or the VGL shutdown time-out interval has expired.

Startup and Shutdown Sequences (Irregular)

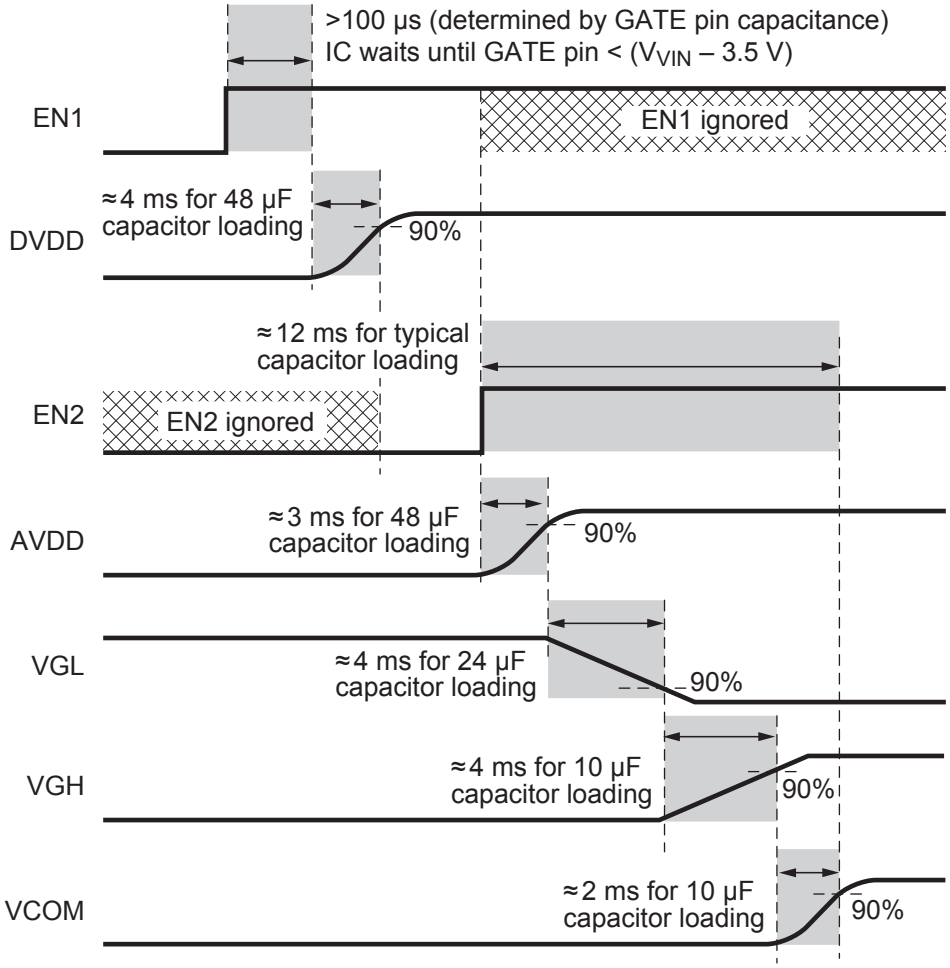


Case 1 (startup) Case 2 (startup) Case 3 (shutdown)

Notes:

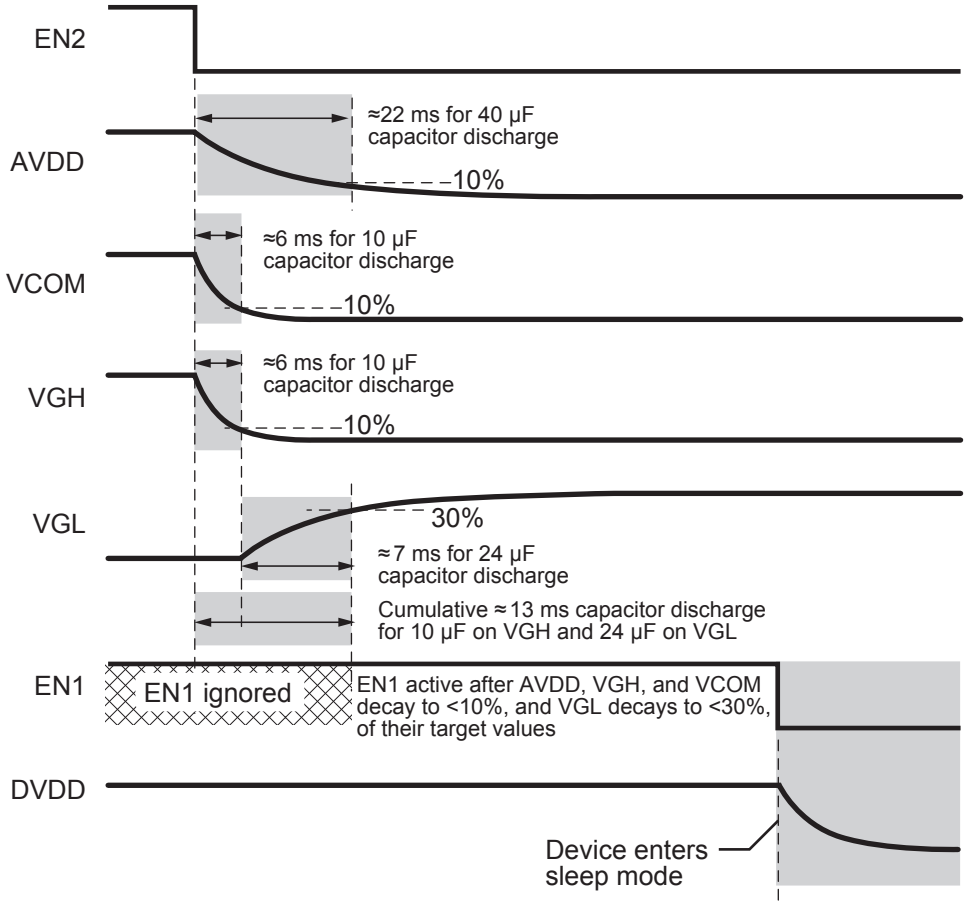
- Case 1 (startup). During a startup sequence, if EN2 goes high before EN1 goes high, EN2 is ignored until EN1 also goes high and DVDD has risen to 90% of its target voltage.
- Case 2 (startup). During a startup sequence, while VIN is below the UVLO level, V_{UVLO}, the IC is in sleep mode. If either EN1 or EN2 goes high while the IC is still in sleep mode, they are ignored until VIN exceeds V_{UVLO}.
- Case 3 (shutdown). During a shutdown sequence, if EN1 goes low before EN2 goes low, EN1 is ignored until EN2 also goes low and VGL has fallen to 30% of its target voltage, or the VGL shutdown time-out interval has expired.

Startup Timing Diagram



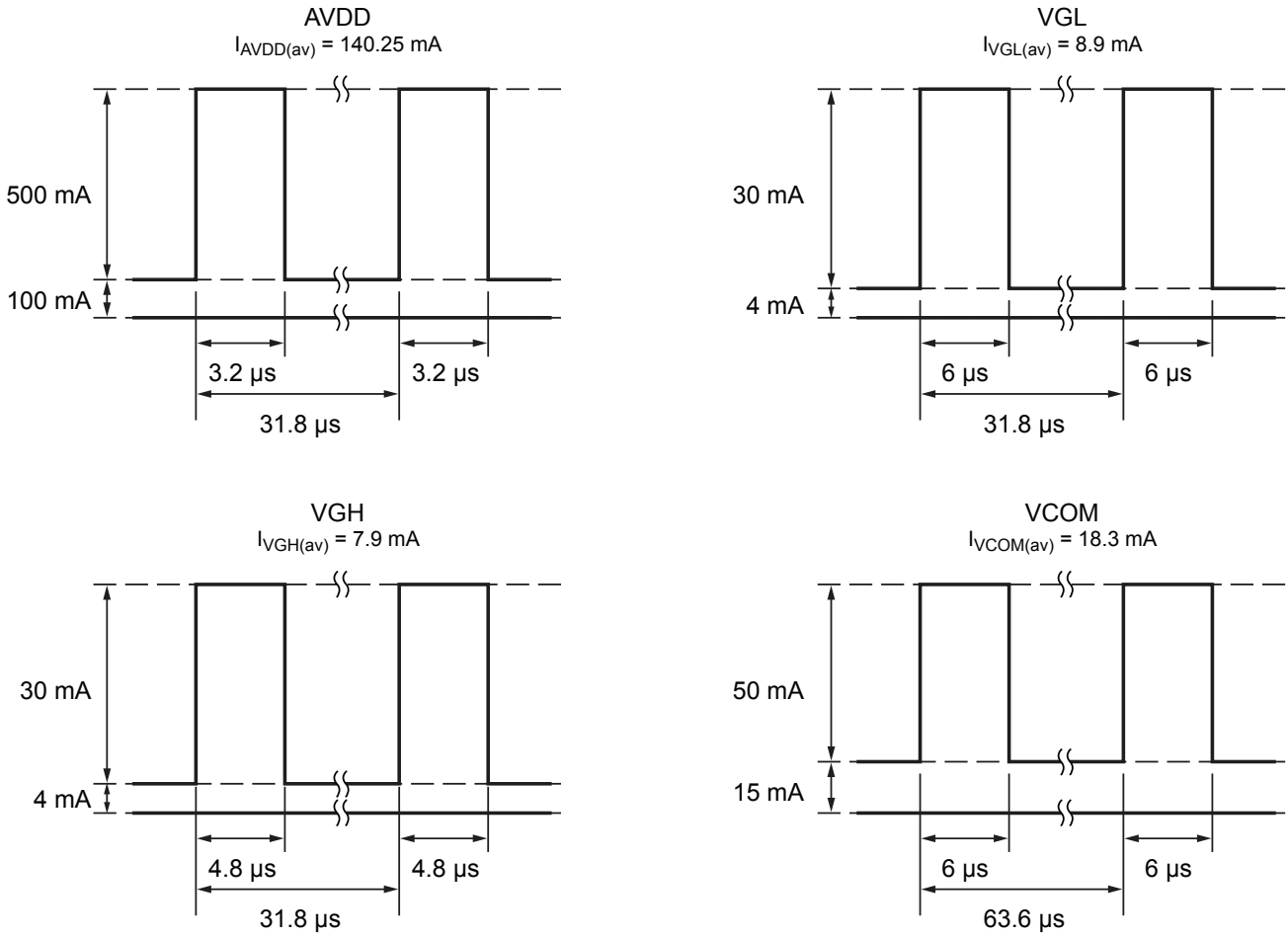
Notes:
- Startup ramps are based on internal timing and are assumed to have ± 20% variation.
- An internal pull-down resistor of 250 Ω is applied to each of the regulator outputs AVDD, VGL, VGH, and VCOM as soon as EN1 = high. That means if any output capacitor was previously charged, it would be discharged by this pull-down resistor. The pull-down is removed just before each regulator is enabled.

Shutdown Timing Diagram



Notes:
- All exponential decays are based on external capacitance and internal pull-down resistance (250 Ω each for AVDD, VCOM, VGH, and VGL). The external DC load is assumed to be off or negligible.
- If any of the outputs AVDD, VCOM, or VGH does not decay to below 10% of target voltage after 50 ms, starting from EN2 is low, it is by-passed and the rest of the shutdown sequence continues without it.
- For VGL, the shutdown detection threshold is set at 30%. Only if the magnitude of VGL has dropped below 30%, when EN1 goes low the IC will shut down completely. After shutdown, all internal pull-down resistors are released, and output capacitor voltages will decay according to external load resistances.

Typical Load Current during Normal Operation



Functional Description

The A8601 is a flexible multi-voltage regulator designed for LCD panel bias applications. It utilizes a high-efficiency boost converter, together with space-saving low-dropout regulator and charge pump circuits to provide five independently adjustable voltage outputs:

- DVDD: Typically 3.3 V. Nominal output current 20 mA, maximum 100 mA. This output is from a low-dropout regulator (item 1 in the Functional Block Diagram) powered by VIN. It is available while EN1 is high.
- AVDD: Typically between 5 and 13.3 V. Nominal current 100 mA. This output is from a low-dropout regulator (item 2 in the Functional Block Diagram) powered by VOUT. It is only available when both EN1 and EN2 are high.
- VCOM: Typically between 3 and 6 V at 50 mA. This voltage is programmable by applying a control voltage at the VINAMP pin (1.5 to 3.2 V from the application microprocessor). The power supply of this regulator is internally connected to AVDD.
- VGL: Typically between –11 and –5.4 V at 4 mA. This voltage is generated by an inverted charge pump, which is powered by VOUT.
- VGH: Typically between 14.5 and 24.6 V at 4 mA. This voltage is generated by a 2× charge pump, which is powered by VOUT.

Linear Regulators

The A8601 uses low-dropout linear regulators (LDO) to provide DVDD from VIN, and AVDD from boost output voltage. A representative block diagram is shown in figure 1. Each LDO is protected against output short or overloading by its own internal OCP limits. Refer to the Fault Conditions section for details.

The AVDD circuit monitors the voltage drop across its LDO (item 2 in the Functional Block Diagram). If this voltage drop is less than 2 V, the AVDD circuit sends a control signal to cause the boost voltage to increase. This ensures there is always enough headroom for regulation.

VCOM Regulator

The VCOM output voltage is determined by the input voltage of VINAMP (see figure 2), according to the following relation:

$$V_{VCOM} = V_{VINAMP} \times 1.94 \quad (1)$$

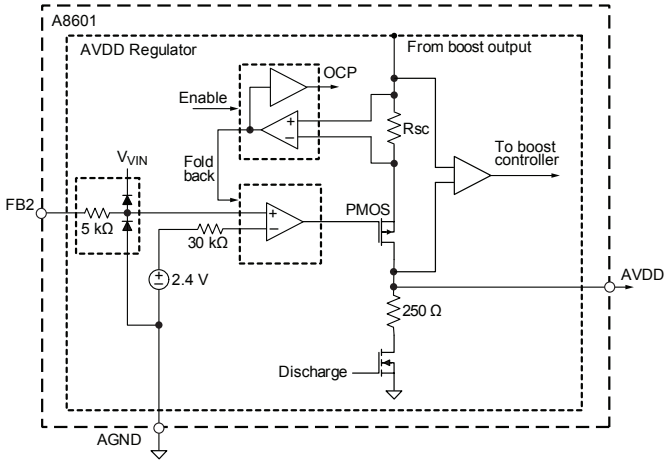


Figure 1. Representative linear regulator (AVDD shown)

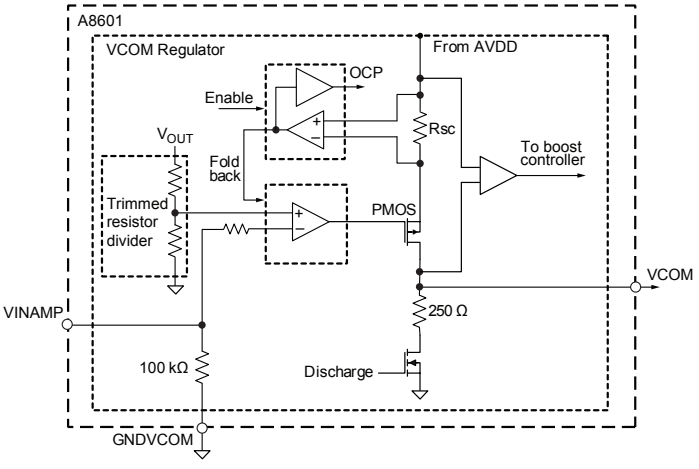


Figure 2. VCOM regulator

The valid range for VINAMP is between 1.5 and 3.2 V, which gives a V_{VCOM} range of 2.9 to 6.2 V (provided that AVDD is at least 1.5 V higher than V_{VCOM}). Beyond this range, the linearity of VCOM cannot be guaranteed.

The supply voltage of VCOM is taken from AVDD. In order to ensure there is enough headroom, AVDD must be at least 1.5 V higher than VCOM.

During the startup sequence, VCOM is allowed to ramp up only after VGH has reached 90% of its target voltage. A valid VINAMP must be asserted prior to VCOM ramp up. If VINAMP starts low (< 1.2 V), the A8601 waits as long as 50 ms for a valid VINAMP to be asserted. If VINAMP is not asserted by that time limit, a fault is generated.

If VCOM is not required, the VCOM pin can be left open, but a small output capacitor (approximately 0.1 µF) must be present to prevent oscillation. Make sure to connect VINAMP to a suitable voltage such as DVDD at 3.3 V. The connection to DVDD can be divided as shown in figure 3, according to the AVDD level required.

Charge Pumps

The A8601 uses a 2× charge pump to generate VGH from boost voltage, and an inverting charge pump to generate VGL. Representative block diagrams are shown in figure 4.

The frequency of the charge pumps is the same as the boost switching frequency (or external SYNC frequency)

When an external SYNC signal is used, it is internally converted into a clock signal with the same frequency, but at 50% duty cycle.

Recommended values of the external flying capacitor, C_{FLYx}, on

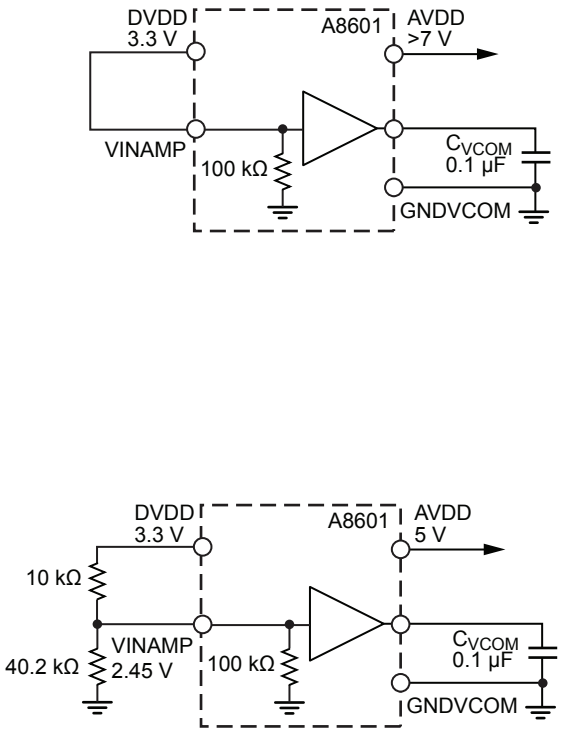


Figure 3. Configuration for unused VCOM: (upper panel) V_{AVDD} > 7 V, and (lower panel) V_{AVDD} = 5 V.

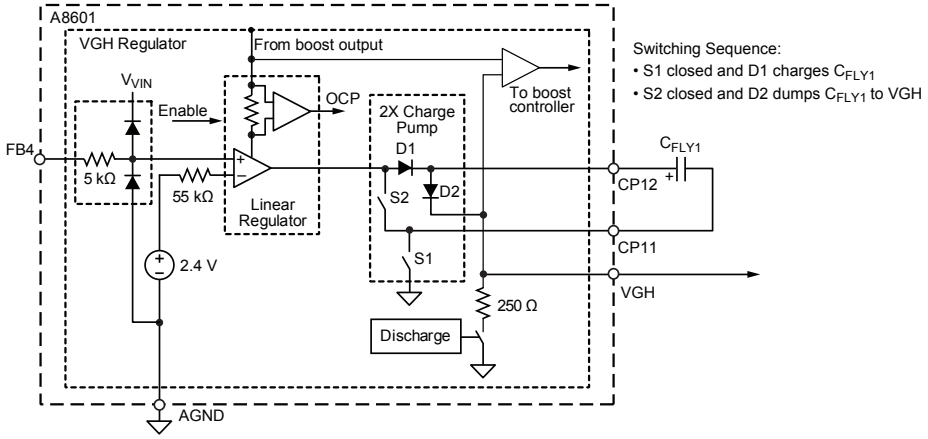


Figure 4A. 2× charge pump for VGH regulator

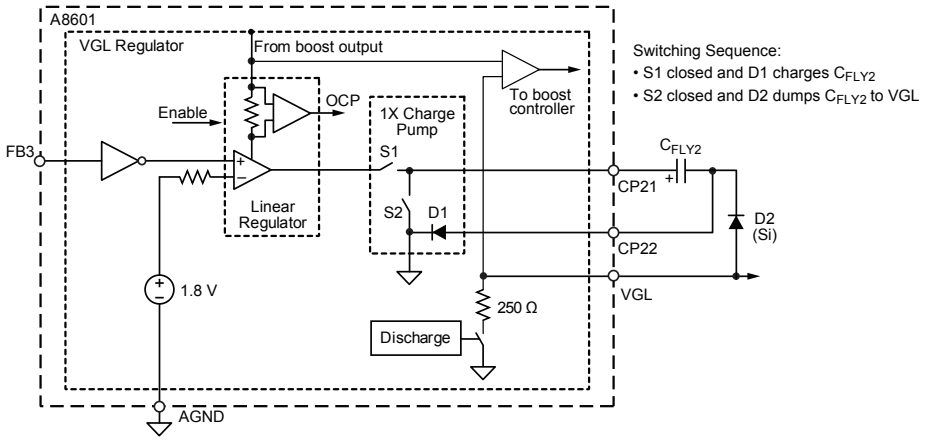


Figure 4B. Inverting (negative) charge pump for VGL regulator

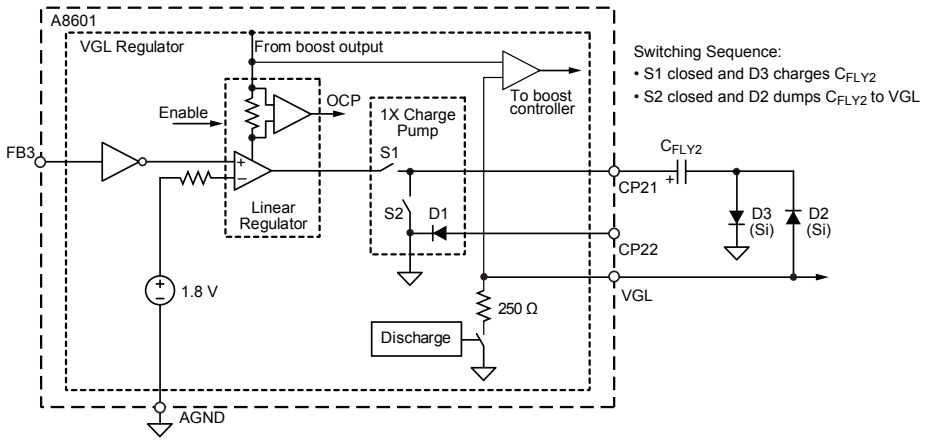


Figure 4C. Inverting (negative) charge pump for VGL regulator, full output current (14 mA)

the CPxx pins depends on the switching frequency as shown in the following table; a voltage rating of 25 V is sufficient:

Switching Frequency (MHz)	C_{FLYx} (µF)
2	≈0.1
1	0.22
0.350	0.47

For the inverted (negative) charge pump, an external silicon diode is used between the VGL and CP22 pins. However, at high temperatures and switching frequencies (such as 125°C and 2 MHz), the maximum VGL output current is limited to about 8 mA. To achieve the full output current, 14 mA, it is necessary to use two external diodes, as shown in figure 4C.

The value of the flying capacitor can be calculates as follows:

1. The equivalent series resistance of the flying capacitor is:

$$ESR_{FLY2} = 1/(f_{SW} \times C_{FLY2}) \quad (2)$$

2. Assuming a flying capacitor ripple voltage of 100 mV, and a maximum output current of 20 mA, the series resistance is:

$$R_{FLY2} = 0.1\ (V) / 0.02\ (A) \leq 5\ \Omega$$

3. Therefore at an f_{SW} of 2 MHz, the required capacitance, C_{FLY2}, is 0.1 µF.

Boost Controller

The A8601 contains an integrated DMOS switch and PWM controller to drive a boost converter. The input voltage, V_{VIN}, (5 V nominal) is boosted to an intermediate voltage, V_{OUT}, which is the lowest voltage required to keep all outputs within regulation. That is, the effective boost voltage is the highest of the boost requirement of the individual regulators, as illustrated in figure 5.

For example: assume the output requirements for a certain LCD panel are: V_{AVDD} = 10 V, V_{VGH} = 18.5 V and V_{VGL} = –7 V, then:

• AVDD (LDO 2): $V_{OUT} \geq V_{AVDD} + 2\ (V) = 12\ V$

• VGH (2× Charge Pump): $V_{OUT} \geq 0.5 \times V_{VGH} + 2.4\ (V) = 11.65\ V$

• VGL (Inverted Charge Pump): $V_{OUT} \geq -V_{VGL} + 3.6\ (V) = 10.6\ V$

In this example, AVDD has the highest requirement, so the intermediate voltage will be regulated at a V_{OUT} of 12 V approximately. However, if V_{VGH} were increased to 23 V, it would be the highest, and then the boost converter would increase the intermediate voltage to 13.9 V to satisfy the charge pump circuit.

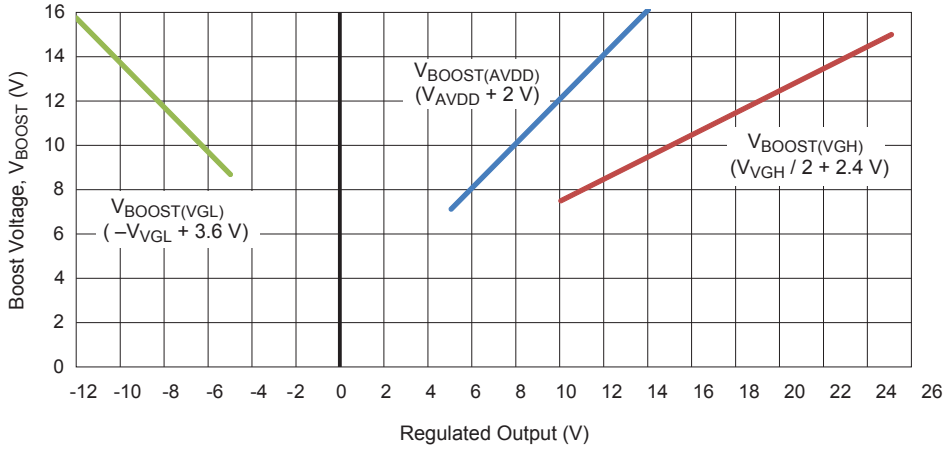


Figure 5. Boost voltage requirement with respect to VGL, AVDD, and VGH

A block diagram of the A8601 boost controller circuit is shown in figure 6. The external COMP capacitor, C_{COMP}, is typically a 0.1 to 1 µF MLCC.

The controller is protected against overvoltage and overcurrent fault conditions.

- The OVP threshold, $V_{SW(OVP)}$, is internally set at approximately 19 V typical. Under normal operating conditions, the boost voltage should always be lower than 16 V (as shown in figure 5), so only in the event of a fault will OVP be tripped (for example: output diode open, or wrong sense resistor values).
- The switching current limit, $I_{SW(MAX)}$, is protected by a pulse-by-pulse OCP threshold (1.5 A typical). In the event of a heavy load or during a transient, the SW peak current may reach OCP level momentarily. In this case, the present on-time period is terminated immediately, but no signal is generated on the $\overline{\text{FAULT}}$ pin.
- In the event of a catastrophic failure (such as shorted inductor), the SW current may exceed 150% of the OCP threshold. In this case, the IC is shut down immediately.

Switching Frequency

The boost stage switching frequency, f_{SW}, of the A8601 can be programmed by using an external resistor between the FSET_SYNC pin to GND, or it can be synchronized to an external clock frequency between 350 kHz and 2.25 MHz.

During startup, the A8601 senses the FSET_SYNC pin for any external SYNC signal. If periodic logic transitions are detected (Low < 0.8 V or High > 1.8 V), this is evaluated as an external clock signal, and the boost switching frequency is synchronized to it. If no periodic signal is detected, the bias current flowing through FSET_SYNC pin is used to determine the switching frequency. The bias current is set by an external resistor, R_{FSET}, on the FSET_SYNC pin. The relation between R_{FSET} and switching frequency is given as:

$$R_{FSET} = 10.21 / (f_{SW} - 0.0025) \quad (3)$$

where R_{FSET} is in kΩ and f_{SW} is in MHz.

This relationship is charted in figure 7. For example, to get a switching frequency of 2 MHz requires an R_{FSET} of 5.11 kΩ.

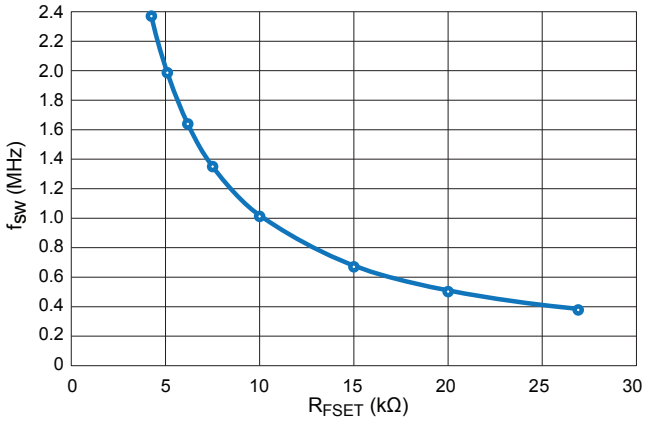


Figure 7. Switching frequency versus FSET resistance

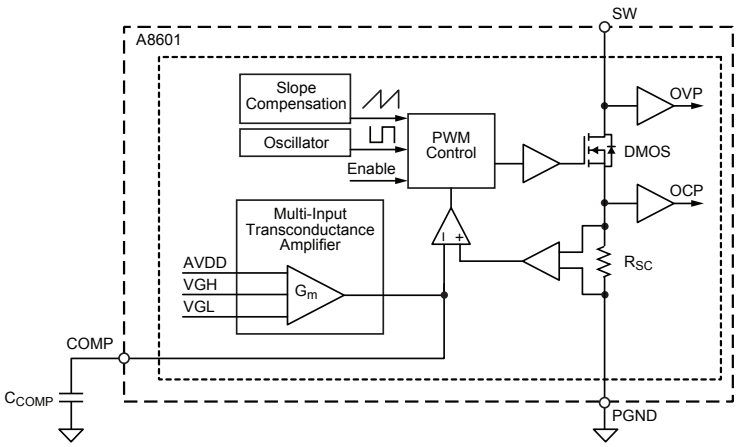


Figure 6. Boost controller circuit

Suppose the A8601 is started up with a valid external SYNC signal, but the SYNC signal is lost during normal operation. In that case, one of the following happens:

- If the external SYNC signal is high impedance (open), the A8601 continues normal operation, at the switching frequency set by R_{FSET}. No $\overline{FAULT}$ flag is generated.
- If the external SYNC signal is low (shorted to ground), the A8601 begins a shutdown sequence, at the switching frequency set by the internal 1 MHz oscillator. The $\overline{FAULT}$ pin is pulled low and the internal error counter is increased by 1.

  Note: If the outcome of the second scenario is not acceptable, the circuit shown in figure 8 can be used to prevent generating a fault when the external SYNC signal goes low. When the circuit is used, after the external SYNC signal goes low, the A8601 will continue to operate normally at the switching frequency set by R_{FSET}. No $\overline{FAULT}$ flag is generated.

Continuous Conduction Mode Operation

It is often preferable for a boost converter to operate in continuous conduction mode (CCM) in order to reduce switching noise and input ripple. However, whether the converter can operate in CCM or discontinuous conduction mode (DCM) is determined by many parameters, including input/output voltages, output current, switching frequency, and inductor value. This is explained as follows, using simplified basic equations for a boost converter (refer to figure 9):

During SW on-time, t_{ON}:

$$i_{ripple} = V_{VIN} / L \times t_{ON} \quad (4)$$

$$= V_{VIN} / L \times T \times D \quad (5)$$

where T is the switching period of the boost converter and D is the duty cycle, t_{ON} / T.

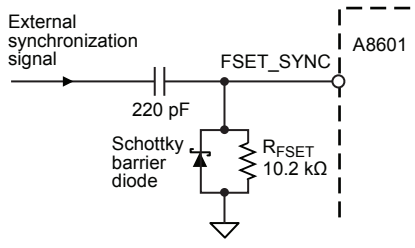


Figure 8. Low FSET_SYNC signal fault counteraction circuit

During SW off-time, t_{OFF}:

$$i_{ripple} = (V_{OUT} + V_{D1} - V_{VIN}) / L \times t_{OFF} \quad (5)$$

$$= (V_{OUT} + V_{D1} - V_{VIN}) / L \times T \times (1 - D) \quad (7)$$

therefore:

$$V_{OUT} + V_{D1} = V_{VIN} \times 1 / (1 - D) \quad (8)$$

In order to operate in CCM, the minimum inductor current must be greater than zero amperes. This means:

$$i_{SW}(min) = i_{SW}(av) - i_{ripple} / 2 \geq 0, \text{ or} \quad (9)$$

$$i_{ripple} \leq 2 \times i_{SW}(av)$$

Average input current is directly related to the input power and voltage, as given by:

$$i_{SW}(av) = P_{VIN} / V_{VIN} = (P_{OUT} / \eta) / V_{VIN} \quad (10)$$

where η is the efficiency of the boost converter (typically around 80%). Ripple current is determined by inductance, period, and duty cycle, as given by:

$$i_{ripple} = V_{VIN} / L \times T \times D \quad (11)$$

where D is $1 - V_{VIN} / (V_{OUT} + V_{D1})$ from equation 8.

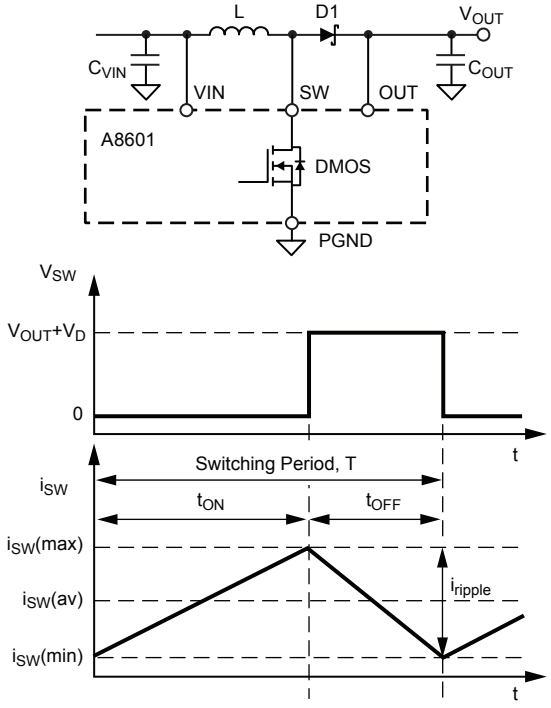


Figure 9. Continuous and discontinuous conduction mode factors

For a given V_{VIN} and V_{OUT}, the duty cycle is fixed. Furthermore, for a given output power, the average input current also is fixed. Therefore the only way to reduce ripple current is either to switch at a higher frequency (a shorter period) or to use a larger inductance.

Figure 10 shows that the minimum inductance required to ensure CCM operation increases with higher output voltage (hence also with higher duty cycle), for a boost regulator with fixed input voltage and output power. Note that the chart is calculated at an f_{SW} of 1 MHz. If the frequency is reduced by half, to 500 kHz, the inductance requirement is doubled.

When selecting the boost inductor, pay attention to the following parameters:

- Inductance. This usually determines whether the boost converter operates in DCM or CCM. Refer to figure 10, or calculate minimum required inductance using the equations provided.
- DCR. Lower resistance is preferred to reduce conduction loss.
- Saturation current. I_{SAT} should be greater than 1.5 A, and preferably 2 A.
- Heating current. $I_{HEATING}$ should be greater than 1.5 A_{RMS}
- Physical size. Smaller size typically means lower I_{SAT} and higher DCR.

The minimum SW on-time and off-time determine the range of duty cycle, and hence the range of boost output voltage. They do not affect whether the converter operates in CCM or DCM.

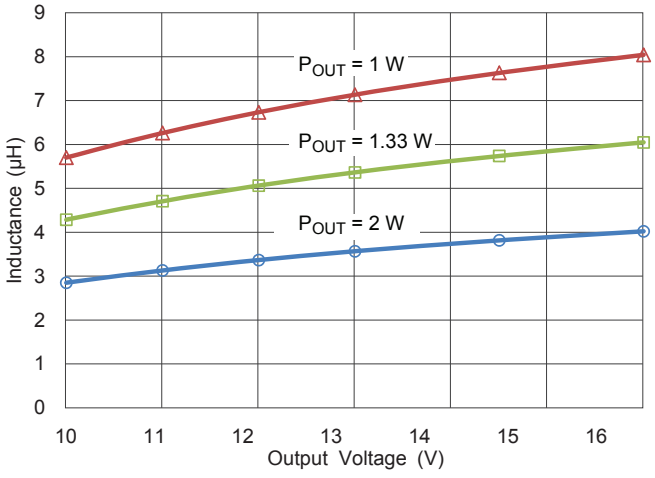


Figure 10. Minimum inductance for CCM as a function of output voltage (at V_{VIN} = 5.5 V and f_{SW} = 1 MHz)

For example, assume f_{SW} is 2 MHz (T = 500 ns), $t_{ON(MIN)}$ is 95 ns, and $t_{OFF(MIN)}$ is 75 ns. Then:

$$D(\min) = t_{ON(MIN)} / T = 95\ (\text{ns}) / 500\ (\text{ns}) = 19\%$$

$$D(\max) = 1 - t_{OFF(MIN)} / T = 1 - 75\ (\text{ns}) / 500\ (\text{ns}) = 85\%$$

Further, assume V_{VIN} is 4.0 to 5.5 V and V_{D1} is 0.4 V. Then the possible V_{OUT} is between 6.4 and 20.7 V. This is wider than the range required by individual regulators under all possible output combinations. Therefore the minimum on-time and off-time are not limiting factors in output regulation.

$$V_{OUT}(\min) = V_{VIN}(\max) \times 1/(1 - D(\min)) - V_{D1} = 6.4\ \text{V}$$

$$V_{OUT}(\max) = V_{VIN}(\min) \times 1/(1 - D(\max)) - V_{D1} = 26.7\ \text{V}$$

Input Disconnect Switch

The A8601 has a gate driver for an external PMOS, in order to provide input disconnect protection function (figure11). During normal startup, the PMOS is turned on gradually to avoid a large inrush current. In the event there is a direct short at the boost stage (either SW or OUT shorted to GND), a high input current would cause the PMOS to turn off. See the Fault Conditions section for details.

The input disconnect current threshold is calculated by:

$$I_{VIN(MAX)} = V_{INS(TH)} / R_{INS} \qquad (12)$$

where $V_{INS(TH)}$ = 100 mV typical.

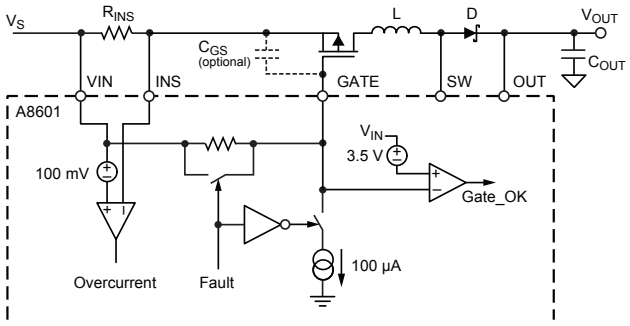


Figure 11. Input disconnect switch circuit

Under normal operation, the input current is protected by the cycle-by-cycle boost switch current limit, $I_{SW(MAX)}$, 1.5 A (typ). Only in the event of a direct short at the boost output (SW pin) will the input disconnect switch be activated. Therefore the input disconnect current threshold should be set slightly higher than the switch current limit; for example, choose an R_{INS} of 0.047 Ω to set an $I_{VIN(MAX)}$ of 2 A approximately.

During a normal power-up sequence, as soon as EN1 reaches high, the A8601 begins pulling the GATE pin low by a 100 µA current. How quickly the external PMOS turns on depends on the gate capacitance C_{GS}. If the gate capacitance is very low, the inrush current may momentarily exceed 2 A and trip the input disconnect protection. In this case, an external C_{GS} capacitor may be added to slow down the PMOS turn-on. A typical value of 4.7 nF should be sufficient in most cases.

When selecting the external PMOS, check the following parameters:

- Drain-source breakdown voltage, $V_{(BR)VDSS}$, should exceed –20 V
- Gate threshold voltage should be fully conducting at V_{GS} = –4 V, and cut-off at –1 V
- $R_{DS(on)}$ is rated at V_{GS} = –4.5 V or similar, not at –10 V; derate for higher temperatures

FAULT Conditions

The A8601 has extensive fault detection mechanisms, to protect against all perceivable faults at the IC level (pin open, pin short to GND, pin short to neighboring pins, and so forth) and at the system level (external component open/short, component value changes from –50% to +100%, and so forth).

All feedback pins (FB1, FB2, FB3, and FB4) are monitored for overvoltage and undervoltage faults during normal operation.

In case of an output short, or an open/short in the sense resistor network, the magnitude of the sensed voltage may make a sudden change that is either +20% over, or –20% under the target voltage. This will trigger the OVP/UVP fault and force the A8601 to shut down.

OVP/UVP detections are disabled during the startup sequence. If any output fails to reach 90% of its target voltage within a time-out period, $t_{SS(TO)}$ (50 ms typical), a fault is generated and then the A8601 shuts down.

Each regulator output (DVDD, AVDD, VGH, VGL and VCOM) is protected by its own independent overcurrent limit. When an output current exceeds its limit, the corresponding regulator goes into overcurrent protection mode to protect itself from damage. See figure 11 for illustrations of the protection characteristics.

If the overcurrent condition persists for 50 ms, all regulators are turned off following the normal shutdown sequence. The same applies when there is an overvoltage fault detected at any of the feedback pins, except that the offending regulator is turned off immediately. The other outputs then shut down following normal sequence.

In general, if a fault is detected, the A8601 halts operation and pulls the $\overline{\text{FAULT}}$ pin low. It then attempts to restart operation after a delay, $t_{RESTART}$, of 100 ms typical. Internally there is a Fault counter that keeps track of how many times any fault has occurred. If the Fault counter reaches eight, the A8601 is completely shut down. The Fault counter is cleared by a completed shutdown sequence with EN1 = EN2 = low, or by a power reset (V_{VIN} drops below UVLO). During startup, all regulators go through a soft-start process, to prevent excessive inrush current from tripping OCP. The same applies to the turn-on of the external input disconnect PMOS.

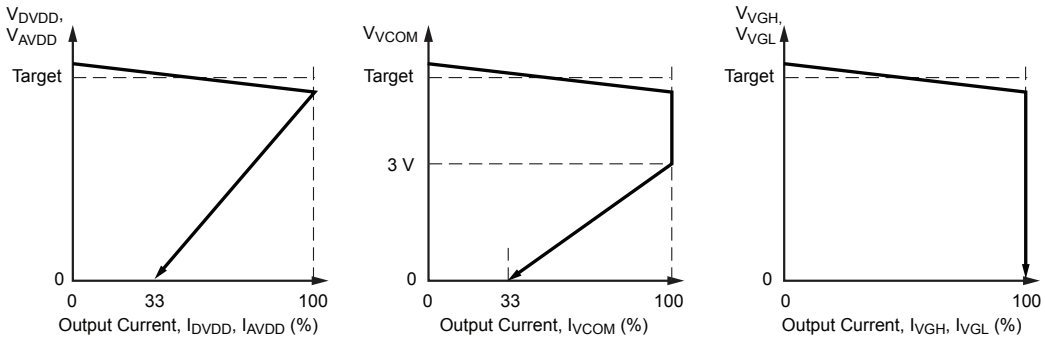


Figure 11. Overcurrent protection characteristics for DVDD, AVDD, VCOM, VGH, and VGL

Pre-Output Fault Detection

When EN1 turns on the A8601, a startup sequence is followed before the regulators are powered up. The sequence checks for extreme conditions and proceeds as described in table 1.

General Fault Detection

The faults described in table 2 are continuously monitored, whether during startup, normal operation, or shutdown.

Table 1. Pre-Output Fault Detection Sequence

Step Number	Step Description	Fault Description	Fault Tripped?
1	Check VIN UVLO	A8601 remains powered-down until V_{VIN} is above V_{UVLO}.	No
2	Power-up internal rail	A8601 initializes.	No
3	Check internal rail UVLO	BIAS charges internal rail indefinitely, until V_{BIAS} is above UVLO.	No
4	Check all FBx pins for short to GND	Any FBx pin is detected as shorted after $t_{SS(TO)}$.	Yes
5	Turn on DVDD	FB1 pin does not reach >90% of target (2.4 V) after $t_{SS(TO)}$.	Yes
	Turn on input disconnect	Pull-down on GATE pin does not reach < V_{VIN} – 3.5 V after $t_{SS(TO)}$.	Yes
6	Turn on SW and AVDD if EN2 = H	FB2 pin does not reach >90% of target (2.4 V) after $t_{SS(TO)}$.	Yes
7	Turn on VGL	FB3 pin does not reach >90% of target (–1.8 V) after $t_{SS(TO)}$.	Yes
8	Turn on VGH	FB4 pin does not reach >90% of target (2.4 V) after $t_{SS(TO)}$.	Yes
9	Turn on VCOM	VCOM pin does not reach >90% of target ($V_{VINAMP} \times A_{VCOM}$) after $t_{SS(TO)}$.	Yes

Table 2. General Fault Detection

Fault Description	A8601 Response to Fault	Fault Tripped?
T_{TSD} exceeded	Shutdown immediately, without using shutdown sequence. Fault counter increased by one, retry after $t_{RESTART}$, and temperature has dropped by $T_{TSD(HYS)}$.	Yes; $\overline{FAULT}$ set during $t_{RESTART}$
V_{FB1}, V_{FB2}, V_{FB3}, or V_{FB4} 20% under target	Shutdown using shutdown sequence. Fault counter increased by one, retry after $t_{RESTART}$.	Yes; $\overline{FAULT}$ set during $t_{RESTART}$
V_{FB1}, V_{FB2}, V_{FB3}, or V_{FB4} 20% over target	Over-target regulator rail shut down without shutdown sequence. Other regulator rails shut down using shutdown sequence. Fault counter increased by one, retry after $t_{RESTART}$.	Yes; $\overline{FAULT}$ set during $t_{RESTART}$
V_{UVLO} reached	Shutdown without using shutdown sequence. Fault counter reset to 0, retry after $t_{RESTART}$.	No
BIAS UVLO	Shutdown without using shutdown sequence. Fault counter reset to 0, retry after $t_{RESTART}$.	No
Overcurrent limit for i_{DVDD}, i_{AVDD}, i_{VCOM}, i_{VGH}, or i_{VGL} exceeded	Over-limit regulator rail goes into current fold-back or current limit. Shutdown using shutdown sequence after $t_{OCP(TO)}$. Fault counter increased by one, retry after $t_{RESTART}$.	Yes; $\overline{FAULT}$ set during $t_{RESTART}$
$V_{INS(TRIP)}$ exceeded	Shutdown without using shutdown sequence. Fault counter increased by one, retry after $t_{RESTART}$.	Yes; $\overline{FAULT}$ set during $t_{RESTART}$
$V_{SW(OVP)}$ exceeded	Shutdown without using shutdown sequence. Fault counter increased by one, retry after $t_{RESTART}$.	Yes; $\overline{FAULT}$ set during $t_{RESTART}$
$I_{SW(MAX)} \times 150\%$ of OCP limit exceeded	Shutdown without using shutdown sequence. Fault counter increased by one, retry after $t_{RESTART}$.	Yes; $\overline{FAULT}$ set during $t_{RESTART}$

Application Information

Output Voltage Selection

Each output voltage of DVDD, AVDD, VGH, or VGL is selected using a simple voltage-sensing (resistor divider) network, as shown in figure 12.

In actual implementation there is a small bias current that is flowing out from each positive FBx pin, and the direction is reversed for any negative FBx pin. This is necessary to detect any pin-open fault at an FBx pin. As shown in figure 13, a common bias current is injected into both the (+) and the (–) terminals of the operational-amplifier. Due to the principal of superposition, the same set of equations as in figure 1 can be used to determine values for R1 and R2 in figure 13.

V_{FB} is the regulation voltage for the feedback pins, and it is specified as 2.40 V for FB1 (DVDD), FB2 (AVDD), and FB4 (VGH). For FB3 it is specified as –1.80 V. The following considerations affect voltage selection:

- To cancel the offset error introduced by input bias currents, and to assure regulation loop stability, it is necessary to keep the external equivalent resistance, that is, the parallel resistance of R1 and R2, as follows:

Pin	Parallel Resistance (kΩ)
FB1 (DVDD)	10 ± 1
FB2 (AVDD)	25 ± 1
FB3 (VGL)	50 ± 2.5
FB4 (VGH)	50 ± 2.5

- To reduce the mismatch error of the sensing network, consider using 0.5% or 0.2% resistors for the resistor divider.
- To reduce effects of switching noises coupled into the FBx pins, add an external filter capacitor (typically a 47 pF MLCC) between the FBx pin and GND. The capacitor should be placed as close as possible to the respective FBx pin.

Table 3 provides some examples of voltage sensing network component values, using E96 1% resistors.

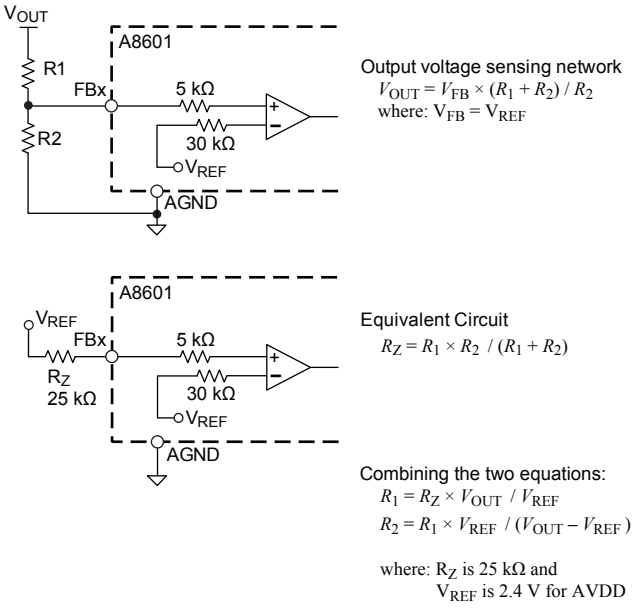


Figure 12. The output voltage sensing network and the equivalent circuit

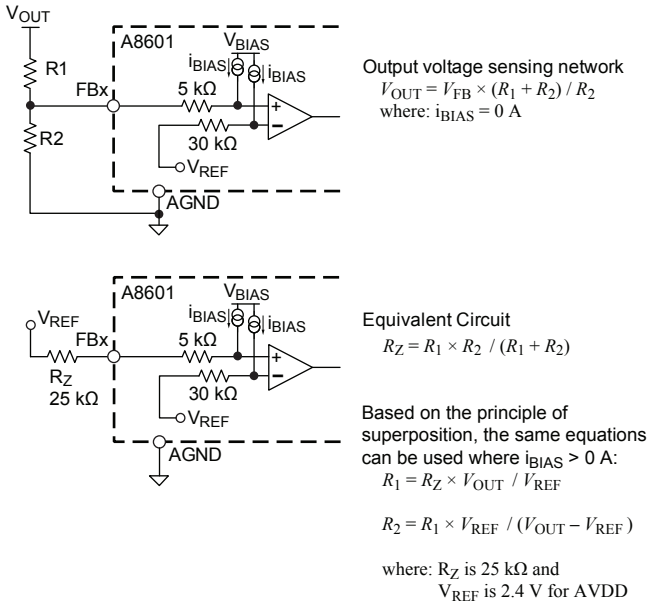


Figure 13. The figure 12 circuits with the same bias current injected into both inputs of the operational amplifier

Output Capacitance

The boost stage requires an output capacitor, C_{OUT}. Use an MLCC with a capacitance of approximately 4.7 to 10 µF and a voltage rating of 25 V. The temperature rating should be either X5R or X7R. Do not use Y5V, which has a very large variation with temperature. Another point to note is the capacitance of MLCC is specified at a 0 V bias. To account for the degradation when the rated DC voltage is applied to an MLCC, the capacitance should be derated by as much as 50%. The derating factor is typically less if the capacitor is physically larger (for example, choose a 1206 package instead of an 0805) and has a higher voltage rating (for example, 50 V instead of 25 V).

To ensure system stability, each output (DVDD, AVDD, VGL, VGH, and VCOM) is required to have an external MLCC with a minimum output capacitance of 2 ±0.1 µF. However, greater capacitance may be required to satisfy transient current requirements. This is illustrated in figure 14. The AVDD load current makes a step from 100 mA (steady state current) to 500 mA, for a duration of 3.2 µs only. Because the linear regulator for AVDD takes a finite time to respond to this load change, the voltage dip is determined primarily by the output capacitance, C_{AVDD}.

The corresponding voltage step, dV1, is determined by the ESR of the output capacitor. When using an MLCC with very low ESR (several mΩ), this drop is only several mV and can be omitted.

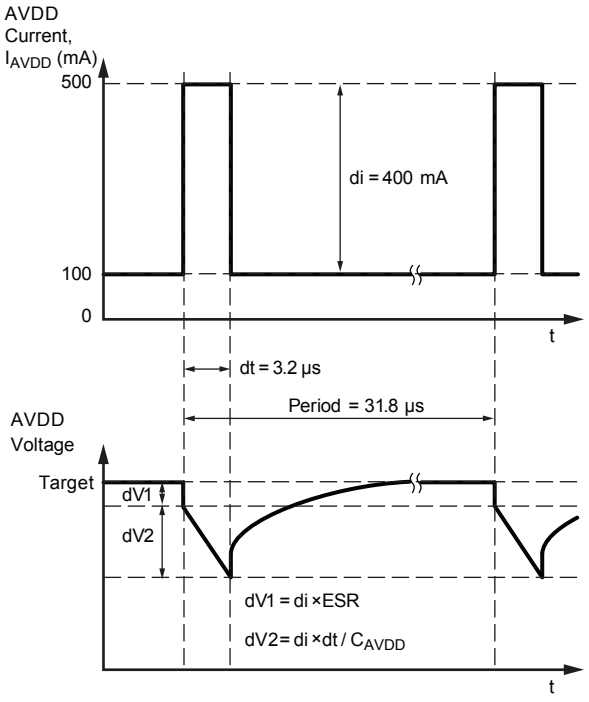


Figure 14. AVDD output voltage transient caused by a step change in load current

Table 3. Examples of Sensing Network Component Values

Output [Pin]	V_{FBx} (V)	Goal Output Values		Calculated Resistor Divider Values		Actual Resistor Divider Values		Calculated Output Values		
		R_Z (kΩ)	V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	R_1 (kΩ)	R_2 (kΩ)	R_Z (kΩ)	V_{OUT} (V)	V_{OUT} Resistor Divider Error (%)
DVDD [FB1]	2.4	10	3.3	13.75	36.67	13.7	36.5	9.96	3.3	0.02
AVDD [FB2]	2.4	25	7	72.92	38.04	73.2	38.3	25.14	6.99	–0.19
			12.8	133.33	30.77	133	30.9	25.07	12.73	–0.55
VGH [FB4]	2.4	50	14.5	302.08	59.92	300	59	49.3	14.6	0.71
			24.6	512.5	55.41	511	54.9	49.57	24.74	0.56
VGL [FB3]	–1.8	50	–5.4	150	75	150	75	50	–5.4	0.00
			–11	305.56	59.78	309	60.4	50.52	–11.01	0.08

Note: Use of series E96 1% resistors assumed.

The second voltage step, dV2, is determined by the output capacitance. For example, assume C_{AVDD} = 20 µF, then:

$$dV2 = 0.4\ (A) \times 3.2\ (\mu s) / 20\ (\mu F) = 64\ mV$$

Operating with Separate VIN and Boost Supplies

If necessary, the A8601 can be powered by a 5 V LDO for VIN, while the boost stage can be powered by a different supply such as 3.3 V. This is illustrated in figure 15.

The LDO for VIN should have an output voltage of 5 V ±10%. The LDO supply current is the sum of the A8601 bias current (approximately 6 mA at 2 MHz) and the DVDD output current.

The boost supply voltage is independent from the VIN voltage. A reasonable range for the boost supply is between 3.3 and 10 V. The boost supply current is determined by the output power of boost stage, as outlined in the Thermal Analysis section.

The boost output voltage, V_{OUT}, is always higher than its input, V_{BOOSTS}. Therefore it is necessary to keep the boost supply voltage below a certain level. This can be determined for a boost converter as follows:

$$V_{OUT} = V_{BOOSTS} / (1 - D) \quad (13)$$

where D is the duty cycle.

Assume a boost PWM frequency of 2 MHz (period = 500 ns). The A8601 minimum on-time, $t_{ON(MIN)}$, is 95 ns worst-case. That results in a minimum PWM duty cycle of 19%.

For a V_{BOOSTS} of 12 V, and a D of 0.19, the calculated V_{OUT} would be 14.8 V. This is higher than the 14 V required by the A8601 output regulators in figure 15. Higher V_{OUT} levels result in excessive power loss and may trigger OVP at the SW pin.

Thermal Analysis

The thermal resistance, $R_{\theta JA}$, of the TSSOP-28 thermally enhanced package is 28°C/W. For long term reliability, the package junction temperature should be kept at 150°C or below. Assuming a maximum ambient temperature of 85°C, the power dissipation budget, P_D(max), is:

$$P_D(max) = (T_J(max) - T_A(max)) / R_{\theta JA} \quad (14)$$
$$= (150\ (°C) - 85\ (°C)) / 28\ (°C/W) = 2.3\ W$$

The power losses of the IC come from two main contributors, the boost stage and the linear regulators. These losses are calculated separately, then summed, as follows.

To estimate the dissipation of the boost stage, calculate and sum the losses due to switching losses, P_{SW}, and conduction losses in the switch, P_{COND}:

$$P_{D(BOOST)} = P_{COND} + P_{SW} \quad (15)$$

1. Estimate the maximum output power for boost stage:

$$P_{OUT}(max) = V_{OUT}(max) \times I_{OUT}(max) \quad (16)$$

$$I_{OUT} = I_{AVDD} + I_{VCOM} + I_{VGL} + 2 \times I_{VGH} \quad (17)$$

Based on the average load current waveforms during normal operation (see Characteristic Performance section), the average output current for the boost stage is estimated to be:

$$I_{OUT} = 140\,(mA) + 18.3\,(mA) + 8.9\,(mA) + (2 \times 7.9\,(mA))$$
$$\approx 183\,mA$$

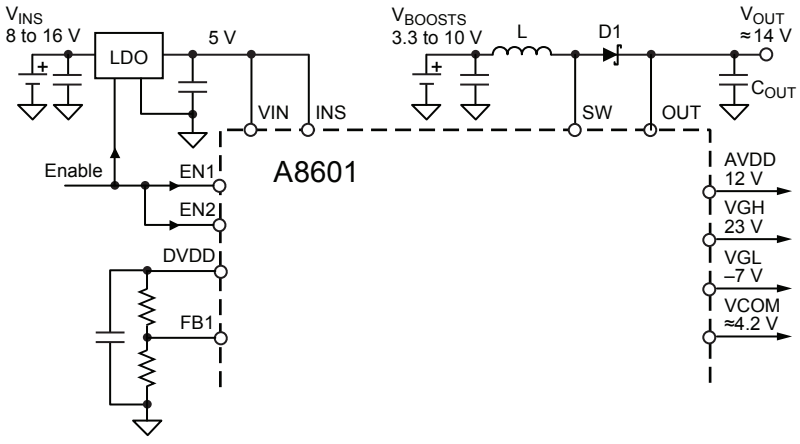


Figure 15. Typical dual supply application

So at a maximum V_{OUT} of 16 V, the maximum P_{OUT} is:

$$P_{OUT}(max) = 16(V) \times 0.183\ (A) = 3\ W$$

2. Estimate the maximum input current:

$$I_{VIN} = P_{VIN} / V_{VIN} \quad (18)$$

$$P_{VIN} = P_{OUT} / \eta \quad (19)$$

where η is efficiency (%). Substituting into equation 10:

$$I_{VIN} = (3\ (W) / 0.85) / 4\ (V) = 0.88\ A.$$

3. Estimate conduction loss for the internal switch:

$$P_{COND} = I^2_{VIN} \times R_{DS(on)} \times D \quad (20)$$

$$D = 1 - V_{VIN} / (V_{OUT} + V_{D1}) \quad (21)$$

where V_{D1} is the forward voltage drop of the external boost diode. Subsituting into equation 20:

$$P_{COND} = (0.88\ (A))^2 \times 0.7\ (\Omega) \times [1 - 4\ (V) / (16(V) + 0.4\ (V))]$$
$$= 0.78 \times 0.7 \times 0.756 = 0.41\ W$$

where $R_{DS(on)}$ is 0.5 Ω typical, plus 40% of typical for temperature compensation at 125°C.

4. Estimate switching loss for the internal switch:

$$P_{SW} = I_{SW} \times V_{SW} \times (t_r + t_f) \times f_{SW} / 2 \quad (22)$$

where t_r is the rise time, and t_f the fall time, of V_{SW}. Subtituting into equation 14:

$$P_{SW} = 0.88\ (A) \times 16.4\ (V) \times (10\ (ns) + 10\ (ns)) \times 2\ (MHz) / 2$$
$$= 0.29\ W$$

Assuming I_{SW} equals I_{VIN} and

$$V_{SW} = V_{OUT} + V_{D1} \quad (23)$$

Substituting into equation 7:

$$P_{D(BOOST)} = P_{COND} + P_{SW}$$
$$= 0.41\ (W) + 0.29\ (W) = 0.70\ W$$

Therefore a total of 0.70W is dissipated on the boost stage.

Note that this analysis is done under the worst-case combination (maximum V_{OUT}, minimum V_{VIN}, maximum f_{SW}, and so forth). Under typical operating conditions, the power loss is lower.

The linear regulator power dissipations are the sum of the individual linear regulators:

$$P_{D(LINREG)} = P_{LDO1} + P_{LDO2} + P_{LDO3} + P_{LDO4} + P_{LDO5} \quad (24)$$

Referring to the Functional Block Diagram notes, LDO1 is the regulator for DVDD, LDO2 is the regulator for AVDD, LDO3 is the regulator for VGL, LDO4 is the regulator for VGH, and LDO5 is the regulator for VCOM.

Estimate the maximum output power for each regulator as follows, using the same worst-case values as for the boost stage calculations:

1. For DVDD:

$$P_{LDO1} = (V_{VIN} - V_{DVDD}) \times I_{DVDD} \quad (25)$$

Substituting into equation 17:

$$P_{LDO1} = (4\ (V) - 3.3\ (V)) \times 20\ (mA) = 0.03\ W$$

2. For AVDD (which is usually the largest contributor of power loss):

$$P_{LDO2} = (V_{OUT} - V_{AVDD}) \times I_{LDO2} \quad (26)$$

$$I_{LDO2} = I_{AVDD} + I_{VCOM} \quad (27)$$

Substituting into equation 18:

$$P_{LDO2} = (16\ (V) - 10\ (V)) \times (140\ (mA) + 18.3\ (mA))$$
$$= 0.95\ W$$

3. For VGL (magnitude of VGL):

$$P_{LDO3} = (V_{OUT} - |V_{VGL}|) \times |I_{VGL}| \quad (28)$$

Substituting into equation 20:

$$P_{LDO3} = (16\ (V) - 12\ (V)) \times 8.9\ (mA) = 0.036\ W$$

4. For VGH:

$$P_{LDO4} = (2 \times V_{OUT} - V_{VGH}) \times I_{VGH} \quad (29)$$

Substituting into equation 29:

$$P_{LDO4} = (2 \times 16\ (V) - (18.5\ (V)) \times 7.9\ (mA) = 0.107\ W$$

5. For VCOM:

$$P_{LDO5} = (V_{AVDD} - V_{VCOM}) \times I_{VCOM} \quad (30)$$

Substituting into equation 30:

$$P_{LDO5} = (10\ (V) - (4.5\ (V)) \times 18.3\ (mA) = 0.101\ W$$

6. Finally, the IC consumes a bias current of approximately 6 mA from VIN when EN1 and EN2 are both high. This adds power consumption of approximately 0.024 W at minimum V_{VIN}.

Substituting into equation 16, including the bias currrent factor:

$$P_{D(LINREG)} = 0.03\ (W) + 0.95\ (W) + 0.036\ (W) +$$
$$0.107\ (W) + 0.101\ (W) + 0.024\ (W)$$
$$= 1.25\ W$$

Therefore the sum of the power dissipations for all of the linear regulators is 1.25 W.

The total power dissipation if the IC is then the sum of the boost stage and the linear regulators: 1.95 W (0.70 W plus 1.25 W). This corresponds to a temperature rise of 60°C. At an ambient temperature of 85°C, the junction temperature could reach 140°C under the above worst-case conditions.

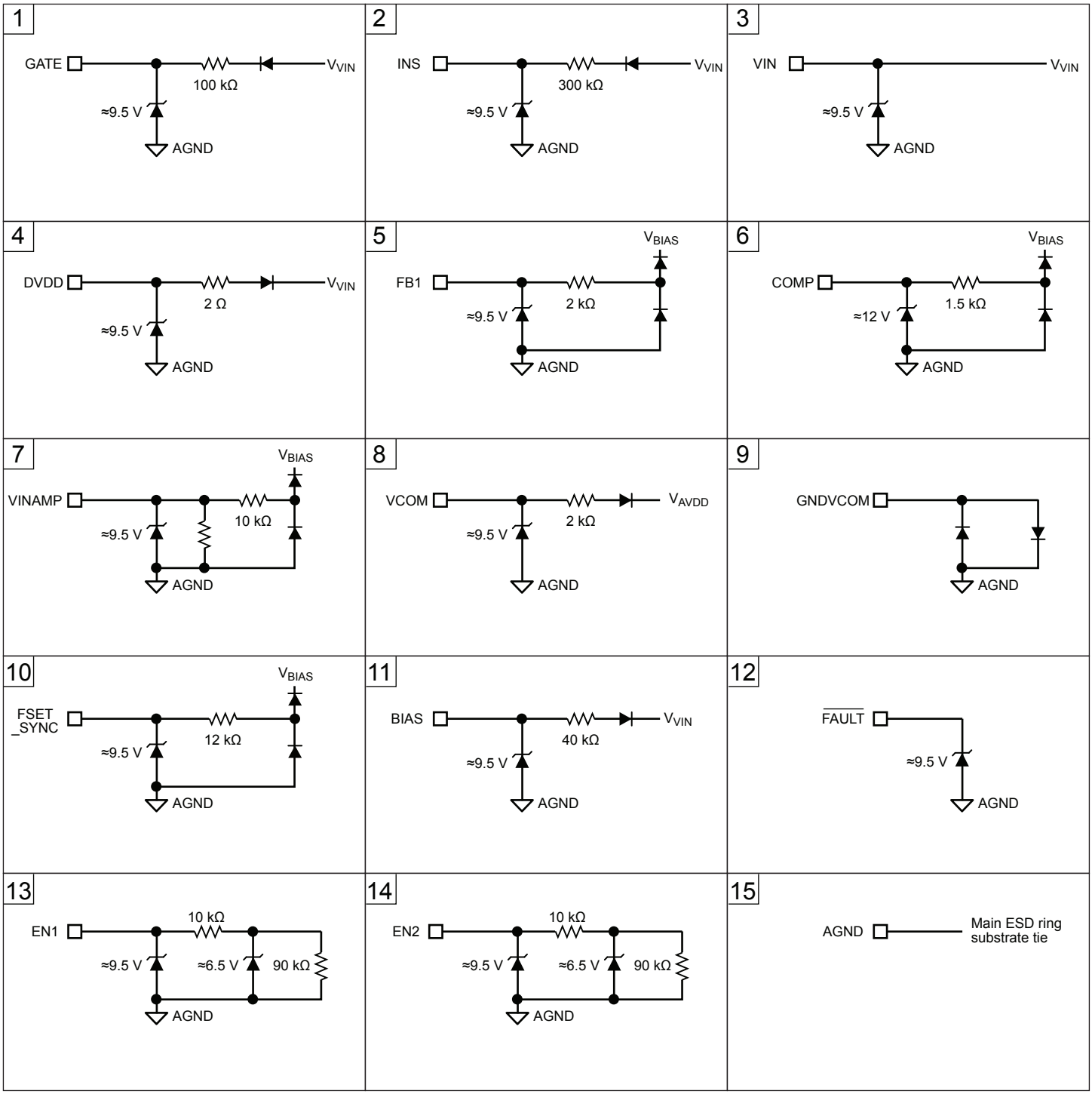
Component Selection Recommendations

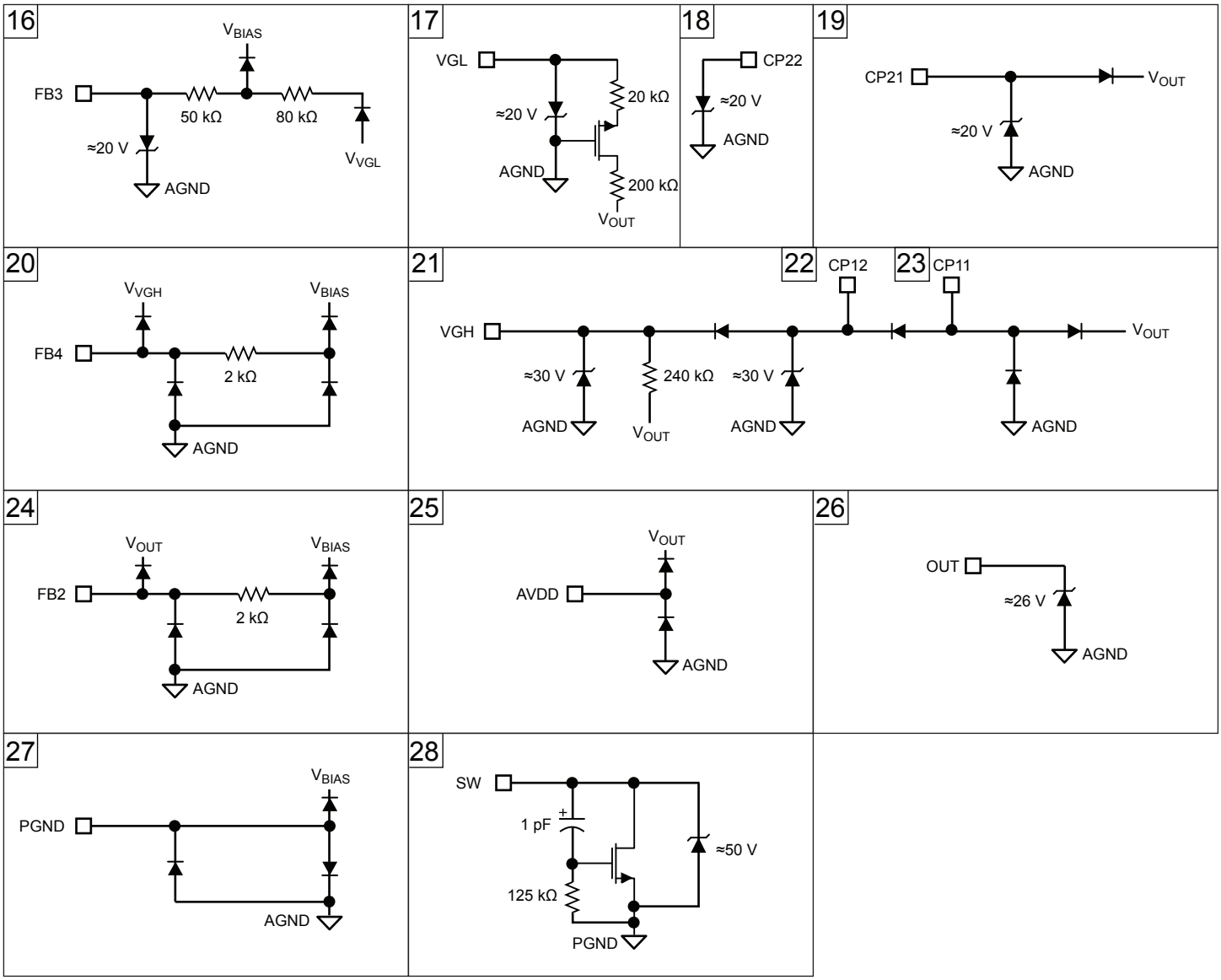
Final component selection is dependent on many system parameters, such as switching frequency, output power, and PCB area. The following recommendations should be used as a starting point only.

Table 4. External Component Recommendations

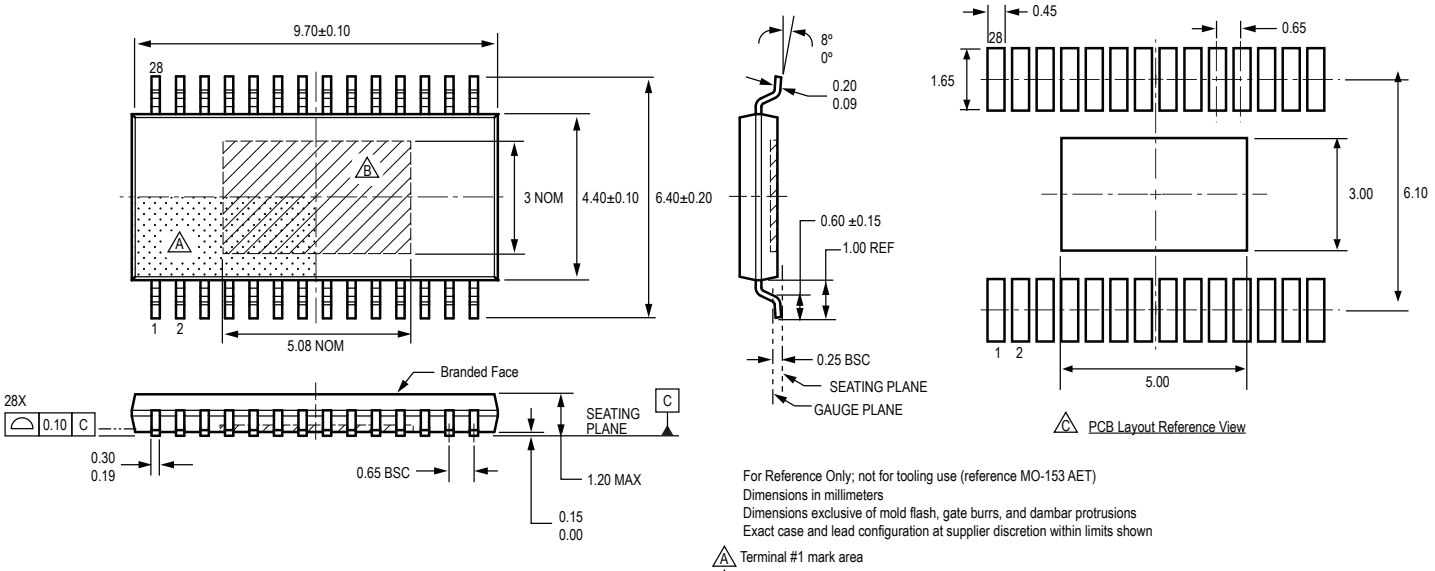
Component	Manufacturer	Description
External PMOS	Renesas uPA1830	$V_{(BR)VDSS}$ = –30 V (min), $V_{GS(off)}$ = –2.0 V (typ), $R_{DS(on)}$ = 28 mΩ (max) at V_{gs} = –4 V, SOP-8
	Toshiba TPC8125	$V_{(BR)VDSS}$ = –30 V (min), V_{th} = –2.0 V (max), $R_{DS(on)}$ = 17 mΩ (max) at V_{gs} = –4.5 V, SOP-8
	Fairchild FDS6675	$V_{(BR)VDSS}$ = –30 V (min), $V_{GS(th)}$ = –3 V (max), $R_{DS(on)}$ = 20 mV (max) at V_{GS} = –4.5 V, SOP-8
Boost Inductor	Vishay IHLP2020BZER3R3M01	L = 3.3 µH, DCR = 79 mΩ (typ), $I_{HEATING}$ = 3.3 A, 5.2 × 5.5 × 2 mm
	TOKO D63CB #A916CY-6R2M	L = 6.2 µH, DCR = 29 mΩ (typ), I_{SAT} = 1.84 A, 6.2 × 6.3 × 3.5 mm
	TDK SLF6045T-100M1R6-3PF	L = 10 µH, DCR = 39 mΩ (typ), I_{SAT} = 1.6 A, 6 × 6 × 4.5 mm
	Sumida CDR7D28MNNP-15Ø N	L = 15 µH, DCR = 65 mΩ (typ), I_{SAT} = 2.1 A at 20°C, 7.3 × 7.3 × 3 mm
Output Diode	ON-Semi MBR130	30 V, 1 A, V_f = 0.47 V (typ) at I_f = 1 A, SOD-123
Boost Output Capacitor	Murata GRM31CR61E106KA12L	10 µF, 25 V, X5R, 1206
Negative Charge Pump External Diode	1N4148W	Switching diode, 100 V, 0.15 A, C_T = 2 pF, SOD-123
	Rohm DAN217	Dual Switching diode, 80 V, 0.1 A, CT = 3.5 pF, SOT-346

I/O pin Equivalent Circuit Diagrams




16
VBIAS
FB3
50 kΩ
80 kΩ
≈20 V
VVGL
AGND
17
VGL
20 kΩ
≈20 V
AGND
200 kΩ
VOUT
18
CP22
≈20 V
AGND
19
CP21
VOUT
≈20 V
AGND
20
VVGH
VBIAS
FB4
2 kΩ
AGND
21
VGH
≈30 V
AGND
240 kΩ
VOUT
22
CP12
≈30 V
AGND
23
CP11
VOUT
AGND
24
VOUT
VBIAS
FB2
2 kΩ
AGND
25
VOUT
AVDD
AGND
26
OUT
≈26 V
AGND
27
VBIAS
PGND
AGND
28
SW
1 pF
≈50 V
125 kΩ
PGND

Package LP, 28-Pin TSSOP with Exposed Thermal Pad



For Reference Only; not for tooling use (reference MO-153 AET)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Revision History

Revision	Revision Date	Description of Revision
3	December 2, 2013	Update R_{FBx}, T_{TSD} fault
4	October 8, 2015	Updated table 1, figure 12, and figure 13

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