



**THE DATASHEET OF  
ESD11A5.0DT5G**



# ESD11A3.3DT5G SERIES

## ESD Protection Diode

### Ultra Small SOT-1123 Package

The ESD11A Series is designed to protect voltage sensitive components from damage due to ESD. These parts provide excellent ESD clamping capability and fast response time to enhance the immunity of the end application from system level ESD stress such as IEC61000-4-2. Two uni-directional surge protection diodes are housed in the ultra small SOT-1123 package, making these parts ideal for ESD protection on designs where board space is at a premium, such as cell phones, MP3 players and many other portable handheld electronic devices.

#### Specification Features:

- Low Clamping Voltage
- Small Body Outline Dimensions:  
0.039" x 0.024" (1.0 mm x 0.6 mm)
- Low Body Height: 0.016" (0.4 mm)
- Stand-off Voltage: 3.3 V – 5 V
- Low Leakage
- Response Time is Typically < 1 ns
- IEC61000-4-2 Level 4 ESD Protection
- AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices

#### Mechanical Characteristics:

**CASE:** Void-free, transfer-molded, thermosetting plastic  
Epoxy Meets UL 94 V-0

**LEAD FINISH:** 100% Matte Sn (Tin)

**MOUNTING POSITION:** Any

**QUALIFIED MAX REFLOW TEMPERATURE:** 260°C

Device Meets MSL 1 Requirements

**Table 1. MAXIMUM RATINGS**

| Rating  | Symbol           | Value       | Unit |
|---|------------------|-------------|------|
| IEC 61000-4-2 (ESD) Contact   |                  | ±15         | kV   |
| Total Power Dissipation on FR-5 Board<br>(Note 1) @ T <sub>A</sub> = 25°C | P <sub>D</sub>   | 150         | mW   |
| Storage Temperature Range   | T <sub>stg</sub> | -55 to +150 | °C   |
| Junction Temperature Range  | T <sub>J</sub>   | -55 to +125 | °C   |
| Lead Solder Temperature – Maximum<br>(10 Second Duration)                 | T <sub>L</sub>   | 260         | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

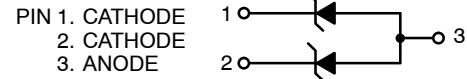
1. FR-5 = 1.0 x 0.75 x 0.62 in.

See Application Note AND8308/D for further description of ESD maximum ratings.



**ON Semiconductor®**

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#### MARKING DIAGRAM



**SOT-1123  
CASE 524AA**



X = Specific Device Code  
M = Date Code

#### ORDERING INFORMATION

| Device       | Package               | Shipping†        |
|--------------|-----------------------|------------------|
| ESD11AxxDT5G | SOT-1123<br>(Pb-Free) | 8000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### DEVICE MARKING INFORMATION

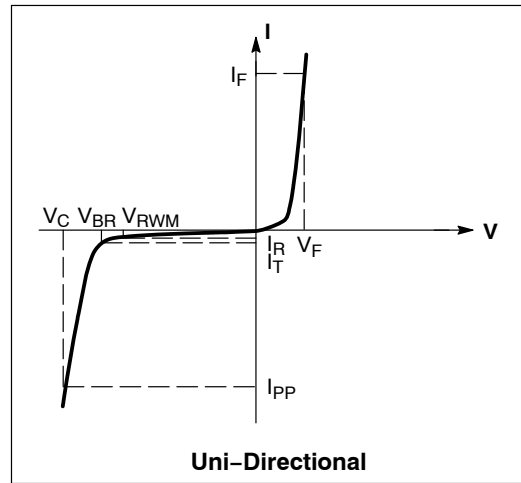
See specific marking information in the device marking column of the table on page 2 of this data sheet.

# ESD11A3.3DT5G SERIES

**Table 2. ELECTRICAL CHARACTERISTICS**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

| Symbol    | Parameter                                   |
|-----------|---|
| $I_{PP}$  | Maximum Reverse Peak Pulse Current          |
| $V_C$     | Clamping Voltage @ $I_{PP}$                 |
| $V_{RWM}$ | Working Peak Reverse Voltage                |
| $I_R$     | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$  | Breakdown Voltage @ $I_T$                   |
| $I_T$     | Test Current                                |
| $I_F$     | Forward Current                             |
| $V_F$     | Forward Voltage @ $I_F$                     |
| $P_{pk}$  | Peak Power Dissipation                      |
| C         | Capacitance @ $V_R = 0$ and $f = 1$ MHz     |



**Table 3. ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted,  $V_F = 0.9$  V Max. @  $I_F = 10$  mA for all types)

| Device        | Device Marking | $V_{RWM}$ (V) | $I_R$ ( $\mu\text{A}$ ) @ $V_{RWM}$ | $V_{BR}$ (V) @ $I_T$ (Note 2) | $I_T$ (mA) | C (pF), uni-directional (Note 3) |     | $V_C$ (V) @ $I_{PP} = 1$ A (Note 5) | $V_C$ (V) IEC61000-4-2 (Note 6) |
|---------------|----------------|---------------|-------------------------------------|-------------------------------|------------|----------------------------------|-----|-------------------------------------|---------------------------------|
|               |                | Max           | Max                                 | Min                           |            | Typ                              | Max | Max                                 | Typ                             |
| ESD11A3.3DT5G | 2*             | 3.3           | 1.0                                 | 5.2                           | 1.0        | 25                               | 35  | 7.8                                 | Figures 1 thru 4                |
| ESD11A5.0DT5G | 3*             | 5.0           | 0.1                                 | 6.2                           | 1.0        | 20                               | 30  | 9.5                                 | Figures 1 thru 4                |

\*Rotated 90° clockwise.

- $V_{BR}$  is measured with a pulse test current  $I_T$  at an ambient temperature of  $25^\circ\text{C}$ .
- Uni-directional capacitance at  $f = 1$  MHz,  $V_R = 0$  V,  $T_A = 25^\circ\text{C}$  (pin1 to pin 3; pin 2 to pin 3).
- Bi-directional capacitance at  $f = 1$  MHz,  $V_R = 0$  V,  $T_A = 25^\circ\text{C}$  (pin1 to pin 2).
- Surge current waveform per Figure 7.
- Typical waveform. For test procedure see Figures 5 and 6 and Application Note AND8307/D.

# ESD11A3.3DT5G SERIES

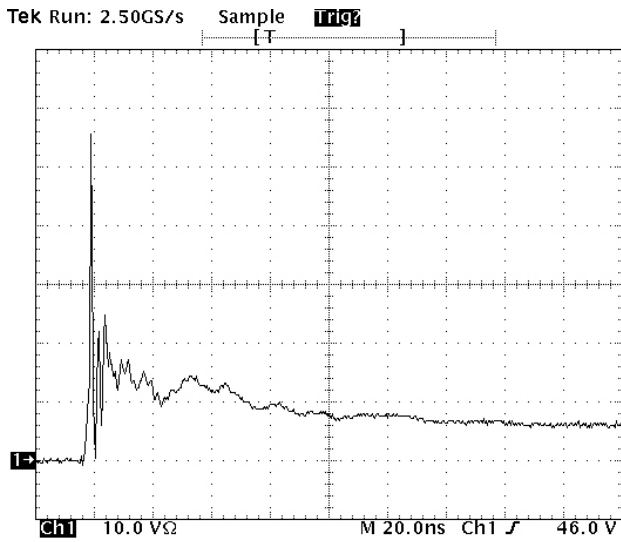


Figure 1. ESD11A3.3D Clamping Voltage Screenshot Positive 8 kV contact per IEC 61000-4-2

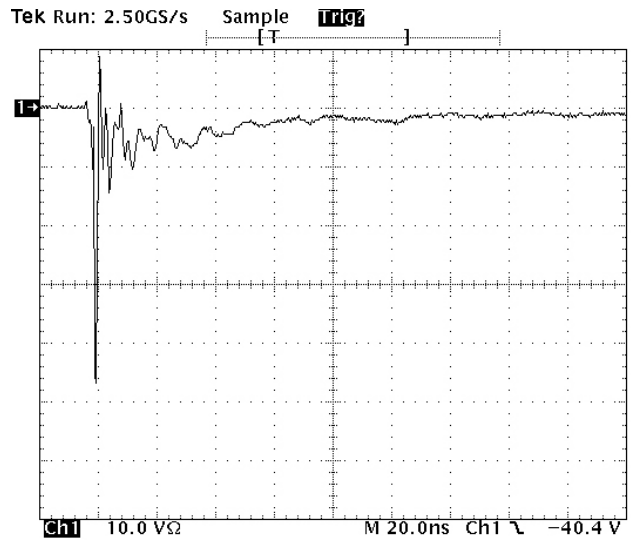


Figure 2. ESD11A3.3D Clamping Voltage Screenshot Negative 8 kV contact per IEC 61000-4-2

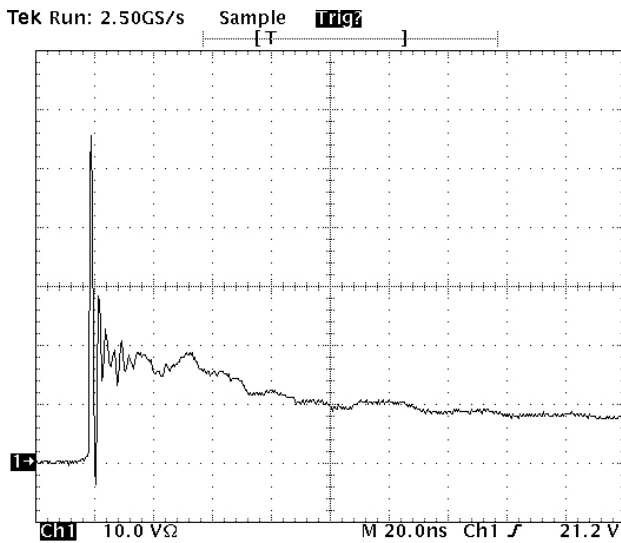


Figure 3. ESD11A5.0D Clamping Voltage Screenshot Positive 8 kV contact per IEC 61000-4-2

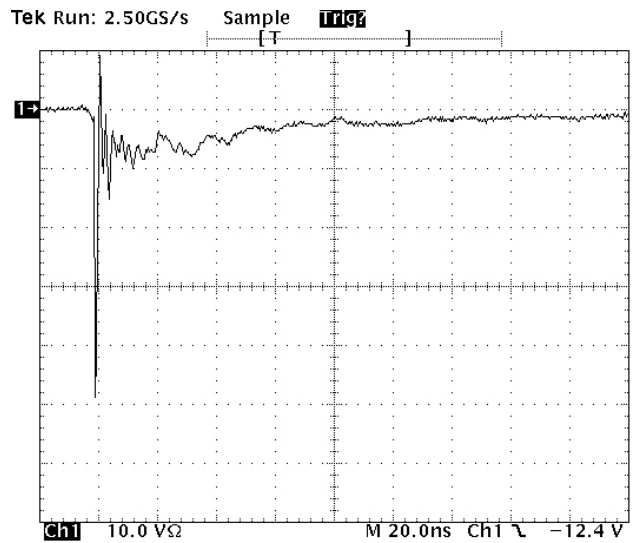


Figure 4. ESD11A5.0D Clamping Voltage Screenshot Negative 8 kV contact per IEC 61000-4-2

# ESD11A3.3DT5G SERIES

## IEC 61000-4-2 Spec.

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|-------|-------------------|------------------------|----------------------|----------------------|
| 1     | 2                 | 7.5                    | 4                    | 2                    |
| 2     | 4                 | 15                     | 8                    | 4                    |
| 3     | 6                 | 22.5                   | 12                   | 6                    |
| 4     | 8                 | 30                     | 16                   | 8                    |



Figure 5. IEC61000-4-2 Spec

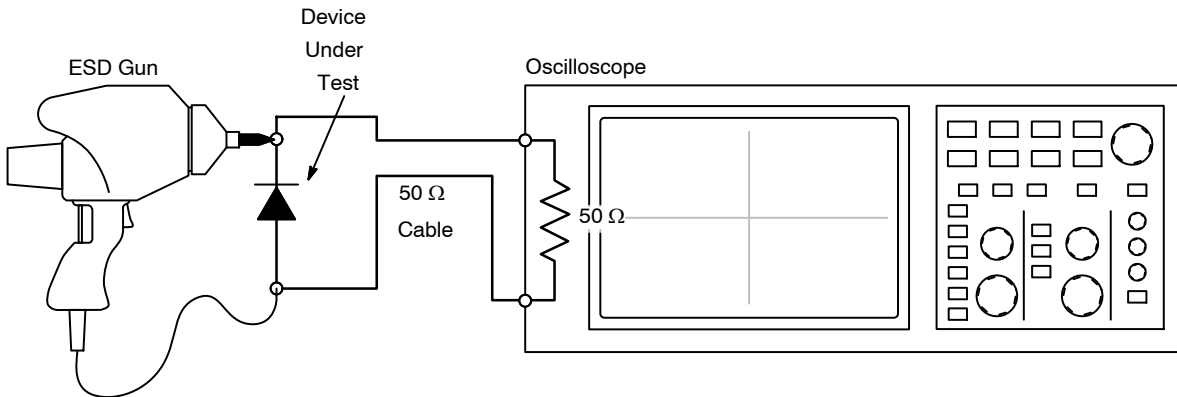


Figure 6. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

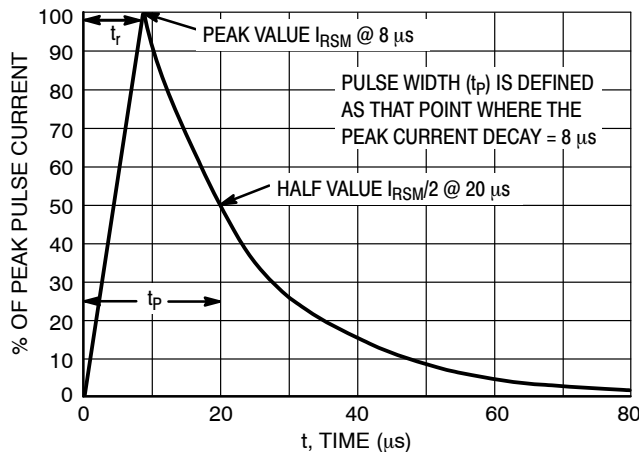
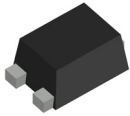


Figure 7. 8 X 20 μs Pulse Waveform

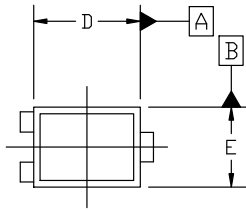
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

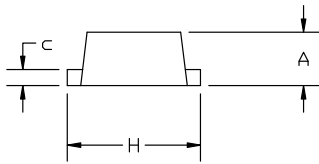


**SOT-1123 0.80x0.60x0.37, 0.35P**  
**CASE 524AA**  
**ISSUE D**

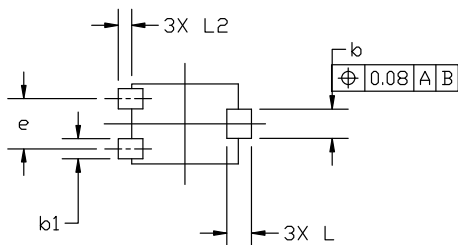
DATE 18 JAN 2024



TOP VIEW

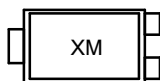


SIDE VIEW



BOTTOM VIEW

### GENERIC MARKING DIAGRAM\*



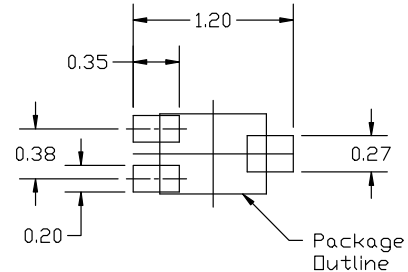
X = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| MILLIMETERS |           |       |       |
|-------------|-----------|-------|-------|
| DIM         | MIN       | NOM   | MAX   |
| A           | 0.34      | 0.37  | 0.40  |
| b           | 0.15      | 0.22  | 0.28  |
| b1          | 0.10      | 0.15  | 0.20  |
| c           | 0.07      | 0.12  | 0.17  |
| D           | 0.75      | 0.80  | 0.85  |
| E           | 0.55      | 0.60  | 0.65  |
| e           | 0.35      | 0.38  | 0.40  |
| H           | 0.950     | 1.000 | 1.050 |
| L           | 0.185 REF |       |       |
| L2          | 0.05      | 0.10  | 0.15  |



### RECOMMENDED MOUNTING FOOTPRINT

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERM/D.

#### STYLE 1:

- PIN 1. BASE
- EMITTER
- COLLECTOR

#### STYLE 2:

- PIN 1. ANODE
- N/C
- CATHODE

#### STYLE 3:

- PIN 1. ANODE
- ANODE
- CATHODE

#### STYLE 4:

- PIN 1. CATHODE
- CATHODE
- ANODE

#### STYLE 5:

- PIN 1. GATE
- SOURCE
- DRAIN

|                         |                                       |  |
|-------------------------|---------------------------------------|--|
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