



**THE DATASHEET OF  
CAT24C08C4ATR**



# CAT24C02, CAT24C04, CAT24C08, CAT24C16

## EEPROM Serial 2/4/8/16 Kb I<sup>2</sup>C

### Description

The CAT24C02/04/08/16 are 2-Kb, 4-Kb, 8-Kb and 16-Kb respectively I<sup>2</sup>C Serial EEPROM devices organized internally as 16/32/64 and 128 pages respectively of 16 bytes each. All devices support both the Standard (100 kHz) as well as Fast (400 kHz) I<sup>2</sup>C protocol.

Data is written by providing a starting address, then loading 1 to 16 contiguous bytes into a Page Write Buffer, and then writing all data to non-volatile memory in one internal write cycle. Data is read by providing a starting address and then shifting out data serially while automatically incrementing the internal address count.

External address pins make it possible to address up to eight CAT24C02, four CAT24C04, two CAT24C08 and one CAT24C16 device on the same bus.

### Features

- Supports Standard and Fast I<sup>2</sup>C Protocol
- 1.7 V to 5.5 V Supply Voltage Range
- 16-Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I<sup>2</sup>C Bus Inputs (SCL and SDA)
- Low power CMOS Technology
- More than 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



ON Semiconductor®

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SOIC-8 WIDE  
X SUFFIX  
CASE 751BE



UDFN8-EP  
HU4 SUFFIX  
CASE 517AZ



TSSOP-8  
Y SUFFIX  
CASE 948AL



TSOT-23  
TD SUFFIX  
CASE 419AE



SOIC-8  
W SUFFIX  
CASE 751BD



WLCSP-4\*\*  
C4A SUFFIX  
CASE 567DC



WLCSP-5\*\*  
C5A SUFFIX  
CASE 567DD



WLCSP-4\*\*  
C4U SUFFIX  
CASE 567NX

\*\* WLCSP are available for the CAT24C04, CAT24C08 and CAT24C16 only.

For serial EEPROM in the US8 package, please consult the N24C02 datasheet

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 18 of this data sheet.

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.



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**Table 2. ABSOLUTE MAXIMUM RATINGS**

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on any pin with respect to Ground (Note 1)	-0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. During input transitions, voltage undershoot on any pin should not exceed -1 V for more than 20 ns. Voltage overshoot on pins A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub> and WP should not exceed V<sub>CC</sub> + 1 V for more than 20 ns, while voltage on the I<sup>2</sup>C bus pins, SCL and SDA, should not exceed the absolute maximum ratings, irrespective of V<sub>CC</sub>.

**Table 3. RELIABILITY CHARACTERISTICS** (Note 2)

Symbol	Parameter	Min	Units
N <sub>END</sub> (Note 3)	Endurance	1,000,000	Program / Erase Cycles
T <sub>DR</sub>	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
3. Page Mode, V<sub>CC</sub> = 5 V, 25°C.

**Table 4. D.C. OPERATING CHARACTERISTICS**

(V<sub>CC</sub> = 1.8 V to 5.5 V, T<sub>A</sub> = -40°C to +125°C and V<sub>CC</sub> = 1.7 V to 5.5 V, T<sub>A</sub> = -40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I <sub>CCR</sub>	Read Current	Read, f <sub>SCL</sub> = 400 kHz		1	mA
I <sub>CCW</sub>	Write Current	Write, f <sub>SCL</sub> = 400 kHz		2	mA
I <sub>SB</sub>	Standby Current	All I/O Pins at GND or V <sub>CC</sub>	T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> ≤ 3.3 V	1	μA
			T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> > 3.3 V	3	
			T <sub>A</sub> = -40°C to +125°C	5	
I <sub>L</sub>	I/O Pin Leakage	Pin at GND or V <sub>CC</sub>		2	μA
V <sub>IL</sub>	Input Low Voltage		-0.5	0.3 x V <sub>CC</sub>	V
V <sub>IH</sub>	Input High Voltage	A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> and WP	0.7 x V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V
		SCL and SDA	0.7 x V <sub>CC</sub>	5.5	
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> > 2.5 V, I <sub>OL</sub> = 3 mA		0.4	
		V <sub>CC</sub> < 2.5 V, I <sub>OL</sub> = 1 mA		0.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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**Table 5. PIN IMPEDANCE CHARACTERISTICS**

( $V_{CC} = 1.8\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }+125^\circ\text{C}$  and  $V_{CC} = 1.7\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
$C_{IN}$ (Note 4)	SDA Pin Capacitance	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$ , $V_{CC} = 5.0\text{ V}$	8	pF
	Other Pins		6	pF
$I_{WP}$ (Note 5)	WP Input Current	$V_{IN} < V_{IH}$ , $V_{CC} = 5.5\text{ V}$	130	$\mu\text{A}$
		$V_{IN} < V_{IH}$ , $V_{CC} = 3.3\text{ V}$	120	
		$V_{IN} < V_{IH}$ , $V_{CC} = 1.7\text{ V}$	80	
		$V_{IN} > V_{IH}$	2	
$I_A$ (Note 5)	Address Input Current (A0, A1, A2) Product Rev H: CAT24C02 Product Rev K: CAT24C04, CAT24C08, CAT24C16	$V_{IN} < V_{IH}$ , $V_{CC} = 5.5\text{ V}$	50	$\mu\text{A}$
		$V_{IN} < V_{IH}$ , $V_{CC} = 3.3\text{ V}$	35	
		$V_{IN} < V_{IH}$ , $V_{CC} = 1.7\text{ V}$	25	
		$V_{IN} > V_{IH}$	2	

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
5. When not driven, the WP, A0, A1 and A2 pins are pulled down to GND internally. For improved noise immunity, the internal pull-down is relatively strong; therefore the external driver must be able to supply the pull-down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer ( $\sim 0.5 \times V_{CC}$ ), the strong pull-down reverts to a weak current source.

**Table 6. A.C. CHARACTERISTICS**

(Note 6) ( $V_{CC} = 1.8\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }+125^\circ\text{C}$  and  $V_{CC} = 1.7\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
$F_{SCL}$	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		$\mu\text{s}$
$t_{LOW}$	Low Period of SCL Clock	4.7		1.3		$\mu\text{s}$
$t_{HIGH}$	High Period of SCL Clock	4		0.6		$\mu\text{s}$
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		$\mu\text{s}$
$t_{HD:DAT}$	Data In Hold Time	0		0		$\mu\text{s}$
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
$t_R$	SDA and SCL Rise Time		1000		300	ns
$t_F$ (Note 6)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		$\mu\text{s}$
$t_{BUF}$	Bus Free Time Between STOP and START	4.7		1.3		$\mu\text{s}$
$t_{AA}$	SCL Low to Data Out Valid		3.5		0.9	$\mu\text{s}$
$t_{DH}$	Data Out Hold Time	100		100		ns
$T_i$ (Note 6)	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		$\mu\text{s}$
$t_{HD:WP}$	WP Hold Time	2.5		2.5		$\mu\text{s}$
$t_{WR}$	Write Cycle Time		5		5	ms
$t_{PU}$ (Notes 7, 8)	Power-up to Ready Mode		1		1	ms

6. Test conditions according to "AC Test Conditions" table.
7. Tested initially and after a design or process change that affects this parameter.
8.  $t_{PU}$  is the delay between the time  $V_{CC}$  is stable and the device is ready to accept commands.

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**Table 7. A.C. TEST CONDITIONS**

Input Drive Levels	0.2 x V <sub>CC</sub> to 0.8 x V <sub>CC</sub>
Input Rise and Fall Time	≤ 50 ns
Input Reference Levels	0.3 x V <sub>CC</sub> , 0.7 x V <sub>CC</sub>
Output Reference Level	0.5 x V <sub>CC</sub>
Output Test Load	Current Source I <sub>OL</sub> = 3 mA (V <sub>CC</sub> ≥ 2.5 V); I <sub>OL</sub> = 1 mA (V <sub>CC</sub> < 2.5 V); C <sub>L</sub> = 100 pF

### Power-On Reset (POR)

Each CAT24Cxx\* incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

A CAT24Cxx device will power up into Standby mode after V<sub>CC</sub> exceeds the POR trigger level and will power down into Reset mode when V<sub>CC</sub> drops below the POR trigger level. This bi-directional POR feature protects the device against ‘brown-out’ failure following a temporary loss of power.

*\*For common features, the CAT24C02/04/08/16 will be referred to as CAT24Cxx.*

### Pin Description

**SCL:** The Serial Clock input pin accepts the Serial Clock generated by the Master.

**SDA:** The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

**A0, A1 and A2:** The Address inputs set the device address when cascading multiple devices. When not driven, these pins are pulled LOW internally.

**WP:** The Write Protect input pin inhibits all write operations, when pulled HIGH. When not driven, this pin is pulled LOW internally.

### Functional Description

The CAT24Cxx supports the Inter-Integrated Circuit (I<sup>2</sup>C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24Cxx acts as a Slave device. Master and Slave alternate as either transmitter or receiver.

### I<sup>2</sup>C Bus Protocol

The I<sup>2</sup>C bus consists of two ‘wires’, SCL and SDA. The two wires are connected to the V<sub>CC</sub> supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see AC Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is high. An SDA transition while SCL is high will be interpreted as a START or STOP condition (Figure 2). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake-up’ call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

***NOTE:** The I/O pins of CAT24Cxx do not obstruct the SCL and SDA lines if the VCC supply is switched off. During power-up, the SCL and SDA pins (connected with pull-up resistors to VCC) will follow the VCC monotonically from VSS (0 V) to nominal VCC value, regardless of pull-up resistor value. The delta between the VCC and the instantaneous voltage levels during power ramping will be determined by the relation between bus time constant (determined by pull-up resistance and bus capacitance) and actual VCC ramp rate.*

### Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. For normal Read/Write operations, the first 4 bits of the Slave address are fixed at 1010 (Ah). The next 3 bits are used as programmable address bits when cascading multiple devices and/or as internal address bits. The last bit of the slave address, R/W, specifies whether a Read (1) or Write (0) operation is to be performed. The 3 address space extension bits are assigned as illustrated in Figure 3. A<sub>2</sub>, A<sub>1</sub> and A<sub>0</sub> must match the state of the external address pins, and a<sub>10</sub>, a<sub>9</sub> and a<sub>8</sub> are internal address bits.

### Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge the address byte and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 5.

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Figure 2. Start/Stop Timing

1	0	1	0	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	R/W	CAT24C02
1	0	1	0	A <sub>2</sub>	A <sub>1</sub>	a <sub>8</sub>	R/W	CAT24C04
1	0	1	0	A <sub>2</sub>	a <sub>9</sub>	a <sub>8</sub>	R/W	CAT24C08
1	0	1	0	a <sub>10</sub>	a <sub>9</sub>	a <sub>8</sub>	R/W	CAT24C16

Figure 3. Slave Address Bits



Figure 4. Acknowledge Timing

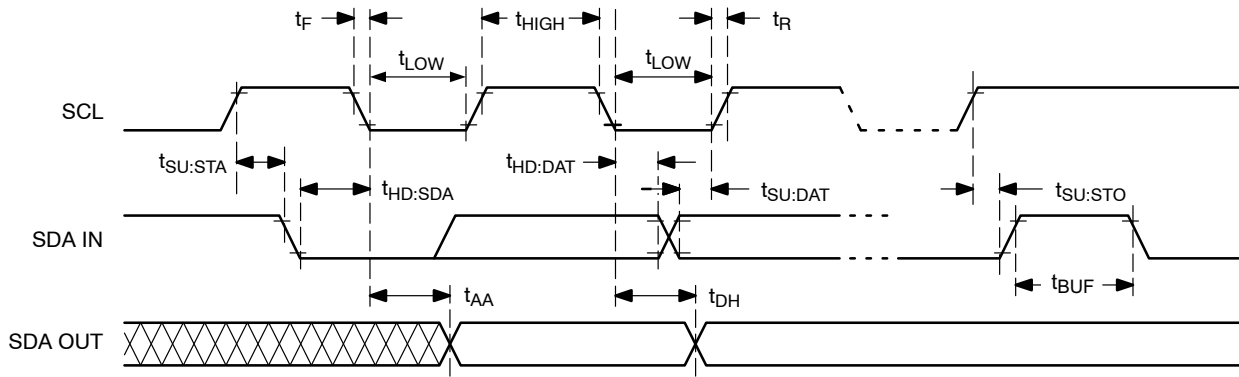


Figure 5. Bus Timing

WRITE OPERATIONS

**Byte Write**

In Byte Write mode, the Master sends the START condition and the Slave address with the R/W bit set to zero to the Slave. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24Cxx. After receiving another acknowledge from the Slave, the Master transmits the data byte to be written into the addressed memory location. The CAT24Cxx device will acknowledge the data byte and the Master generates the STOP condition, at which time the device begins its internal Write cycle to nonvolatile memory (Figure 6). While this internal cycle is in progress ( $t_{WR}$ ), the SDA output will be tri-stated and the CAT24Cxx will not respond to any request from the Master device (Figure 7).

**Page Write**

The CAT24Cxx writes up to 16 bytes of data in a single write cycle, using the Page Write operation (Figure 8). The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the data byte is transmitted, the Master is allowed to send up to fifteen additional bytes. After each byte has been transmitted the CAT24Cxx will respond with an acknowledge and internally increments the four low order address bits. The high order bits that define the page address remain unchanged. If the Master transmits more than sixteen bytes prior to sending the STOP condition, the address counter ‘wraps around’ to the beginning of page and previously transmitted data will be overwritten. Once all

sixteen bytes are received and the STOP condition has been sent by the Master, the internal Write cycle begins. At this point all received data is written to the CAT24Cxx in a single write cycle.

**Acknowledge Polling**

The acknowledge (ACK) polling routine can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host’s write operation, the CAT24Cxx initiates the internal write cycle. The ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24Cxx is still busy with the write operation, NoACK will be returned. If the CAT24Cxx has completed the internal write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

**Hardware Write Protection**

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24Cxx. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the CAT24Cxx will not acknowledge the data byte and the Write request will be rejected.

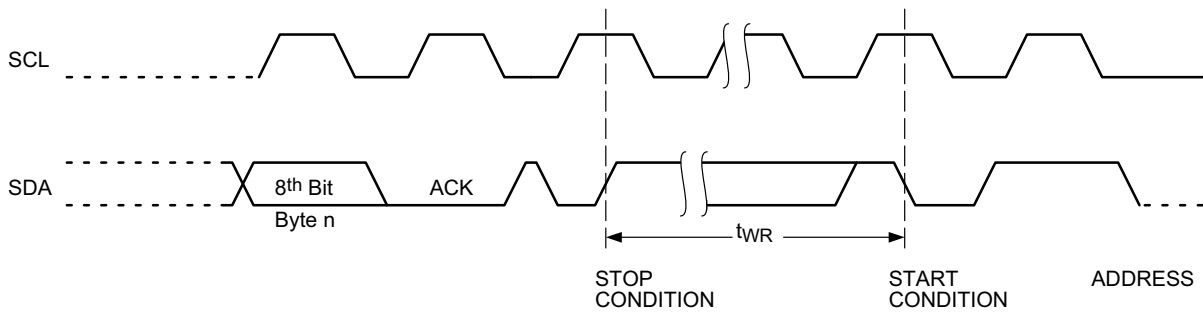
**Delivery State**

The CAT24Cxx is shipped erased, i.e., all bytes are FFh.

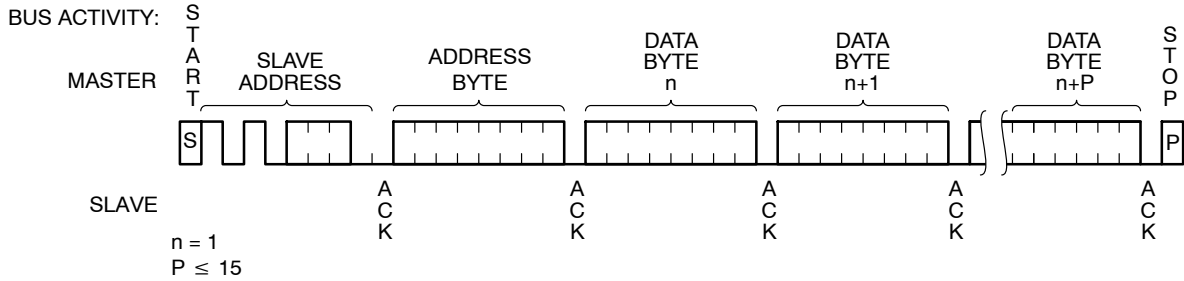


Figure 6. Byte Write Sequence

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**Figure 7. Write Cycle Timing**



**Figure 8. Page Write Sequence**



**Figure 9. WP Timing**

READ OPERATIONS

**Immediate Read**

Upon receiving a Slave address with the R/W bit set to '1', the CAT24Cxx will interpret this as a request for data residing at the current byte address in memory. The CAT24Cxx will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the CAT24Cxx returns to Standby mode.

**Selective Read**

Selective Read operations allow the Master device to select at random any memory location for a read operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte

address of the location it wishes to read. After the CAT24Cxx acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/W bit set to one. The CAT24Cxx then responds with its acknowledge and sends the requested data byte. The Master device does not acknowledge the data (NoACK) but will generate a STOP condition (Figure 11).

**Sequential Read**

If during a Read session, the Master acknowledges the 1<sup>st</sup> data byte, then the CAT24Cxx will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap-around at end of memory (rather than end of page).



Figure 10. Immediate Read Sequence and Timing



Figure 11. Selective Read Sequence



Figure 12. Sequential Read Sequence

# CAT24C02, CAT24C04, CAT24C08, CAT24C16

## PACKAGE DIMENSIONS

SOIC-8, 208 mils  
CASE 751BE-01  
ISSUE O



SYMBOL	MIN	NOM	MAX
A			2.03
A1	0.05		0.25
b	0.36		0.48
c	0.19		0.25
D	5.13		5.33
E	7.75		8.26
E1	5.13		5.38
e	1.27 BSC		
L	0.51		0.76
$\theta$	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

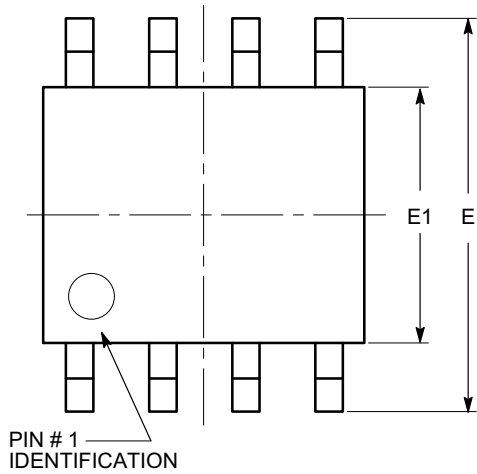
**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with EIAJ EDR-7320.

# CAT24C02, CAT24C04, CAT24C08, CAT24C16

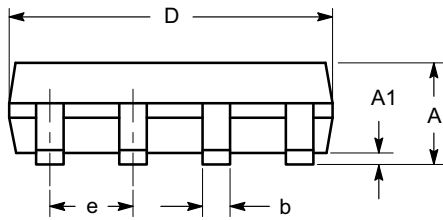
## PACKAGE DIMENSIONS

SOIC 8, 150 mils  
CASE 751BD  
ISSUE O

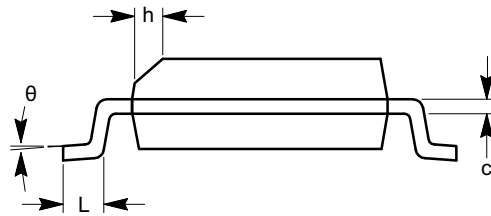


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
$\theta$	0°		8°



SIDE VIEW



END VIEW

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

# CAT24C02, CAT24C04, CAT24C08, CAT24C16

## PACKAGE DIMENSIONS

TSSOP8, 4.4x3  
CASE 948AL  
ISSUE O



SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
$\theta$	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

# CAT24C02, CAT24C04, CAT24C08, CAT24C16

## PACKAGE DIMENSIONS

TSOT-23, 5 LEAD  
CASE 419AE  
ISSUE O



TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 TYP		
L	0.30	0.40	0.50
L1	0.60 REF		
L2	0.25 BSC		
$\theta$	0°		8°



SIDE VIEW



END VIEW

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-193.

# CAT24C02, CAT24C04, CAT24C08, CAT24C16

## PACKAGE DIMENSIONS

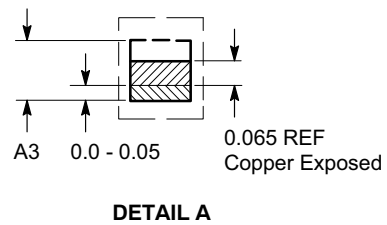
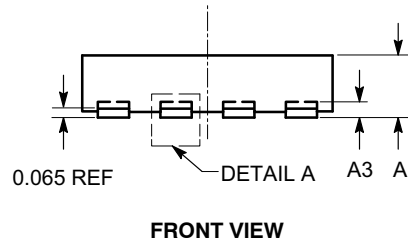
### UDFN8, 2x3 EXTENDED PAD CASE 517AZ ISSUE O



SYMBOL	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
A3	0.127 REF		
b	0.20	0.25	0.30
D	1.95	2.00	2.05
D2	1.35	1.40	1.45
E	2.95	3.00	3.05
E2	1.25	1.30	1.35
e	0.50 REF		
L	0.25	0.30	0.35

**Notes:**

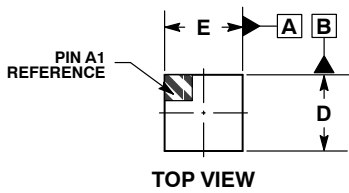
- (1) All dimensions are in millimeters.
- (2) Refer JEDEC MO-236/MO-252.



# CAT24C02, CAT24C04, CAT24C08, CAT24C16

## PACKAGE DIMENSIONS

WLCSP4, 0.84x0.86  
CASE 567NX  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
  4. COPLANARITY APPLIES TO SPHERICAL CROWNS OF THE CONTACT BALLS.
  5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	---	---	0.30
A1	0.08	0.10	0.12
A2	0.15 REF		
A3	0.025 REF		
b	0.16	0.18	0.20
D	0.82	0.84	0.86
E	0.84	0.86	0.88
e	0.40 BSC		

### RECOMMENDED SOLDERING FOOTPRINT\*



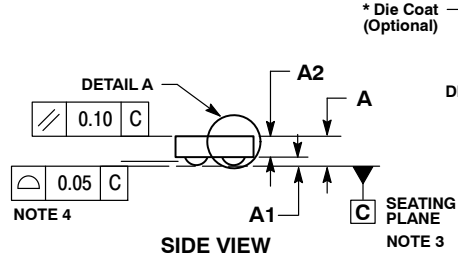
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# CAT24C02, CAT24C04, CAT24C08, CAT24C16

## PACKAGE DIMENSIONS

WLCSP4, 0.84x0.86  
CASE 567DC  
ISSUE D



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

DIM	MILLIMETERS	
	MIN	MAX
A	0.28	0.38
A1	0.08	0.12
A2	0.23 REF	
A3*	0.025 REF	
b	0.16	0.20
D	0.84 BSC	
E	0.86 BSC	
e	0.40 BSC	

\* Die Coat (Optional)

### RECOMMENDED SOLDERING FOOTPRINT\*



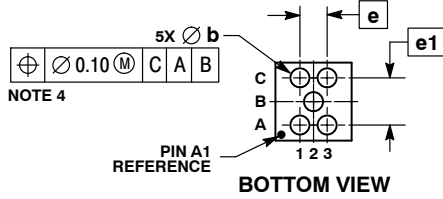
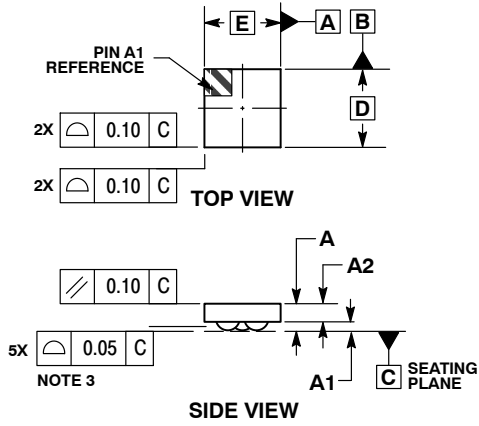
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# CAT24C02, CAT24C04, CAT24C08, CAT24C16

## PACKAGE DIMENSIONS

WLCSP5, 0.86x0.84  
CASE 567DD  
ISSUE C

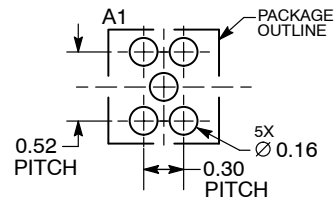


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

DIM	MILLIMETERS	
	MIN	MAX
A	0.29	0.39
A1	0.10	0.14
A2	0.23	REF
b	0.14	0.18
D	0.86	BSC
E	0.84	BSC
e	0.30	BSC
e1	0.52	BSC

**RECOMMENDED SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## CAT24C02, CAT24C04, CAT24C08, CAT24C16

### Ordering Information

#### CAT24C02 Ordering Information (Notes 10, 11)

Device Order Number	Specific Device Marking	Package Type	Temperature Range (Note 9)	Lead Finish	Shipping
CAT24C02TDI-GT3A	C1	TSOT-23-5	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel

#### CAT24C04 Ordering Information

Device Order Number	Specific Device Marking	Package Type	Temperature Range (Note 9)	Lead Finish	Shipping
CAT24C04WI-GT3	24C04K	SOIC-8	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C04XI-T2 (Note 17)	TBD	SOIC-8	Industrial	Matte-Tin	Tape & Reel, 2,000 Units / Reel
CAT24C04YI-GT3	C04K	TSSOP-8	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C04C4UTR	R	WLCSP-4	Industrial	N/A	(Notes 12 and 13)
CAT24C04C4ATR	4	WLCSP-4	Industrial	N/A	Tape & Reel, 5,000 Units / Reel
CAT24C04C5ATR	4	WLCSP-5	Industrial	N/A	Tape & Reel, 5,000 Units / Reel
CAT24C04TDI-GT3	C2	TSOT-23-5	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C04HU4I-GT3	C2U	UDFN8-EP	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel

#### CAT24C08 Ordering Information

Device Order Number	Specific Device Marking	Package Type	Temperature Range (Note 9)	Lead Finish	Shipping
CAT24C08WI-GT3	24C08K	SOIC-8	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C08XI-T2 (Note 17)	TBD	SOIC-8	Industrial	Matte-Tin	Tape & Reel, 2,000 Units / Reel
CAT24C08YI-GT3	C08K	TSSOP-8	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C08C4UTR	T	WLCSP-4	Industrial	N/A	(Notes 12 and 13)
CAT24C08C4ATR	8	WLCSP-4	Industrial	N/A	Tape & Reel, 5,000 Units / Reel
CAT24C08C4CTR**	8	WLCSP-4	Industrial	N/A	Tape & Reel, 5,000 Units / Reel
CAT24C08C5ATR	8	WLCSP-5	Industrial	N/A	Tape & Reel, 5,000 Units / Reel
CAT24C08TDI-GT3	C3	TSOT-23-5	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C08HU4I-GT3	C3U	UDFN8-EP	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel

#### CAT24C16 Ordering Information

Device Order Number	Specific Device Marking	Package Type	Temperature Range (Note 9)	Lead Finish	Shipping
CAT24C16WI-GT3	24C16K	SOIC-8	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C16XI-T2 (Note 17)	TBD	SOIC-8	Industrial	Matte-Tin	Tape & Reel, 2,000 Units / Reel
CAT24C16YI-GT3	C16K	TSSOP-8	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C16C4UTR	6	WLCSP-4	Industrial	N/A	(Notes 12 and 13)
CAT24C16C4ATR	6	WLCSP-4	Industrial	N/A	Tape & Reel, 5,000 Units / Reel
CAT24C16C5ATR	6	WLCSP-5	Industrial	N/A	Tape & Reel, 5,000 Units / Reel
CAT24C16TDI-GT3	C4	TSOT-23-5	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C16HU4I-GT3	C4U	UDFN8-EP	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C16HU4E-GT3 (Note 17)	C4E	UDFN8-EP	Extended	NiPdAu	Tape & Reel, 3,000 Units / Reel

9. Industrial temperature range is -40°C to +85°C and Extended temperature range is -40°C to +125°C.

10. Part numbers ending with "A" for the CAT24C02 are for Gresham (Product Rev H) only die.

11. The CAT24C02 "non-A" Device Order Numbers use Gresham die (Rev H) for date codes, starting August 1st, 2012. Therefore the Specific Device Marking for these OPNs reflect Rev H die.

12. Contact local sales office for availability.

13. CAUTION: The EEPROM devices delivered in WLCSP must never be exposed to ultraviolet light. When exposed to ultraviolet light the EEPROM cells lose their stored data.

14. All packages are RoHS-compliant (Lead-free, Halogen-free).

15. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

16. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at [www.onsemi.com](http://www.onsemi.com)

17. In Development

\*\* CAT24C08C4CTR is a backside coated version. Contact factory for other densities.

# CAT24C02, CAT24C04, CAT24C08, CAT24C16

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