THE DATASHEET OF

AD9867BCPZRL

Broadband Modem Mixed-Signal Front End

AD9867

FEATURES

Low cost, 3.3 V CMOS MxFE® for broadband modems
10-bit digital-to-analog converter (DAC)
- **2×/4× interpolation filter**
- **250 MSPS DAC update rate**

10-bit, 75 MSPS ADC
Low noise RxPGA
- **Dual channel muxed input**
- **6 dB input overload attenuator**
- **−12 dB to +48 dB (without attenuator)**
- **Third-order programmable low-pass filter**

Flexible digital datapath interface
- **Half-duplex and full-duplex operation**
- **Programmable delay Tx driver disable signal**

Various power-down/reduction modes
Internal clock multiplier (PLL)
2 auxiliary programmable clock outputs
64-lead LFCSP

APPLICATIONS

Power-line networking

FUNCTIONAL BLOCK DIAGRAM

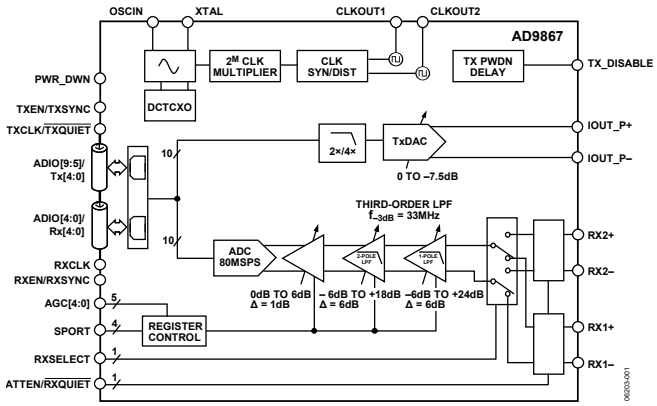

Figure 1.

GENERAL DESCRIPTION

The AD9867 is a mixed-signal front-end (MxFE) IC for transceiver applications requiring Tx and Rx path functionality with data rates up to 75 MSPS. Its flexible digital interface, power-saving modes, and high Tx-to-Rx isolation make the part well suited for half-duplex and full-duplex applications. The digital interface is extremely flexible allowing simple interfaces to digital back ends. Power-saving modes can reduce power consumption of individual functional blocks or can power down unused blocks in half-duplex applications. A serial port interface (SPI®) allows software programming of the various functional blocks. An on-chip PLL clock multiplier and synthesizer provide all the required internal clocks, as well as two external clocks from a single crystal or clock source.

The Tx signal path consists of a bypassable 2×/4× low-pass interpolation filter and a 10-bit, 250 MSPS TxDAC. The transmit path signal bandwidth can be as high as 33.6 MHz at an input data rate of 75 MSPS. The TxDAC provides differential current outputs that can be steered directly to a differential or single-ended external load. Tx power can be digitally controlled over a 7.5 dB range in 0.5 dB steps.

The receive path consists of a programmable amplifier (RxPGA), a tunable low-pass filter (LPF), and a 10-bit analog-to-digital converter (ADC). The low noise RxPGA has a programmable gain range of −12 dB to +48 dB in 1 dB steps. Its input referred noise is less than 3.6 nV/√Hz for gain settings beyond 36 dB. An optional attenuator provides an additional 6 dB (or more) of attenuation (when combined with external series resistors). The receive path LPF cutoff frequency can either be set over a 22 MHz to 38 MHz range or simply bypassed. The 10-bit ADC achieves excellent dynamic performance over a 5 MSPS to 75 MSPS span. Both the RxPGA and the ADC offer scalable power consumption allowing power/performance optimization.

The AD9867 provides a highly integrated solution for broadband modems. It is available in a space-saving, 64-lead LFCSP and is specified over the commercial (−40°C to +85°C) temperature range.

For more information on the AD9867, contact Analog Devices, Inc. at email MxFE_Support@analog.com.

Rev. SpB

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NOTES

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