



**THE DATASHEET OF  
ADN4666ARUZ**



### FEATURES

- ±8 kV ESD IEC 61000-4-2 contact discharge on receiver input pins
- 400 Mbps (200 MHz) switching rates
- 100 ps channel-to-channel skew (typical)
- 100 ps differential skew (typical)
- 3.3 ns propagation delay (maximum)
- 3.3 V power supply
- High impedance outputs on power-down
- Low power design (10 mW quiescent typical)
- Interoperable with existing 5 V LVDS drivers
- Accepts small swing (350 mV typical) differential input signal levels
- Supports open, short, and terminated input fail-safe
- Conforms to TIA/EIA-644 LVDS standard
- Industrial operating temperature range of -40°C to +85°C
- Available in surface-mount SOIC package and low profile TSSOP package

### APPLICATIONS

- Point-to-point data transmission
- Multidrop buses
- Clock distribution networks
- Backplane receivers

### GENERAL DESCRIPTION

The ADN4666 is a quad-channel, CMOS low voltage differential signaling (LVDS) line receiver offering data rates of over 400 Mbps (200 MHz) and ultralow power consumption.

The device accepts low voltage (350 mV typical) differential input signals and converts them to a single-ended, 3 V TTL/CMOS logic level.

The ADN4666 also offers active high and active low enable/disable inputs (EN and  $\overline{\text{EN}}$ ) that control all four receivers. These inputs

### FUNCTIONAL BLOCK DIAGRAM

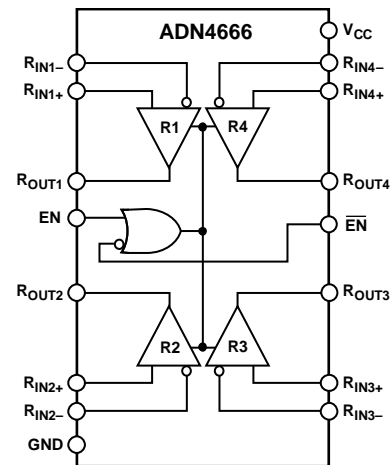


Figure 1.

disable the receivers and switch the outputs to a high impedance state. Consequently, the outputs of one or more ADN4666 devices can be multiplexed together to reduce the quiescent power consumption to 10 mW typical.

The ADN4666 and its companion driver, the [ADN4665](#), offer a new solution to high speed, point-to-point data transmission and offer a low power alternative to emitter-coupled logic (ECL) or positive emitter-coupled logic (PECL).

#### Rev. 0

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## REVISION HISTORY

6/09—Revision 0: Initial Version

## SPECIFICATIONS

$V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $C_L = 15\text{ pF}$  to GND, all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.<sup>1, 2</sup>

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>LVDS INPUTS (<math>R_{INX+}</math>, <math>R_{INX-}</math>)</b>						
Differential Input High Threshold at $R_{INX+}$ , $R_{INX-}$ <sup>3</sup>	$V_{TH}$		20	100	mV	$V_{CM} = 1.2\text{ V}$ , $0.05\text{ V}$ , $2.95\text{ V}$
Differential Input Low Threshold at $R_{INX+}$ , $R_{INX-}$ <sup>3</sup>	$V_{TL}$	-100	-20		mV	$V_{CM} = 1.2\text{ V}$ , $0.05\text{ V}$ , $2.95\text{ V}$
Common-Mode Voltage Range at $R_{INX+}$ , $R_{INX-}$ <sup>4</sup>	$V_{CMR}$	0.1		2.3	V	$V_{ID} = 200\text{ mV p-p}$
Input Current at $R_{INX+}$ , $R_{INX-}$	$I_{IN}$	-10	$\pm 5$	+10	$\mu\text{A}$	$V_{IN} = 2.8\text{ V}$ , $V_{CC} = 3.6\text{ V}$ or $0\text{ V}$
		-10	$\pm 1$	+10	$\mu\text{A}$	$V_{IN} = 0\text{ V}$ , $V_{CC} = 3.6\text{ V}$ or $0\text{ V}$
		-20	$\pm 1$	+20	$\mu\text{A}$	$V_{IN} = 3.6\text{ V}$ , $V_{CC} = 0\text{ V}$
Input High Voltage	$V_{IH}$	2.0		$V_{CC}$	V	
Input Low Voltage	$V_{IL}$	GND		0.8	V	
Input Current	$I_{IN}$	-10	$\pm 1$	+10	$\mu\text{A}$	$V_{IN} = 0\text{ V}$ or $V_{CC}$ , other input = $V_{CC}$ or GND
Input Clamp Voltage	$V_{CL}$	-1.5	-0.8		V	$I_{CL} = -18\text{ mA}$
<b>OUTPUTS (<math>R_{OUTX}</math>)</b>						
Output High Voltage	$V_{OH}$	2.7	3.0		V	$I_{OH} = -0.4\text{ mA}$ , $V_{ID} = 200\text{ mV}$
		2.7	3.0		V	$I_{OH} = -0.4\text{ mA}$ , input terminated
		2.7	3.0		V	$I_{OH} = -0.4\text{ mA}$ , input shorted
Output Low Voltage	$V_{OL}$		0.1	0.25	V	$I_{OL} = 2\text{ mA}$ , $V_{ID} = -200\text{ mV}$
Output Short-Circuit Current <sup>5</sup>	$I_{OS}$	-15	-48	-120	mA	Outputs enabled, $V_{OUT} = 0\text{ V}$
Output Off State Current	$I_{OZ}$	-10	$\pm 1$	+10	$\mu\text{A}$	Outputs disabled, $V_{OUT} = 0\text{ V}$ or $V_{CC}$
<b>POWER SUPPLY</b>						
No Load Supply, Current Receivers Enabled	$I_{CC}$		10	15	mA	$\overline{EN}$ and $\overline{EN} = V_{CC}$ or GND, inputs open
No Load Supply, Current Receivers Disabled	$I_{CCZ}$		3	5	mA	$\overline{EN} = \text{GND}$ and $\overline{EN} = V_{CC}$ , inputs open
<b>ESD PROTECTION</b>						
$R_{INX+}$ , $R_{INX-}$ Pins			$\pm 8$		kV	IEC 61000-4-2 contact discharge
			$\pm 15$		kV	Human body model
All Pins Except $R_{INX+}$ , $R_{INX-}$			$\pm 4$		kV	Human body model

<sup>1</sup> Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground, unless otherwise specified.

<sup>2</sup> All typical values are given for  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

<sup>3</sup>  $V_{CC}$  is always higher than the  $R_{INX+}$  and  $R_{INX-}$  voltage.  $R_{INX-}$  and  $R_{INX+}$  have a voltage range of  $-0.2\text{ V}$  to  $V_{CC} - V_{ID}/2$ . However, to be compliant with ac specifications, the common-mode voltage range is  $0.1\text{ V}$  to  $2.3\text{ V}$ .

<sup>4</sup>  $V_{CMR}$  is reduced for larger input differential voltage ( $V_{ID}$ ). For example, if  $V_{ID}$  is  $400\text{ mV}$ ,  $V_{CMR}$  is  $0.2\text{ V}$  to  $2.2\text{ V}$ . The fail-safe condition with inputs shorted is not supported over the common-mode range of  $0\text{ V}$  to  $2.4\text{ V}$ , but is supported only with inputs shorted and no external common-mode voltage applied.  $V_{ID}$  up to  $V_{CC} - 0\text{ V}$  can be applied to the  $R_{INX+}/R_{INX-}$  inputs with the common-mode voltage set to  $V_{CC}/2$ . Propagation delay and differential pulse skew decrease when  $V_{ID}$  is increased from  $200\text{ mV}$  to  $400\text{ mV}$ . Skew specifications apply for  $200\text{ mV} \leq V_{ID} \leq 800\text{ mV}$  over the common-mode range.

<sup>5</sup> Output short-circuit current ( $I_{OS}$ ) is specified as magnitude only; a minus sign indicates direction only. Note that only one output should be shorted at a time; do not exceed the maximum junction temperature specification ( $150^\circ\text{C}$ ).

# ADN4666

## TIMING SPECIFICATIONS

$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $C_L = 15\text{ pF to GND}$ , all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.<sup>1</sup>

Table 2.

Parameter <sup>2</sup>	Symbol	Min	Typ <sup>3</sup>	Max	Unit	Test Conditions/Comments <sup>4, 5</sup>
AC CHARACTERISTICS						
Differential Propagation Delay, High to Low	$t_{PHLD}$	1.8		3.3	ns	$C_L = 15\text{ pF}$ , $V_{ID} = 300\text{ mV}$ (see Figure 2 and Figure 3)
Differential Propagation Delay, Low to High	$t_{PLHD}$	1.8		3.3	ns	$C_L = 15\text{ pF}$ , $V_{ID} = 300\text{ mV}$ (see Figure 2 and Figure 3)
Differential Pulse Skew <sup>6</sup> $ t_{PHLD} - t_{PLHD} $	$t_{SKD1}$	0	0.1	0.35	ns	$C_L = 15\text{ pF}$ , $V_{ID} = 300\text{ mV}$ (see Figure 2 and Figure 3)
Differential Channel-to-Channel Skew (Same Device) <sup>7</sup>	$t_{SKD2}$	0	0.1	0.5	ns	$C_L = 15\text{ pF}$ , $V_{ID} = 300\text{ mV}$ (see Figure 2 and Figure 3)
Differential Part-to-Part Skew <sup>8</sup>	$t_{SKD3}$			1.0	ns	$C_L = 15\text{ pF}$ , $V_{ID} = 300\text{ mV}$ (see Figure 2 and Figure 3)
Differential Part-to-Part Skew <sup>9</sup>	$t_{SKD4}$			1.5	ns	$C_L = 15\text{ pF}$ , $V_{ID} = 300\text{ mV}$ (see Figure 2 and Figure 3)
Rise Time	$t_{TLH}$		0.35	1.2	ns	$C_L = 15\text{ pF}$ , $V_{ID} = 300\text{ mV}$ (see Figure 2 and Figure 3)
Fall Time	$t_{THL}$		0.35	1.2	ns	$C_L = 15\text{ pF}$ , $V_{ID} = 300\text{ mV}$ (see Figure 2 and Figure 3)
Disable Time, High to Z	$t_{PHZ}$		8	12	ns	$R_L = 2\text{ k}\Omega$ , $C_L = 15\text{ pF}$ (see Figure 4 and Figure 5)
Disable Time, Low to Z	$t_{PLZ}$		8	12	ns	$R_L = 2\text{ k}\Omega$ , $C_L = 15\text{ pF}$ (see Figure 4 and Figure 5)
Enable Time, Z to High	$t_{PZH}$		11	17	ns	$R_L = 2\text{ k}\Omega$ , $C_L = 15\text{ pF}$ (see Figure 4 and Figure 5)
Enable Time, Z to Low	$t_{PZL}$		11	17	ns	$R_L = 2\text{ k}\Omega$ , $C_L = 15\text{ pF}$ (see Figure 4 and Figure 5)
Maximum Operating Frequency <sup>10</sup>	$f_{MAX}$	200	250		MHz	All channels switching

<sup>1</sup> Generator waveform for all tests, unless otherwise specified:  $f = 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_{TLH}$  and  $t_{THL}$  (0% to 100%)  $\leq 3\text{ ns}$  for  $R_{INx+}/R_{INx-}$ .

<sup>2</sup> AC parameters are guaranteed by design and characterization.

<sup>3</sup> All typical values are given for  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

<sup>4</sup> Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground, unless otherwise specified.

<sup>5</sup>  $C_L$  includes load and jig capacitance.

<sup>6</sup>  $t_{SKD1}$  is the magnitude difference in the differential propagation delay time between the positive-going edge and the negative-going edge of the same channel.

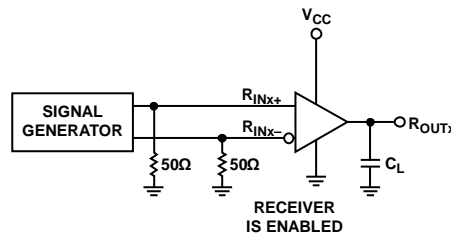
<sup>7</sup> Channel-to-channel skew,  $t_{SKD2}$ , is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.

<sup>8</sup>  $t_{SKD3}$  part-to-part skew is the differential channel-to-channel skew of any event between devices. The  $t_{SKD3}$  specification applies to devices at the same  $V_{CC}$  and within  $5^\circ\text{C}$  of each other within the operating temperature range.

<sup>9</sup>  $t_{SKD4}$  part-to-part skew is the differential channel-to-channel skew of any event between devices. The  $t_{SKD4}$  specification applies to devices over the recommended operating temperature and voltage ranges and across process distribution.  $t_{SKD4}$  is defined as |maximum – minimum| differential propagation delay.

<sup>10</sup>  $f_{MAX}$  generator input conditions:  $f = 200\text{ MHz}$ ,  $t_{TLH} = t_{THL} < 1\text{ ns}$  (0% to 100%), 50% duty cycle, differential (1.05 V to 1.35 V p-p).  $f_{MAX}$  generator output criteria: 60%/40% duty cycle,  $V_{OL}$  (maximum = 0.4 V),  $V_{OH}$  (minimum = 2.7 V), and load = 15 pF (stray plus probes).

## Test Circuits and Timing Diagrams



### NOTES

- $C_L = \text{LOAD AND TEST JIG CAPACITANCE.}$

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Figure 2. Test Circuit for Receiver Propagation Delay and Transition Time

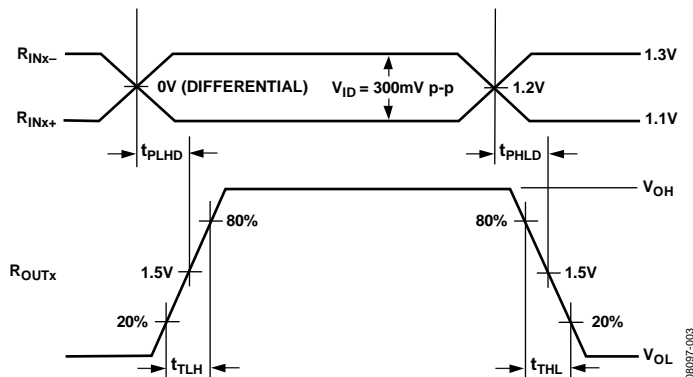
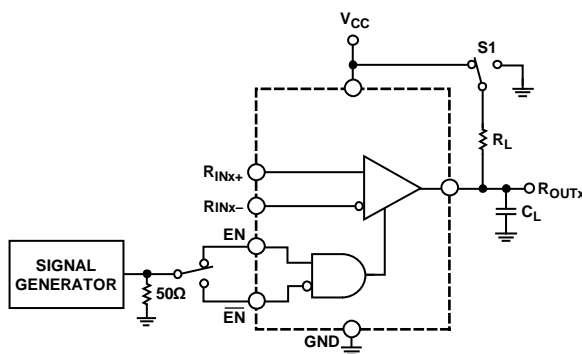


Figure 3. Receiver Propagation Delay and Transition Time Waveforms



- NOTES
1.  $C_L$  INCLUDES LOAD AND TEST JIG CAPACITANCE.
  2. S1 CONNECTED TO  $V_{CC}$  FOR  $t_{PZL}$  AND  $t_{PLZ}$  MEASUREMENTS.
  3. S1 CONNECTED TO GND FOR  $t_{PZH}$  AND  $t_{PHZ}$  MEASUREMENTS.

Figure 4. Test Circuit for Receiver Enable/Disable Delay

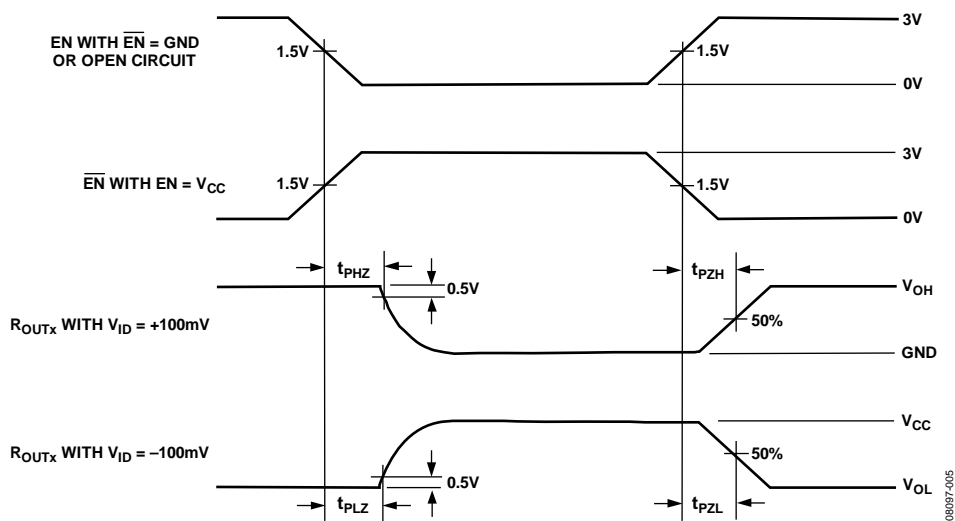


Figure 5. Receiver Enable/Disable Delay Waveforms

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
$V_{CC}$ to GND	-0.3 V to +4 V
Input Voltage ( $R_{INX+}$ , $R_{INX-}$ ) to GND	-0.3 V to $V_{CC} + 0.3$ V
Enable Input Voltage ( $\overline{EN}$ , $\overline{EN}$ ) to GND	-0.3 V to $V_{CC} + 0.3$ V
Output Voltage ( $R_{OUTX}$ ) to GND	-0.3 V to $V_{CC} + 0.3$ V
Industrial Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature ( $T_{J\text{MAX}}$ )	150°C
$\theta_{JA}$ Thermal Impedance	150.4°C/W
Power Dissipation	$(T_{J\text{MAX}} - T_A)/\theta_{JA}$
Reflow Soldering Peak Temperature, Pb-Free	260°C $\pm$ 5°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

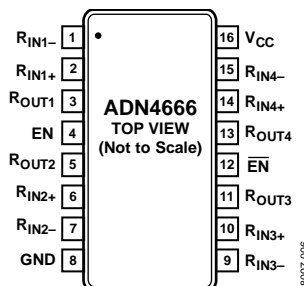


Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RIN1-	Receiver Channel 1 Inverting Input. When this input is more negative than RIN1+, ROUT1 is high. When this input is more positive than RIN1+, ROUT1 is low.
2	RIN1+	Receiver Channel 1 Noninverting Input. When this input is more positive than RIN1-, ROUT1 is high. When this input is more negative than RIN1-, ROUT1 is low.
3	ROUT1	Receiver Channel 1 Output (3 V TTL/CMOS). If the differential input voltage between RIN1+ and RIN1- is positive, this output is high. If the differential input voltage is negative, this output is low.
4	EN	Active High Enable and Power-Down Input (3 V TTL/CMOS). When EN is low and $\overline{\text{EN}}$ is high, the receiver outputs are disabled and are in a high impedance state. When EN is high and $\overline{\text{EN}}$ is low or when EN is low and $\overline{\text{EN}}$ is low, the receiver outputs are enabled. When EN is high and $\overline{\text{EN}}$ is high, the receiver outputs are enabled.
5	ROUT2	Receiver Channel 2 Output (3 V TTL/CMOS). If the differential input voltage between RIN2+ and RIN2- is positive, this output is high. If the differential input voltage is negative, this output is low.
6	RIN2+	Receiver Channel 2 Noninverting Input. When this input is more positive than RIN2-, ROUT2 is high. When this input is more negative than RIN2-, ROUT2 is low.
7	RIN2-	Receiver Channel 2 Inverting Input. When this input is more negative than RIN2+, ROUT2 is high. When this input is more positive than RIN2+, ROUT2 is low.
8	GND	Ground Reference Point for All Circuitry on the Part.
9	RIN3-	Receiver Channel 3 Inverting Input. When this input is more negative than RIN3+, ROUT3 is high. When this input is more positive than RIN3+, ROUT3 is low.
10	RIN3+	Receiver Channel 3 Noninverting Input. When this input is more positive than RIN3-, ROUT3 is high. When this input is more negative than RIN3-, ROUT3 is low.
11	ROUT3	Receiver Channel 3 Output (3 V TTL/CMOS). If the differential input voltage between RIN3+ and RIN3- is positive, this output is high. If the differential input voltage is negative, this output is low.
12	$\overline{\text{EN}}$	Active Low Enable and Power-Down Input with Pull-Down (3 V TTL/CMOS). When EN is low and $\overline{\text{EN}}$ is high, the receiver outputs are disabled and are in a high impedance state. When EN is high and $\overline{\text{EN}}$ is low or when EN is low and $\overline{\text{EN}}$ is low, the receiver outputs are enabled. When EN is high and $\overline{\text{EN}}$ is high, the receiver outputs are enabled.
13	ROUT4	Receiver Channel 4 Output (3 V TTL/CMOS). If the differential input voltage between RIN4+ and RIN4- is positive, this output is high. If the differential input voltage is negative, this output is low.
14	RIN4+	Receiver Channel 4 Noninverting Input. When this input is more positive than RIN4-, ROUT4 is high. When this input is more negative than RIN4-, ROUT4 is low.
15	RIN4-	Receiver Channel 4 Inverting Input. When this input is more negative than RIN4+, ROUT4 is high. When this input is more positive than RIN4+, ROUT4 is low.
16	VCC	Power Supply Input. The ADN4666 can be operated from 3.0 V to 3.6 V.

## TYPICAL PERFORMANCE CHARACTERISTICS

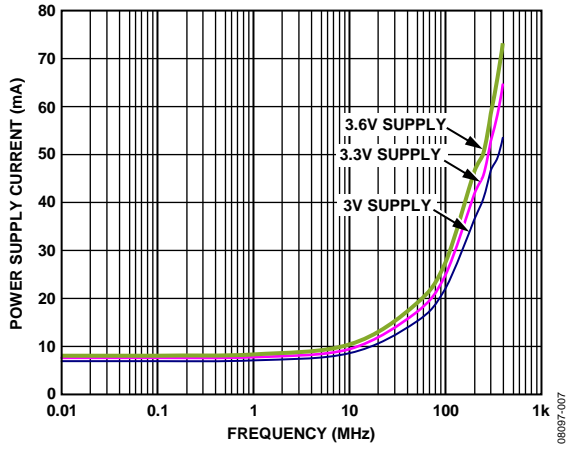


Figure 7. Power Supply Current vs. Frequency

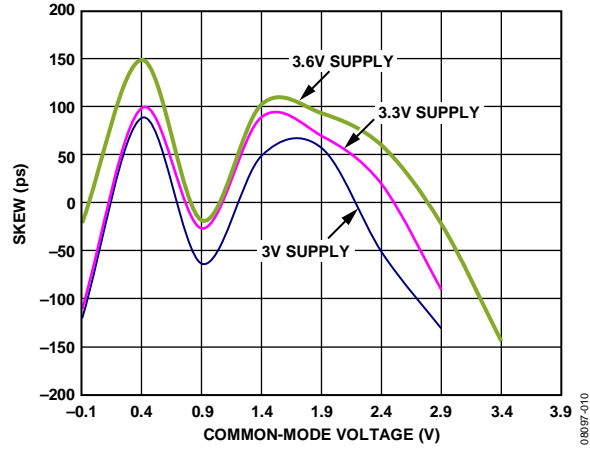


Figure 10. Skew vs. Common-Mode Voltage, 25°C

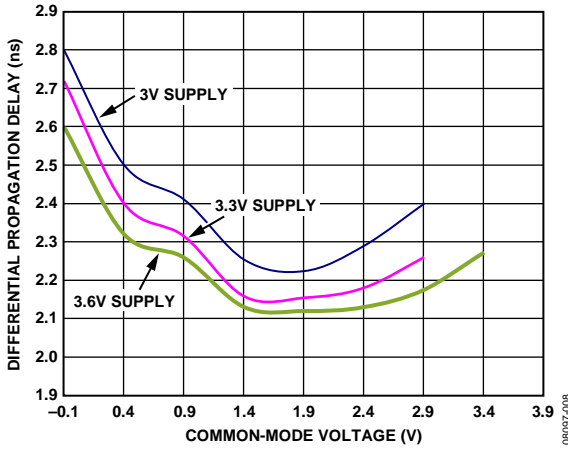


Figure 8. Differential Propagation Delay ( $t_{PLHD}$ ) vs. Common-Mode Voltage, 25°C

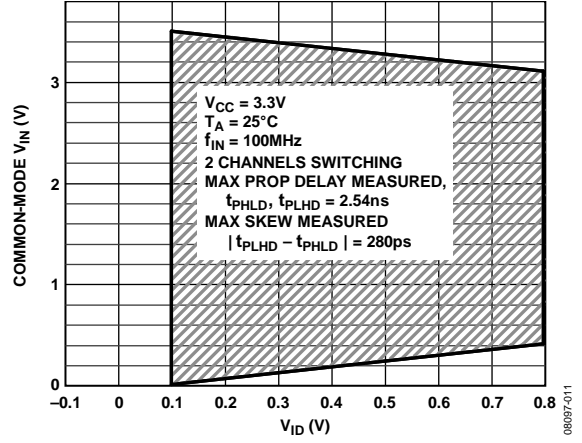


Figure 11. Typical Common-Mode Range Variation with Respect to the Amplitude of the Differential Input

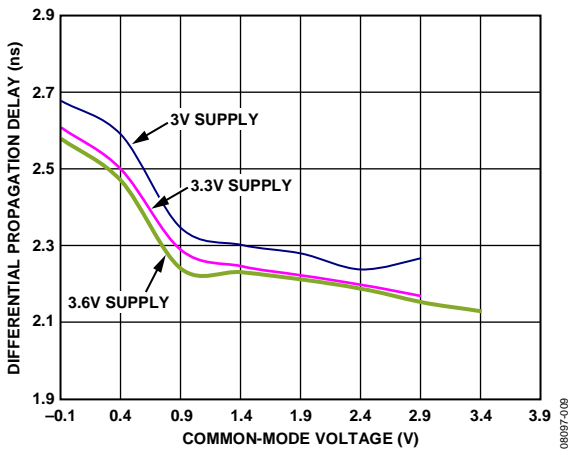


Figure 9. Differential Propagation Delay ( $t_{PLHD}$ ) vs. Common-Mode Voltage, 25°C

## THEORY OF OPERATION

The ADN4666 is a quad-channel line receiver for low voltage differential signaling (LVDS). It takes a differential input signal of 350 mV typical and converts it into a single-ended, 3 V TTL/CMOS logic signal.

A differential current input signal, received via a transmission medium such as a twisted pair cable, develops a voltage across a termination resistor,  $R_T$ . This resistor is chosen to match the characteristic impedance of the medium, typically around 100  $\Omega$ . The differential voltage is detected by the receiver and converted back into a single-ended logic signal.

When the noninverting receiver input,  $R_{INx+}$ , is positive with respect to the inverting input,  $R_{INx-}$  (that is, when current flows through  $R_T$  from  $R_{INx+}$  to  $R_{INx-}$ ),  $R_{OUTx}$  is high. When the noninverting receiver input,  $R_{INx+}$ , is negative with respect to the inverting input,  $R_{INx-}$  (that is, when current flows through  $R_T$  from  $R_{INx-}$  to  $R_{INx+}$ ),  $R_{OUTx}$  is low.

Using the ADN4665 as a driver, the received differential current is between  $\pm 2.5$  mA and  $\pm 4.5$  mA ( $\pm 3.5$  mA typical), developing between  $\pm 250$  mV and  $\pm 450$  mV across a 100  $\Omega$  termination resistor. The received voltage is centered around the receiver offset of 1.2 V. Therefore, the noninverting receiver input is typically 1.375 V (that is,  $1.2 \text{ V} + [350 \text{ mV}/2]$ ) and the inverting receiver input is 1.025 V (that is,  $1.2 \text{ V} - [350 \text{ mV}/2]$ ) for a Logic 1. For a Logic 0, the inverting and noninverting input voltages are reversed. Note that because the differential voltage reverses polarity, the peak-to-peak voltage swing across  $R_T$  is twice the differential voltage.

Current-mode drivers offer considerable advantages over voltage-mode drivers, such as the RS-422 drivers. The operating current remains fairly constant with increased switching frequency, whereas the operating current of voltage-mode drivers increases exponentially in most cases. This increase is caused by the overlap as internal gates switch between high and low, causing currents to flow from  $V_{CC}$  to ground. A current-mode device reverses a constant current between its two outputs, with no significant overlap currents.

This is similar to emitter-coupled logic (ECL) and positive emitter-coupled logic (PECL), but without the high quiescent current of ECL and PECL.

### ENABLE INPUTS

The ADN4666 has active high and active low enable inputs that put all the logic outputs into a high impedance state when disabled, reducing device current consumption from 10 mA typical to 3 mA typical. See Table 5 for a truth table of the enable inputs.

Table 5. Enable Inputs Truth Table

Pin Logic Level		$R_{INx+}$	$R_{INx-}$	$R_{OUTx}$
EN	$\overline{\text{EN}}$			
Low	High	X <sup>1</sup>	X <sup>1</sup>	High-Z
Low	Low	1.025 V	1.375 V	0
Low	Low	1.375 V	1.025 V	1
High	Low	1.025 V	1.375 V	0
High	Low	1.375 V	1.025 V	1

<sup>1</sup> X = don't care.

### APPLICATIONS INFORMATION

Figure 12 shows a typical application for point-to-point data transmission using the ADN4665 as the driver and the ADN4666 as the receiver.

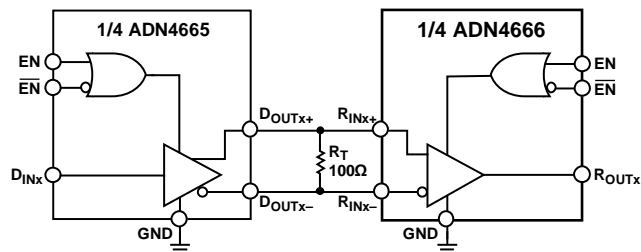
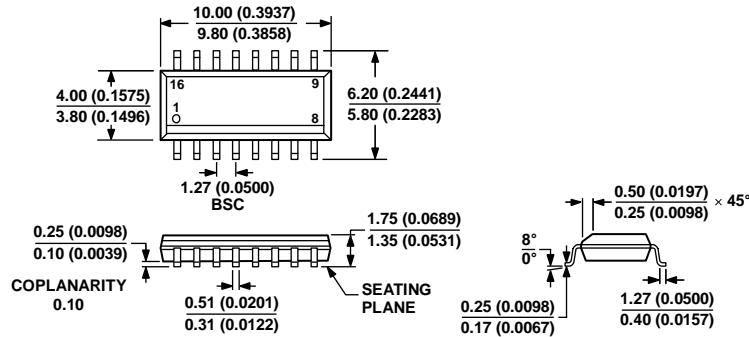


Figure 12. Typical Application Circuit

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## OUTLINE DIMENSIONS



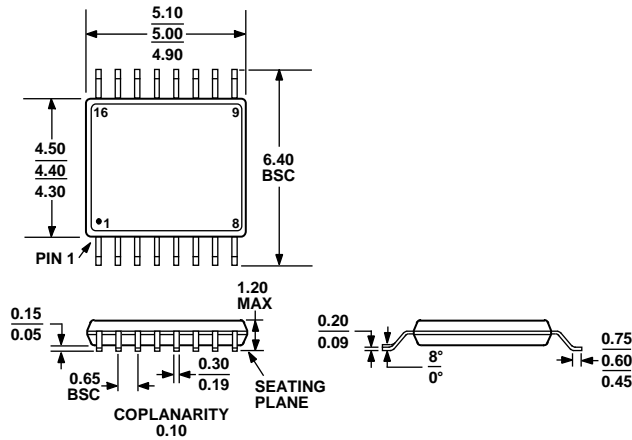
COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 13. 16-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-16)

Dimensions shown in millimeters and (inches)

060606-A



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 14. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADN4666ARZ <sup>1</sup>	-40°C to +85°C	16-Lead Thin Standard Small Outline Package [SOIC_N]	R-16
ADN4666ARZ-REEL <sup>7</sup>	-40°C to +85°C	16-Lead Thin Standard Small Outline Package [SOIC_N]	R-16
ADN4666ARUZ <sup>1</sup>	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADN4666ARUZ-REEL <sup>7</sup>	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**ADN4666**

**NOTES**

## Looking for pricing, stock, or lifecycle information?

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- ⊖ [View ADN4666ARUZ on WIN SOURCE](#)
- ⊖ [Analog Devices Inc. Information](#)

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