THE DATASHEET OF

MAX9258AGCM/V+T

www.win-source.net 0086-755-83957316

19-5891; Rev 1; 9/11

EVALUATION KIT AVAILABLE

MAX9257A/MAX9258A

Fully Programmable Serializer/Deserializer with UART/I²C Control Channel

General Description

The MAX9257A serializer pairs with the MAX9258A deserializer to form a complete digital video serial link. The devices feature programmable parallel data width, parallel clock frequency range, spread spectrum, and preemphasis. An integrated control channel transfers data bidirectionally at power-up during video blanking over the same differential pair used for video data. This feature eliminates the need for external CAN or LIN interface for diagnostics or programming. The clock is recovered from input serial data at MAX9258A, hence eliminating the need for an external reference clock.

The MAX9257A serializes 10, 12, 14, 16, and 18 bits with the addition of two encoding bits for AC-coupling. The MAX9258A deserializer links with the MAX9257A to deserialize a maximum of 20 (data + encoding) bits per pixel/parallel clock period for a maximum serial-data rate of 840Mbps. The word length can be adjusted to accommodate a higher pixel/parallel clock frequency. The pixel clock can vary from 5MHz to 70MHz, depending on the serial-word length. Enabling parity adds two parity bits to the serial word. The encoding bits reduce ISI and allow AC-coupling.

The MAX9258A receives programming instructions from the electronic control unit (ECU) during the control channel and transmits to the MAX9257A over the serial video link. The instructions can program or update the MAX9257A, MAX9258A, or an external peripheral device, such as a camera. The MAX9257A communicates with the peripheral device with I²C or UART.

The devices operate from a +3.3V core supply and feature separate supplies for interfacing to +1.8V to +3.3V logic levels. These devices are available in 40-lead TQFN or 48-pin LQFP packages. These devices are specified over the -40°C to +105°C temperature range.

Applications

Automotive Cameras

Industrial Cameras

Navigation Systems Display

In-Vehicle Entertainment Systems

Features

- **10/12/14/16/18-Bit Programmable Parallel Data Width**
- **MAX9258A Does Not Require Reference Clock**
- **Parity Protection for Video and Control Channels**
- **Programmable Spread Spectrum**
- **Programmable Rising or Falling Edge for HSYNC, VSYNC, and Clock**
- **Up to 10 Remotely Programmable GPIO on MAX9257A**
- **Automatic Resynchronization in Case of Loss of Lock**
- **MAX9257A Parallel Clock Jitter Filter PLL with Bypass**
- **DC-Balanced Coding Allows AC-Coupling**
- **Levels of Preemphasis for Up to 20m STP Cable Drive**
- **Integrity Test Using On-Chip Programmable PRBS Generator and Checker**
- **LVDS I/O Meet ISO 10605 ESD Protection (±10kV Contact and ±30kV Air Discharge)**
- **LVDS I/O Meet IEC 61000-4-2 ESD Protection (±8kV Contact and ±20kV Air Discharge)**
- **LVDS I/O Meet ±200V Machine Model ESD Protection**
- **-40°C to +105°C Operating Temperature Range**
- **Space-Saving, 40-Pin TQFN (5mm x 5mm) with Exposed Pad or 48-Pin LQFP Packages**
- **3.3V Core Supply and 1.8V to 3.3V I/O Supply**

***Ordering Information** appears at end of data sheet.*

Typical Operating Circuit and Pin Configurations appear at end of data sheet.

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX9257A.related**.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

$V_{CC_}$ to GND ..... -0.5V to +4.0V
Any Ground to Any Ground ..... -0.5V to +0.5V
SDI+, SDI-, SDO+, SDO- to GND ..... -0.5V to +4.0V
SDO+, SDO- Short Circuit to GND or V_{CCLVDS} ..... Continuous
DIN[0:15], GPIO[0:9], PCLK_IN, HSYNC_IN, VSYNC_IN, SCL/TX, SDA/RX, REM to GND ..... -0.5V to (V_{CCIO} + 0.5V)
DOUT[0:15], PCLK_OUT, CCEN, HSYNC_OUT, VSYNC_OUT, RX, LOCK, TX, $\overline{PD}$, ERROR to GND ..... -0.5V to (V_{CCOUT} + 0.5V)
Continuous Power Dissipation (TA = +70°C)
40-Lead TQFN
Multilayer PCB (derate 35.7mW/°C above +70°C) ... 2857mW
48-Lead LQFP
Multilayer PCB (derate 21.7mW/°C above +70°C) ... 1739mW
ESD Protection
Human Body Model (RD = 1.5kΩ, CS = 100pF)
All Pins to GND ..... ±3kV
IEC 61000-4-2 (RD = 330Ω, CS = 150pF)
Contact Discharge
(SDI+, SDI-, SDO+, SDO-) to GND ..... ±8kV
Air Discharge
(SDI+, SDI-, SDO+, SDO-) to GND ..... ±20kV
ISO 10605 (RD = 2kΩ, CS = 330pF)
Contact Discharge
(SDI+, SDI-, SDO+, SDO-) to GND ..... ±10kV
Air Discharge
(SDI+, SDI-, SDO+, SDO-) to GND ..... ±30kV
Machine Model (RD = 0Ω, CS = 200pF)
All Pins to GND ..... ±200V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA})
40-Pin TQFN ..... 28°C/W
48-Pin LQFP ..... 46°C/W
Junction-to-Case Thermal Resistance (θ_{JC})
40-Pin TQFN ..... 1.7°C/W
48-Pin LQFP ..... 10°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

MAX9257A DC ELECTRICAL CHARACTERISTICS

($V_{CC_}$ = +3.0V to +3.6V, V_{CCIO} = +1.71V to +3.6V, R_L = 50Ω ±1%, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC_}$ = +3.3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS						
High-Level Input Voltage	V_{IH}	V_{CCIO} = +1.71V to +3V	0.65 x V_{CCIO}		V_{CCIO} + 0.3	V
		V_{CCIO} = +3V to +3.6V	2		V_{CCIO} + 0.3	
		REM input	2		V_{CC} + 0.3	
Low-Level Input Voltage	V_{IL}	V_{CCIO} = +1.71V to +3V	0		0.3 x V_{CCIO}	V
		V_{CCIO} = +3V to +3.6V	0		0.8	
		REM input	0		0.8	

MAX9257A DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC_}$ = +3.0V to +3.6V, V_{CCIO} = +1.71V to +3.6V, R_L = 50Ω ±1%, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC_}$ = +3.3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current	I_{IN}	V_{IN} = 0 to V_{CCIO}		-20		+20	µA
		V_{IN} = 0 to V_{CC}, REM input		-20		+20	
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
SINGLE-ENDED OUTPUTS							
High-Level Output Voltage	V_{OH}	I_{OH} = -100µA		V_{CCIO} - 0.1			V
		I_{OH} = -2mA		V_{CCIO} - 0.35			
Low-Level Output Voltage	V_{OL}	I_{OL} = 100µA				0.1	V
		I_{OL} = 2mA				0.3	
Output Short-Circuit Current	I_{OS}	Shorted to GND	V_{CCIO} = +1.71V to +3V	-40		-4	mA
			V_{CCIO} = +3V to +3.6V	-50		-10	
		Shorted to V_{CCIO}	V_{CCIO} = +1.71V to +3V	4		40	
			V_{CCIO} = +3V to +3.6V	10		50	
I²C/UART I/O							
Input Leakage Current	I_{ILKG}	V_I = V_{CCIO}		-1		+1	µA
High-Level Input Voltage SDA/RX	V_{IH2}			0.7 x V_{CCIO}			V
Low-Level Input Voltage SDA/RX	V_{IL2}					0.3 x V_{CCIO}	V
Low-Level Output Voltage SCL, SDA	V_{OL2}	R_{PULLUP} = 1.6kΩ to V_{CCIO}				0.4	V
LVDS OUTPUTS (SDO+, SDO-)							
Differential Output Voltage	V_{OD}	Preemphasis off (Figure 1)		250	350	460	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}					25	mV
Common-Mode Voltage	V_{OS}			1.050	1.25	1.375	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}					30	mV
Output Short-Circuit Current	I_{OS}	V_{SDO+} or V_{SDO-} = 0 or 3.6V		-15		+15	mA
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V				15	mA
CONTROL CHANNEL TRANSCEIVER							
Differential Output Voltage	V_{OD}			250	350	460	mV
Input Hysteresis (Figure 2)	V_{HYST+}	Differential low-to-high threshold		25	90	165	mV
	V_{HYST-}	Differential high-to-low threshold		-25	-90	-165	

MAX9257A DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC_}$ = +3.0V to +3.6V, V_{CCIO} = +1.71V to +3.6V, R_L = 50Ω ±1%, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC_}$ = +3.3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Worst-Case Supply Current (Figure 3) C_L = 8pF, 12 bits	I_{CCW}	±2% spread, preemphasis off, PRATE = 60MHz, SRATE = 840Mbps		102	138	mA
		No spread, preemphasis off, PRATE = 60MHz, SRATE = 840Mbps		101	130	
		No spread, preemphasis = 20%, PRATE = 60MHz, SRATE = 840Mbps		102	135	
		No spread, preemphasis = 60%, PRATE = 60MHz, SRATE = 840Mbps		111	137	
		No spread, preemphasis = 100%, PRATE = 60MHz, SRATE = 840Mbps		113	139	
		±2% spread, preemphasis off, PRATE = 28.57MHz, SRATE = 400Mbps		80	104	
		No spread, preemphasis off, PRATE = 28.57MHz, SRATE = 400Mbps		79	100	
		No spread, preemphasis = 100%, PRATE = 28.57MHz, SRATE = 400Mbps		88	111	
		±2% spread, preemphasis off, PRATE = 14.29MHz, SRATE = 200Mbps		56	74	
		No spread, preemphasis off, PRATE = 14.29MHz, SRATE = 200Mbps		55	72	
		No spread, preemphasis = 100%, PRATE = 14.29MHz, SRATE = 200Mbps		61	78	
		±2% spread, preemphasis off, PRATE = 7.14MHz, SRATE = 100Mbps		45	59	
		No spread, preemphasis off, PRATE = 7.14MHz, SRATE = 100Mbps		44	57	
		No spread, preemphasis = 100%, PRATE = 7.14MHz, SRATE = 100Mbps		47	61	
		±2% spread, preemphasis off, PRATE = 5MHz, SRATE = 70Mbps		34	45	
		No spread, preemphasis off, PRATE = 5MHz, SRATE = 70Mbps		34	44	
		No spread, preemphasis = 100%, PRATE = 5MHz, SRATE = 70Mbps		36	47	
Sleep Mode Supply Current	I_{CCS}	Sleep mode			92	µA

MAX9257A AC ELECTRICAL CHARACTERISTICS

($V_{CC_}$ = +3.0V to +3.6V, V_{CCIO} = +1.71V to +3.6V, R_L = 50Ω ±1%, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC_}$ = +3.3V, T_A = +25°C.) (Notes 5, 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PCLK_IN TIMING REQUIREMENTS						
Clock Period	t_T		14.28		200.00	ns
Clock Frequency	f_{CLK}	$1/t_T$	5		70	MHz
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T	35	50	65	%
Clock Transition Time	t_R, t_F	(Figure 7)			4	ns
SWITCHING CHARACTERISTICS						
LVDS Output Rise Time	t_R	20% to 80% (Figure 4)		315	370	ps
LVDS Output Fall Time	t_F	20% to 80% (Figure 4)		315	370	ps
Control Transceiver Transition Time	t_{R1A}, t_{F1A}	20% to 80% (Figure 16)	642	970	1390	ps
	t_{R2}, t_{F2}		810	1140	1420	
	t_{R1B}, t_{F1B}		290	386	490	
Input Setup Time	t_S	(Figure 5)	0			ns
Input Hold Time	t_H	(Figure 5)	3			ns
Parallel-to-Serial Delay	t_{PSD1}	Spread off (Figure 6)			$(4.55 \times t_T) + 11$	ns
	t_{PSD2}	±4% spread			$(36.55 \times t_T) + 11$	
PLL Lock Time	t_{LOCK}	Combined FPLL and SPLL; PCLK_IN stable			$32,768 \times t_T$	ns
Random Jitter	t_{RJ}	420MHz LVDS output, spread off, FPLL = bypassed			12	ps (RMS)
Deterministic Jitter	t_{DJ}	2^{18} - 1 PRBS, SRATE = 840Mbps, 18 bits, no spread			142	ps (P-P)
SCL/TX, SDA/RX						
Rise Time	t_{RS}	0.3 x V_{CCIO} to 0.7 x V_{CCIO}, C_L = 30pF, R_{PULLUP} = 10kΩ			400	ns
		0.3 x V_{CCIO} to 0.7 x V_{CCIO}, C_L = 30pF, R_{PULLUP} = 1.6kΩ			60	
Fall Time	t_{FS}	0.7 x V_{CCIO} to 0.3 x V_{CCIO}, C_L = 30pF			40	ns
Pulse Width of Spike Suppressed in SDA	t_{SPK}	95kbps to 400kbps	100			ns
		400kbps to 1000kbps	50			
		1000kbps to 4250kbps	10			
		DC to 10Mbps (bypass mode)	10			
Data Setup Time	t_{SETUP}	400kbps	100			ns
		4.25Mbps, C_L = 10pF	60			
Data Hold Time	t_{HOLD}	400kbps	100			ns
		4.25Mbps, C_L = 10pF	0			

MAX9257A AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC_}$ = +3.0V to +3.6V, V_{CCIO} = +1.71V to +3.6V, R_L = 50Ω ±1%, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC_}$ = +3.3V, T_A = +25°C.) (Notes 5, 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING (Note 8)						
Maximum SCL Clock Frequency	f_{SCL}			4.25		MHz
Minimum SCL Clock Frequency	f_{SCL}			95		kHz
Start Condition Hold Time	$t_{HD:STA}$	(Figure 30)	0.6			µs
Low Period of SCL Clock	t_{LOW}	(Figure 30)	1.1			µs
High Period of SCL Clock	t_{HIGH}	(Figure 30)	0.6			µs
Repeated START Condition Setup Time	$t_{SU:STA}$	(Figure 30)	0.5			µs
Data Hold Time	$t_{HD:DAT}$	(Figure 30)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Figure 30)	100			ns
Setup Time for STOP Condition	$t_{SU:STO}$	(Figure 30)	0.5			µs
Bus Free Time	t_{BUF}	(Figure 30)	1.1			µs

MAX9258A DC ELECTRICAL CHARACTERISTICS

($V_{CC_}$ = +3.0V to +3.6V, V_{CCIO} = +1.71V to +3.6V, R_L = 50Ω ±1%, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|V_{ID}/2|$, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC_}$ = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS							
High-Level Input Voltage	V_{IH}	V_{CCOUT} = +1.71V to +3V		0.65 x V_{CCOUT}		V_{CCOUT} + 0.3	V
		V_{CCOUT} = +3V to +3.6V		2.0		V_{CCOUT} + 0.3	
Low-Level Input Voltage	V_{IL}	V_{CCOUT} = +1.71V to +3V		0		0.3 x V_{CCOUT}	V
		V_{CCOUT} = +3V to +3.6V		0		0.8	
Input Current	I_{IN}	V_{IN} = 0 to V_{CCOUT}	TXIN	-60		+60	µA
			$\overline{PD}$	-20		+20	
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V

MAX9258A DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC_}$ = +3.0V to +3.6V, V_{CCIO} = +1.71V to +3.6V, R_L = 50Ω ±1%, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|V_{ID}/2|$, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC_}$ = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED OUTPUTS							
High-Level Output Voltage	V_{OH}	I_{OH} = -100µA		V_{CCOUT} - 0.1			V
		I_{OH} = -2mA		V_{CCOUT} -0.35			
Low-Level Output Voltage	V_{OL}	I_{OL} = 100µA				0.1	V
		I_{OL} = 2mA				0.3	
High-Impedance Output Current	I_{OZ}	$\overline{PD}$ = low, V_O = 0 to V_{CCOUT}		-1		+1	µA
Output Short-Circuit Current	I_{OS}	V_O = 0V (Note 4)	V_{CCOUT} = +1.71V to +3V	-4		-44	mA
			V_{CCOUT} = +3V to +3.6V	-16		-65	
		PCLK_OUT, V_O = 0V	V_{CCOUT} = +1.71V to +3.6V	-5		-55.1	
			V_{CCOUT} = +3V to +3.6V	-22		-80	
OPEN-DRAIN OUTPUTS							
Output Low Voltage	V_{OL}	V_{CCOUT} = +3V, I_{OL} = 6.4mA				0.55	V
		V_{CCOUT} = +1.71V, I_{OL} = 1.95mA				0.3	
Leakage Current	I_{LEAK}	V_O = 0V or V_{CCOUT}				1	µA
LVDS INPUTS (SDI+, SDI-)							
Differential Input High Threshold	V_{TH}					50	mV
Differential Input Low Threshold	V_{TL}			-50			mV
Input Current	I_{IN+}, I_{IN-}			-60		+60	µA
Power-Off Input Current	I_{INO+}, I_{INO-}	$V_{CC_}$ = 0 or open		-70		+70	µA
Activity-Detector Input Offset	V_{OFFSET}	ACTOFFSET = 00			23		mV
		ACTOFFSET = 01			11		
		ACTOFFSET = 10			59		
		ACTOFFSET = 11			75		
CONTROL CHANNEL TRANSCEIVER							
Differential Output Voltage	V_{OD}			250		460	mV
Input Hysteresis (Figure 2)	V_{HYST+}	Differential low-to-high threshold		25	90	165	mV
	V_{HYST-}	Differential high-to-low threshold		-25	-90	-165	

MAX9258A DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC_}$ = +3.0V to +3.6V, V_{CCIO} = +1.71V to +3.6V, R_L = 50Ω ±1%, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|V_{ID}/2|$, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC_}$ = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Worst-Case Supply Current C_L = 8pF, 12 bits (Figure 8)	I_{CCW}	±4% spread, PRATE = 60MHz, SRATE = 840Mbps		95	135	mA
		Spread off, PRATE = 60MHz, SRATE = 840Mbps		80	120	
		±4% spread, PRATE = 28.57MHz, SRATE = 400Mbps		67	102	
		Spread off, PRATE = 28.57MHz, SRATE = 400Mbps		57	84	
		±4% spread, PRATE = 14.29MHz, SRATE = 200Mbps		55	82	
		Spread off, PRATE = 14.29MHz, SRATE = 200Mbps		46	67	
		±4% spread, PRATE = 5MHz, SRATE = 70Mbps		42	57	
		Spread off, PRATE = 5MHz, SRATE = 70Mbps		34	49	
Power-Down Supply Current	I_{CCZ}	$\overline{PD}$ = low		10	50	µA

MAX9258A AC ELECTRICAL CHARACTERISTICS

($V_{CC_}$ = +3.0V to +3.6V, V_{CCIO} = +1.71V to +3.6V, R_L = 50Ω ±1%, C_L = 8pF, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - IVID/2I, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC_}$ = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C) (Notes 5, 6 and 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
Output Transition Time	t_R, t_F	(Figure 9)	0.7		2.2	ns
Output Transition Time, PCLK_OUT	t_R, t_F	(Figure 9)	0.5		1.5	ns
Output Transition Time	t_R, t_F	V_{CCOUT} = 1.71V (Figure 9)	1.0		2.8	ns
Output Transition Time, PCLK_OUT	t_R, t_F	V_{CCOUT} = 1.71V (Figure 9)	0.7		2.2	ns
Control Channel Transition Time	t_{R1A}, t_{F1A}, t_{R1B}, t_{F1B}	(Figure 16)	0.5		1.2	ns
Control Channel Transition Time	t_{R2}, t_{F2}	(Figure 16)	0.6		1.3	ns
PCLK_OUT High Time	t_{HIGH}	(Figure 10)	0.4 x t_T		0.6 x t_T	ns
PCLK_OUT Low Time	t_{LOW}	(Figure 10)	0.4 x t_T		0.6 x t_T	ns

MAX9258A AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC_}$ = +3.0V to +3.6V, V_{CCIO} = +1.71V to +3.6V, R_L = 50Ω ±1%, C_L = 8pF, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|VID/2|$, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC_}$ = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C) (Notes 5, 6 and 7)

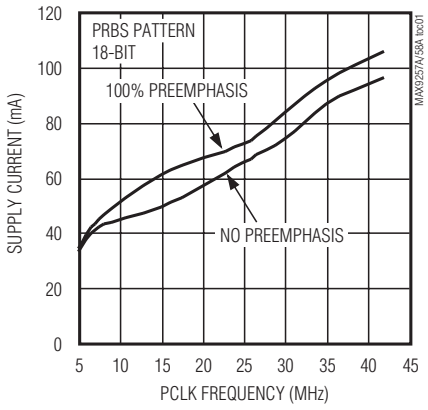
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Data Valid Before PCLK_ OUT	t_{DVB}	(Figure 11)		0.35 x t_T			ns
Data Valid After PCLK_OUT	t_{DVA}	(Figure 11)		0.35 x t_T			ns
Serial-to-Parallel Delay	t_{SPD1}	Spread off (Figure 14)				$8t_T$	ns
	t_{SPD2}	±4% spread				$40t_T$	
Power-Up Delay	t_{PUD}	(Figure 12)				100	ns
Power-Down to High Impedance	t_{PDD}	(Figure 13)				100	ns
Jitter Tolerance	t_{JT}	Each half of the UI, 12 bit, SRATE = 840Mbps, PRBS pattern (Figure 15)	No spread	0.25	0.30		UI

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH} and V_{TL}.
Note 3: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +105°C.
Note 4: One output at a time.
Note 5: AC parameters are guaranteed by design and characterization, and are not production tested.
Note 6: C_L includes probe and test jig capacitance.
Note 7: t_T is the period of the PCLK_OUT.
Note 8: For high-speed mode timing, see the *Detailed Description* section.
Note 9: I²C timing parameters are specified for fast-mode I²C. Max data rate = 400kbps.

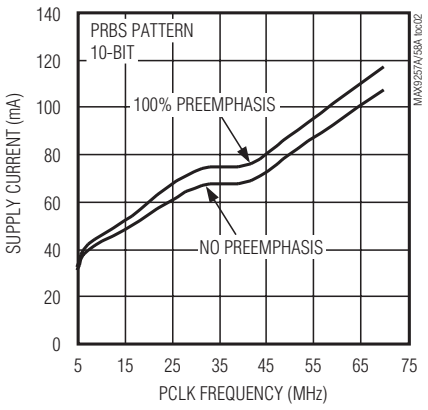
Typical Operating Characteristics

($V_{CC_}$ = +3.3V, R_L = 50O, C_L = 8pF, T_A = +25°C, unless otherwise noted.)

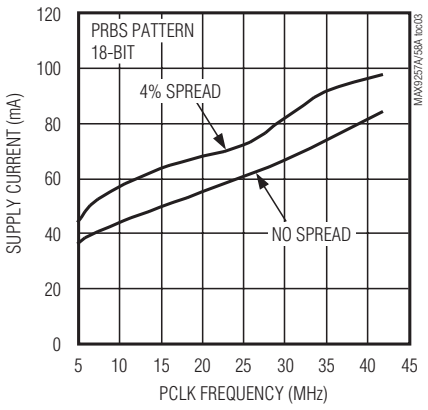
MAX9257A SUPPLY CURRENT vs. FREQUENCY



MAX9257A SUPPLY CURRENT vs. FREQUENCY



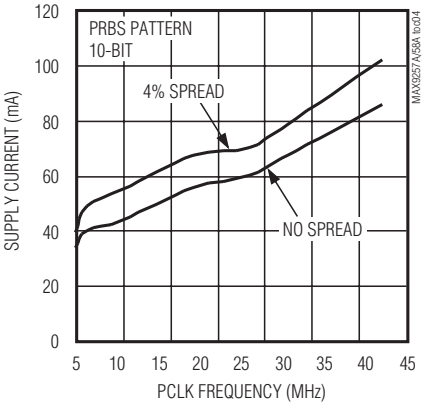
MAX9258A SUPPLY CURRENT vs. FREQUENCY



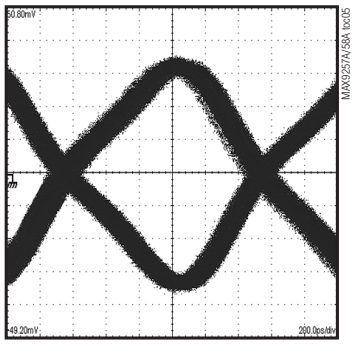
Typical Operating Characteristics (continued)

($V_{CC_}$ = +3.3V, R_L = 50Ω, C_L = 8pF, T_A = +25°C, unless otherwise noted.)

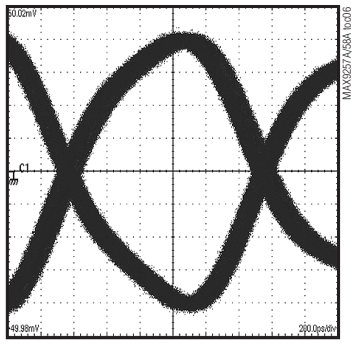
MAX9258A SUPPLY CURRENT vs. FREQUENCY



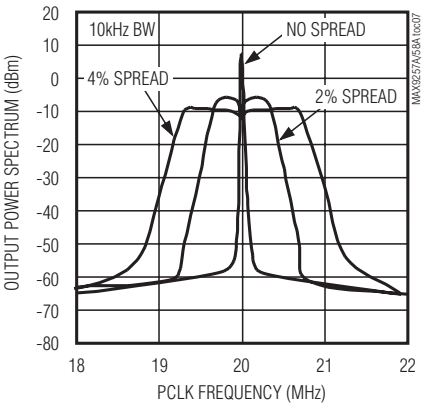
SERIAL LINK SWITCHING PATTERN WITHOUT PREEMPHASIS (BIT RATE = 840MHz, 2m STP CABLE)



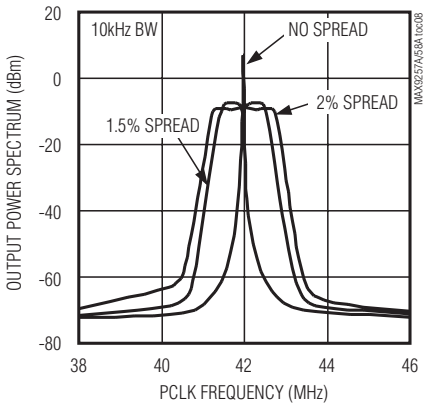
SERIAL LINK SWITCHING PATTERN WITH PREEMPHASIS (BIT RATE = 840MHz, 2m STP CABLE) (PREEMPHASIS = 100%)



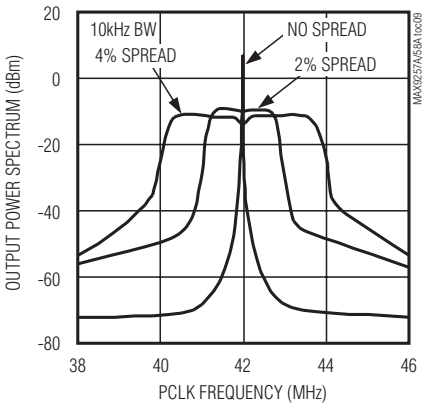
MAX9257A OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY



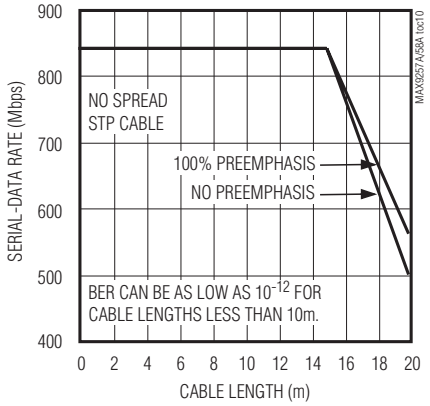
MAX9257A OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY



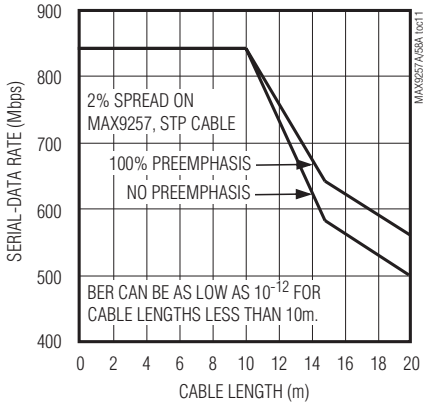
MAX9258A OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY



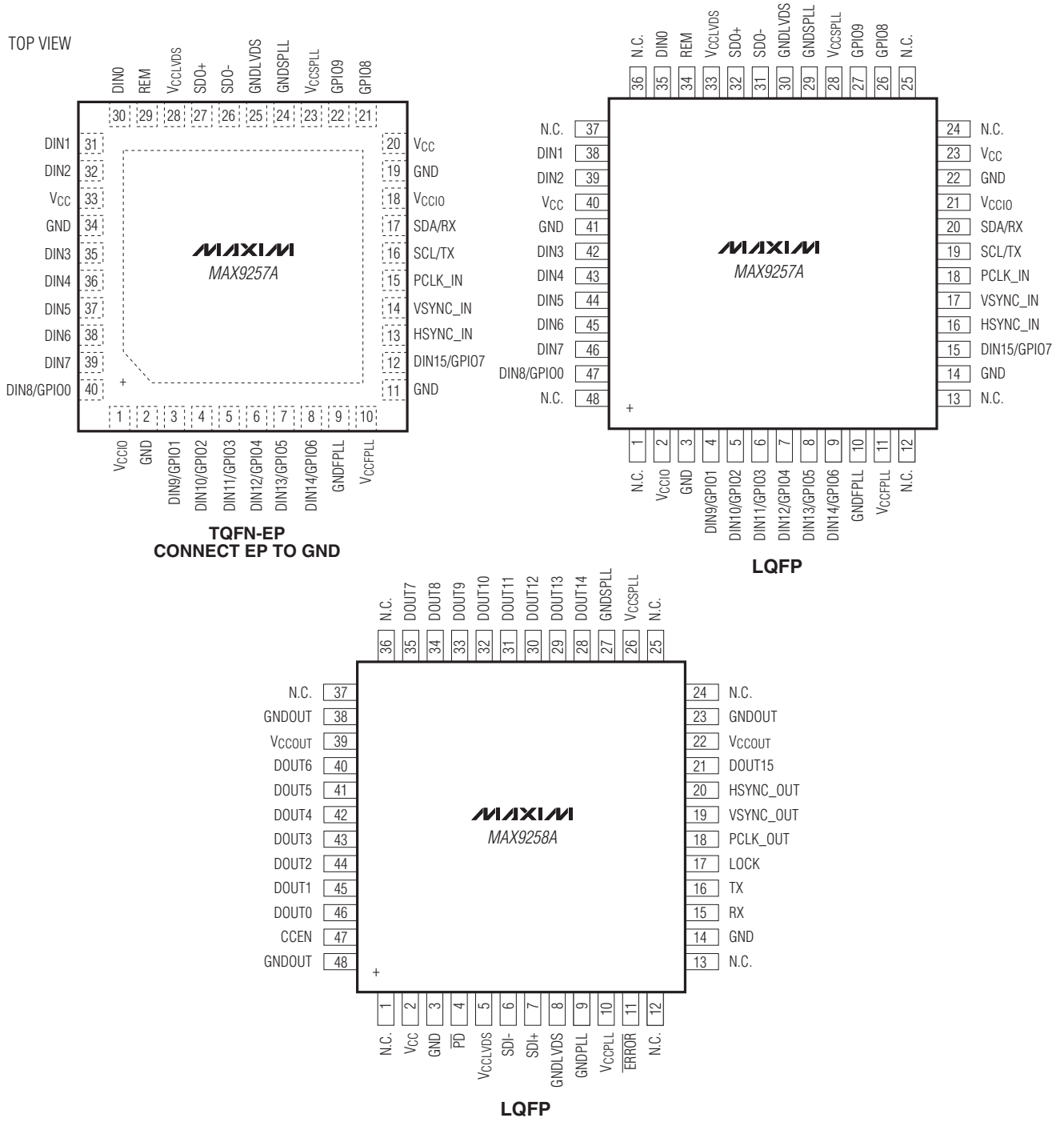
BIT ERROR RATE (< 10^{-9}) vs. CABLE LENGTH



BIT ERROR RATE (< 10^{-9}) vs. CABLE LENGTH



Pin Configuration



MAX9257A Pin Description

PIN		NAME	FUNCTION
TQFN	LQFP		
1, 18	2, 21	V_{CCIO}	Single-Ended Input/Output Buffer Supply Voltage. Bypass V_{CCIO} to GND with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCIO}.
2, 11, 19, 34	3, 14, 22, 41	GND	Digital Supply Ground
3–8	4–9	DIN[9:14]/ GPIO[1:6]	Data Input/General Purpose Input/Output. When a serial-data word is less than 18 bits word length, DIN_ not programmed as data inputs becomes GPIO (Table 22). DIN[9:14] are internally pulled down to ground.
9	10	GNDFPLL	Filter PLL Ground
10	11	V_{CCFPLL}	Filter PLL Supply Voltage. Bypass V_{CCFPLL} to GNDFPLL with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCFPLL}.
12	15	DIN15/GPIO7	Data Input/General Purpose Input/Output. When a serial-data word is less than 18 bits word length, DIN_ not programmed as data input becomes GPIO (Table 22). DIN15 is internally pulled down to ground.
13	16	HSYNC_IN	Horizontal SYNC Input. HSYNC_IN is internally pulled down to ground.
14	17	VSYNC_IN	Vertical SYNC Input. VSYNC_IN is internally pulled down to ground.
15	18	PCLK_IN	Parallel Clock Input. PCLK_IN latches data and sync inputs and provides the PLL reference clock. PCLK_IN is internally pulled down to ground.
16	19	SCL/TX	Open-Drain Control Channel Output. SCL/TX becomes SCL output when UART-to-I²C is active. SCL/TX becomes TX output when UART-to-I²C is bypassed. Externally pull up to V_{CC}.
17	20	SDA/RX	Open-Drain Control Channel Input/Output. SDA/RX becomes bidirectional SDA when UART-to-I²C is active. SDA/RX becomes RX input when UART-to-I²C is bypassed. SDA output requires a pullup to V_{CC}.
20, 33	23, 40	V_{CC}	Digital Supply Voltage. Bypass V_{CC} to ground with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CC}.
21	26	GPIO8	General Purpose Input/Output
22	27	GPIO9	General Purpose Input/Output
23	28	V_{CCSPLL}	Spread PLL Supply Voltage. Bypass V_{CCSPLL} to GNDSPLL with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCSPLL}.
24	29	GNDSPLL	SPLL Ground
25	30	GNDLVDS	LVDS Ground
26	31	SDO-	Serial LVDS Inverting Output
27	32	SDO+	Serial LVDS Noninverting Output
28	33	V_{CCLVDS}	LVDS Supply Voltage. Bypass V_{CCLVDS} to GNDLVDS with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCLVDS}.

MAX9257A Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	LQFP		
29	34	REM	Remote Power-Up/Power-Down Select Input. Connect REM to ground for power-up to follow V_{CC}. Connect REM high to V_{CC} through 10kΩ resistor for remote power-up. REM is internally pulled down to GND.
30, 31, 32, 35–39	35, 38, 39, 42–46	DIN[0:7]	Data Inputs. DIN[0:7] are internally pulled down to ground.
40	47	DIN8/GPIO0	Data Input/General Purpose Input/Output. When a serial-data word is less than 18 bits word length, DIN_ not programmed as data input becomes GPIO (Table 22). DIN8 is internally pulled down to ground.
—	1, 12, 13 24, 25, 36, 37, 48	N.C.	No Connection. Not internally connected.
—	—	EP	Exposed Pad for TQFN Package Only. Connect EP to ground.

MAX9258A Pin Description

PIN	NAME	FUNCTION
1, 12, 13, 24, 25, 36, 37	N.C.	No Connection. Not internally connected.
2	V_{CC}	Digital Supply Voltage. Bypass V_{CC} to GND with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CC}.
3, 14	GND	Digital Supply Ground
4	$\overline{PD}$	LVCMOS/LVTTL Power-Down Input. Drive $\overline{PD}$ high to power up the device and enable all outputs. Drive $\overline{PD}$ low to put all outputs in high impedance and reduce supply current. $\overline{PD}$ is internally pulled down to ground.
5	V_{CCLVDS}	LVDS Supply Voltage. Bypass V_{CCLVDS} to GNDLVDS with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCLVDS}.
6	SDI-	Serial LVDS Inverting Input
7	SDI+	Serial LVDS Noninverting Input
8	GNDLVDS	LVDS Supply Ground
9	GNDPLL	PLL Supply Ground
10	V_{CCPLL}	PLL Supply Voltage. Bypass V_{CCPLL} to GNDPLL with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible with the smallest value capacitor closest to V_{CCPLL}.
11	ERROR	Active-Low, Open-Drain Error Output. ERROR asserts low to indicate a data transfer error was detected (parity, PRBS, or UART control channel error). ERROR is high to indicate no error detected. ERROR resets when the error registers are read for parity, control channel errors, and when PRBS enable bit is reset for PRBS errors. Pull up to V_{CCOUT} with a 1kΩ resistor.
15	RX	LVCMOS/LVTTL Control Channel UART Output

MAX9258A Pin Description (continued)

PIN	NAME	FUNCTION
16	TX	LVCMOS/LVTTL Control Channel UART Input. TX is internally pulled up to V_{CCOUT}.
17	LOCK	Open-Drain Lock Output. LOCK asserts high to indicate PLLs are locked with correct serial-word boundary alignment. LOCK asserts low to indicate PLLs are not locked or incorrect serial-word boundary alignment was detected. Pull up to V_{CCOUT} with a 1kΩ resistor.
18	PCLK_OUT	LVCMOS/LVTTL Recovered Clock Output
19	VSYNC_OUT	LVCMOS/LVTTL Vertical SYNC Output
20	HSYNC_OUT	LVCMOS/LVTTL Horizontal SYNC Output
21, 28–35, 40–46	DOUT[15:0]	LVCMOS/LVTTL Data Outputs
22, 39	V_{CCOUT}	Output Supply Voltage. V_{CCOUT} is the supply for all output buffers. Bypass V_{CCOUT} to GNDOUT with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCOUT}.
23, 38, 48	GNDOUT	Output Supply Ground
26	V_{CCSPLL}	Spread-Spectrum PLL Supply Voltage. Bypass V_{CCSPLL} to GNDSPLL with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCSPLL}.
27	GNDSPLL	SPLL Ground
47	CCEN	LVCMOS/LVTTL Control Channel Enabled Output. CCEN asserts high to indicate that control channel is enabled.

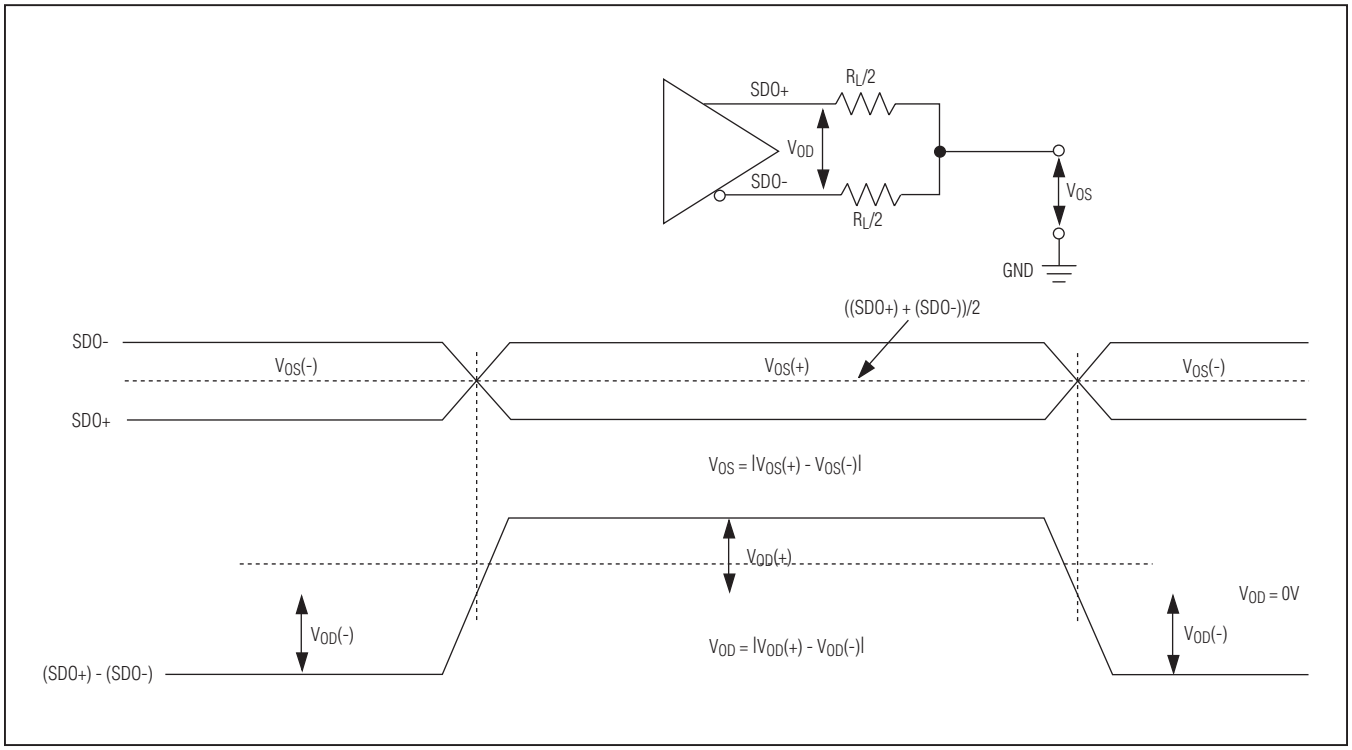


Figure 1. MAX9257A LVDS DC Output Parameters

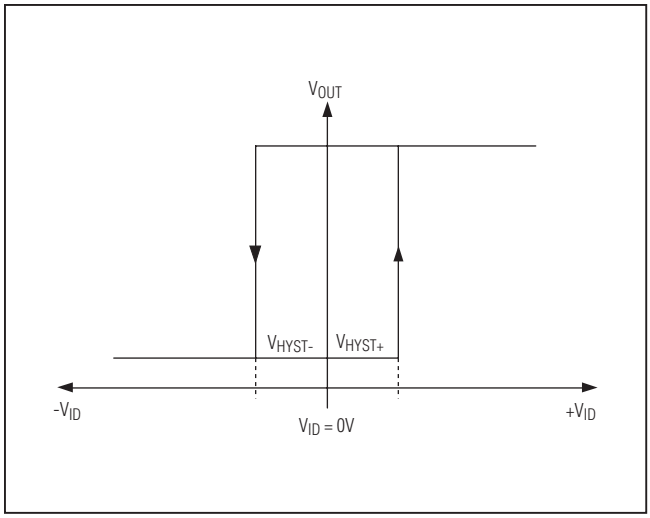


Figure 2. Input Hysteresis

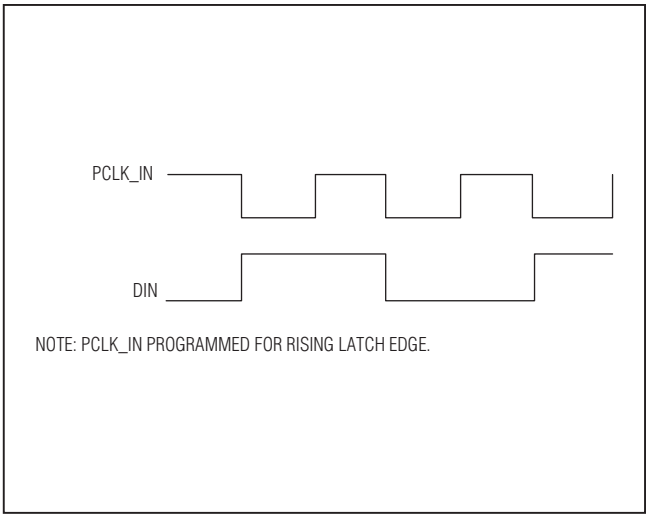


Figure 3. MAX9257A Worst-Case Pattern Input

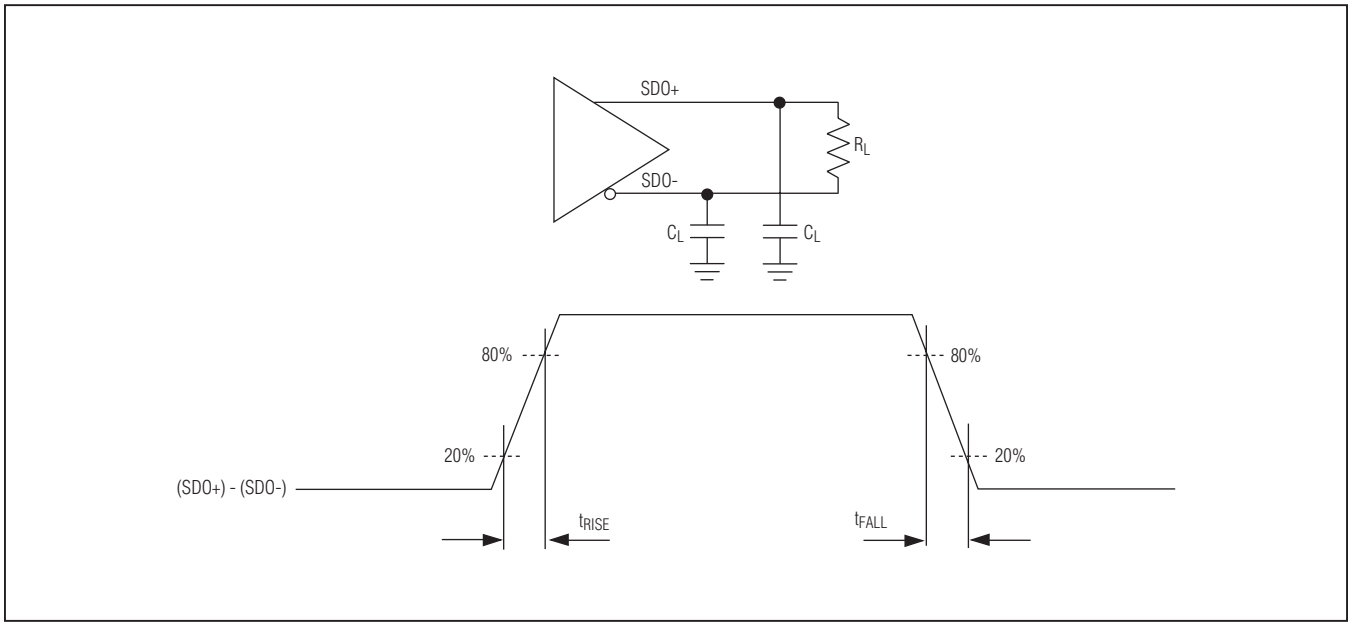


Figure 4. MAX9257A LVDS Control Channel Output Load and Output Rise/Fall Times

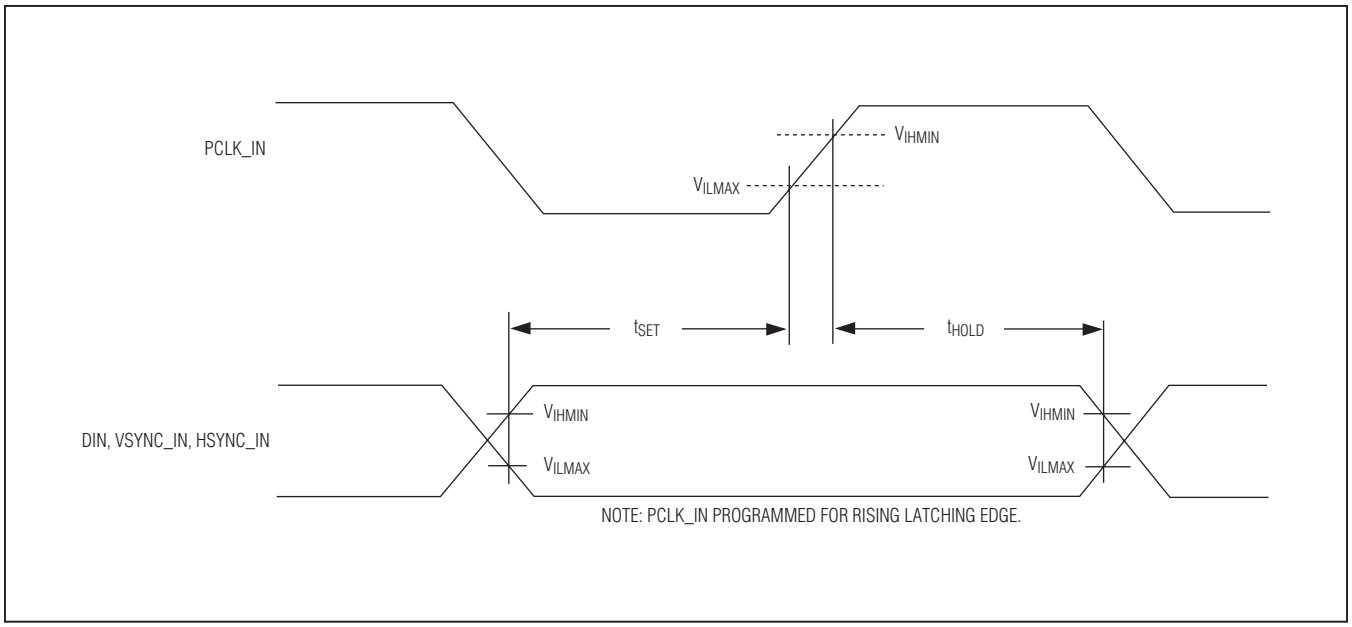


Figure 5. MAX9257A Input Setup and Hold Times

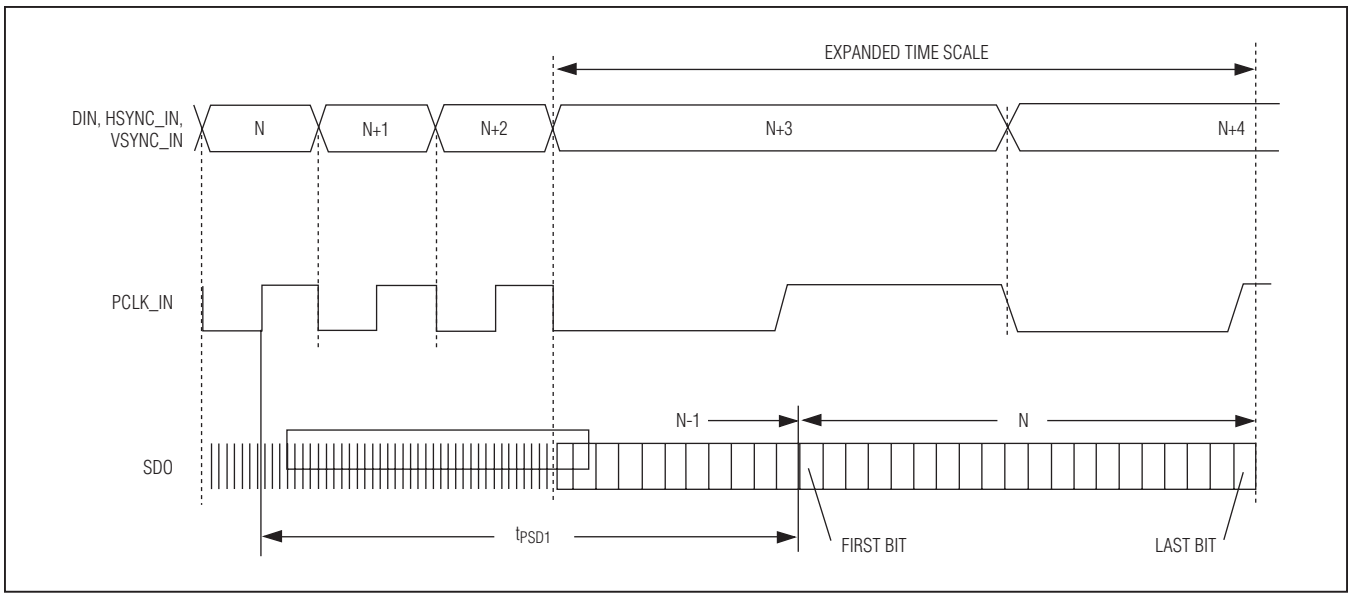


Figure 6. MAX9257A Parallel-to-Serial Delay

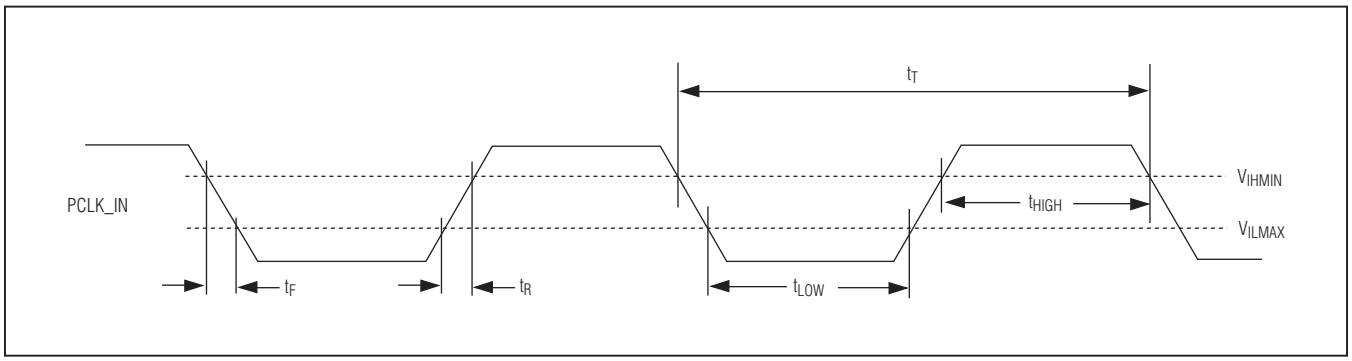


Figure 7. MAX9257A Parallel Input Clock Requirements

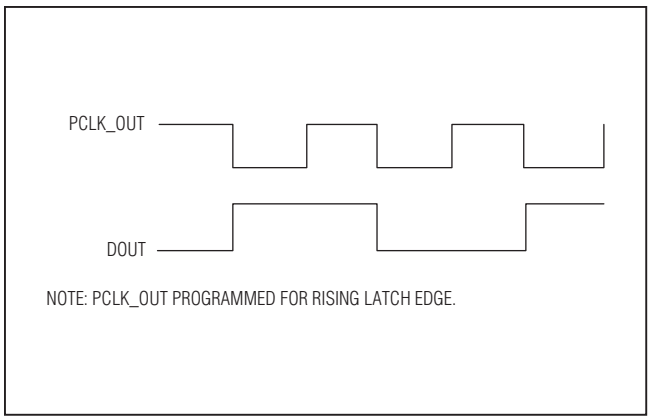


Figure 8. MAX9258A Worst-Case Pattern Output

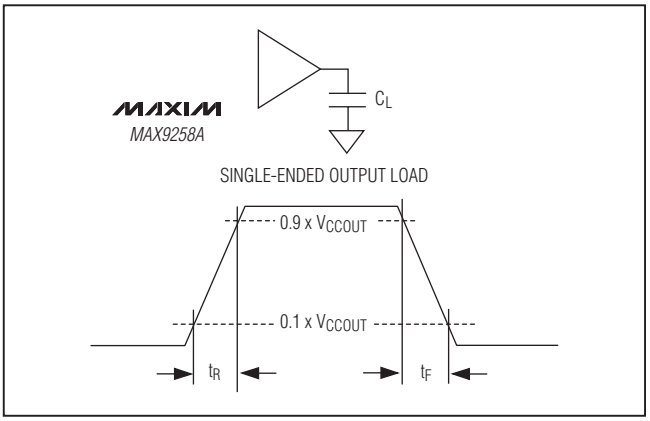


Figure 9. MAX9258A Output Rise and Fall Times

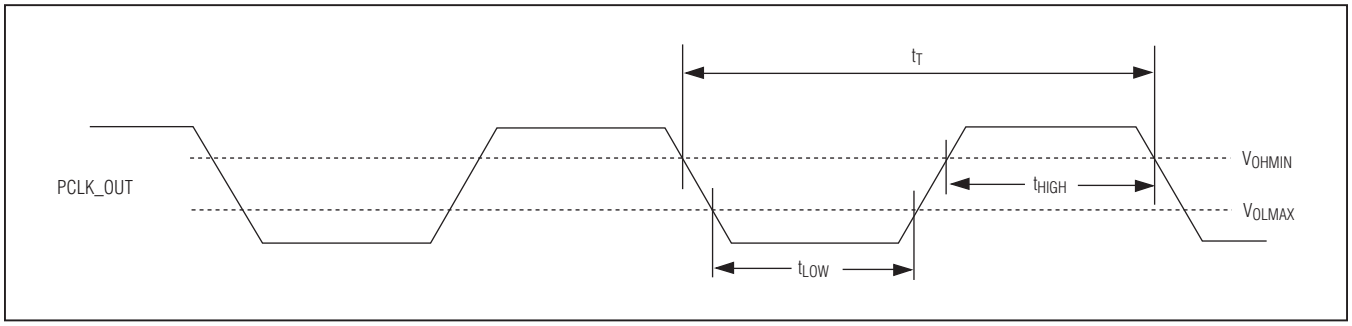


Figure 10. MAX9258A Clock Output High and Low Time

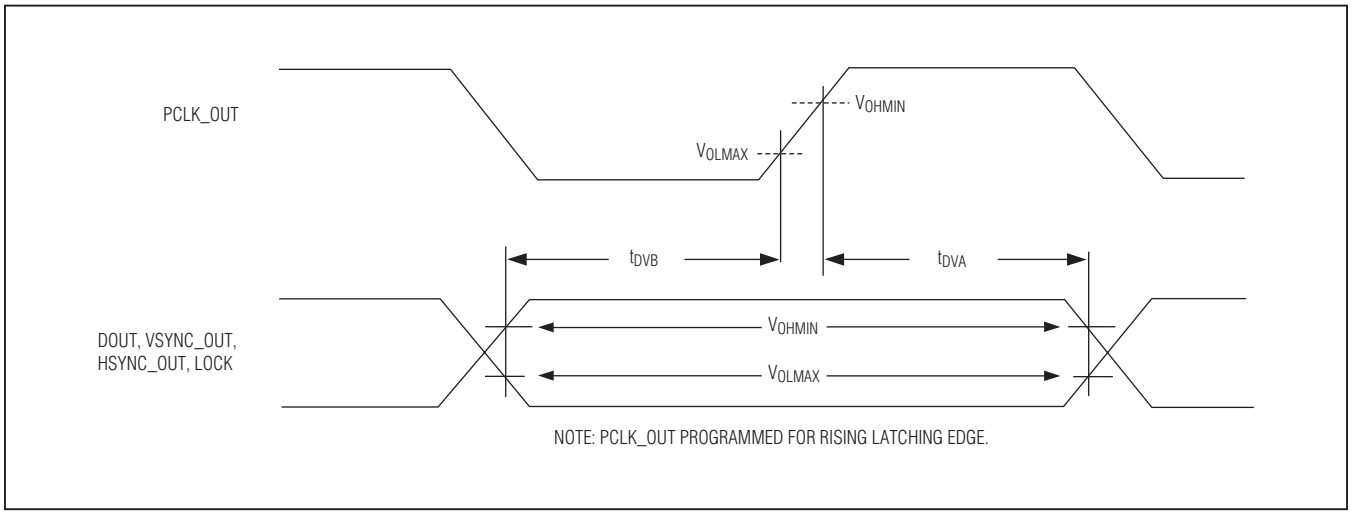


Figure 11. MAX9258A Output Data Valid Times

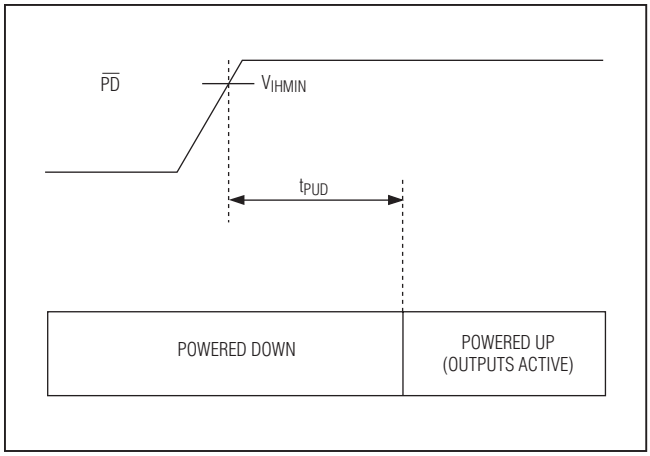


Figure 12. MAX9258A Power-Up Delay

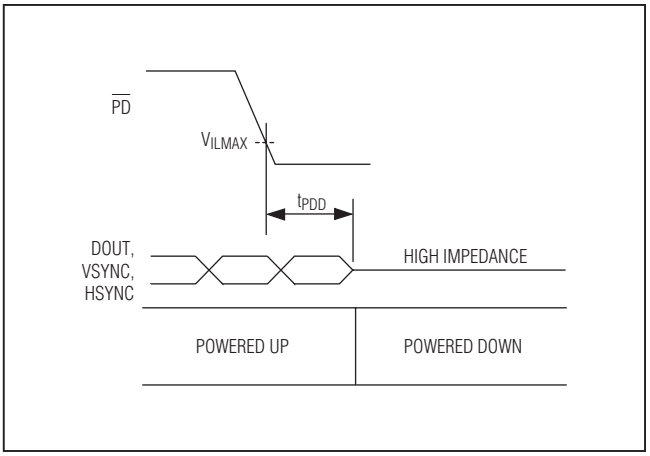


Figure 13. MAX9258A Power-Down Delay

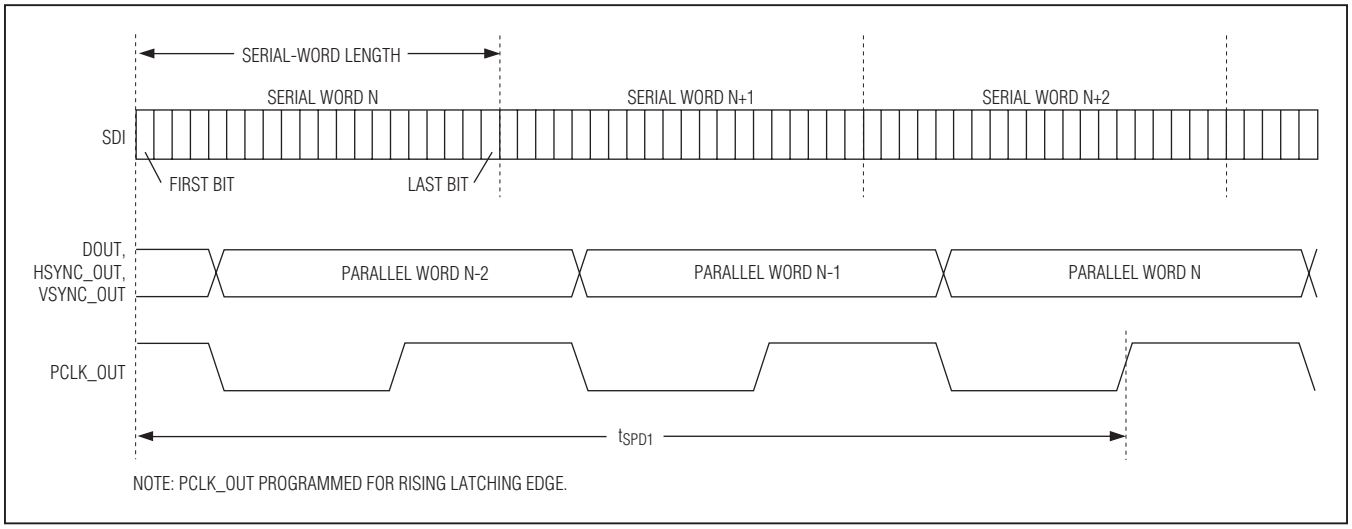


Figure 14. MAX9258A Serial-to-Parallel Delay

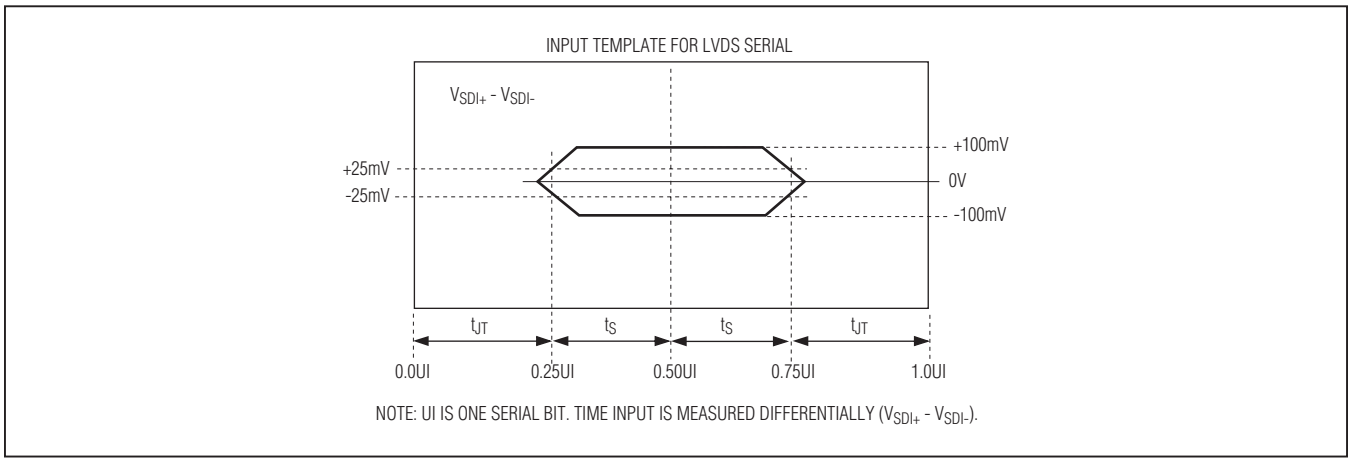


Figure 15. MAX9258A Jitter Tolerance

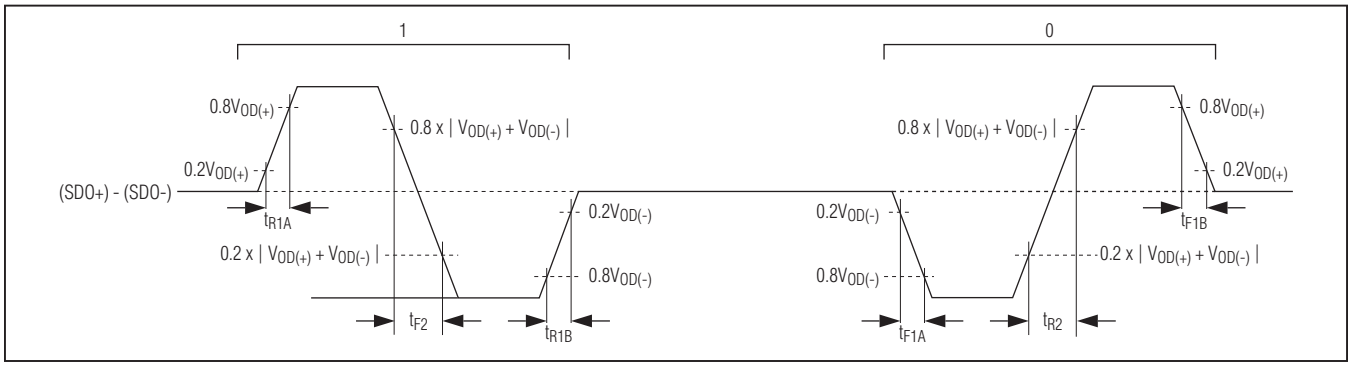


Figure 16. Control Channel Transition Time

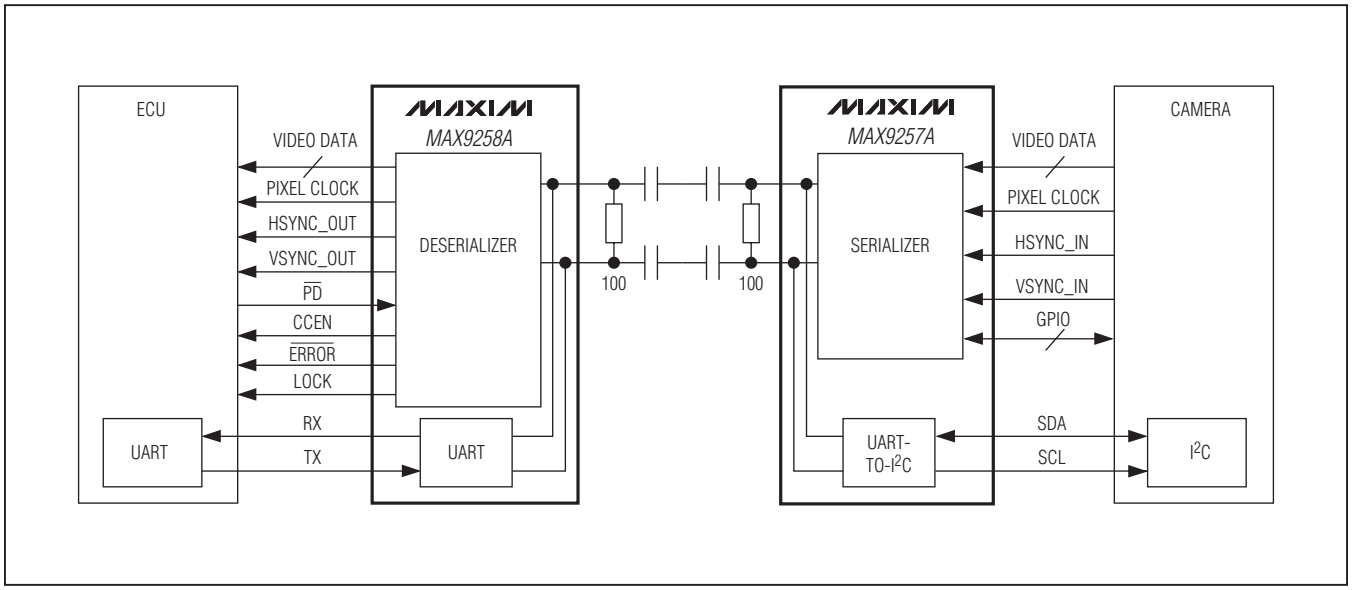


Figure 17. Serial Link with I²C Camera Programming Interface (Base Mode)

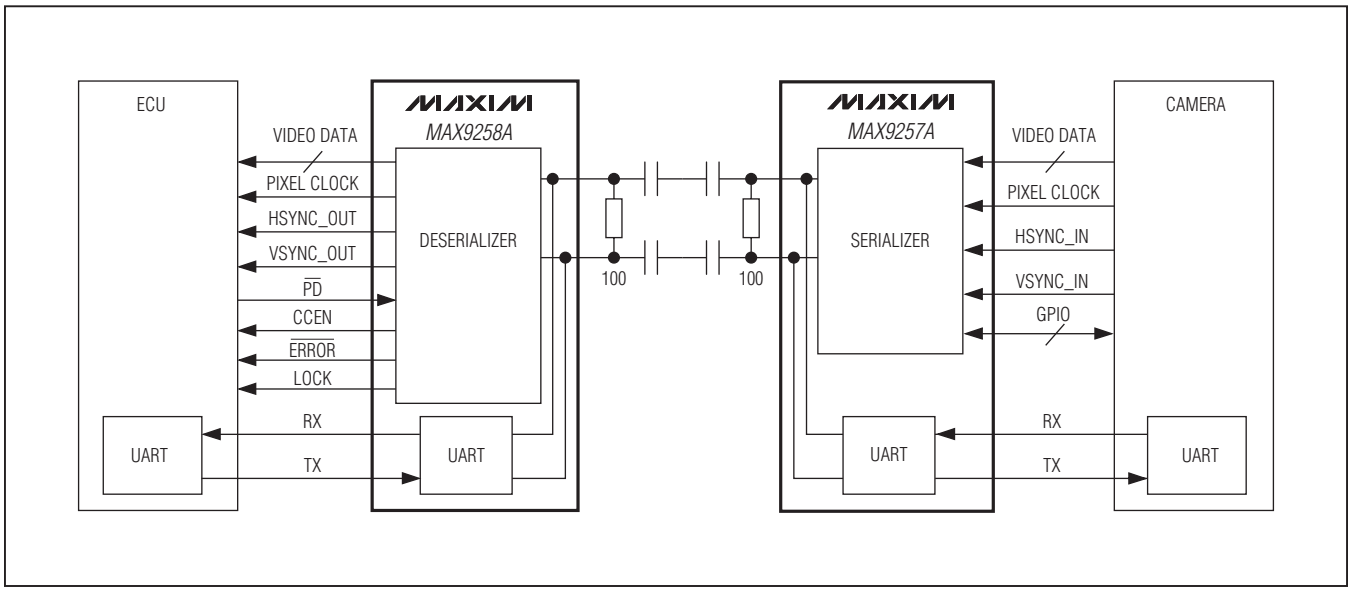


Figure 18. Serial Link with UART Camera Programming Interface (Bypass Mode)

Detailed Description

The MAX9257A serializer pairs with the MAX9258A deserializer to form a complete digital video serial link. The electronic control unit (ECU) programs the registers in the MAX9257A, MAX9258A, and peripheral devices, such as a camera, during the control channel phase that occurs at startup or during the vertical blanking time. All control channel communication is half-duplex. The UART communication between the MAX9258A and the MAX9257A is encoded to allow transmission through AC-coupling capacitors. The MAX9257A communicates to the peripheral device through UART or I²C.

The MAX9257A/MAX9258A DC-balanced serializer and deserializer operate from a 5MHz-to-70MHz parallel clock frequency, and are capable of serializing and deserializing programmable 10, 12, 14, 16, and 18 bits parallel data during the video phase. The devices have two phases of operation: video and control channel (Figure 19 and 20). During the video phase, the MAX9257A accepts parallel video data and transmits serial encoded data over the LVDS link. The MAX9258A accepts the encoded serial LVDS data and converts it back to parallel output data. The MAX9257A has dedicated inputs for HSYNC and VSYNC. The selected VSYNC edge causes the MAX9257A/MAX9258A to enter the control channel phase. Nonactive VSYNC edge can be asserted after eight pixel clock cycles.

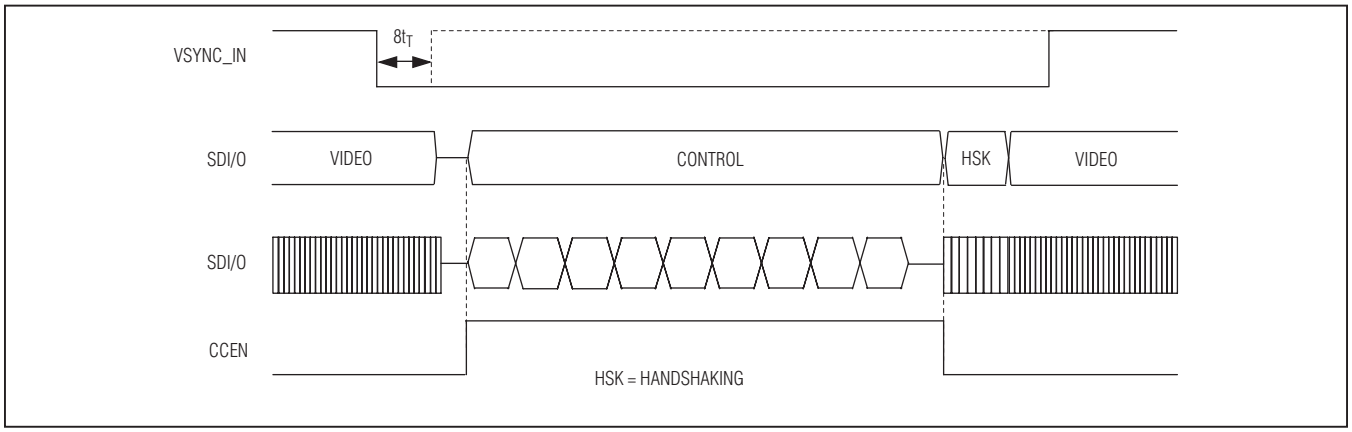


Figure 19. Video and Control Channel Phases (Spread Off)

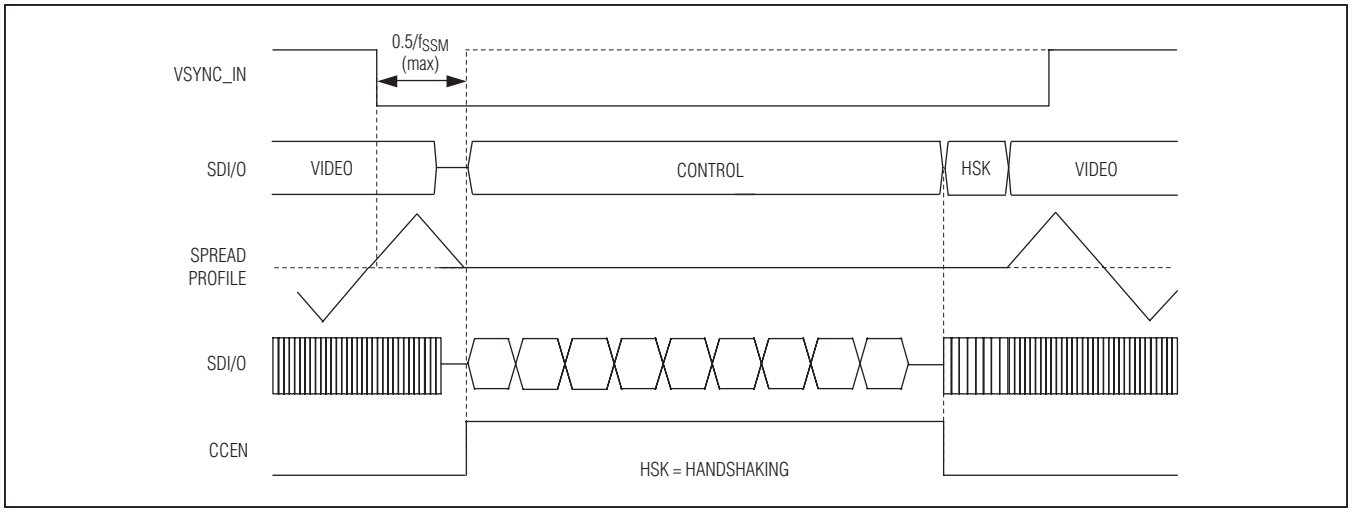


Figure 20. Video and Control Channel Phases (MAX9257A Spread is Enabled)

The video data are coded using two overhead bits (EN0 and EN1) resulting in a serial-word length of N+2 bits. The devices feature programmable parity encoding that adds two parity bits to the serial word. Bit 0 (EN0) is the LSB that is serialized first without parity enabled. The parity bits are serialized first when parity is enabled.

The ECU programs the MAX9258A, MAX9257A, and peripheral devices at startup and during the control channel phase. In a digital video system, the control channel phase occurs during the vertical blanking time and synchronizes to the VSYNC signal. The programmable active edge of VSYNC initiates the control channel phase. Nonactive edge of VSYNC can transition at any time after 8 x t_T if MAX9257A spread is not enabled and 0.5/f_{SSM} when enabled. At the end of video phase, the MAX9258A drives CCEN high to indicate to the ECU that the control channel is open. Programmable timers and ECU signal activity determine how long the control channel stays open. The timers are reset by ECU signal activity. ECU programming must not exceed the vertical blanking time to avoid loss of video data.

After the control channel phase closes, the MAX9257A sends a 546 or 1090 word pattern as handshaking (HSK) to synchronize the MAX9258A's internal clock recovery circuit to the MAX9257A's transmitted data. Following the handshaking, the control channel is closed and the video phase begins. The serial LVDS data is recovered and parallel data is valid on the programmed edge of the recovered pixel clock.

Table 1 and 2 show the default power-up values for the MAX9257A/MAX9258A registers. Tables 3 and 4 show the input and output supply references.

Table 1. MAX9257A Power-Up Default Register Map (see the *MAX9257A Register Table*)

REGISTER NAME	REGISTER ADDRESS (hex)	POWER-UP VALUE (hex)	POWER-UP DEFAULT SETTINGS
REG0	0x00	0xB5	PRATE = 10, 20MHz to 40MHz SRATE = 11, 400Mbps to 840Mbps PAREN = 0, parity disabled PWIDTH = 101, parallel data width = 18
REG1	0x01	0x1F	SPREAD = 000, spread = off Reserved = 11111
REG2	0x02	0xA0	STODIV = 1010, STO clock is pixel clock divided by 1024 STOCNT = 0000, STO counter counts to 1
REG3	0x03	0xA0	ETODIV = 1010, ETO clock is pixel clock divided by 1024 ETOCNT = 0000, ETO counter counts to 1
REG4	0x04	1) REM = 0, 0x28 2) REM = 1, 0x30	VEDGE = 0, VSYNC active edge is falling Reserved = 0 CKEDGE = 1, pixel clock active edge is rising PD: 1) If REM = 0, PD = 0 2) If REM = 1, PD = 1 SEREN: 1) If REM = 0, SEREN = 1 2) If REM = 1, SEREN = 0 BYPFPLL = 0, filter PLL is active Reserved = 0 PRBSEN = 0, PRBS test disabled

Table 1. MAX9257A Power-Up Default Register Map (continued)

REGISTER NAME	REGISTER ADDRESS (hex)	POWER-UP VALUE (hex)	POWER-UP DEFAULT SETTINGS
REG5	0x05	0xFA	MAX9257A address = 1111 1010
REG6	0x06	0xFF	End frame = 1111 1111
REG7	0x07	0xF8	MAX9258A address = 1111 1000
REG8	0x08	0x00	INTMODE = 0, interface with peripheral is UART INTEN = 0, interface with peripheral is disabled FAST = 0, UART bit rate = DC to 4.25Mbps CTO = 000, never come back BITRATE = 00, base mode bit rate = 95kbps to 400kbps
REG9	0x09	0x00	PRBSLEN = 0000, PRBS word length = 2^{21} GPIO9DIR = 0, GPIO9 = input GPIO8DIR = 0, GPIO8 = input GPIO9 = 0 GPIO8 = 0
REG10	0x0A	0x00	GPIO7DIR = 0, GPIO7 = input GPIO6DIR = 0, GPIO6 = input GPIO5DIR = 0, GPIO5 = input GPIO4DIR = 0, GPIO4 = input GPIO3DIR = 0, GPIO3 = input GPIO2DIR = 0, GPIO2 = input GPIO1DIR = 0, GPIO1 = input GPIO0DIR = 0, GPIO0 = input
REG11	0x0B	0x00	GPIO7 = 0 GPIO6 = 0 GPIO5 = 0 GPIO4 = 0 GPIO3 = 0 GPIO2 = 0 GPIO1 = 0 GPIO0 = 0
REG12	0x0C	0xE0	PREEMP = 111, preemphasis = 0% Reserved = 00000
REG13	0x0D	0x00	Reserved = 000000 I2CFILT = 00, I²C glitch filter settings: 1) 95kbps to 400kbps = 100ns 2) 400kbps to 1000kbps = 50ns 3) 1000kbps to 4250kbps = 10ns
REG14	0x0E	0x00	Reserved = 0000 000 LOCKED = read only

Table 2. MAX9258A Power-Up Default Register Map (see the *MAX9258A Register Table*)

REGISTER NAME	REGISTER ADDRESS (hex)	POWER-UP VALUE (hex)	POWER-UP DEFAULT SETTINGS
REG0	0x00	0xB5	PRATE = 10, 20MHz to 40MHz SRATE = 11, 400Mbps to 840Mbps PAREN = 0, parity disabled PWIDTH = 101, parallel data width = 18
REG1	0x01	0x00	SPREAD = 00, spread spectrum = off AER = 0, error count is reset by reading error registers ACTOFFSET = 00, 23mV offset Reserved = 000
REG2	0x02	0xA0	STODIV = 1010, STO clock is pixel clock divided by 1024 STOCNT = 0000, STO counter counts to 1
REG3	0x03	0xA0	ETODIV = 1010, ETO clock is pixel clock divided by 1024 ETOCNT = 0000, ETO counter counts to 1
REG4	0x04	0x20	VEDGE = 0, VSYNC active edge is falling HEDGE = 0, HSYNC active edge is falling CKEDGE = 1, pixel clock active edge is rising Reserved = 0 ACTLP = 0, short stretcher output pulse Reserved = 00 PRBSEN = 0, PRBS test disabled
REG5	0x05	0xF8	MAX9258 address = 1111 1000
REG6	0x06	0xFF	End frame = 1111 1111
REG7	0x07	0x00	INTMODE = 0, interface with peripheral is UART INTEN = 0, interface with peripheral is disabled FAST = 0, UART bit rate = DC to 4.25Mbps CTO = 000, never come back BITRATE = 00, base mode bit rate = 95kbps to 400kbps
REG8	0x08	0x10	PATHRLO = 0001 0000 parity threshold = 16
REG9	0x09	0x00	PATHRHI = 0000 0000, parity threshold = 16
REG10	0x0A	0x00	Parity errors video (8 LSBs) = read only
REG11	0x0B	0x00	Parity errors video (8 MSBs) = read only
REG12	0x0C	0x00	PRBS bit errors = read only
REG13	0x0D	0x00	Reserved = 000 Parity error, communication with MAX9258A = read only Frame error, communication with MAX9258A = read only Parity error, communication with MAX9257A = read only Frame error, communication with MAX9257A = read only I²C error, communication with peripheral = read only

Parallel-Word Width

The parallel-word width is made up of the video data bits, HSYNC, and VSYNC. The video data bits are programmable from 8 to 16 depending on the pixel clock, serial-data rate, and parity. Table 16 shows the parallel-word width.

Serial-Word Length

The serial-word length is made up of the parallel-word width, encoding bits, and parity bits. Tables 5–9 show the serial video format and serial-word lengths without parity. Tables 10–13 show with parity bits included.

Table 3. MAX9257A I/O Supply

INPUTS/OUTPUTS	SUPPLY
PCLK_IN, HSYNC_IN, VSYNC_IN, DIN[0:7], DIN[8:15]/GPIO[0:7], GPIO8, GPIO9, SCL/TX, SDA/RX	V_{CCIO}
SDO+, SDO-	V_{CCLVDS}
REM	V_{CC}

Table 4. MAX9258A I/O Supply

INPUTS/OUTPUTS	SUPPLY
All inputs and outputs	V_{CCOUT}
SDI+, SDI-	V_{CCLVDS}

Table 5. Serial Video Data Format for 20-Bit Serial-Word Length (Parallel-Word Width = 18)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NAME	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15

Table 6. Serial Video Data Format for 18-Bit Serial-Word Length (Parallel-Word Width = 16)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
NAME	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13

Table 7. Serial Video Data Format for 16-Bit Serial-Word Length (Parallel-Word Width = 14)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
NAME	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11

Table 8. Serial Video Data Format for 14-Bit Serial-Word Length (Parallel-Word Width = 12)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14
NAME	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9

Table 9. Serial Video Data Format for 12-Bit Serial-Word Length (Parallel-Word Width = 10)

BIT	1	2	3	4	5	6	7	8	9	10	11	12
NAME	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7

Table 10. Format for 20-Bit Serial-Word Length with Parity (Parallel-Word Width = 16)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NAME	PR	PRB	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13

Table 11. Format for 18-Bit Serial-Word Length with Parity (Parallel-Word Width = 14)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
NAME	PR	PRB	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11

Table 12. Format for 16-Bit Serial-Word Length with Parity (Parallel-Word Width = 12)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
NAME	PR	PRB	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9

Table 13. Format for 14-Bit Serial-Word Length with Parity (Parallel-Word Width = 10)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14
NAME	PR	PRB	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7

LVDS Serial Data

Serial LVDS data is transmitted least significant bit (LSB) to most significant bit (MSB) as shown in Tables 5 through 13. The ECU at startup can program the parallel word width, serial frequency range, parity, spread-spectrum, and pixel clock frequency range (see the *MAX9257A Register Table* and the *MAX9258A Register Table*).

Pixel Clock Frequency Range

The devices each have registers that can be configured at startup. Depending on the word length, the MAX9257A multiplies PCLK_IN (pixel clock) by 12, 14, 16, 18, or 20 using an internal PLL to generate the serial clock. Use Table 20 for proper selection of available PCLK frequency and serial-data ranges. Parallel data is serialized using the serial-clock and serialized bits are transmitted at the MAX9257A LVDS outputs. The devices support a wide range for PCLK_IN (Table 14). If the pixel clock frequency needs to change to a frequency outside the programmed range, the ECU must program both the MAX9257A and the MAX9258A in the same control channel session.

Serial-Data Rate Range

The word length and pixel clock is limited by the maximum serial-data rate of 840Mbps. The following formula shows the relation between word length, pixel clock, and serial clock:

Serial-word length x pixel clock = serial-data rate = 840Mbps

For example, if PCLK_IN is 70MHz, the serial-word length has to be 12 bits including DC balance bits if parity is not enabled to keep the serial-data rate under 840Mbps. If the serial-word length is 20 bits, the maximum PCLK_IN frequency is 42MHz. The serial-data rate can vary from 60Mbps to 840Mbps and can be programmed at power-up (Table 15). Use Table 20 for proper selection of available PCLK frequency and serial data ranges. Operating in the incorrect range for either the serial-data rate or PCLK_IN can result in excessive current dissipation and failure of the MAX9258A to lock to the MAX9257A.

Table 14. MAX9257A Pixel Clock Range (PCLK_IN)

FREQUENCY (MHz)	PRATE (REG0[7:6])
5–10	00
10–20	01
20–40	10
40–70	11

Table 15. Serial-Data Rate Range

SERIAL-DATA RATE (Mbps)	SRATE (REG0[5:4])
60–100	00
100–200	01
200–400	10
400–840	11

LVDS Common-Mode Bias

The output common-mode bias is 1.2V at the LVDS inputs on the MAX9258A and LVDS outputs on the MAX9257A. No external resistors are required to provide bias for AC-coupling the LVDS inputs and outputs.

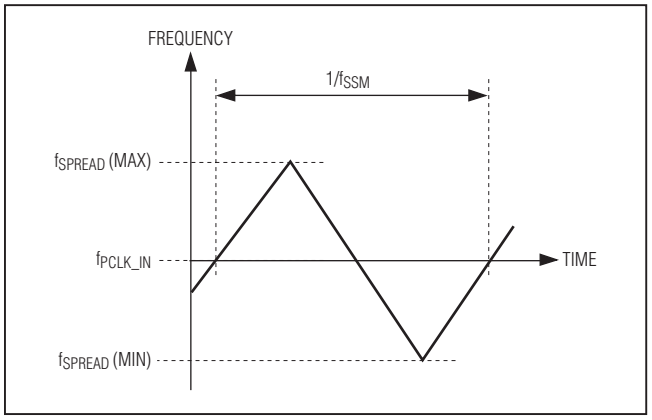


Figure 21. Simplified Modulation Profile for the MAX9257A/ MAX9258A

LVDS Termination

Terminate the LVDS link at both ends with the characteristic impedance of the transmission line (typically 100Ω differential). The LVDS inputs and outputs are high impedance to GND and differentially.

Spread-Spectrum Selection

The devices each have spread-spectrum options. Both should not be turned on at the same time. When the MAX9257A is programmed for spread spectrum, the MAX9258A tracks and passes the spread to its clock and data outputs. The MAX9257A/MAX9258A are both center spread (Figure 21). The control channel does not use spread spectrum, but has slower transition times.

MAX9258A Spread Spectrum

The MAX9258A features a programmable spread-spectrum clock and data outputs for reduced EMI. The single-ended data outputs are programmable for no spread, ±2%, or ±4% (see the *Typical Operating Characteristics*) around the recovered pixel clock frequency. The output spread is programmed in register REG1[7:6]. Table 17 shows the spread options, and Table 18 shows the various modulation rates.

MAX9257A Spread Spectrum

The MAX9257A features programmable spread spectrum for the LVDS outputs. Table 19 shows various spread options, and Table 20 shows the various modulation rates. Only one device (the MAX9257A or the MAX9258A) should be programmed for spread spectrum at a time. If the MAX9257A is programmed for spread, the MAX9258A tracks and passes the spread to the data and clock outputs. The PRATE range of 00 and 01 (5MHz ≤ PCLK ≤ 20MHz) supports all the spread options. The PRATE range of 10 and 11 (20MHz ≤ PCLK ≤ 70MHz) requires that the spread be 2% or less.

Table 16. Parallel-Word Width

PARALLEL-WORD WIDTH	PWIDTH (REG0[2:0])
10	000
12	001
14	010
16	011
18	1XX

Table 17. MAX9258A Spread

PRATE (REG1[7:6])	SPREAD (%)
00	Off
01	±2
10	Off
11	±4

Table 18. MAX9258A Modulation Rate

PRATE (REG1[7:6])	MODULATION RATE	f_{SSM} RANGE (kHz)
00	PCLK/312	16 to 32
01	PCLK/520	19.2 to 38.5
10	PCLK/1040	19.2 to 38.5
11	PCLK/1248	32 to 56

Table 19. MAX9257A LVDS Output Spread

REG1[7:5]	SPREAD (%)
000	Off
001	±1.5
010	±1.75
011	±2
100	Off
101	±3
110	±3.5
111	±4

Pixel Clock Jitter Filter

The MAX9257A has a PLL to filter high-frequency pixel clock jitter on PCLK_IN. The FPLL can be bypassed by writing 1 to REG4[2]. The FPLL improves the MAX9258A's data recovery by filtering out the high-frequency components from the pixel clock that the MAX9258A cannot track. The 3dB bandwidth of the FPLL is 100kHz (typ).

Table 20. MAX9257A Modulation Rate

SERIAL-WORD LENGTH	SRATE	PRATE	PCLK RANGE (MHz)	MODULATION RATE	f_{SSM} RANGE (kHz)
12	11	11	40–70	PCLK/2728	14.7 to 25.7
	11	10	33.3–40	PCLK/1736	19.2 to 23.0
	10	10	20–33.3	PCLK/1612	12.4 to 20.7
	10	01	16.6–20	PCLK/992	16.7 to 20.2
	01	01	10–16.6	PCLK/1116	9.0 to 14.9
	01	00	8.3–10	PCLK/744	11.2 to 13.4
	00	00	5–8.3	PCLK/868	5.8 to 9.6
14	11	11	40–60	PCLK/2304	17.4 to 26.0
	11	10	28.6–40	PCLK/1728	16.6 to 23.1
	10	10	20–28.6	PCLK/1440	13.9 to 19.9
	10	01	14.3–20	PCLK/1008	14.2 to 19.8
	01	01	10–14.3	PCLK/1008	9.9 to 14.2
	01	00	7.1–10	PCLK/720	9.9 to 13.9
	00	00	5–7.1	PCLK/720	6.9 to 9.9
16	11	11	40–52.5	PCLK/1968	20.3 to 26.7
	11	10	25–40	PCLK/1640	15.2 to 24.4
	10	10	20–25	PCLK/1312	15.2 to 19.1
	10	01	12.5–20	PCLK/984	12.7 to 20.3
	01	01	10–12.5	PCLK/820	12.2 to 15.2
	01	00	6.25–10	PCLK/656	9.5 to 15.2
	00	00	5–6.25	PCLK/656	7.6 to 9.5
18	11	11	40–46.6	PCLK/1840	21.7 to 25.3
	11	10	22.2–40	PCLK/1472	15.1 to 27.2
	10	10	20–22.2	PCLK/1104	18.1 to 20.1
	10	01	11.1–20	PCLK/920	12.1 to 21.7
	01	01	10–11.1	PCLK/736	13.6 to 15.1
	01	00	5.6–10	PCLK/736	7.6 to 13.6
	00	00	5–5.6	PCLK/552	9.1 to 10.1
20	11	11	40–42	PCLK/1632	24.5 to 25.7
	11	10	20–40	PCLK/1632	12.3 to 24.5
	10	01	10–20	PCLK/1020	9.8 to 19.6
	01	00	5–10	PCLK/816	6.1 to 12.3

LVDS Output Preemphasis (SDO±)

The MAX9257A features programmable preemphasis where extra current is added when the LVDS outputs transition on the serial link. Preemphasis provides additional current to the normal drive current. For example, 20% preemphasis provides 20% greater current than the normal drive current. Current is boosted only on the transitions and returns to the normal drive current after switching. Select the preemphasis level to optimize the eye diagram. Preemphasis boosts the high-frequency content of the LVDS outputs to enable driving greater cable lengths. The amount of preemphasis is programmed in REG12[7:5] (Table 21).

VSYNC, HSYNC, and Pixel Clock Polarity

PCLK: The MAX9257A is programmable to latch data on either rising or falling edge of PCLK. The polarity of PCLKOUT at the MAX9258A can be independent of the MAX9257A PCLK active edge. The polarity of PCLK can be programmed using REG4[5] of the MAX9257A and the MAX9258A.

VSYNC: The MAX9257A and the MAX9258A enter control channel on the falling edge of VSYNC. The default register settings are VSYNC active falling edge for both the MAX9257A and the MAX9258A. If the VSYNC active edge is programmed for rising edge at the MAX9257A, the MAX9258A VSYNC active edge must also be programmed for rising edge to reproduce VSYNC rising edge at the MAX9258A output. However, matching the polarity of the VSYNC active edge between the MAX9257A and the MAX9258A is not a requirement for proper operation.

HSYNC: HSYNC active-edge polarity is programmable for the MAX9258A.

General-Purpose I/Os (GPIOs)

The MAX9257A has up to 10 GPIOs available. GPIO8 and GPIO9 are always available while GPIO[0:7] are available depending on the parallel-word width (Table 22). If GPIOs are not available, the corresponding GPIO bits are not used.

A GPIO can be programmed to drive an LVCMOS logic level or to read a logic input. The register bit that sets the output level when the GPIO is programmed as an output stores the input level when the GPIO is programmed as an input.

Table 21. Preemphasis

REG12[7:5]	PREEMPHASIS (%)
000,101,110	20
001	40
010	60
011	80
100	100
111	0

Table 22. GPIOs vs. Parallel-Word Width

PARALLEL-WORD WIDTH (N)	GPIOs AVAILABLE
18	GPIO[8:9]
16	GPIO[6:9]
14	GPIO[4:9]
12	GPIO[2:9]
10	GPIO[0:9]

Open-Drain Outputs (LOCK, $\overline{\text{ERROR}}$)

LOCK and $\overline{\text{ERROR}}$ are open-drain outputs that require a pullup resistor to an external supply. $\overline{\text{ERROR}}$ asserts low when an error occurs and LOCK is high impedance when the MAX9258A is locked to the MAX9257A and remains high under the locked condition. When the devices are in shutdown, the channel is not locked and LOCK goes high impedance, is pulled high, and should be ignored. $\overline{\text{ERROR}}$ is high impedance at shutdown and remains high. In choosing pullup resistors, there is a tradeoff between power dissipation and speed; 10kΩ pullup should be sufficient.

The LOCK and $\overline{\text{ERROR}}$ outputs can be wired in an AND configuration if you have multiple serializers and deserializers, or a single serializer fanned out to multiple deserializers through a repeater. For such situations, wire the multiple LOCK outputs together and use a single pullup resistor to pull up all the lines high. LOCK is high if all the devices are locked. Do the same thing for $\overline{\text{ERROR}}$; $\overline{\text{ERROR}}$ is low if any MAX9258A reports errors.

Base Mode and Bypass Mode (Basics)

In the control channel phase, there are two modes: base and bypass. In base mode, ECU always communicates using the MAX9257A/MAX9258A UART protocol and communication with a peripheral device is performed in I²C by the MAX9257A. Packets not addressed to the MAX9257A or the MAX9258A get converted to I²C and passed to the peripheral device. Similarly, I²C packets from the peripheral device get converted to UART packets in the reverse direction. ECU can disable communication to the peripheral device by writing a 0 to INTEN (REG8[6] in the MAX9257A and REG7[6] in the MAX9258A). Base mode is the default mode. Bypass mode is entered by writing a 0 to INTMODE and 1 to INTEN (Table 23). Bypass mode is exited if there is no activity from ECU in the control channel for the duration of CTO. When CTO times out, INTEN reverts back to 0 and the devices revert back to base mode. To permanently stay in bypass mode, ECU can lock the CTO timer or program CTO to be longer than ETO and STO.

Timers

The devices feature three different timers. The start timeout (STO) and end timeout (ETO) control the duration of the control channel. The come-back timeout (CTO) controls the duration of bypass mode.

Table 23. Selection of Base Mode or Bypass Mode

INTEN MAX9257A REG8[6], MAX9258A REG7[6]	INTMODE MAX9257A REG8[7], MAX9258A REG7[7]	MODE
0	X	Base mode, communication with peripheral is not enabled
1	1	Base mode, communication with peripheral is enabled (I²C)
1	0	Bypass mode, communication with MAX9257A/MAX9258A is not enabled, communication with peripheral is enabled (UART)

STO Timer

The STO (start timeout) timer closes the control channel if the ECU does not start using the control channel within the STO timeout period. The STO timer is configured by register REG2 for both the MAX9257A and the MAX9258A. The four bits of REG2[7:4] select the divide ratio (STODIV) for the STO clock as a function of the pixel clock (Table 24). The timeout period is determined by counter bits REG2[3:0] that increment once every STO clock period. Write to REG2[3:0] to determine the counter end time. The STO counter counts to the programmed STOCNT + 1. The ECU must begin communicating before STO times out, otherwise, the control channel closes (Figure 22). The STO timeout period is given by:

$$t_{STO} = \left(\frac{1}{f_{CLK}}\right) \times STODIV \times (STOCNT + 1)$$

For example:

If the pixel clock frequency is set to 16MHz, STODIV is set to 1010 (STODIV = 1024), and STOCNT is set to 1001 (STOCNT = 9), the STO timer counts with 15.625kHz STO clock (16MHz/1024) internally until it reaches 10 and timer expires. The t_{STO} is equal to t_T x 1024 x 10 = 640µs.

The default value for STODIV is 1024 while the default value for STOCNT is 0. That means the STO timeout period is equal 1024 pixel clock cycles. Activity from the ECU on the control channel shuts off the STO timer and starts the ETO timer.

Table 24. STO Clock Divide Ratio

REG2[7:4]	STODIV
00XX	16
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16,384
1111	32,768

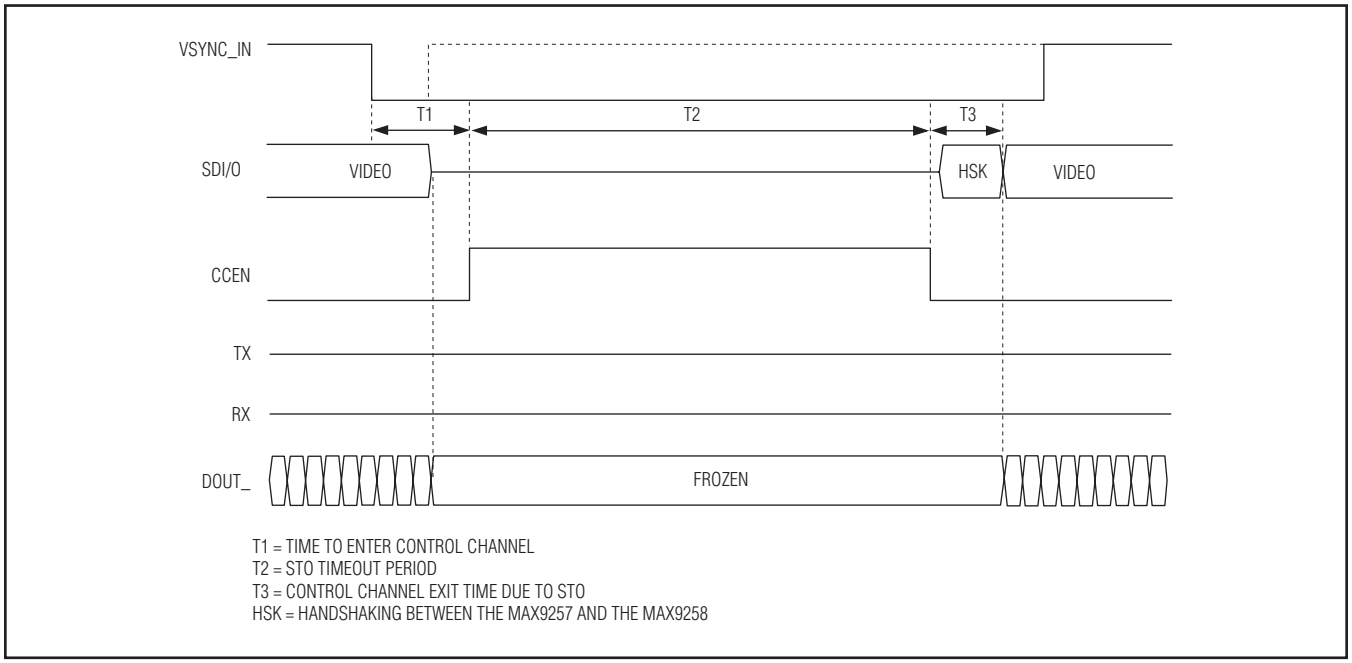


Figure 22. Control Channel Closing Due to STO Timeout

ETO Timer

The ETO (end timeout) timer closes the control channel if the ECU stops communicating for the ETO timeout period. Configure register REG3[7:4] for both the MAX9257A and the MAX9258A to select the divide ratio (ETODIV) for the ETO clock as a function of the pixel clock (Table 25). The timeout period is determined by counter bits REG3[3:0] that increment once every ETO clock period. Write to REG3[3:0] to determine the counter end time. The ETO counter counts to the programmed ETOCNT + 1. Any ECU activity resets the ETO timer. When the ECU stops transmitting data for the ETO timeout period, the control channel closes (Figure 23).

$$t_{ETO} = \left(\frac{1}{f_{CLK}}\right) \times ETODIV \times (ETOCNT + 1)$$

For example:

If the pixel clock frequency is set to 16MHz, ETODIV is set to 1010 (ETODIV = 1024), and ETOCNT is set to 1001 (ETOCNT = 9), the ETO timer counts with the 15.625kHz ETO clock (16MHz/1024) internally until it reaches 10 and timer expires. The t_{ETO} is equal to t_T x 1024 x 10 = 640µs.

Table 25. ETO Clock Divide Ratio

REG3[7:4]	ETODIV
00XX	16
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16,384
1111	32,768

The default value for ETODIV is 1024 while the default value for ETOCNT is 0. That means the ETO timeout period is equal to 1,024 pixel clock cycles.

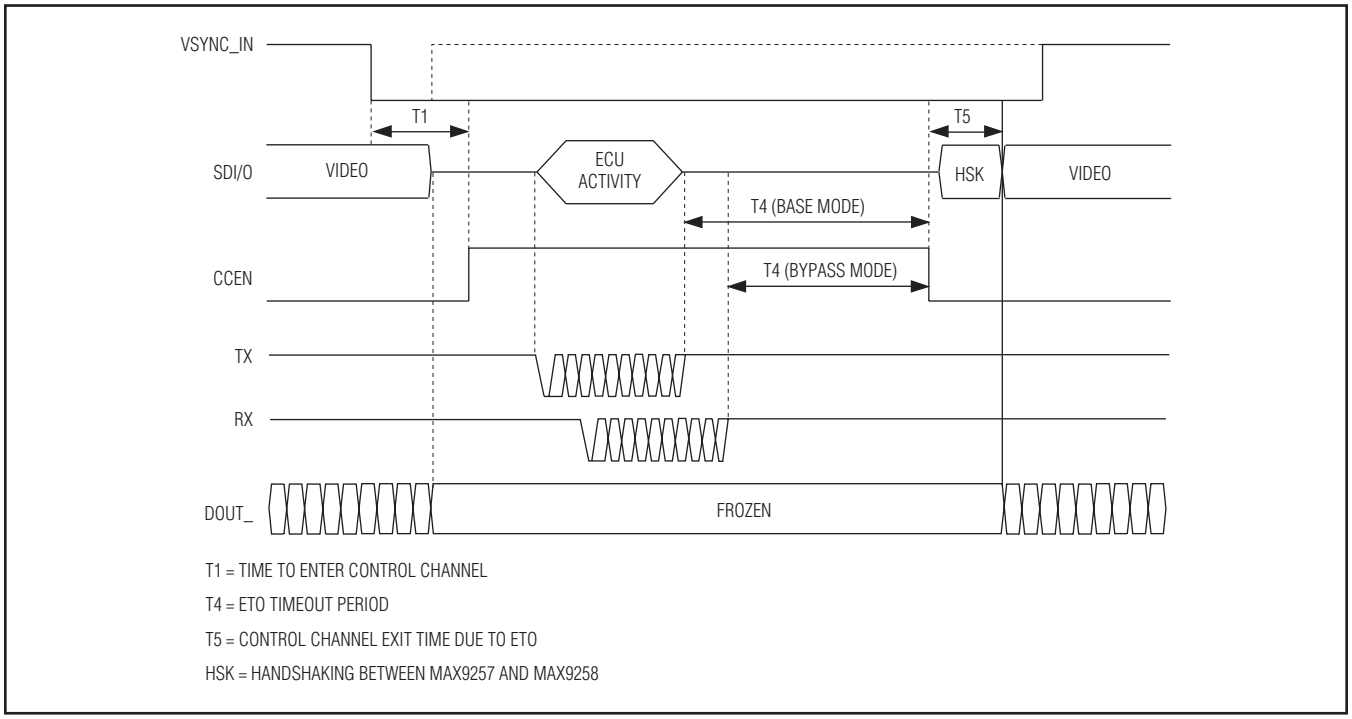


Figure 23. Control Channel Closing Due to ETO Timeout

Closing the Control Channel

After the MAX9257A detects the active VSYNC edge, it sends three synchronization words. Once the MAX9258A sees the active VSYNC transition and detects three synchronization words, it enters the control channel phase and CCEN goes high. There is a brief delay of T1 between the VSYNC transition and CCEN transitioning high. The ECU is allowed to communicate when CCEN is high.

If the ECU does not communicate while CCEN is high (Figure 22), the link remains silent and STO starts counting towards its preset timeout counter value. If STO times out (T2), CCEN transitions low and the control channel closes.

If the ECU communicates while CCEN is high and before STO expires (Figure 23), the STO timer is turned off and ETO timer is enabled. The ETO counter (ETOCNT+1) is reset to 0 whenever activity from ECU (base mode) or ECU and Camera (bypass mode) is detected. As long as there is activity from ECU (base mode) or ECU and Camera (bypass mode) on the link, the channel does not close and the ETO counter resets. After the ECU (base mode) or ECU and Camera (bypass mode) ceases link activity, ETO times out (T4), CCEN transitions low, and the control channel closes.

Another way to close the control channel in base mode is for the ECU to send an end frame (EF) to close the control channel without waiting for ETO to time out. Whenever EF is received by both the devices, control channel closes immediately and CCEN goes low. A synchronization frame must precede EF. End frame cannot be used in bypass mode. The control channel must close by EF to report errors back to the ECU.

After the control channel closes, there is a brief handshake period (T3 in Figure 22 and T5 in Figure 23) between the MAX9257A and the MAX9258A. The MAX9258A sends a special lock frame to the MAX9257A to indicate if PLL is still locked. The MAX9258A sends the lock frame if the number of decoding errors didn't exceed a threshold in the last LVDS video phase session. The MAX9258A features a proprietary VCO lock that prevents frequency drift while in the control channel for extended periods of time. If MAX9257A receives the lock frame, it understands that the MAX9258A is in a locked state and sends a short training sequence. If the lock frame is not received by the MAX9257A, it assumes that the MAX9258A is not locked and sends a long training sequence. After the short or long training sequence is complete, the MAX9257A

sends three special synchronization words before entering the video phase. Training sequence is used to resynchronize the devices before the video phase starts.

The MAX9257A/MAX9258A control channel duration is independent of VSYNC. The control channel does not close when VSYNC deasserts, which allows the use of a VSYNC interrupt signal on VSYNC_IN. The control channel must be closed by STO, ETO, or EF. If the control channel does not close before video data becomes available, video data can be lost.

STO/ETO Timer Programming

STO and ETO can be programmed given the values of T2, T4, and maximum values of T1, T3, and T5 (Figures 28, 23):

t_T = pixel clock period, t_{UCLK} = UART period

When spread spectrum is not enabled in MAX9257A:

$$max(T1) = 2.5\mu s + (3 \times t_T) + (4 \times t_{UCLK})$$

When spread spectrum is enabled in MAX9257A:

$$max(T1) = 2.5\mu s + (1400 \times t_T) + (4 \times t_{UCLK})$$

$$T2 = t_{STO}$$

$$T4 = t_{ETO}$$

When pixel clock frequency range (PRATE) is 00 or 01:

$$max(T3) = \left(\left(\frac{t_{STO}}{8}\right) + 546\right) \times t_T + (20 \times t_{UCLK})$$

$$max(T5) = \left(\left(\frac{t_{ETO}}{8}\right) + 546\right) \times t_T + (20 \times t_{UCLK})$$

When pixel clock frequency range (PRATE) is 10 or 11:

$$max(T3) = \left(\left(\frac{t_{STO}}{8}\right) + 1090\right) \times t_T + (20 \times t_{UCLK})$$

$$max(T5) = \left(\left(\frac{t_{ETO}}{8}\right) + 1090\right) \times t_T + (20 \times t_{UCLK})$$

CTO Timer

The CTO (come-back timeout) timer temporarily or permanently blocks programming to the MAX9257A/MAX9258A registers. CTO keeps the devices in bypass mode for the CTO timeout period (Table 26). Bypass mode can only be exited when the CTO timer expires. The CTO timer uses the UART bit times for its counter. Note that STO and ETO timers use the pixel clock while

Table 26. CTO Counter Timeout Period

MAX9257A REG2[7:4] MAX9258A REG3[7:4]	COUNTER USING UART BIT TIMES
000	Never come back (lockout)
001	16
010	32
011	48
100	64
101	80
110	96
111	112

CTO uses the UART bit times. The UART period t_{UCLK} synchronizes with the UART bit times, which synchronize every time the SYNC frame is sent.

When the CTO timer times out, INTEN bit in both devices is set to 0 and the devices revert back to base mode. If communication with the MAX9257A/MAX9258A is not needed after initial programming is complete, CTO may be set to 000 (never come back). In this case, CTO never expires and the devices stay in bypass mode until they are powered down. This prevents accidental programming of the devices while ECU communicates with the peripheral using a different UART protocol from the MAX9257A/MAX9258A UART protocol.

The overall CTO timeout is calculated as follows:

$$t_{CTO} = t_{UCLK} \times CTO$$

Assuming a UART bit rate of 2Mbps, REG2[7:4], REG3[7:4] = 100 (Table 26), CTO = 64, CTO timeout calculated as:

$$t_{CTO} = (0.5\mu s) \times 64 = 32\mu s$$

Link Power-Up

The MAX9258A powers up when the power-down input $\overline{PD}$ goes high. After approximately 130µs, CCEN goes high, indicating the control channel is available. This delay is required because the analog circuitry has to fully wake up. There are two ways to power up the MAX9257A. The MAX9257A powers up according to the state of REM. ECU powers up MAX9257A remotely (ECU sends command to power up) when REM is pulled to V_{CC}. The MAX9257A powers up according to the supply voltage when REM is grounded.

Powering the MAX9257A with Serialization Enabled (REM = Ground at Power-Up)

When REM is grounded, the MAX9257A fully powers up when power is applied. The power-down bit PD (REG4[4]) is disabled and serialization bit SEREN (REG4[3]) is enabled. If PCLK_IN is not running, the MAX9257A stays in the control channel. After PCLK_IN is applied, the control channel times out due to STO, ETO, or EF. The MAX9257A starts the handshaking after the MAX9257A locks to PCLK after 32,768 clock cycles. If PCLK_IN is running, serialization starts automatically after PLL of the MAX9257A locks to PCLK_IN with default values in the registers.

Remote Power-Up of the MAX9257A (REM = Pulled Up to V_{CC})

When REM is pulled up to V_{CC}, the MAX9257A wakes up in a low power state, drawing less than 100µA supply current. To wake-up the MAX9257A, the ECU first transmits a dummy frame 0xDB and then waits at least 100µs to allow the MAX9257A's internal analog circuitry to fully power up. Then the ECU configures the MAX9257A registers, including a write to disable the PD bit (REG4[4]) so that the MAX9257A does not return back to the low power state. Every packet needs to start with a synchronization frame (see the *UART* section). If the PD bit is not disabled within 70ms after transmitting the dummy frame, the MAX9257A returns to the low power state and the whole power-up sequence needs to be repeated. After configuration is complete, the ECU also needs to enable the SEREN bit to start the video phase.

At initial power-up with REM pulled to V_{CC}, default value of SEREN bit is 0, so STO and ETO timers are not active. Control channel is enabled as long as SEREN is 0. This allows the control channel to be used for extensive programming at initial power-up without the channel timing out. UART, parity, framing and packet errors in the control channel communications are reported if end frame is used to close control channel (see the *MAX9258A Error Checking and Reporting* section). For faster identification of errors, verify every write command by reading back the registers before enabling serialization.

Link Power-Down

When the control channel is open, the ECU writes to the PD bit to power down the MAX9257A. In this case, to power up the MAX9257A again, the power-up sequence explained in the *Remote Power-Up of the MAX9257A (REM = Pulled Up to VCC)* section needs to be repeated. The MAX9258A has a $\overline{PD}$ input that powers down the device.

MAX9258A Error Checking and Reporting

The MAX9258A has an open-drain $\overline{ERROR}$ output. This output indicates various error conditions encountered during the operation of the system. When an error condition is detected and needs to be reported, $\overline{ERROR}$ asserts low. $\overline{ERROR}$ indicates three error conditions: UART, video parity, and PRBS errors.

UART Errors

During control channel communication in base mode, the devices record UART frame, parity, and packet errors. I²C errors are also recorded by MAX9257A when I²C interface is enabled. If ECU closes the control channel by using end frame (EF), the MAX9257A sends a special internal UART frame back to the MAX9258A called error frame. The MAX9257A UART and I²C errors are reset at the next control channel. The MAX9258A receives the error frame and records the error status in its UART error register (REG13). ECU must use end frame to the close control channel for the MAX9257A to report back UART and I²C errors to the MAX9258A. Whenever one of the bits in the UART error register is 1, $\overline{ERROR}$ asserts low. The UART error register is reset when ECU reads it, and $\overline{ERROR}$ deasserts high immediately if UART errors were the only reason that $\overline{ERROR}$ was asserted low. If the MAX9258A is not locked (LOCK = low), UART error is not reported.

Video Parity Errors

When video parity check is enabled (REG0[3] in both devices), the MAX9258A counts the number of video parity errors by checking recovered video words. Value of this counter is reflected in PAERRHI (8 MSB bits, REG11) and PAERRLO (8 LSB bits, REG10). If the number of detected parity errors is greater than or equal to the parity error threshold PATHRHI (REG9) and PATHRLO (REG8), then ERROR asserts low. In this case, $\overline{ERROR}$ deasserts high after next video phase starts if video parity errors were the only reason that $\overline{ERROR}$ was asserted low. To report parity errors in bypass mode, program autoerror reset (AER) to 1 (REG1[5] = 1).

Autoerror Reset

The default method to reset errors is to read the respective error registers in the MAX9258A (registers 10, 11, and 13). If errors were present before the next control channel, the error count gets incremented to the previous number. By setting the autoerror reset (AER) bit to 1, the error registers reset when the control channel ends. Setting AER to 1 does not reset PRBS errors.

PRBS Errors

During the PRBS test, the MAX9258A checks received PRBS data words by comparing them to internally generated PRBS data. Detected errors are counted in the PRBS error register (REG12) in the MAX9258A. Whenever the number of detected PRBS errors is more than 0, $\overline{ERROR}$ asserts low. The PRBS error register is reset when ECU writes a 0 to PRBSEN register (REG4[0]). In this case, $\overline{ERROR}$ deasserts high immediately if PRBS errors were the only reason that $\overline{ERROR}$ was asserted low.

Short Synchronization Pattern

The short synchronization pattern is part of the handshaking procedure between the MAX9257A and MAX9258A after the control channel phase. It is used to resynchronize the MAX9258A's clock and data recovery circuit to the MAX9257A before the video phase begins. The MAX9257A transmits the short synchronization pattern when it receives the lock frame from the MAX9258A. The length of short synchronization pattern is dependant on the PRATE range. When PRATE is 00 or 01, the short synchronization pattern consists of 546 words and when PRATE is 10 or 11, the short synchronization pattern consists of 1090 words. Every word is one pixel clock period.

Long Synchronization Pattern

At power-up or when the MAX9257A does not receive a lock frame from the MAX9258A, the MAX9257A transmits a long synchronization pattern. The long synchronization pattern consists of 17,410 words. Every word is one pixel clock period. When REM is high, if synchronization is not achieved after 62 attempts, the MAX9257A resets SEREN to 0 so that the control channel stays open to allow troubleshooting. When REM is low, the MAX9257A/MAX9258A continuously tries to reestablish the connection.

Lock Verification (Handshaking)

At the end of every vertical blanking time, the MAX9257A verifies that the MAX9258A did not lose lock. The MAX9258A handshakes with the MAX9257A to indicate lock status. The handshaking occurs after the channel closes (Figures 28 and 23). If the number of decoding errors in a time window did not exceed a certain threshold during the last video phase, the MAX9258A sends back the lock frame that indicates lock. If the MAX9257A receives the lock frame, the MAX9257A transmits a short synchronization pattern. The MAX9258A features a proprietary VCO mechanism that prevents frequency drift while in the control channel. This allows for successful resynchronization after extended use of control channel. If the number of decoding errors in a time window exceeds a certain threshold, the MAX9258A loses lock, LOCK goes low, and the lock frame is not sent. The MAX9258A also loses lock if handshaking is not successful. If the MAX9257A does not receive the lock frame, it transmits a long synchronization pattern before the start of next video phase. When REM = 1, if the lock frame is not received by the MAX9257A after 62 consecutive attempts to synchronize, SEREN is disabled so that the control channel opens permanently for troubleshooting.

Table 27. Link Status

LOCK	CCEN	INDICATION
1	0	LVDS channel active
1	1	Control channel active
0	X	PLL loss of lock

Link Status (LOCK and CCEN)

The LOCK output indicates whether the MAX9258A is locked to the MAX9257A. LOCK is an open-drain output that needs to be pulled up to V_{CC}. LOCK asserts low to indicate that the MAX9258A is not locked to the MAX9257A and high when it is. In the control channel phase, LOCK stays high if LOCK is high in the video phase. While in the control channel phase, the MAX9258A PLL frequency is held constant, PCLK output is active and data outputs are frozen at their last valid value before entering the control channel. CCEN output indicates whether the devices are in the control channel phase or video phase. CCEN goes high when the devices are in the control channel phase (Table 27). Only at initial power-up, CCEN goes high before communication in the control channel is ready (see the *Link Power-Up* section).

Control Channel

Overview of Control Channel Operation

The control channel is used by the ECU to program registers in the MAX9257A, MAX9258A, and peripheral devices (such as a camera) during vertical blanking, after power-up, or when serialization is disabled. Control channel communication is half-duplex UART. The peripheral interface on the MAX9257A can be programmed to be I²C or UART. Operation of the control channel is synchronized with the VSYNC input after the ECU starts serialization of video data. Programmable timers, ECU signal activity, and end frame determine how long the control channel stays open. The control channel remains open as long as there is signal activity from the ECU. When the control channel closes, the LVDS serial link is reestablished.

Once serialization is enabled, the programming of registers (including the control channel overhead time) must be completed within the vertical blanking time to avoid loss of video data. VSYNC can deassert while control channel remains open after eight pixel clock cycles.

The control channel phase begins on the transition of the programmed active edge of VSYNC_IN. In video applications, the VSYNC signal of the peripheral device is connected to VSYNC_IN on the MAX9257A. In other applications, a different signal can be used to trigger the control channel phase. When the devices detect the VSYNC_IN transition, the LVDS video phase disables and the control channel phase is enabled.

The control channel operates in two modes: base and bypass. In base mode, the ECU issues UART commands in a specified format to program the MAX9257A/MAX9258A registers. GPIO on the MAX9257A are also programmed in base mode. UART commands are translated to I2C and output to peripheral devices connected to the MAX9257A when not addressed to either the MAX9257A or the MAX9258A.

In bypass mode, programming of the MAX9257A/MAX9258A registers are temporarily or permanently blocked depending on the programmed value of CTO. Blocking prevents unintentional programming of the MAX9257A/MAX9258A registers when the ECU communicates with the peripheral using a UART protocol different than the one specified to program the devices. When the control channel is open, the MAX9258A continues outputting the pixel clock while HSYNC and video data are held at the last value. If spread is enabled on the MAX9258A, the pixel clock is spread.

Control Channel Overhead

Control channel overhead consists of lock frame, short synchronization sequence, and error frame. The lock frame is transmitted between the MAX9257A and the MAX9258A without action by the ECU. The error frame is only sent in response to end frame. When MAX9257A spread spectrum is enabled, the control channel is entered after spread reaches center frequency. The overhead from VSYNC falling edge to control channel enable accounts for a maximum of 1400 pixel clock cycles.

Base Mode (Details)

Base mode allows the ECU to communicate with the devices in UART and a peripheral device in I2C. UART programming of the peripheral device is not possible in base mode. UART packets from the ECU need to follow a certain protocol to program the MAX9257A and the MAX9258A (Figures 28 and 29). Packets not addressed to the MAX9257A/MAX9258A get converted to I2C by the MAX9257A and pass to the peripheral device. The MAX9257A receives I2C packets from the peripheral device and converts them to UART packets to send back to the ECU. To disable communication to the peripheral device, write a 0 to INTEN (REG8[6] in the MAX9257A and REG7[6] in the MAX9258A).

In base mode, the STO/ETO timers and the EF command are used to control the duration of the control channel. STO and ETO count up and expire when they reach their programmed value. STO and ETO are not enabled at the same time. STO is enabled after CCEN goes high. If there is activity from the ECU before STO times out, STO is disabled and ETO is enabled. The ECU must begin a transaction within an STO timeout or else the channel closes. The ECU can close the channel by allowing ETO to time-out. Activity from the ECU resets the ETO timer. Another way to close the control channel is by sending an end frame (EF). EF closes the channel within 2 to 3 bit times after being received by the MAX9257A/MAX9258A. The default value of EF is 0xFF, but can be programmed to any other value besides the MAX9257A and the MAX9258A device addresses. The control channel must be closed with EF for control channel errors to be reported.

Program STO to be longer than the time the ECU takes to respond to opening of channel. Program ETO to be longer than the time the ECU pauses between transactions. As long as the ECU performs transactions, ETO is reset and the channel stays open.

The ECU must wait 14 or more bit times before addressing another device during the same control channel session. Failure to wait 14 bit times may result in the packet boundary not being reset. Internal handshaking operations are automatically performed after the channel is closed and before the video phase begins.

UART-to-I2C Converter

The UART-to-I2C converter accepts UART read or write packets issued by the ECU and converts them to an I2C master protocol when in base mode. A slave can use an ACK or NACK to indicate a busy or wait state, but cannot hold SCL low to indicate a wait state. Multiple slaves are supported. The UART-to-I2C conversion delay is less than 22 UART bit times and needs to be taken into account when setting the ETO and STO timeout periods for read commands. UART-to-I2C converter converts standard UART format to standard I2C format (Figure 25). This

includes data-bit ordering conversion because UART transmits the LSB in first while I²C transmits the MSB first. UART/I²C read delay is a maximum 34 bit times when reading from an I²C peripheral.

The devices store their own 7-bit device addresses in register REG5. All packets not addressed to the MAX9257A/MAX9258A are forwarded to the UARTto-I²C converter. The I²C interfaces (SDA and SCL) are open drain and actively drive a low state. When idle, SDA and SCL are high impedance and pulled high by a pullup resistor. SDA and SCL are idle when packets are addressed to the MAX9257A or MAX9258A. SDA and SCL are also idle when the I²C interface is programmed to be disabled.

Bypass Mode (Details)

In bypass mode, ECU activity and UART communication from the camera reset the ETO and CTO timers. This allows the control channel to stay in bypass as long as there is camera activity. In base mode, only ECU activity resets the ETO and CTO timers.

Bypass mode temporarily or permanently blocks programming of the devices. Bypass mode allows only UART programming of peripheral device by ECU. There is no I²C connection in bypass mode. Bypass mode is entered by writing a 0 to INTMODE and by writing a 1 to INTEN (Table 23). Bypass mode disables ECU programming of the devices to allow any UART communication protocol with the peripheral device. Once bypass mode is entered, the devices stay in bypass mode until CTO times out.

In bypass mode, the STO and ETO timers determine the control channel duration. CTO timer determines whether to revert back to base mode or not, and EF is not recognized.

A useful setting in bypass mode is to set STO > CTO > ETO because this setting is an alternative to permanent bypass (Figure 24). Use this setting to stay in bypass mode to avoid the overhead of entering from base mode every time the control channel opens. If the ECU uses the channel within a CTO timeout, ETO is activated and then ETO times out before CTO. The channel closes because ETO times out, but channel stays in bypass mode because CTO does not time out. At the next vertical blanking time, bypass mode continues with CTO reset and the ECU can immediately send commands to the camera. If the ECU or camera does not use the channel, CTO times out before STO. STO closes the channel (because ETO is not enabled) if no communication is sent, but since CTO timed out, bypass mode ends and base mode is active for the next vertical blanking period.

With STO > CTO > ETO, bypass mode can be made continuous by having the ECU send real commands or dummy commands (such as a command to a nonexisting address) each time the control channel opens. Then the ECU does not have to send a command to enter bypass mode each time it wants to program the peripheral device.

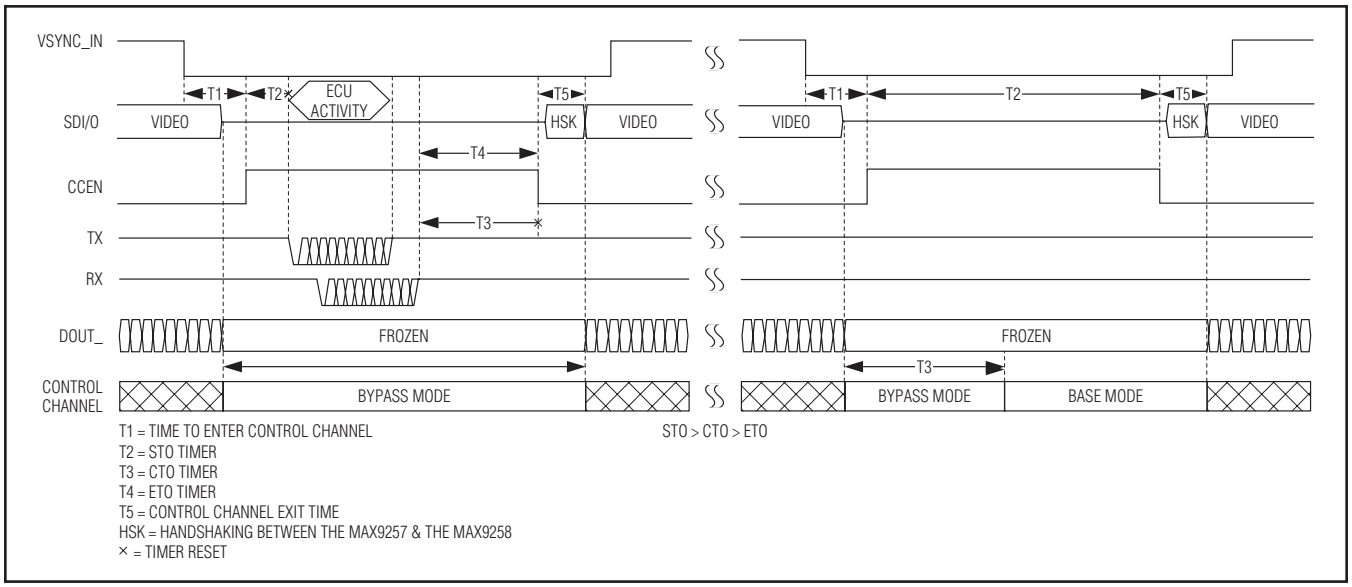


Figure 24. CTO Timing

UART

UART Frame Format

The UART frame used to program the MAX9257A and the MAX9258A has a low start bit, eight data bits, an even parity bit and a high stop bit. The data following the start bit is the LSB. With even parity, when there are an odd number of 1s in the data bits (D0 through D7) the parity bit is set to 1. The stop bit is sampled and if it is not high, a frame error is generated (Figure 26).

UART Synchronization Frame

The synchronization frame must precede any read or write packets (Figure 26). Transitions in the frame calibrate the oscillators on the devices. The baud rate of the synchronization frame sets the operating baud rate of the control channel. At power-up, UART data rate must be between 95kbps to 400kbps. After power-up, UART data rate can be programmed according to Tables 28 and 29. Data is serialized starting with the LSB first. The synchronization frame is 0x54 as shown in Figure 27.

Write Packet

The ECU writes the sync frame, 7-bit device address plus read/write bit (R/W = 0 for write), 8-bit register address, number of bytes to be written, and data bytes (Figure 28). The ECU must follow this UART protocol to correctly program the devices.

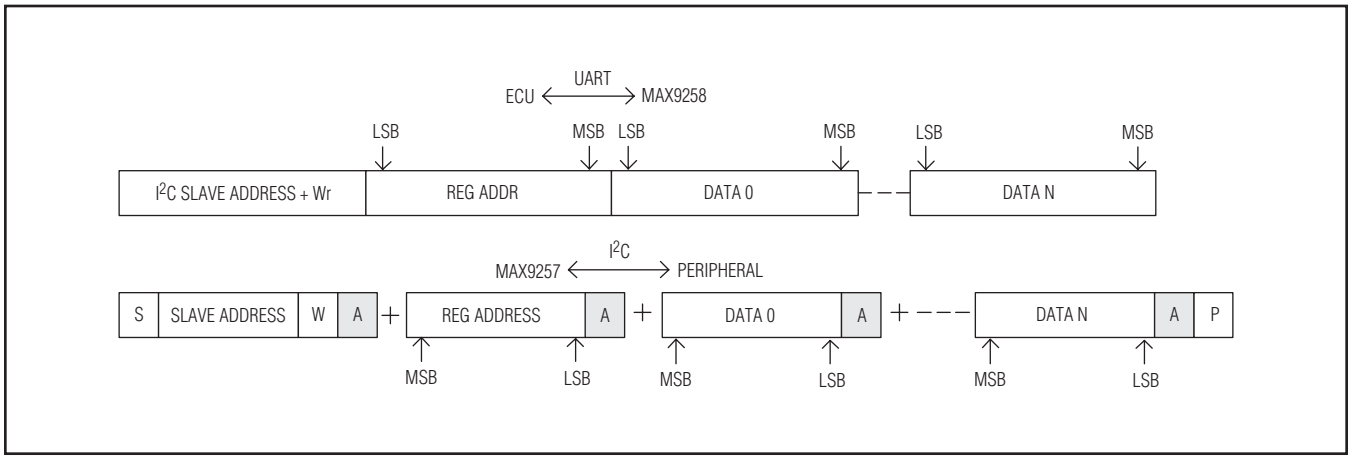


Figure 25. UART-to-I²C Conversion

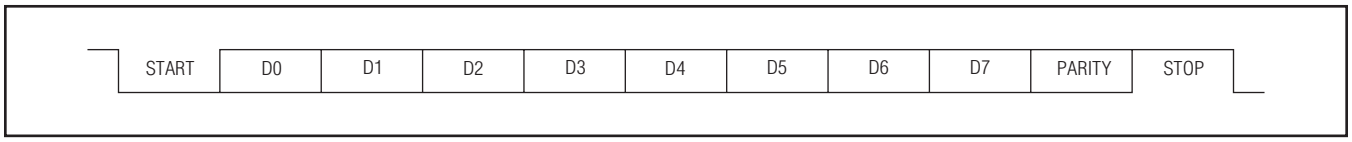


Figure 26. UART Frame Format

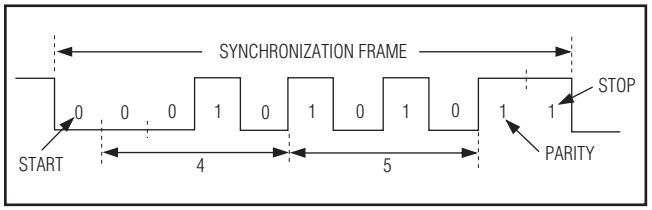


Figure 27. UART Synchronization Frame

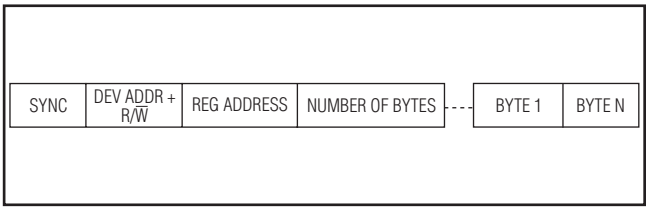


Figure 28. UART Write Packet to MAX9257A/MAX9258A

Read Packet

The ECU writes the sync frame, 7-bit device address plus read/write bit (R/W = 1 for read), 8-bit register address, and number of bytes to be read. The addressed device responds with read data bytes (Figure 29). UART read delay is maximum 4 bit times when reading from the MAX9257A or the MAX9258A.

Time Between Frames

Up to two high bit times are allowed between frames.

Reset of Packet Boundary

A high time ranging from 14 UART bit times or more resets the packet boundary. In this case, the next frame received is assumed to belong to a new packet by the MAX9257A/MAX9258A and UART-to-I2C converter. Resetting the boundary is required. Not resetting the boundary treats the following packets as part of the first packet, and they may be processed incorrectly.

Data Rate

The control channel data rate in base mode is between 95kbps to 4.25Mbps (Table 28). In bypass mode, the allowed data rate is DC to 10Mbps (Table 29). For data rates faster than 4.25Mbps in bypass mode, REG8[5] in MAX9257A and REG7[5] in MAX9258A must be set high. Set the control channel data rate in base mode by writing to REG8[1:0] in the MAX9257A and REG7[1:0] in the MAX9258A. These write commands take effect in the next control channel.

Programming the FAST bit takes effect in the same control channel. Both the MAX9257A and the MAX9258A should have the same settings for FAST. It is recommended to first program the FAST bit in the MAX9257A. Programming FAST to 1 results in shorter UART pulses on the differential link.

MAX9257A/MAX9258A Device Address Programming

The MAX9257A/MAX9258A have device addresses that can be programmed to any 7-bit address. Table 30 shows the default addresses.

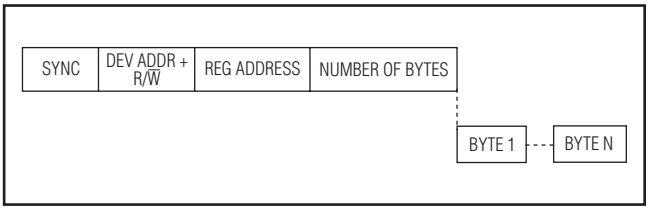


Figure 29. UART Read Packet

Table 28. Control Channel Data Rate in Base Mode

MAX9257A REG8[1:0] MAX9258A REG7[1:0]	RANGE
00	95kbps–400kbps (default)
01	400kbps–1Mbps
10	1Mbps–4.25Mbps
11	1Mbps–4.25Mbps

Table 29. Control Channel Data Rate in Bypass Mode

MAX9257A REG8[5] MAX9258A REG7[5]	RANGE
0	DC–4.25Mbps
1	4.25Mbps–10Mbps

Table 30. Default Device Address

DEVICE	DEFAULT	
	BINARY	HEX
MAX9257A	1111 1010	0xFA
MAX9258A	1111 1000	0xF8

I2C

The MAX9257A features a UART-to-I2C converter that converts UART packets to I2C. The UART-to-I2C converter works as a repeater between the ECU and external I2C slave devices. The MAX9257A acts as the master and converts UART read/write packets from the ECU to I2C read/write for external I2C slave devices. For writes, the UART-to-I2C converts the UART packets received directly into I2C. For reads, the UART-to-I2C converter follows the UART packet protocol. The I2C SCL clock period is approximately the same as the UART bit clock period (tUCLK). The I2C speed varies with UART speed.

I2C reads from the peripheral device do not disable the ETO timer. Choose ETO large enough so that I2C read commands are not lost due to ETO timing out.

I2C Timing

The MAX9257A acts like a master in I2C communication with the peripheral device. The MAX9257A takes less than 22 UART bit times to convert UART packets into I2C. The SCL and SDA timings are based on the UART bit clock. The I2C data rate is determined by UART and can range from 95kbps to 4.25Mbps. The I2C timing requirements scale linearly from fast mode to higher speeds. Table 31 shows the I2C timing information for data rates greater than 400kbps. The I2C parameters scale with t_{UCLK}. See Figure 30 for timing parameters.

Table 31. Timing Information for I2C Data Rates Greater than 400kbps

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCL Clock Frequency	f_{SCL}	1	1		t_{UCLK}*
Start Condition Hold Time	$t_{HD:STA}$	1	1		t_{UCLK}
Low Period of SCL Clock	t_{LOW}	0.5	0.5		t_{UCLK}
High Period of SCL Clock	t_{HIGH}	0.5	0.5		t_{UCLK}
Repeated START Condition Setup Time	$t_{SU:STA}$	0.25	0.25		t_{UCLK}
Data Hold Time	$t_{HD:DAT}$	0.25	0.25		t_{UCLK}
Data Setup Time	$t_{SU:DAT}$	0.25	0.25		t_{UCLK}
Setup Time for STOP Condition	$t_{SU:STO}$	0.25	0.25		t_{UCLK}
Bus Free Time	t_{BUF}	0.5	0.5		t_{UCLK}

t_{UCLK} is equal to one UART period.

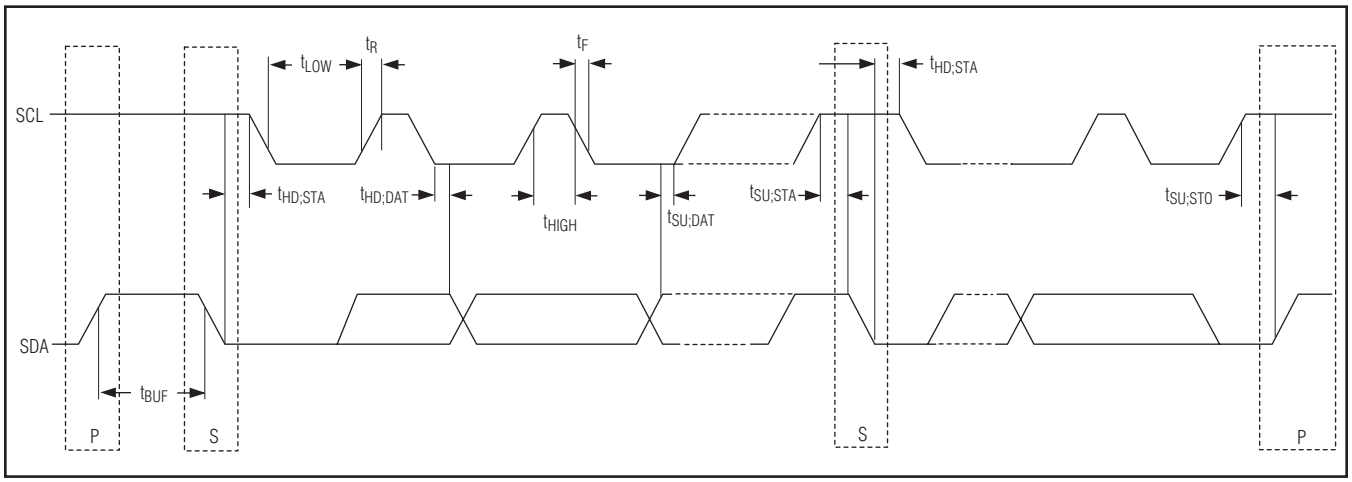


Figure 30. I2C Timing Parameters

Applications Information

PRBS Test

The devices have built-in circuits for testing bit errors on the serial link. The MAX9257A has a PRBS generator and the MAX9258A has a PRBS checker. The length of the PRBS pattern is programmable from 221 to 235 word length or continuous by programming REG9[7:4] in the MAX9257A. In case of errors, errors are counted in the MAX9258A PRBSERR register (REG12), and the $\overline{\text{ERROR}}$ output on the MAX9258A goes low. To start the test, the ECU writes a 1 to PRBSEN bit of both the MAX9257A and the MAX9258A. The PRBS test can be performed with or without spread spectrum. If the PRBS test is programmed to run continuously, the MAX9257A must be powered down to stop the test. When programmed for a finite number of repetitions, the control channel is enabled after the PRBS test finishes and serialization enable (SEREN) is reset to 0. To start normal operation, the ECU must disable PRBSEN and enable SEREN.

Video Data Parity

Parity protection of video data is programmable for parallel-word widths of 16 bits or less. When programmed, two parity bits are appended to each parallel word latched into the MAX9257A. In the MAX9258A, a 16-bit parity error counter logs parity errors. The ERROR output on the MAX9258A goes low if parity errors exceed a programmable threshold.

Table 32. Maximum Data Rate at Different Input Offset Settings

OFFSET BITS (REG1[4:3)	TYPICAL INPUT OFFSET (mV)	MAXIMUM FREQUENCY (Mbps)
00	23	780
01	11	940
10	59	520
11	75	400

Activity Detector

Most applications use the default activity-detector settings. If there is excessive noise on the link when the link is not driven (during control channel mode), increase the activity-detector offset to filter out noise amplitudes. Using a larger offset threshold affects the maximum data rate available. Table 32 lists the maximum recommended data rate at different input offset settings for a 150mV peak input signal.

AC-Coupling Benefits

AC-coupling increases the input voltage of the LVDS receiver to the voltage rating of the capacitor. Two from 18MHz to 42MHz capacitors are sufficient for isolation, but four capacitors—two at the serializer output and two at the deserializer input—provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and common-mode noise.

Selection of AC-Coupling Capacitors

See Figure 31 for calculating the capacitor values for AC-coupling depending on the parallel clock frequency. The plot shows minimum capacitor values for two- and four-capacitor-per-link systems. To block the highest common-mode frequency shift, choose the minimum capacitor value shown in Figure 31. In general, 0.1µF capacitors are sufficient.

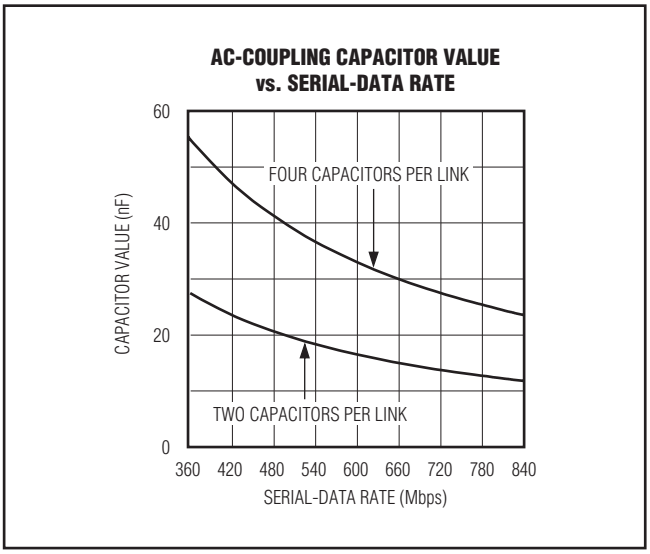


Figure 31. AC-Coupling Capacitor Values vs. Clock Frequency from 18MHz to 42MHz

Optimally Choosing AC-Coupling Capacitors

Voltage droop and the digital sum variaton (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the LVDS receiver termination resistor (R_{TR}), the LVDS driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is (C x (R_{TD} + R_{TR}))/4. RTD and RTR are required to match the transmission line impedance (usually 100Ω). This leaves the capacitor selection to change the system time constant. In the following example, the capacitor value for a droop of 2% is calculated:

$$C = -\frac{4 \times t_B \times DSV}{\ln(1 - D) \times (R_{TR} + R_{TD})}$$

where:

C = AC-coupling capacitor (F)

t_B = bit time(s)

DSV = digital sum variation (integer)

ln = natural log

D = droop (% of signal amplitude)

R_{TD} = driver termination resistor (Ω)

R_{TR} = receiver termination resistor (Ω)

The bit time (t_B) is the serial-clock period or the period of the pixel clock divided by the total number of bits. The maximum DSV for the MAX9257A encoding equals to the total number of bits transmitted in one pixel clock cycle. This means that t_B x DSV = t_T.

The capacitor for 2% maximum droop at 16MHz parallel rate clock is:

$$C = -\frac{4 \times t_B \times DSV}{\ln(1 - D) \times (R_{TR} + R_{TD})}$$

Total number of bits is = 10 (data) + 2 (HSYNC and VSYNC) + 2 (encoding) + 2 (parity) = 16

$$C = -\frac{4 \times 3.91ns \times 16}{\ln(1 - .02) \times (100\Omega + 100\Omega)}$$

C ≥ 0.062µF

Jitter due to droop is proportional to the droop and transition time:

$t_J = t_{TT}$ x D

where:

t_J = jitter(s)

t_{TT} = transition time(s) (0 to 100%)

D = droop (% of signal amplitude)

Jitter due to 2% droop and assumed 1ns transition time is:

t_J = 1ns x 0.02

t_J = 20ps

The transition time in a real system depends on the frequency response of the cable driven by the serializer.

The capacitor value decreases for a higher frequency parallel clock and for higher levels of droop and jitter. Use high-frequency, surface-mount ceramic capacitors.

Power-Supply Circuits and Bypassing

All single-ended inputs and outputs on the MAX9257A are powered from V_{CCIO}. All single-ended outputs on the MAX9258A are powered from V_{CCOUT}. V_{CCIO} and V_{CCOUT} can be connected to a +1.71V to +3.6V supply. The input levels or output levels scale with these supply rails.

Board Layout

Separate the LVCMOS/LVTTL signals and LVDS signals to prevent crosstalk. A four-layer PCB with separate layers for power, ground, LVDS, and digital signals is recommended. Layout PCB traces for 100Ω differential characteristic impedance. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer.

Route the PCB traces for an LVDS channel (there are two conductors per LVDS channel) in parallel to maintain the differential characteristic impedance. Place the 100Ω (typ) termination resistor at both ends of the LVDS driver and receiver. Avoid vias. If vias must be used, use only one pair per LVDS channel and place the via for each line at the same point along the length of the PCB traces. This way, any reflections occur at the same time. Do not make vias into test points for ATE. Make the PCB traces that make up a differential pair the same length to avoid skew within the differential pair.

Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode that is rejected by the LVDS receiver.

Choosing I2C Pullup Resistors

I2C requires pullup resistors to provide a logic-high level to data and clock lines. There are tradeoffs between power dissipation and speed, and a compromise must be made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when device is not in operation. I2C specifies 300ns rise times to go from low to high (30% to 70%) for fast mode, which is defined for a date rate up to 400kbps (see *I2C* specifications for details). To meet the rise time requirement, choose the pullup resistors so the rise time $t_R = 0.85R_{PULLUP} \times C_{BUS} < 300ns$. If the transition time becomes too slow, the setup and hold times may not be met and waveforms will not be recognized.

MAX9257A Register Table

ADDRESS	BITS	DEFAULT	NAME	DESCRIPTION
0	7:6	10	PRATE	Pixel clock frequency range 00 = 5MHz to 10MHz 01 = 10MHz to 20MHz 10 = 20MHz to 40MHz (default) 11 = 40MHz to 70MHz
	5:4	11	SRATE	Serial-data rate range 00 = 60Mbps to 100Mbps 01 = 100Mbps to 200Mbps 10 = 200Mbps to 400Mbps 11 = 400Mbps to 840Mbps (default)
	3	0	PAREN	Parity enable 0 = disabled (default), 1 = enabled
	2:0	101	PWIDTH	Parallel data width (includes HSYNC and VSYNC, excludes DCB, INV, and parity bits) 000 = 10 100 = 18 001 = 12 101 = 18 (default) 010 = 14 110 = 18 011 = 16 111 = 18
1	7:5	000	SPREAD	Spread-spectrum setting For PRATE ranges 00, 01: all spread options possible For PRATE ranges 10, 11: maximum spread is 2% 000 = Off (default) 100 = Off 001 = 1.5% 101 = 3% 010 = 1.75% 110 = 3.5% 011 = 2% 111 = 4%
	4:0	11111		Reserved (set to 11111)

MAX9257A Register Table (continued)

ADDRESS	BITS	DEFAULT	NAME	DESCRIPTION
2	Control channel start timeout: (STO) times out if ECU does not start using control channel within this amount of time after control channel session is enabled.			
	7:4	1010	STODIV	Control channel start timeout divider Pixel clock is first divided by: 0000 = 16 1000 = 256 0001 = 16 1001 = 512 0010 = 16 1010 = 1024 (default) 0011 = 16 1011 = 2048 0100 = 16 1100 = 4096 0101 = 32 1101 = 8192 0110 = 64 1110 = 16,384 0111 = 128 1111 = 32,768
	3:0	0000	STOCNT	Control channel start timeout counter Divided pixel clock is used to count up to (STOCNT + 1)
3	Control channel end timeout: (ETO) times out if ECU does not use control channel for this amount of time after it has already used at least once.			
	7:4	1010	ETODIV	Control channel end timeout divider Pixel clock is first divided by: 0000 = 16 1000 = 256 0001 = 16 1001 = 512 0010 = 16 1010 = 1024 (default) 0011 = 16 1011 = 2048 0100 = 16 1100 = 4096 0101 = 32 1101 = 8192 0110 = 64 1110 = 16,384 0111 = 128 1111 = 32,768
	3:0	0000	ETOCNT	Control channel end timeout counter Divided pixel clock is used to count up to (ETOCNT + 1)

MAX9257A Register Table (continued)

ADDRESS	BITS	DEFAULT	NAME	DESCRIPTION
4	7	0	VEDGE	VSYNC active edge at camera interface 0 = falling (default), 1 = rising
	6	0		Reserved (set to 0)
	5	1	CKEDGE	PCLK active edge at camera interface 0 = falling, 1 = rising (default)
	4	0	PD	Power mode 0 = power-up, 1 = power-down (when REM = 1 default is 1)
	3	1	SEREN	Serialization enable 0 = disabled, 1 = enabled (when REM = 1 default is 0)
	2	0	BYPFPLL	Bypass filter PLL 0 = active (default), 1 = bypass
	1	0		Reserved (set to 0)
	0	0	PRBSEN	PRBS test enable 0 = disabled (default), 1 = enabled
5	7:1	1111101	DEVICEID	7-bit address of MAX9257A
	0	0		Reserved (set to 0)
6	7:1	1111111	EF	End frame to close control channel
	0	1		Reserved (set to 1)
7	7:1	1111100	DESID	7-bit address ID of MAX9258A
	0	0		Reserved (set to 0)
8	7	0	INTMODE	Interface mode 0 = UART (default), 1 = I²C
	6	0	INTEN	Interface enable 0 = disabled (default), 1 = enabled
	5	0	FAST	Fast UART transceiver 0 = bit rate = DC to 4.25Mbps (default), 1 = bit rate = 4.25Mbps to 10Mbps
	4:2	000	CTO	Timer to come back from bypass mode (in bit time) 000 = never come back (default) 100 = 64 001 = 16 101 = 80 010 = 32 110 = 96 011 = 48 111 = 112
	1:0	00	BITRATE	Control channel bit rate range in base mode 00 = 95kbps to 400kbps (default) 01 = 400kbps to 1000kbps 10 = 1000kbps to 4250kbps 11 = 1000kbps to 4250kbps

MAX9257A Register Table (continued)

ADDRESS	BITS	DEFAULT	NAME	DESCRIPTION
9	7:4	0000	PRBSLEN	PRBS test number of words 1111 = continuous else = $2^{(PRBSLEN + 21)}$
	3	0	GPIO9DIR	GPIO 9 direction 0 = input (default), 1 = output
	2	0	GPIO8DIR	GPIO 8 direction 0 = input (default), 1 = output
	1	0	GPIO9*	General purpose input output 9
	0	0	GPIO8*	General purpose input output 8
10	7	0	GPIO7DIR	GPIO 7 direction 0 = input (default), 1 = output
	6	0	GPIO6DIR	GPIO 6 direction 0 = input (default), 1 = output
	5	0	GPIO5DIR	GPIO 5 direction 0 = input (default), 1 = output
	4	0	GPIO4DIR	GPIO 4 direction 0 = input (default), 1 = output
	3	0	GPIO3DIR	GPIO 3 direction 0 = input (default), 1 = output
	2	0	GPIO2DIR	GPIO 2 direction 0 = input (default), 1 = output
	1	0	GPIO1DIR	GPIO 1 direction 0 = input (default), 1 = output
	0	0	GPIO0DIR	GPIO 0 direction 0 = input (default), 1 = output
11	7	0	GPIO7*	General purpose input output 7
	6	0	GPIO6*	General purpose input output 6
	5	0	GPIO5*	General purpose input output 5
	4	0	GPIO4*	General purpose input output 4
	3	0	GPIO3*	General purpose input output 3
	2	0	GPIO2*	General purpose input output 2
	1	0	GPIO1*	General purpose input output 1
	0	0	GPIO0*	General purpose input output 0
12	7:5	111	PREEMP	LVDS driver preemphasis setting 000 = 20% 111 = off (default) 001 = 40% 101 = 20% 010 = 60% 110 = 20% 011 = 80% 100 = 100%
	4:0	00000		Reserved (set to 00000)
13	7:2	000000		Reserved (set to 000000)
	1:0	00	I²CFILT	I²C glitch filter setting 00 = set according to programmed bit rate (default) 100ns at (95kbps to 400kbps) bit rate 50ns at (400kbps to 1000kbps) bit rate 10ns at (1000kbps to 4250kbps) bit rate 01 = 10ns, 10 = 50ns, 11 = 100ns
14	7:1	(RO)		Reserved
	0	(RO)	LOCKED	PLL locked to pixel clock
15	7:0	(RO)		Reserved

MAX9258A Register Table

ADDRESS	BITS	DEFAULT	NAME	DESCRIPTION
0	7:6	10	PRATE	Pixel clock frequency range 00 = 5MHz to 10MHz 01 = 10MHz to 20MHz 10 = 20MHz to 40MHz (default) 11 = 40MHz to 70MHz
	5:4	11	SRATE	Serial-data rate range 00 = 60Mbps to 100Mbps 01 = 100Mbps to 200Mbps 10 = 200Mbps to 400Mbps 11 = 400Mbps to 840Mbps (default)
	3	0	PAREN	Parity enable 0 = disabled (default), 1 = enabled
	2:0	101	PWIDTH	Parallel data width (includes HSYNC and VSYNC, excludes encoding and parity bits) 000 = 10 100 = 18 001 = 12 101 = 18 (default) 010 = 14 110 = 18 011 = 16 111 = 18
1	7:6	00	SPREAD	Spread-spectrum setting 00 = Off (default) 10 = Off 01 = 2% 11 = 4%
	5	0	AER	Autoerror reset 1 = Reset error count when control channel ends. 0 = Reset upon reading error registers 10, 11, 13 (default)
	4:3	00	ACTOFFSET	Activity detector offset level 00 = 23mV offset 01 = 11mV offset 10 = 59mV offset 11 = 75mV offset
	2:0	000		Reserved (set to 000)
2	Control channel start timeout: (STO) times out if ECU does not start using control channel within this amount of time after control channel session is enabled.			
	7:4	1010	STODIV	Control channel start timeout divider Pixel clock is first divided by : 0000 = 16 1000 = 256 0001 = 16 1001 = 512 0010 = 16 1010 = 1024 (default) 0011 = 16 1011 = 2048 0100 = 16 1100 = 4096 0101 = 32 1101 = 8192 0110 = 64 1110 = 16,384 0111 = 128 1111 = 32,768
	3:0	0000	STOCNT	Control channel start timeout counter Divided pixel clock is used to count up to (STOCNT + 1)

MAX9258A Register Table (continued)

ADDRESS	BITS	DEFAULT	NAME	DESCRIPTION
3	Control channel end timeout: (ETO) times out if ECU does not use control channel for this amount of time after it has already used at least once.			
	7:4	1010	ETODIV	Control channel end timeout divider Pixel clock is first divided by: 0000 = 16 1000 = 256 0001 = 16 1001 = 512 0010 = 16 1010 = 1024 (default) 0011 = 16 1011 = 2048 0100 = 16 1100 = 4096 0101 = 32 1101 = 8192 0110 = 64 1110 = 16,384 0111 = 128 1111 = 32,768
	3:0	0000	ETOCNT	Control channel end timeout counter Divided pixel clock is used to count up to (ETOCNT + 1)
4	7	0	VEDGE	VSYNC active edge at ECU interface 0 = falling (default), 1 = rising
	6	0	HEDGE	HSYNC active edge at ECU interface 0 = falling (default), 1 = rising
	5	1	CKEDGE	PCLK active edge at ECU interface 0 = falling, 1 = rising (default)
	4	0		Reserved (set to 0)
	3	0	ACTLP	0 = stretcher output pulse is short 1 = stretcher output pulse is long
	2:1	00		Reserved (set to 00)
	0	0	PRBSEN	PRBS test enable 0 = disabled (default), 1 = enabled
5	7:1	1111100	DEVICEID	7-bit address of MAX9258A
	0	0		Reserved (set to 0)
6	7:1	1111111	EF	End frame to close control channel
	0	1		Reserved (set to 1)

MAX9258A Register Table (continued)

ADDRESS	BITS	DEFAULT	NAME	DESCRIPTION
7	7	0	INTMODE	Interface mode 0 = UART (default), 1 = I²C
	6	0	INTEN	Interface enable 0 = disabled (default), 1 = enabled
	5	0	FAST	Fast UART transceiver 0 = bit rate = DC to 4.25Mbps (default), 1 = bit rate = 4.25Mbps to 10 Mbps
	4:2	000	CTO	Timer to come back from bypass mode (in bit time) 000 = never come back (default) 100 = 64 001 = 16 101 = 80 010 = 32 110 = 96 011 = 48 111 = 112
	1:0	00	BITRATE	Control channel bit rate range in base mode 00 = 95kbps to 400kbps (default) 01 = 400kbps to 1000kbps 10 = 1000kbps to 4250kbps 11 = 1000kbps to 4250kbps
8	7:0	00010000	PATHRLO	Threshold for number of video parity errors (8 LSBs) If the number of errors exceeds this value, ERR pin is asserted.
9	7:0	00000000	PATHRHI	Threshold for number of video parity errors (8 MSBs) If the number of errors exceeds this value, ERR pin is asserted.
10	7:0	(RO)	PAERRLO	Number of video parity errors (8 LSBs)
11	7:0	(RO)	PAERRHI	Number of video parity errors (8 MSBs)
12	7:0	(RO)	PRBSERR	PRBS test number of bit errors Automatically reset when PRBS test is disabled 0xFF indicates 255 or more errors
13	7:5	(RO)		Reserved
	4	(RO)	DESPERR	Parity error during communication with deserializer
	3	(RO)	DESFERR	Frame error during communication with deserializer
	2	(RO)	SERPERR	Parity error during communication with serializer
	1	(RO)	SERFERR	Frame error during communication with serializer
	0	(RO)	I²CERR	Error during communication with camera in I²C mode
14	7:0	(RO)		Reserved

ESD Protection

The MAX9257A/MAX9258A ESD tolerance is rated for Human Body Model, Machine Model, IEC 61000-4-2 and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. LVDS outputs on the MAX9257A and LVDS inputs on the MAX9258A meet ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All other pins meet the Human Body Model and Machine Model ESD tolerances. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 33). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 32). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 34). The Machine Model discharge components are C_S = 200pF and R_D = 0Ω (Figure 35).

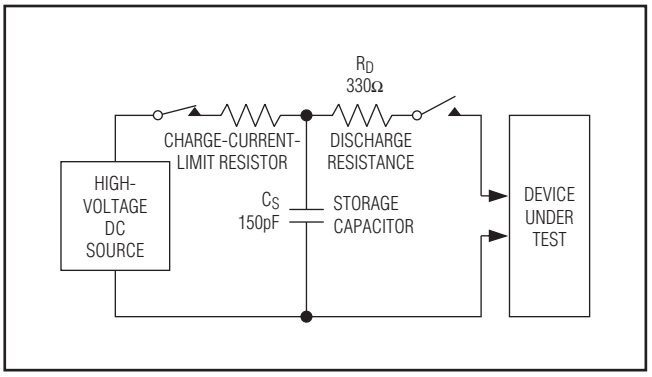


Figure 32. IEC 61000-4-2 Contact Discharge ESD Test Circuit

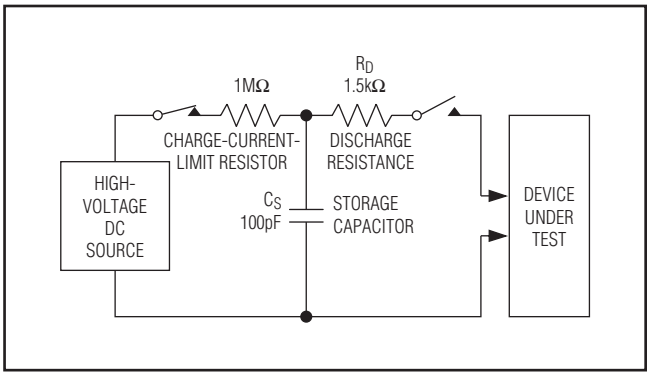


Figure 33. Human Body ESD Test Circuit

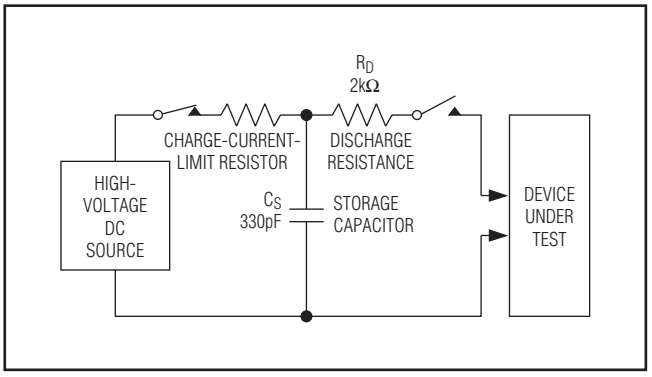


Figure 34. ISO 10605 Contact Discharge ESD Test Circuit

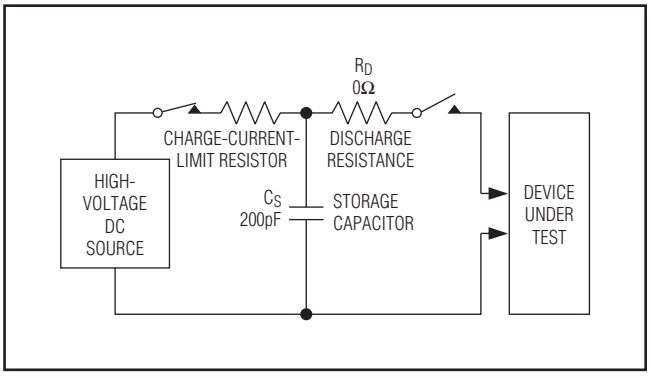
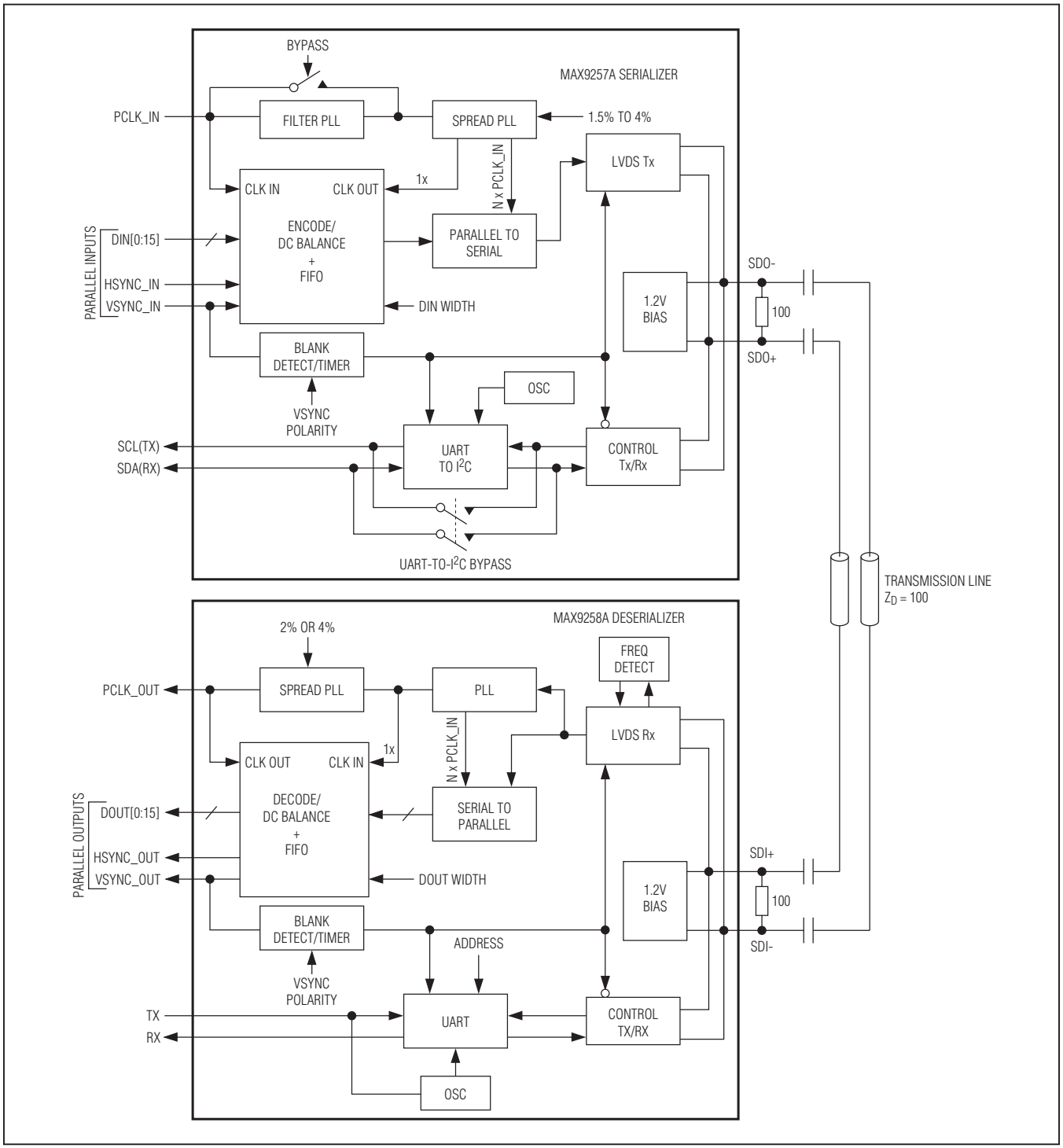


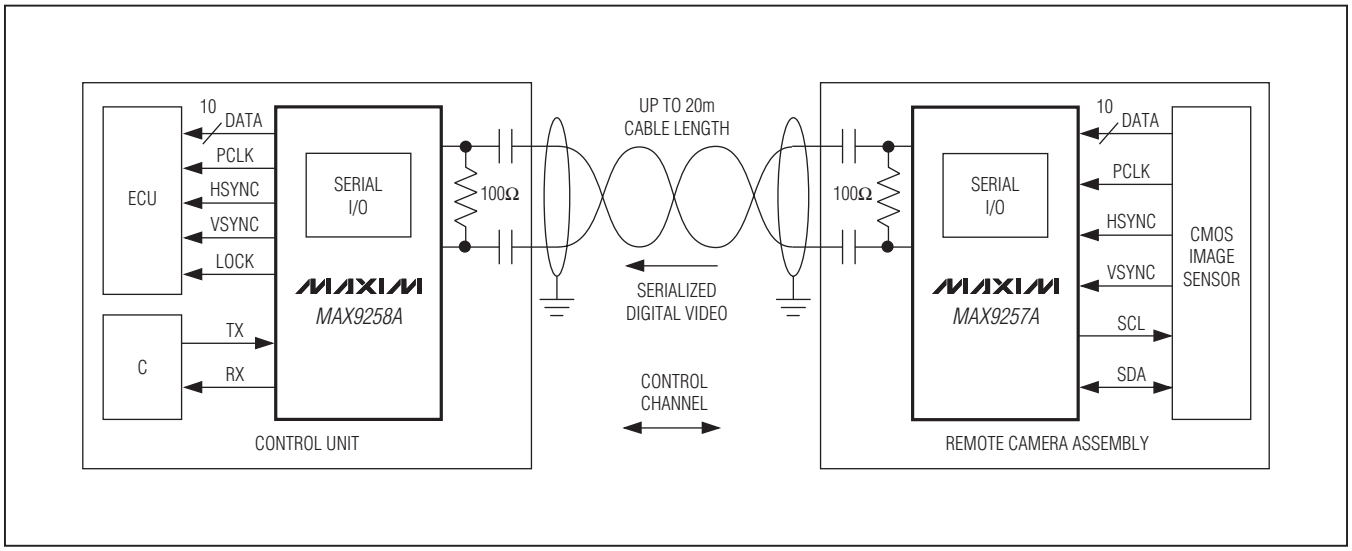
Figure 35. Machine Model ESD Test Circuit

Functional Diagram



Fully Programmable Serializer/Deserializer with UART/I²C Control Channel

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9257AGTL/V+	-40°C to +105°C	40 TQFN-EP*
MAX9257AGCM/V+	-40°C to +105°C	48 LQFP
MAX9258AGCM/V+	-40°C to +105°C	48 LQFP

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN	T4055+1	21-0140	90-0016
48 LQFP	C48+3	21-0054	90-0093

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	9/11	Changed ACTOFFSET range settings from 00 = 11mV to 23mV and 01 = 23mV to 11mV	7, 24, 41, 47

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