THE DATASHEET OF

ISL6842IUZ-T

ISL6840, ISL6841, ISL6842, ISL6843, ISL6844

Improved Industry Standard Single-Ended Current Mode PWM Controller

The ISL6840, ISL6841, ISL6842, ISL6843, and ISL6844 (ISL684x) family of adjustable frequency, low power, Pulse-Width Modulating (PWM) current mode controllers is designed for a wide range of power conversion applications including boost, flyback, and isolated output configurations. Peak current mode control effectively handles power transients and provides inherent overcurrent protection.

This advanced BiCMOS design is pin-compatible with the industry standard 384x family of controllers and offers significantly improved performance. Features include low operating current, 60µA start-up current, adjustable operating frequency to 2MHz, and high peak current drive capability with 20ns rise and fall times.

Part Number	Rising UVLO (V)	MAX. Duty Cycle (%)
ISL6840	7.0	100
ISL6841	7.0	50
ISL6842	14.4	100
ISL6843	8.4	100
ISL6844	14.4	50

Related Literature

For a full list of related documents, visit our website:

ISL6840, ISL6841, ISL6842, ISL6843, ISL6844 device pages

Features

- 1A MOSFET gate driver
- 60µA start-up current, 100µA maximum
- 25ns propagation delay current sense to output
- Fast transient response with peak current mode control
- Adjustable switching frequency to 2MHz
- 20ns rise and fall times with 1nF output load
- Trimmed timing capacitor discharge current for accurate deadtime/maximum duty cycle control
- High bandwidth error amplifier
- Tight tolerance voltage reference over line, load, and temperature
- Tight tolerance current limit threshold
- Pb-free available (RoHS compliant)

Applications

- Telecom and datacom power
- Wireless base station power
- File server power
- Industrial power systems
- PC power supplies
- Isolated buck and flyback regulators
- Boost regulators

1. Overview

1.1 Typical Applications

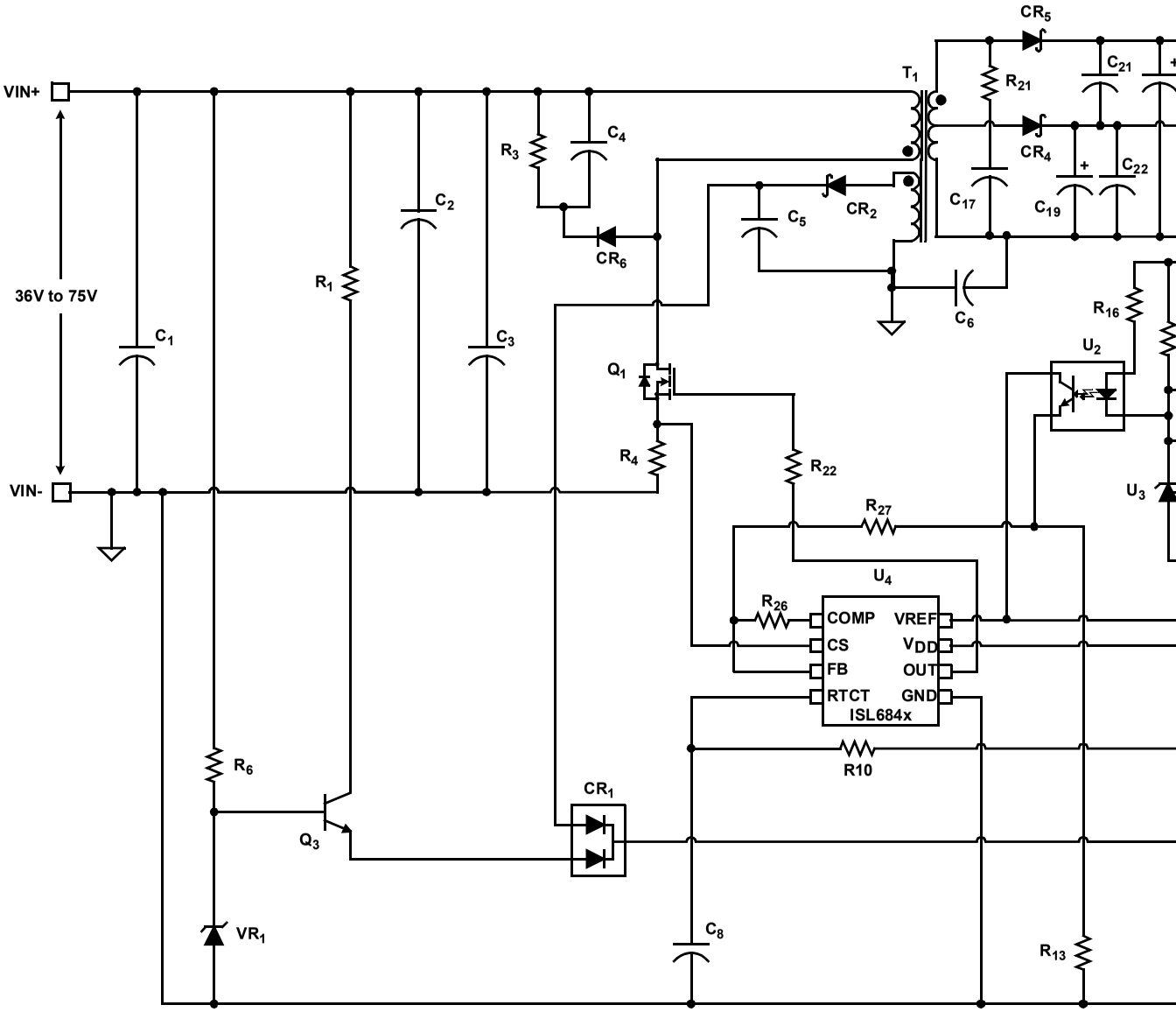


Figure 1. 48V Input Dual Output Flyback

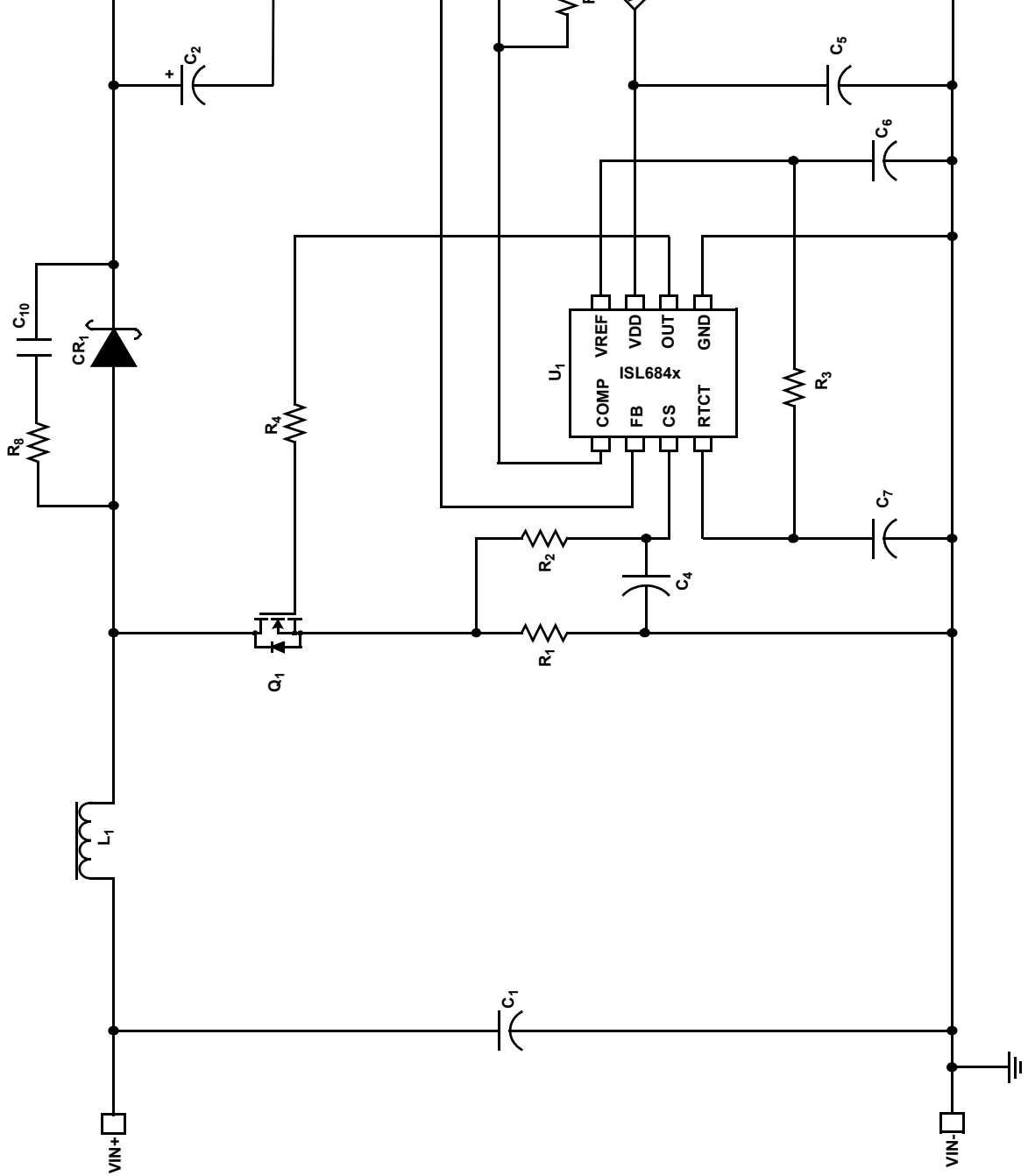


Figure 2. Boost Converter

1.2 Functional Block Diagram

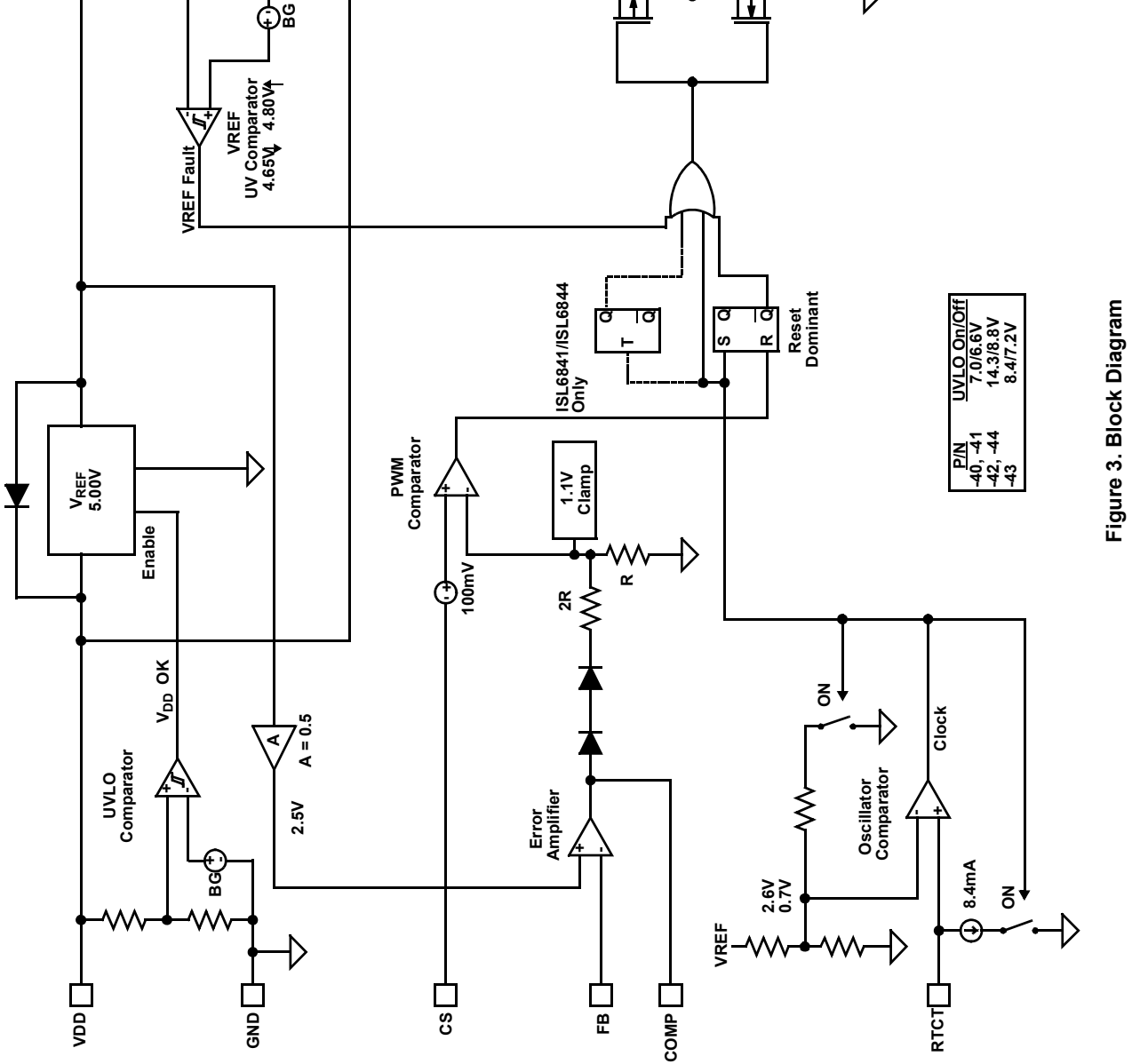


Figure 3. Block Diagram

1.3 Ordering Information

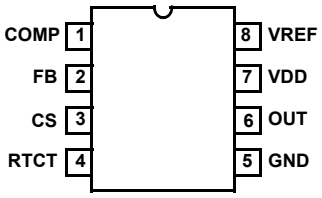
Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package	Pkg. Dwg. #
ISL6840IBZ-T	6840 IBZ	-40 to +105	2.5k	8 Ld SOIC	M8.15
ISL6840IRZ-T	40Z	-40 to +105	6k	8 Ld 2x3 DFN	L8.2x3
ISL6840IUZ	6840Z	-40 to +105	-	8 Ld MSOP	M8.118
ISL6840IUZ-T	6840Z	-40 to +105	2.5k	8 Ld MSOP	M8.118
ISL6841IUZ **(No longer available, recommended replacement: ISL8841AAUZ)**	6841Z	-40 to +105	-	8 Ld MSOP	M8.118
ISL6841IUZ-T **(No longer available, recommended replacement: ISL8841AAUZ-T)**	6841Z	-40 to +105	2.5k	8 Ld MSOP	M8.118
ISL6842IBZ	6842 IBZ	-40 to +105	-	8 Ld SOIC	M8.15
ISL6842IBZ-T	6842 IBZ	-40 to +105	2.5k	8 Ld SOIC	M8.15
ISL6843IBZ	6843 IBZ	-40 to +105	-	8 Ld SOIC	M8.15
ISL6843IBZ-T	6843 IBZ	-40 to +105	2.5k	8 Ld SOIC	M8.15
ISL6843IUZ	6843Z	-40 to +105	-	8 Ld MSOP	M8.118
ISL6843IUZ-T	6843Z	-40 to +105	2.5k	8 Ld MSOP	M8.118
ISL6844IBZ **(No longer available, recommended replacement: ISL8844AABZ)**	6844 IBZ	-40 to +105		8 Ld SOIC	M8.15
ISL6841EVAL3Z **(No longer available or supported)**	Evaluation Board				

Notes:

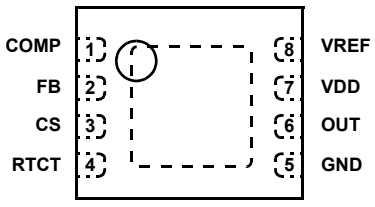
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL6840, ISL6841, ISL6842, ISL6843, and ISL6844 device information pages. For more information about MSL, see TB363.

1.4 Pin Configurations

8 LD SOIC, MSOP
Top View



8 Ld DFN
Top View



1.5 Pin Descriptions

Pin Number	Pin Name	Description
1	COMP	The error amplifier output and the PWM comparator input. The control loop frequency compensation network is connected between the COMP and FB pins.
2	FB	The output voltage feedback is connected to the inverting input of the error amplifier through this pin. The non-inverting input of the error amplifier is internally tied to a reference voltage.
3	CS	The current sense input to the PWM comparator. The input signal range is nominally 0V to 1.0V and has an internal offset of 100mV.
4	RTCT	The oscillator timing control pin. The operational frequency and maximum duty cycle are set by connecting a resistor, RT, between VREF and this pin and a timing capacitor, CT, from this pin to GND. The oscillator produces a sawtooth waveform with a programmable frequency range up to 2.0MHz. The charge time, t_C, the discharge time, t_D, the switching frequency, f, and the maximum duty cycle, Dmax, can be calculated from Equations 1, 2, 3 and 4: (EQ. 1) $t_C \approx 0.583 \bullet RT \bullet CT$ (EQ. 2) $t_D \approx -RT \bullet CT \bullet \ln\left(\frac{0.0083 \bullet RT - 4.3}{0.0083 \bullet RT - 2.4}\right)$ (EQ. 3) $f = 1/(t_C + t_D)$ (EQ. 4) $D = t_C \bullet f$ Figure 7 on page 10 can be used as a guideline in selecting the capacitor and resistor values required for a given frequency.
5	GND	The power and small signal reference ground for all functions.
6	OUT	The drive output to the power switching device. It is a high current output capable of driving the gate of a power MOSFET with peak currents of 1.0A.
7	VDD	The power connection for the devices. The total supply current depends on the load applied to OUT. Total I_{DD} current is the sum of the operating current and the average output current. Knowing the operating frequency, f, and the MOSFET gate charge, Qg, the average output current can be calculated in Equation 5: (EQ. 5) $I_{OUT} = Qg \times f$ To optimize noise immunity, bypass V_{DD} to GND with a ceramic capacitor as close to the VDD and GND pins as possible.
8	VREF	The 5V reference voltage output. +1.0/-1.5% tolerance over line, load, and operating temperature. Bypass to GND with a 0.1µF to 3.3µF capacitor to filter this output as needed.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DD}	GND - 0.3	+20.0	V
OUT	GND - 0.3	V_{DD} + 0.3	V
Signal Pins	GND - 0.3	6.0	V
Peak GATE Current		1	A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Notes 5, 7)	55	6
SOIC Package (Notes 4, 6)	100	60
MSOP Package (Notes 4, 6)	165	62

Notes:

4. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
6. For θ_{JC}, the “case temp” location is taken at the package top center.
7. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-55	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage Range (Typical, Note 8)			
ISL6840, ISL6841	7.5	14	V
ISL6843	9	16	V
ISL6842, ISL6844	15	18	V
Temperature Range			
ISL684xIx	-40	+105	°C

Note:

8. All voltages are with respect to GND

2.4 Electrical Specifications

Recommended operating conditions unless otherwise noted. See Functional Block Diagram and Typical Applications schematics. V_{DD} = 15V (Note 12), R_t = 10kΩ, C_t = 3.3nF, T_A = -40°C to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C**.

Parameter	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
Undervoltage Lockout					
START Threshold (ISL6840, ISL6841)		**6.5**	7.0	**7.5**	V
START Threshold (ISL6843)		**7.8**	8.4	**9.0**	V
START Threshold (ISL6842, ISL6844)		**13.3**	14.3	**15.3**	V
STOP Threshold (ISL6840, ISL6841)		**6.1**	6.6	**6.9**	V
STOP Threshold (ISL6843)		**6.7**	7.2	**7.7**	V
STOP Threshold (ISL6842, ISL6844)		**8.0**	8.8	**9.6**	V
Hysteresis (ISL6840, ISL6841)			0.4		V
Hysteresis (ISL6843)			0.8		V
Hysteresis (ISL6842, ISL6844)			5.4		V
Start-Up Current, I_{DD}	V_{DD} < START threshold		60	**100**	µA
Operating Current, I_{DD}	(Note 10)		3.3	**4.0**	mA
Operating Supply Current, I_D	Includes 1nF GATE loading		4.1	**5.5**	mA
Reference Voltage					
Overall Accuracy	Over line (V_{DD} = 12V to 18V), load, temperature	**4.925**	5.000	**5.050**	V
Long Term Stability	T_A = +125°C, 1000 hours (Note 11)		5		mV
Fault Voltage		**4.40**	4.65	**4.85**	V
VREF Good Voltage		**4.60**	4.80	**VREF - 0.05**	V
Hysteresis		**50**	165	**250**	mV
Current Limit, Sourcing		**-20**			mA
Current Limit, Sinking		**5**			mA
Current Sense					
Input Bias Current	V_{CS} = 1V	**-1.0**		**1.0**	µA
CS Offset Voltage	V_{CS} = 0V (Note 11)	**95**	100	**105**	mV
COMP to PWM Comparator Offset Voltage	V_{CS} = 0V (Note 11)	**0.80**	1.15	**1.30**	V
Input Signal, Maximum		**0.91**	0.97	**1.03**	V
Gain, $A_{CS} = \Delta V_{COMP}/\Delta V_{CS}$	0 < V_{CS} < 910mV, V_{FB} = 0V (Note 11)	**2.5**	3.0	**3.5**	V/V
CS to OUT Delay	(Note 11)		25	**40**	ns
Error Amplifier					
Open-Loop Voltage Gain	(Note 11)	**60**	90		dB
Reference Voltage	$V_{FB} = V_{COMP}$	**2.475**	2.514	**2.55**	V
FB Input Bias Current	V_{FB} = 0V	**-1.0**	-0.2	**1.0**	µA
COMP Sink Current	V_{COMP} = 1.5V, V_{FB} = 2.7V	**1.0**			mA
COMP Source Current	V_{COMP} = 1.5V, V_{FB} = 2.3V	**-0.4**			mA
COMP V_{OH}	V_{FB} = 2.3V	**4.80**		**VREF**	V
COMP V_{OL}	V_{FB} = 2.7V	**0.4**		**1.0**	V
PSRR	Frequency = 120Hz, V_{DD} = 12V to 18V (Note 11)	**60**	80		dB
Oscillator					
Frequency Accuracy	Initial, T_J = +25°C	**49**	52	**55**	kHz
Frequency Variation with V_{DD}	T = +25°C (f_{18V} - f_{12V})/f_{12V}		0.2	**1.0**	%
Temperature Stability	(Note 11)		-	**5**	%

Recommended operating conditions unless otherwise noted. See Functional Block Diagram and Typical Applications schematics. V_{DD} = 15V (Note 12), R_t = 10kΩ, C_t = 3.3nF, T_A = -40°C to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

Parameter	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
Amplitude, Peak-to-Peak			1.9		V
RTCT Discharge Voltage			0.7		V
Discharge Current	RTCT = 2.0V	**7.2**	8.4	**9.5**	mA
Output					
Gate VOH	V_{DD} to OUT, I_{OUT} = -200mA		1.0	**2.0**	V
Gate VOL	OUT to GND, I_{OUT} = 200mA		1.0	**2.0**	V
Peak Output Current	C_{OUT} = 1nF (Note 11)		1.0		A
Rise Time	C_{OUT} = 1nF (Note 11)		20	**40**	ns
Fall Time	C_{OUT} = 1nF (Note 11)		20	**40**	ns
PWM					
Maximum Duty Cycle	ISL6840, ISL6842, ISL6843	**94**	96		%
	ISL6841, ISL6844	**47**	48		%
Minimum Duty Cycle	ISL6840, ISL6842, ISL6843			**0**	%
	ISL6841, ISL6844			**0**	%

Notes:

9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.
11. Limits established by characterization and are not production tested.
12. Adjust V_{DD} above the start threshold and then lower to 15V.

3. Typical Performance Curves

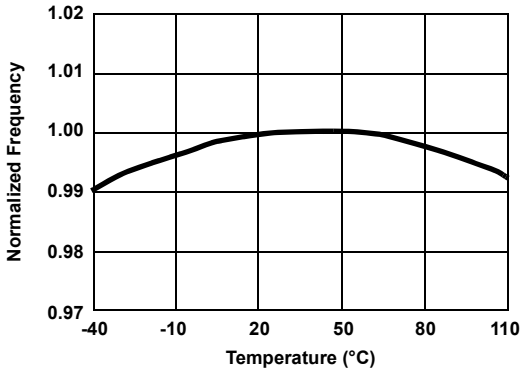


Figure 4. Frequency vs Temperature

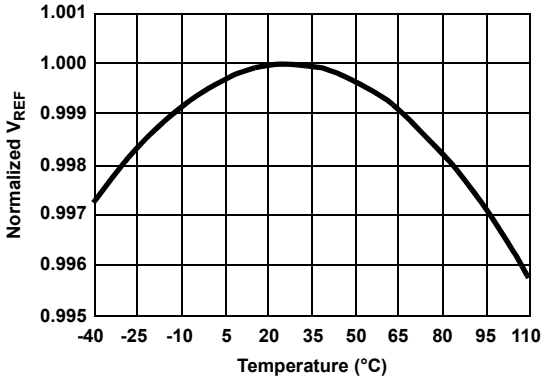


Figure 5. Reference Voltage vs Temperature

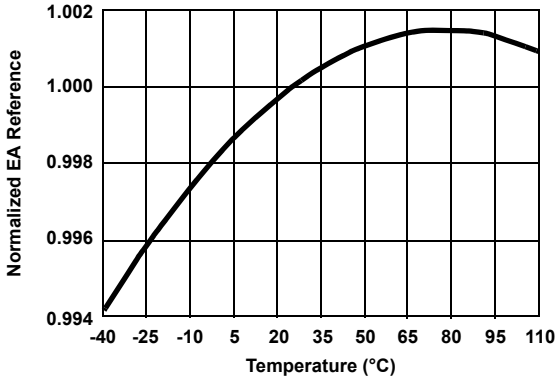


Figure 6. EA Reference vs Temperature

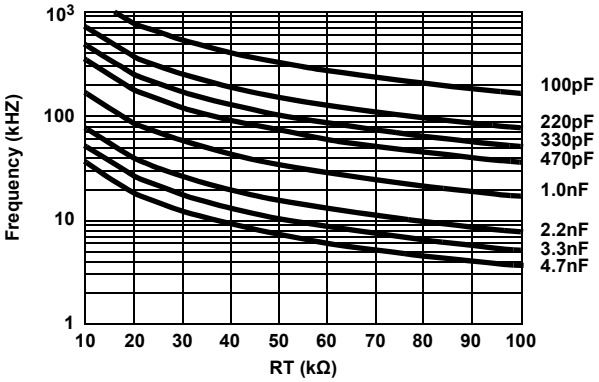


Figure 7. Resistance for CT Capacitor Values Given

4. Functional Description

4.1 Features

The ISL684x current mode PWMs make an ideal choice for low-cost flyback and forward topology applications. With its greatly improved performance over industry standard parts, it is the obvious choice for new designs or existing designs which require updating.

4.2 Oscillator

The ISL684x family of controllers have a sawtooth oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor from VREF and a capacitor to GND on the RTCT pin. (See Figure 7 on page 10 for the resistor and capacitance required for a given frequency.)

4.3 Soft-Start Operation

Soft-start must be implemented externally. Figure 8 shows one method that clamps the voltage on COMP.

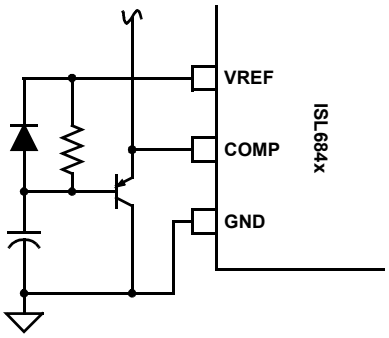


Figure 8. Soft-Start

4.4 Gate Drive

The ISL684x family is capable of sourcing and sinking 1A peak current. To limit the peak current through the ICs, an optional external resistor can be placed between the totem-pole output of the IC (OUT pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

4.5 Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation can be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability. The minimum amount of slope compensation required corresponds to 1/2 the inductor downslope. Adding excessive slope compensation, however, results in a control loop that behaves more as a voltage mode controller than as a current mode controller.

Slope compensation may be added to the CS signal shown in Figure 10 on page 12.

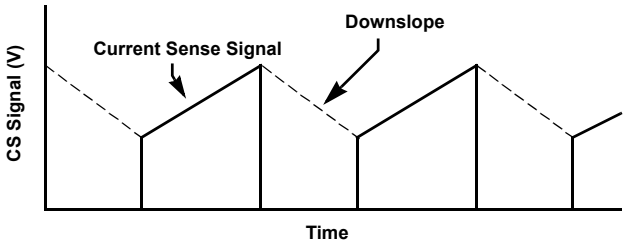


Figure 9. Current Sense Downslope

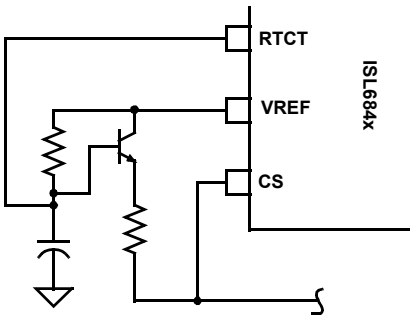


Figure 10. Slope Compensation

4.6 Fault Conditions

A fault condition occurs if VREF falls below 4.65V. When a fault is detected, OUT is disabled. When VREF exceeds 4.80V, the fault condition clears, and OUT is enabled.

4.7 Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. Bypass V_{DD} directly to GND with good high-frequency capacitors.

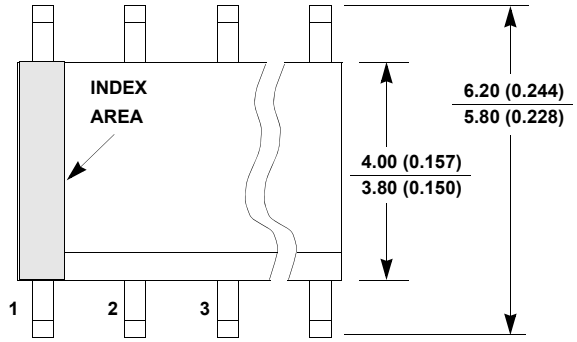
5. Revision History

Rev.	Date	Description
14	Jul.22.19	Applied new formatting and template. Added Related Literature section Updated Ordering Information table by adding tape and reel information, removing retired parts, and updating notes. Removed Note 2. Updated Theta JA for DFN package changed from 77 to 55. Updated Theta JC for SOIC package changed from N/A to 60. Added Note 8 and updated references. Removed ISL6843C information from document. Removed ISL6845 information from document. Updated the disclaimer.
13	Feb.18.16	-Updated Ordering Information table on page 5
12	Sep.29.15	- Updated Ordering Information Table on page 5. - Added Revision History. - Added About Intersil Verbiage. - Updated POD L8.2X3 to latest revision changes are as follow: -Revision 1 to Revision 2 Changes: Tiebar Note 5 updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).

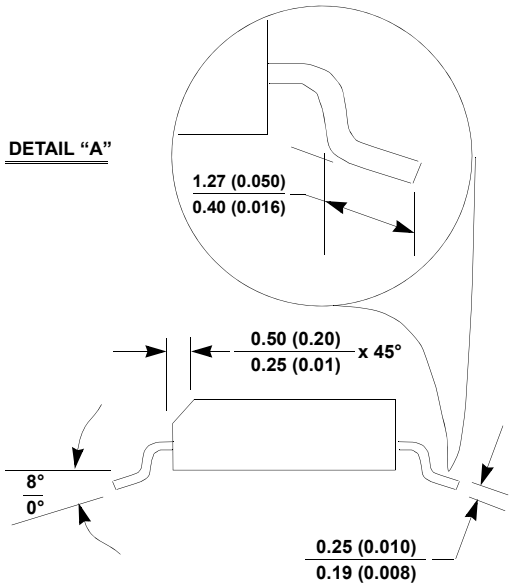
6. Package Outline Drawings

For the most recent package outline drawing, see M8.15.

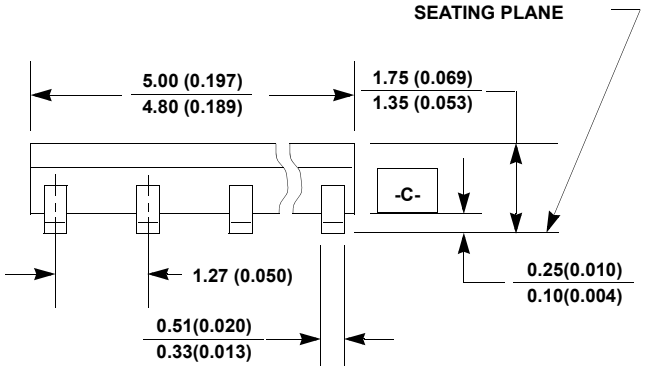
M8.15
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 4, 1/12



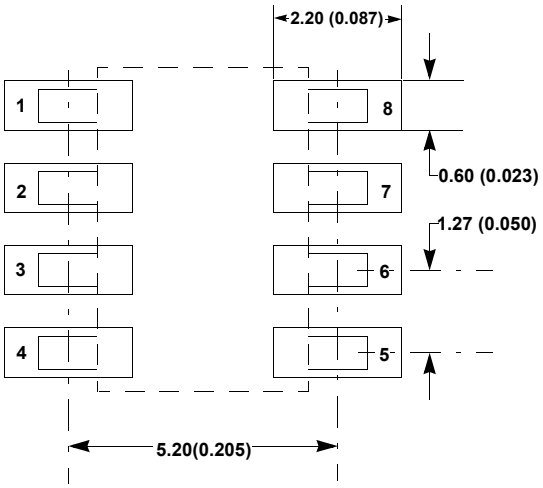
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A



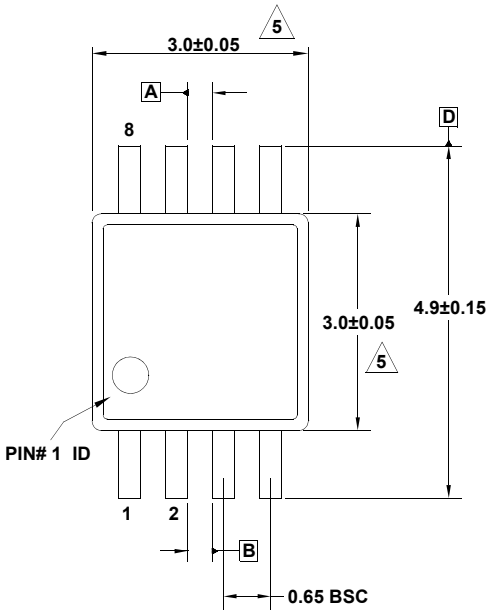
TYPICAL RECOMMENDED LAND PATTERN

Notes:

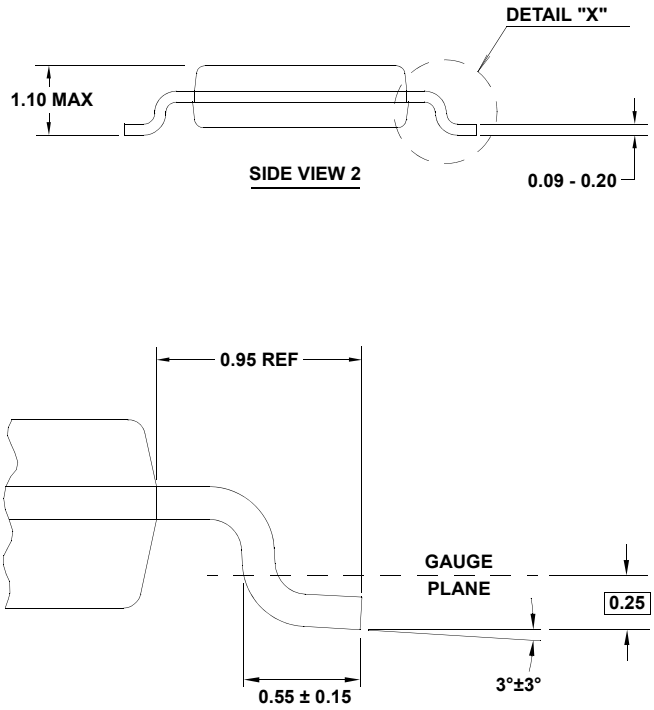
1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the

M8.118
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE
Rev 4, 7/11

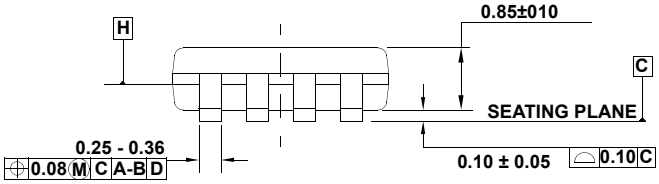
For the most recent package outline drawing, see M8.118.



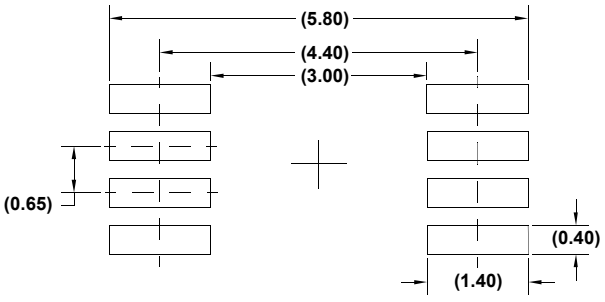
TOP VIEW



DETAIL "X"



SIDE VIEW 1



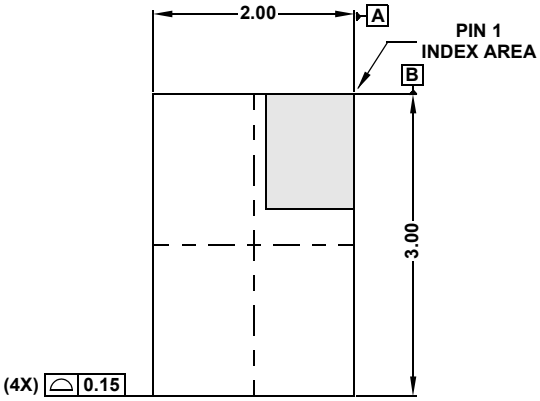
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

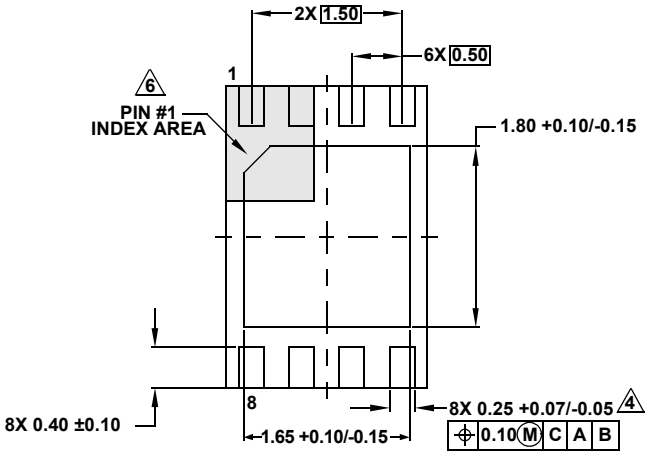
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

L8.2x3
8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 3/15

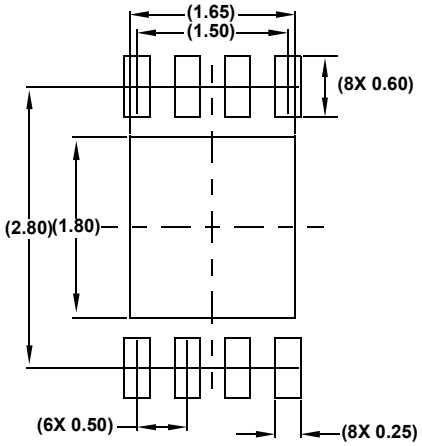
For the most recent package outline drawing, see L8.2x3.



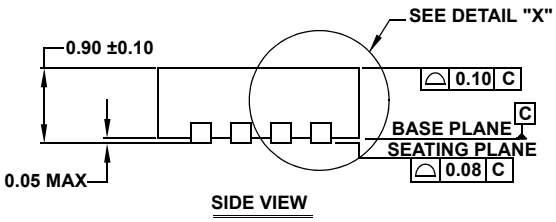
TOP VIEW



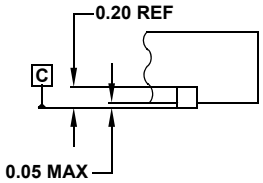
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compies to JEDEC MO-229 VCED-2.

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(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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